

SN54AHC126, SN74AHC126 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCLS257L – DECEMBER 1995 – REVISED JULY 2003

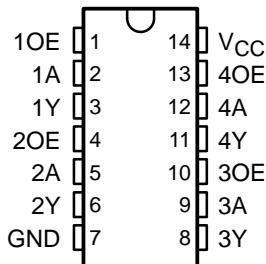
- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17

description/ordering information

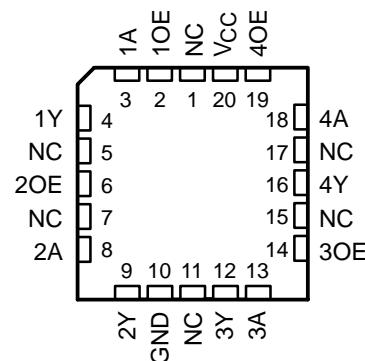
The 'AHC126 devices are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low. When OE is high, the respective gate passes the data from the A input to its Y output.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

SN54AHC126 . . . J OR W PACKAGE
SN74AHC126 . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC126 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74AHC126N	SN74AHC126N
	SOIC – D	Tube	SN74AHC126D	AHC126
		Tape and reel	SN74AHC126DR	
	SOP – NS	Tape and reel	SN74AHC126NSR	AHC126
	SSOP – DB	Tape and reel	SN74AHC126DBR	HA126
	TSSOP – PW	Tube	SN74AHC126PW	HA126
		Tape and reel	SN74AHC126PWR	
-55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHC126DGVR	HA126
	CDIP – J	Tube	SNJ54AHC126J	SNJ54AHC126J
	CFP – W	Tube	SNJ54AHC126W	SNJ54AHC126W
	LCCC – FK	Tube	SNJ54AHC126FK	SNJ54AHC126FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

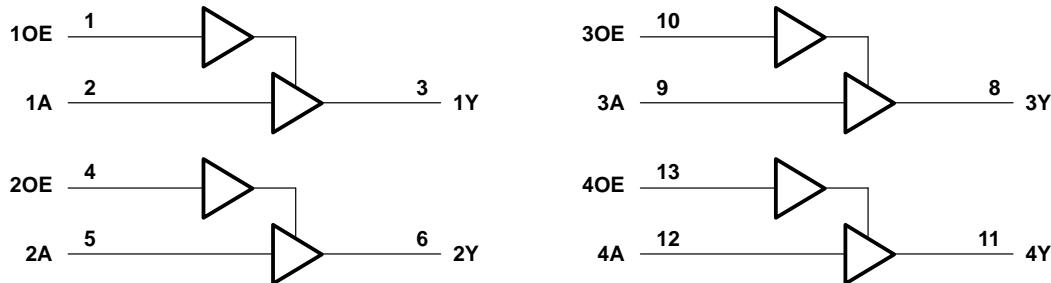
**SN54AHC126, SN74AHC126
QUADRUPLE BUS BUFFER GATES
WITH 3-STATE OUTPUTS**

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FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	86°C/W
DB package	96°C/W
DGV package	127°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

			SN54AHC126		SN74AHC126		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5			V
		V _{CC} = 3 V	2.1	2.1			
		V _{CC} = 5.5 V	3.85	3.85			
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5			V
		V _{CC} = 3 V	0.9	0.9			
		V _{CC} = 5.5 V	1.65	1.65			
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	-50			µA
		V _{CC} = 3.3 V ± 0.3 V	-4	-4			mA
		V _{CC} = 5 V ± 0.5 V	-8	-8			
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50			µA
		V _{CC} = 3.3 V ± 0.3 V	4	4			mA
		V _{CC} = 5 V ± 0.5 V	8	8			
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V	100	100			ns/V
		V _{CC} = 5 V ± 0.5 V	20	20			
T _A	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC126	SN74AHC126	UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	2 V	1.9	2		1.9	1.9	V
		3 V	2.9	3		2.9	2.9	
		4.5 V	4.4	4.5		4.4	4.4	
	I _{OH} = -4 mA	3 V	2.58			2.48	2.48	
	I _{OH} = -8 mA	4.5 V	3.94			3.8	3.8	
V _{OL}	I _{OL} = 50 µA	2 V		0.1		0.1	0.1	V
		3 V		0.1		0.1	0.1	
		4.5 V		0.1		0.1	0.1	
	I _{OL} = 4 mA	3 V		0.36		0.5	0.44	
	I _{OL} = 8 mA	4.5 V		0.36		0.5	0.44	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V		±0.1		±1*	±1	µA
I _{OZ}	V _O = V _{CC} or GND	5.5 V		±0.25		±2.5	±2.5	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		4		40	40	µA
C _i	V _I = V _{CC} or GND	5 V		4	10		10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

**SN54AHC126, SN74AHC126
QUADRUPLE BUS BUFFER GATES
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**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC126	SN74AHC126	UNIT	
				MIN	TYP	MAX	MIN	MAX		
t_{PLH}	A	Y	$C_L = 15 \text{ pF}$	5.6*	8*	1*	9.5*	1	9.5	ns
t_{PHL}				5.6*	8*	1*	9.5*	1	9.5	
t_{PZH}	OE	Y	$C_L = 15 \text{ pF}$	5.4*	8*	1*	9.5*	1	9.5	ns
t_{PZL}				5.4*	8*	1*	9.5*	1	9.5	
t_{PHZ}	OE	Y	$C_L = 15 \text{ pF}$	7*	9.7*	1*	11.5*	1	11.5	ns
t_{PLZ}				7*	9.7*	1*	11.5*	1	11.5	
t_{PLH}	A	Y	$C_L = 50 \text{ pF}$	8.1	11.5	1	13	1	13	ns
t_{PHL}				8.1	11.5	1	13	1	13	
t_{PZH}	OE	Y	$C_L = 50 \text{ pF}$	7.9	11.5	1	13	1	13	ns
t_{PZL}				7.9	11.5	1	13	1	13	
t_{PHZ}	OE	Y	$C_L = 50 \text{ pF}$	9.5	13.2	1	15	1	15	ns
t_{PLZ}				9.5	13.2	1	15	1	15	
$t_{sk(o)}$			$C_L = 50 \text{ pF}$	1.5**			1.5		ns	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC126	SN74AHC126	UNIT	
				MIN	TYP	MAX	MIN	MAX		
t_{PLH}	A	Y	$C_L = 15 \text{ pF}$	3.8*	5.5*	1*	6.5*	1	6.5	ns
t_{PHL}				3.8*	5.5*	1*	6.5*	1	6.5	
t_{PZH}	OE	Y	$C_L = 15 \text{ pF}$	3.6*	5.1*	1*	6*	1	6	ns
t_{PZL}				3.6*	5.1*	1*	6*	1	6	
t_{PHZ}	OE	Y	$C_L = 15 \text{ pF}$	4.6*	6.8*	1*	8*	1	8	ns
t_{PLZ}				4.6*	6.8*	1*	8*	1	8	
t_{PLH}	A	Y	$C_L = 50 \text{ pF}$	5.3	7.5	1	8.5	1	8.5	ns
t_{PHL}				5.3	7.5	1	8.5	1	8.5	
t_{PZH}	OE	Y	$C_L = 50 \text{ pF}$	5.1	7.1	1	8	1	8	ns
t_{PZL}				5.1	7.1	1	8	1	8	
t_{PHZ}	OE	Y	$C_L = 50 \text{ pF}$	6.1	8.8	1	10	1	10	ns
t_{PLZ}				6.1	8.8	1	10	1	10	
$t_{sk(o)}$			$C_L = 50 \text{ pF}$	1**			1		ns	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

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noise characteristics, $V_{CC} = 5$ V, $C_L = 50$ pF, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	SN74AHC126		UNIT
	MIN	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}	4.4		V
$V_{IH(D)}$ High-level dynamic input voltage	3.5		V
$V_{IL(D)}$ Low-level dynamic input voltage		1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

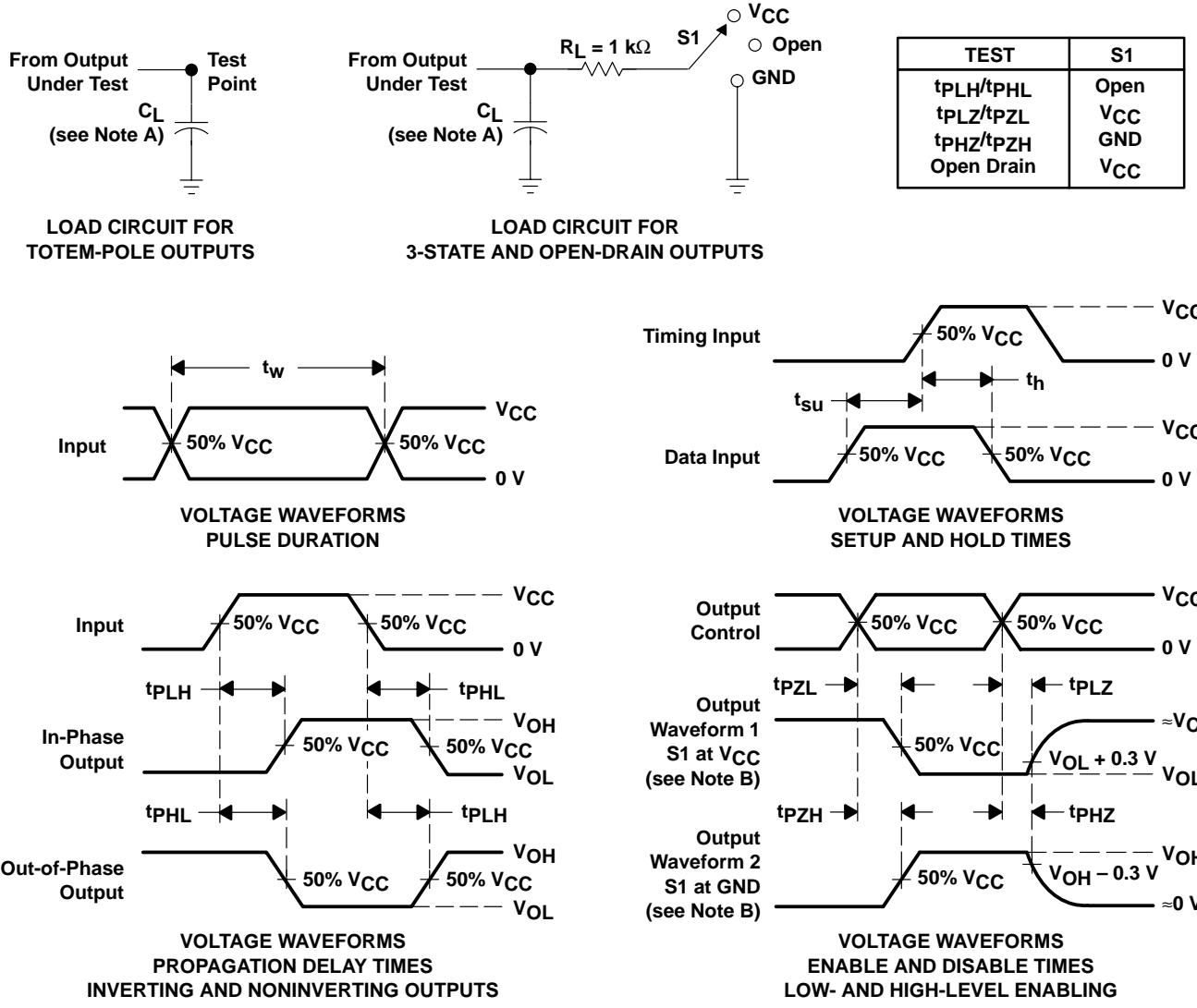
operating characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1$ MHz	14	pF

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PARAMETER MEASUREMENT INFORMATION



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
- The outputs are measured one at a time with one input transition per measurement.
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9686201Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686201Q2A SNJ54AHC126FK	Samples
5962-9686201QDA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686201QD A SNJ54AHC126W	Samples
SN74AHC126D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC126	Samples
SN74AHC126DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA126	Samples
SN74AHC126DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC126	Samples
SN74AHC126DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA126	Samples
SN74AHC126DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC126	Samples
SN74AHC126N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC126N	Samples
SN74AHC126NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC126	Samples
SN74AHC126PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA126	Samples
SN74AHC126PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA126	Samples
SN74AHC126PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA126	Samples
SNJ54AHC126FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686201Q2A SNJ54AHC126FK	Samples
SNJ54AHC126W	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686201QD A SNJ54AHC126W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AHC126, SN74AHC126 :

- Catalog : [SN74AHC126](#)
- Military : [SN54AHC126](#)

NOTE: Qualified Version Definitions:

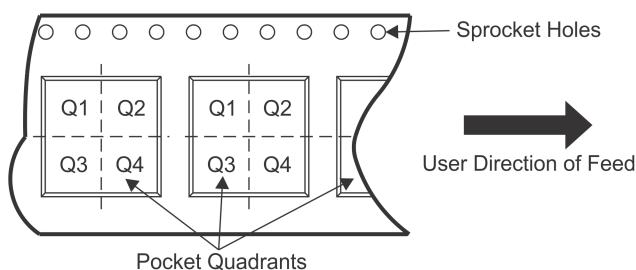
- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

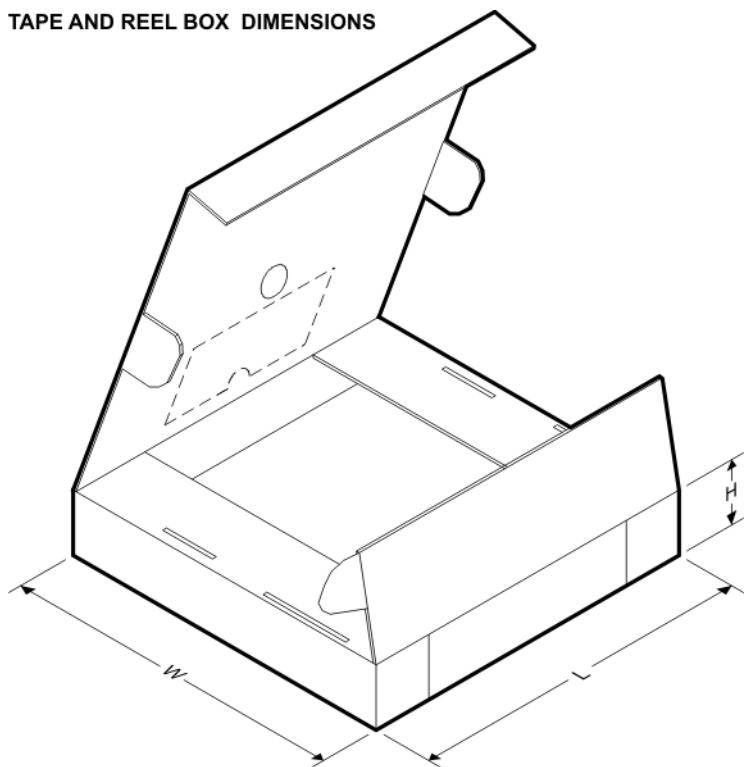
TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


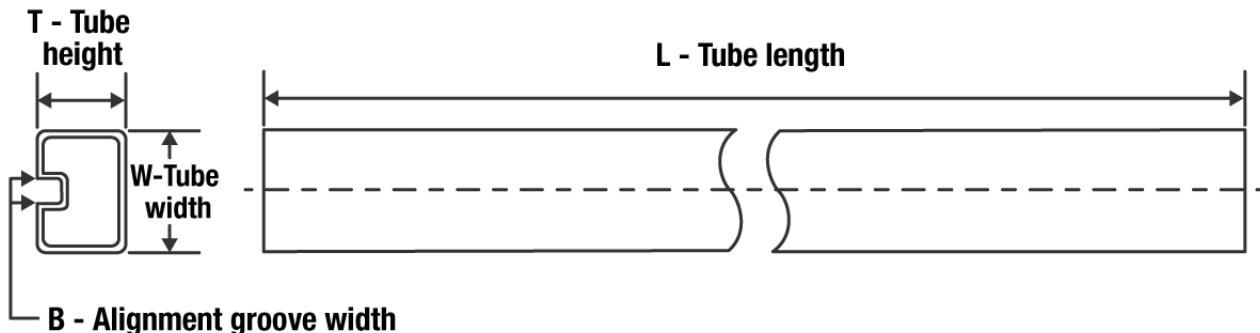
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC126DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC126DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC126NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC126DBR	SSOP	DB	14	2000	853.0	449.0	35.0
SN74AHC126DGVR	TVSOP	DGV	14	2000	853.0	449.0	35.0
SN74AHC126DR	SOIC	D	14	2500	853.0	449.0	35.0
SN74AHC126NSR	SO	NS	14	2000	853.0	449.0	35.0
SN74AHC126PWR	TSSOP	PW	14	2000	853.0	449.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9686201Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74AHC126D	D	SOIC	14	50	506.6	8	3940	4.32
SN74AHC126DG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74AHC126N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC126N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC126PW	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54AHC126FK	FK	LCCC	20	1	506.98	12.06	2030	NA

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

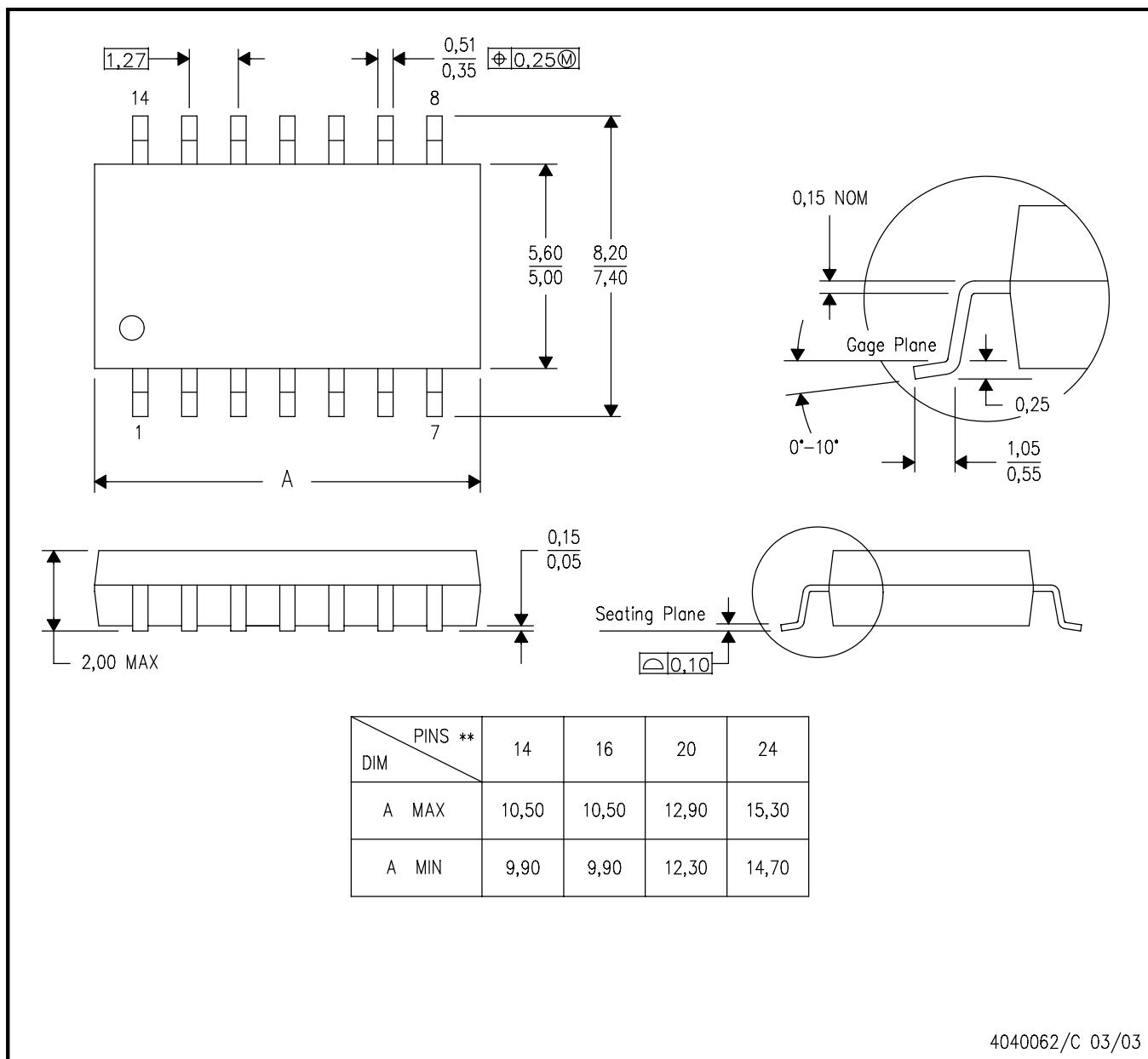
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MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

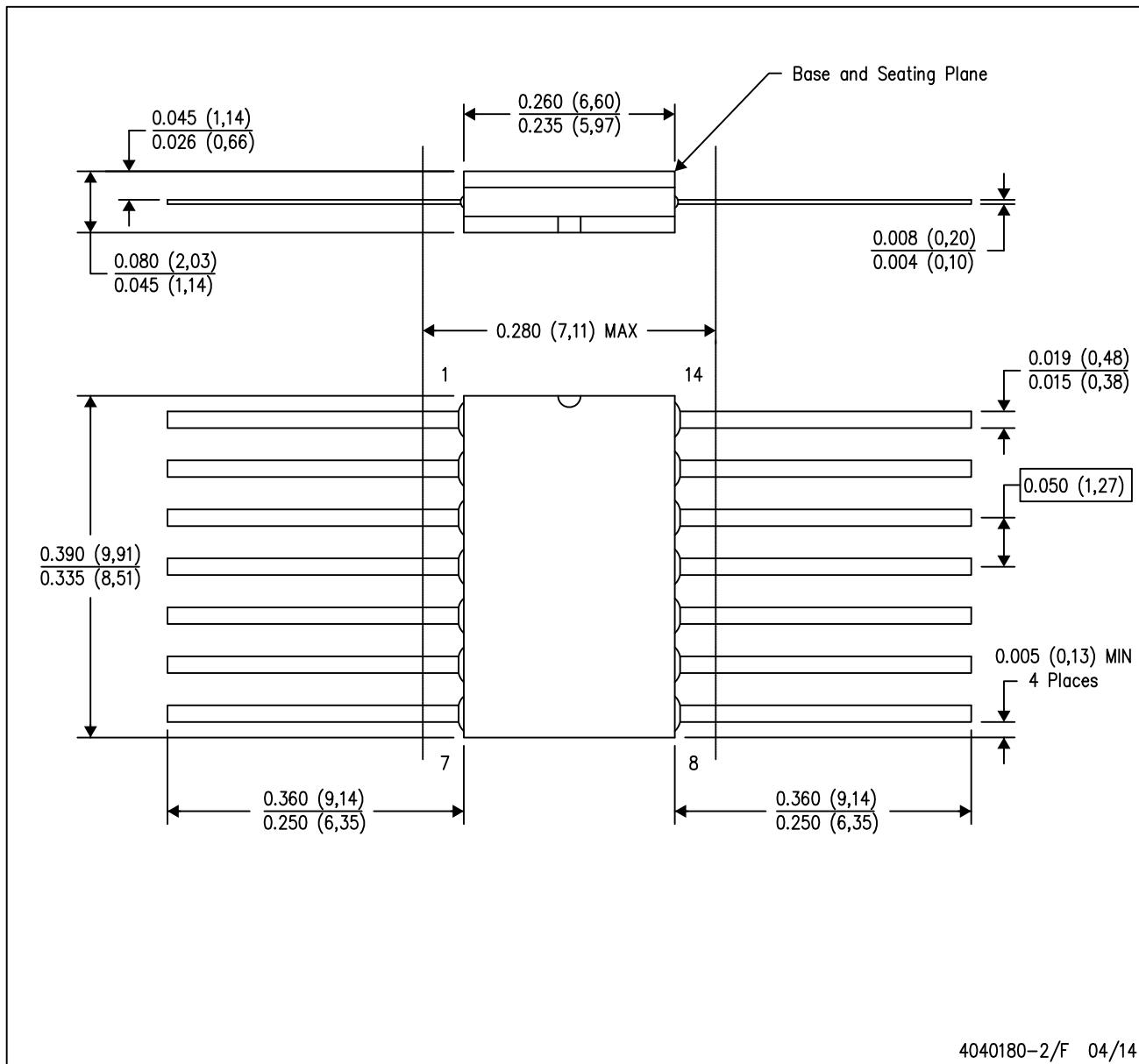


NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

4040062/C 03/03

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

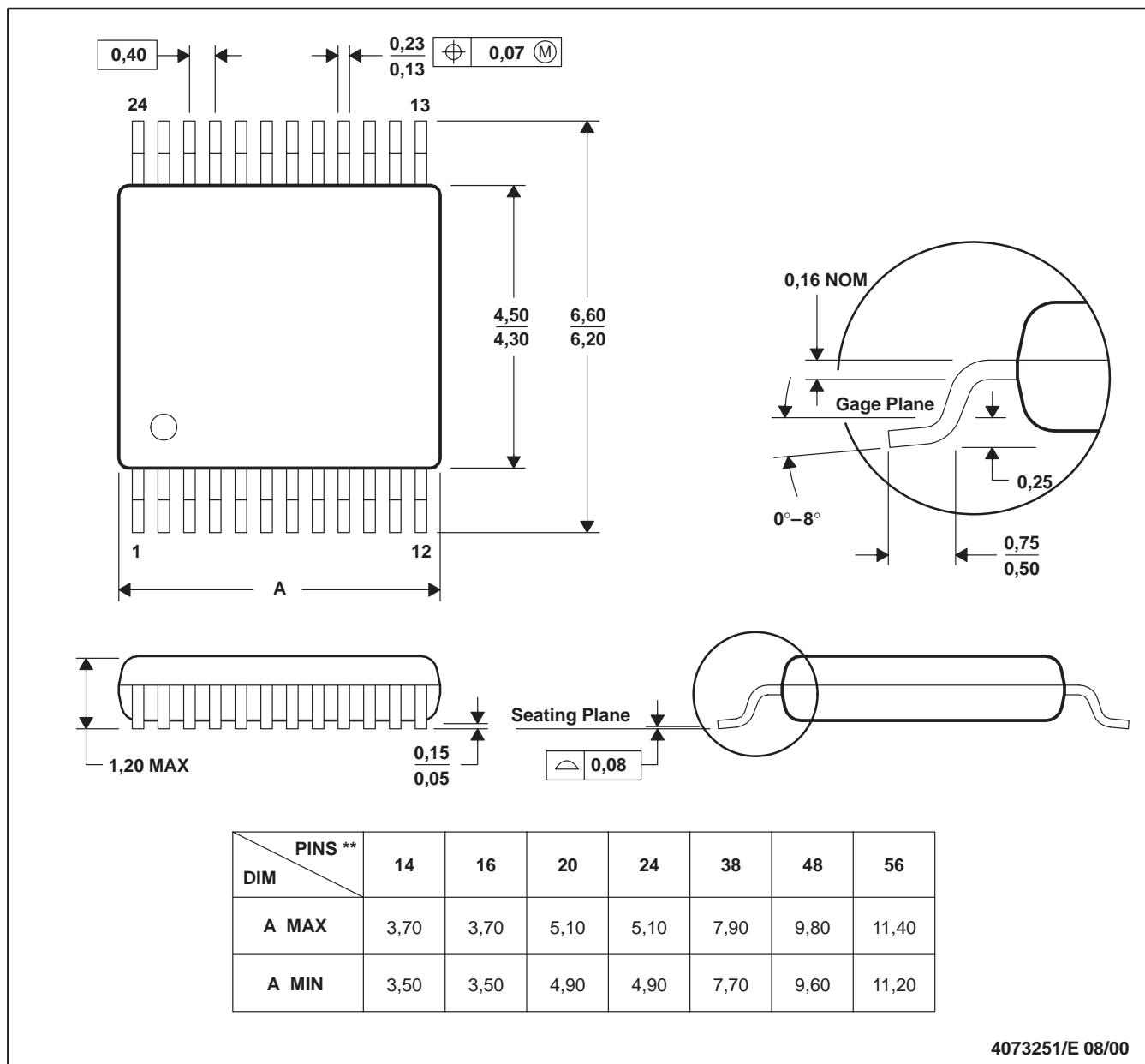
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP1-F14

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

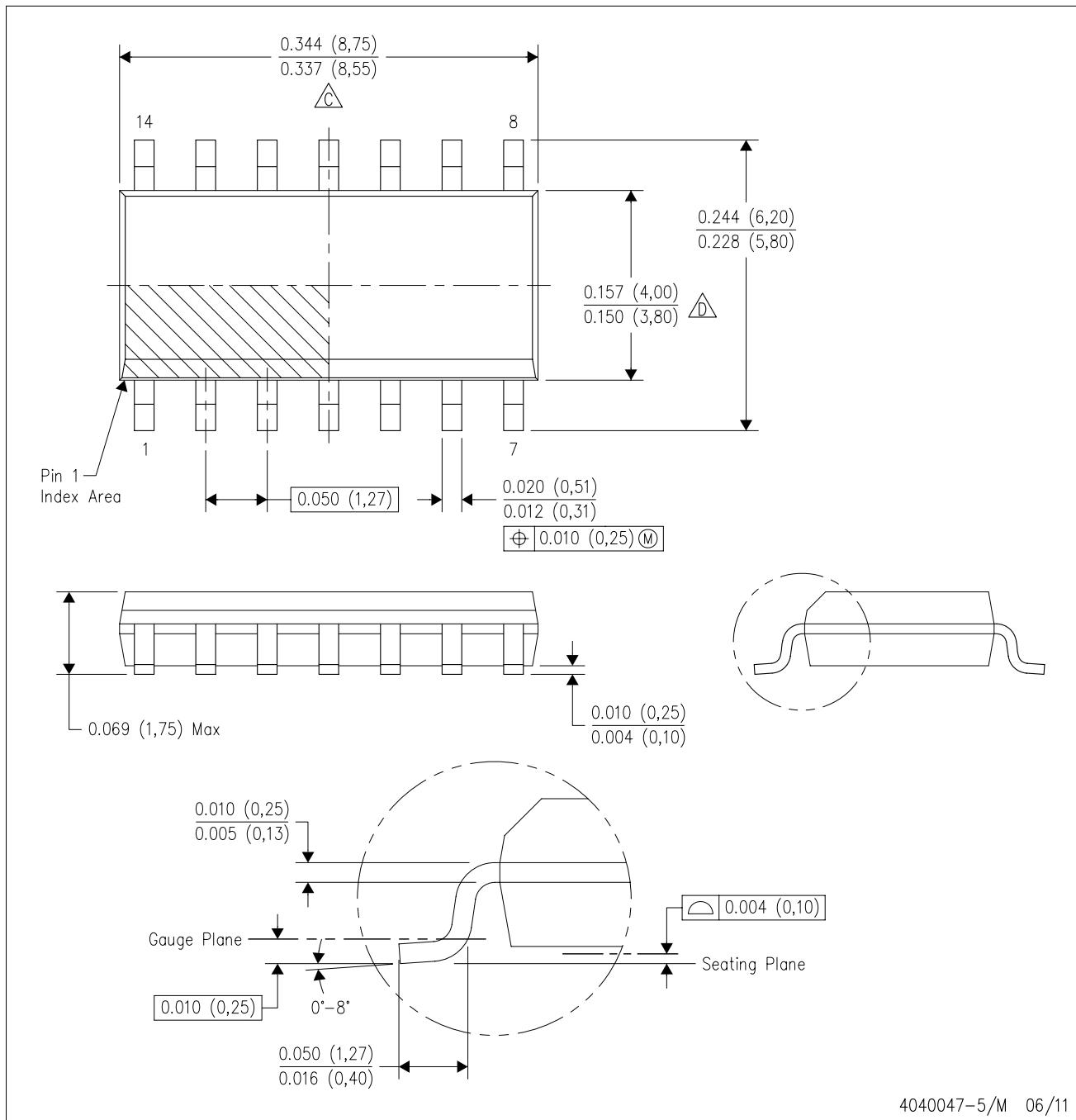
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

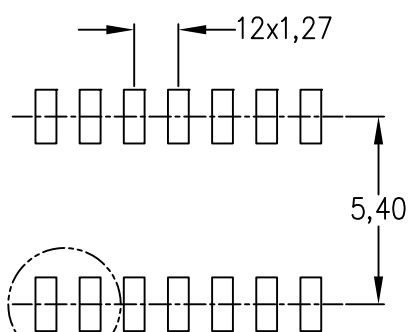
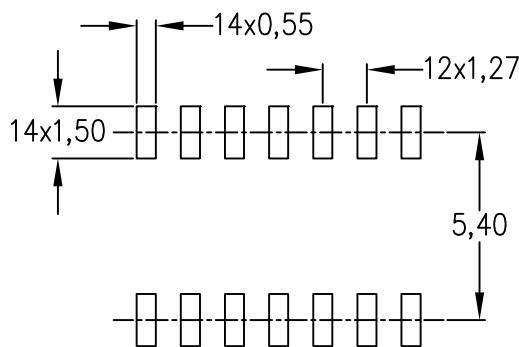
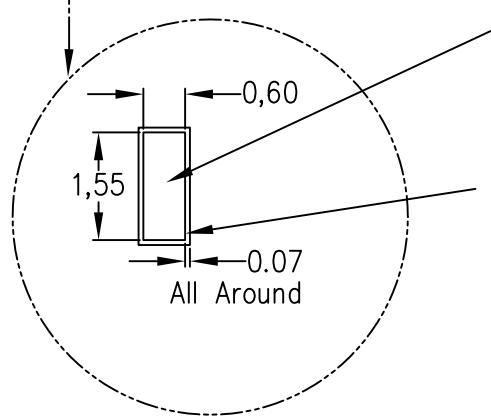
(C) Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

(D) Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

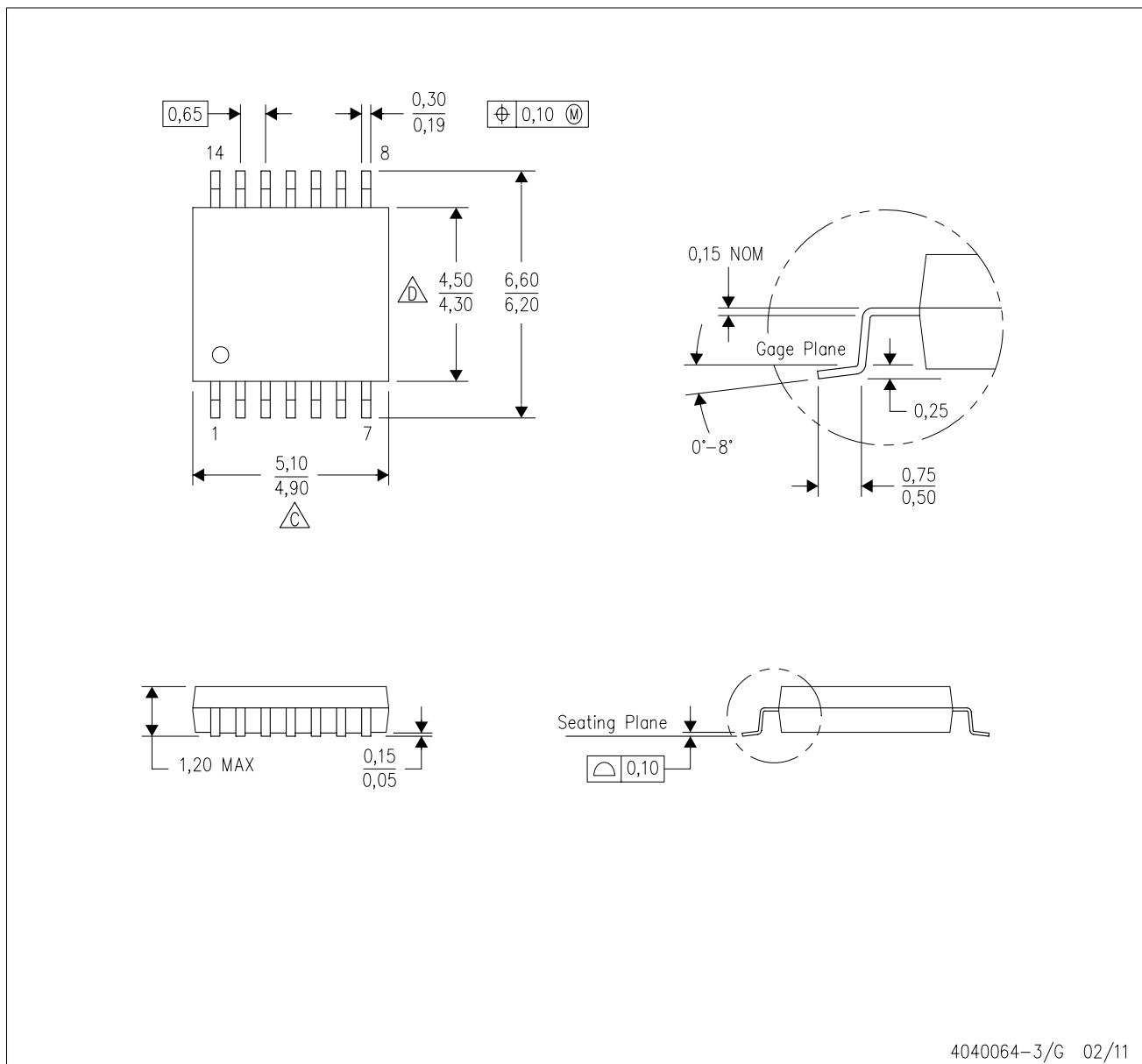
4211283-3/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

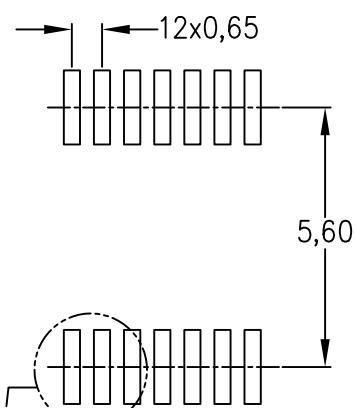
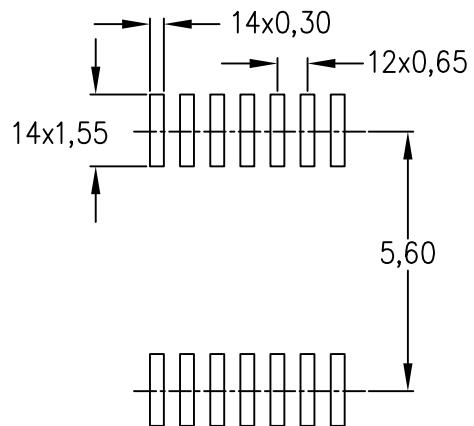
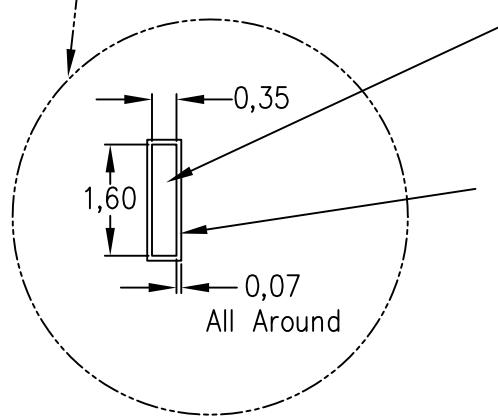
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

4040064-3/G 02/11

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211284-2/G 08/15

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

16 PINS SHOWN

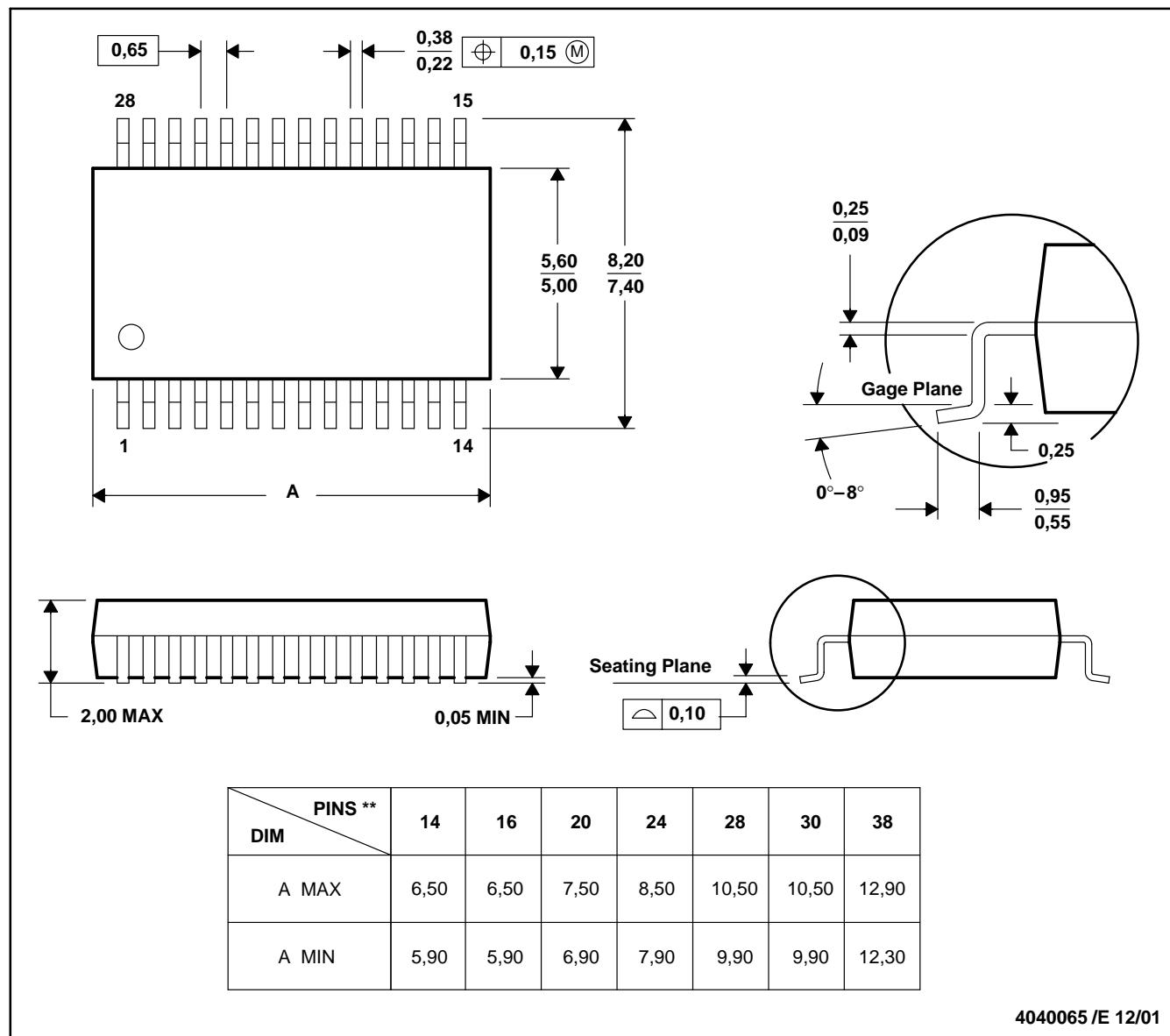
PLASTIC DUAL-IN-LINE PACKAGE



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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