OPAx187 0.001μV/°C 温漂、低功耗、轨至轨输出 36V 运算放大器零漂移系列

1 特性

- 低失调电压：10μV（典型值）
- 零漂移：0.001μV/°C
- 低噪声：15nV/√Hz
- 电源抑制比 (PSRR)：160dB
- 共模抑制比 (CMRR)：140dB
- AOL：160dB
- 静态电流：100μA
- 宽电源电压：±2.25V 至 ±18V
- 轨至轨输出运行
- 输入包括负电源轨
- 低偏置电流：100pA（典型值）
- 已滤除电磁干扰 (EMI) 的输入
- 微型封装

2 应用

- 桥式放大器
- 应力计
- 测试和测量仪器
- 变频器应用
- 温度测量
- 电子称
- 医疗仪表
- 热电阻 (RTD) 放大器
- 精密有源滤波器
- 低侧电流监控

3 说明

OPAx187 系列运算放大器采用自动归零技术，可在时间和温度范围内同步提供低失调电压 (1μV) 以及近似为零的漂移。此类微型、高精度、低静态电流放大器提供高输入阻抗和流入高阻抗负载的摆幅在 5mV 电源轨范围内的轨至轨输出。输入共模范围包括负电源轨。单电源或双电源可在 4.5V 至 36V（±2.25V 至 ±18V）范围内使用。

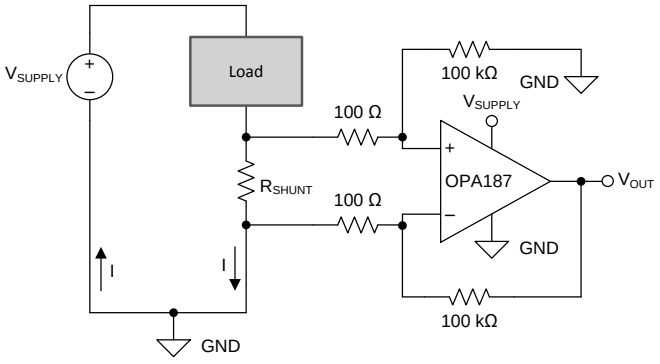
OPAx187 器件的单通道版本采用微型 8 引脚超薄小外形尺寸 (VSSOP) 封装、5 引脚 SOT-23 封装和 8 引脚小外形尺寸集成电路 (SOIC) 封装。双通道版本采用 8 引脚 VSSOP 和 8 引脚 SOIC 封装。四通道版本采用 14 引脚 SOIC、14 引脚 TSSOP 和 16 引脚 WQFN 封装。所有版本的额定工作温度范围均为 –40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA187	SOIC (8)	4.90mm × 3.91mm
	SOT-23 (5)	2.90mm × 1.60mm
	VSSOP (8)	3.00mm × 3.00mm
OPA2187 的 VSON 封装选项	SOIC (8)	4.90mm × 3.91mm
	VSSOP (8)	3.00mm × 3.00mm
OPA4187	SOIC (14)	8.70mm × 3.90mm
	TSSOP (14)	5.00mm × 4.40mm
	WQFN (16)（预览）	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

OPAx187 具有高精度低侧电流测量功能



$G = 1000 \cdot R_{SHUNT} \cdot I$

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (December 2018) to Revision D — **Page**

- 已更改 将 OPA4187 SOIC 和 TSSOP 封装从产品预览改为了生产数据 ... 1
- Changed offset drift (high and low supply) max to ±15nV/°C ... 8

Changes from Revision B (October 2018) to Revision C — **Page**

- 首次将 OPA187 SOIC 器件作为生产用途发布 ... 1

Changes from Revision A (July 2017) to Revision B — **Page**

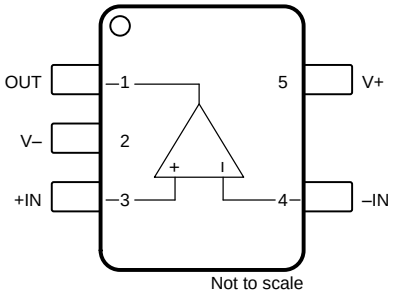
- 已更改 将 OPA187 SOIC 的状态改为了预览 ... 1
- 已更改 将 OPA4187 SOIC、TSSOP 和 WQFN 状态改为了预览 ... 1
- Changed offset drift (high supply) typical from ±5 nV/℃ to ±1 nV/℃ and max from ±50 nV/℃ to ±20 nV/℃ ... 7
- Changed input bias current max (high supply) from ±5 nA to ±7.5 nA ... 7
- Changed input offset current max (high supply) from ±5 nA to ±14.5 nA ... 7
- Changed offset drift (low supply) typical from ±5 nV/℃ to ±1 nV/℃ and max from ±50 nV/℃ to ±20 nV/℃ ... 8
- 已更改 Offset Voltage Production Distribution figure ... 10

Changes from Original (December 2016) to Revision A — **Page**

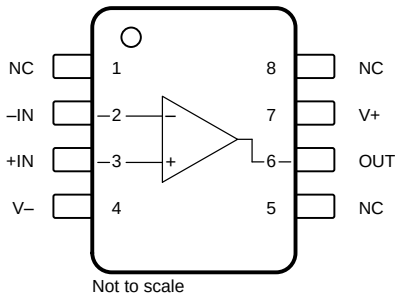
- 已删除 删除了说明部分的 VSON 封装选项 ... 1
- 已删除 删除了*器件信息* 表 ... 1
- 已添加 将 WQFN 封装选项添加到了*器件信息* 表 ... 1
- Deleted OPA187 DRG package option from *Pin Configuration and Functions* ... 3
- Added WQFN package to *Pin Configuration and Functions* ... 4

5 Pin Configuration and Functions

OPA187: DBV Package
5-Pin SOT-23
Top View



OPA187: D and DGK Packages
8-Pin SOIC and 8-pin VSSOP
Top View

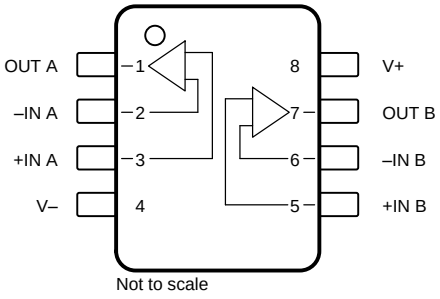


(1) NC denotes no internal connection.

Pin Functions: OPA187

PIN			I/O	DESCRIPTION
NAME	DBV	D and DGK		
+IN	3	3	I	Non-inverting input
–IN	4	2	I	Inverting input
NC	—	1, 5, 8	—	No connection (can be left floating)
OUT	1	6	O	Output signal
V+	5	7	—	Positive (highest) supply voltage
V–	2	4	—	Negative (lowest) supply voltage

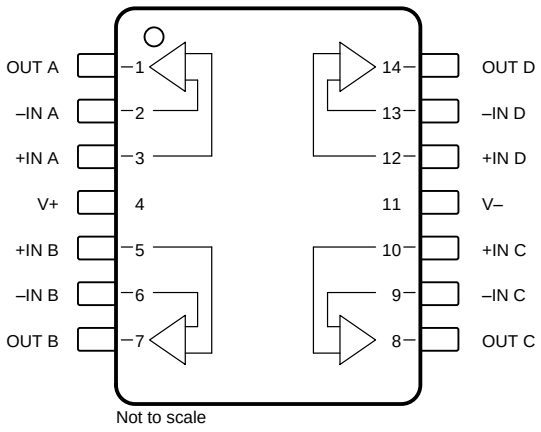
OPA2187: D and DGK Packages
8-Pin SOIC and 8-Pin VSSOP
Top View



Pin Functions: OPA2187

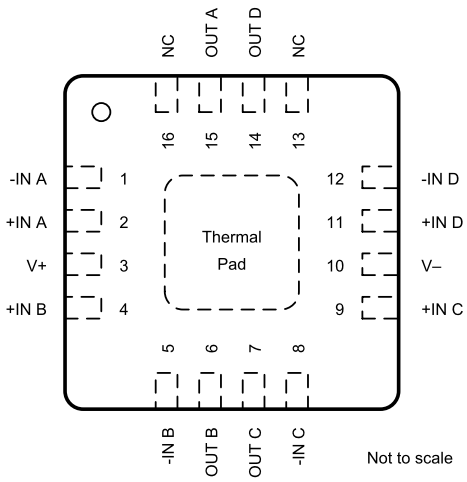
PIN		I/O	DESCRIPTION
NAME	D and DGK		
+IN A	3	I	Non-inverting input, channel A
–IN A	2	I	Inverting input, channel A
+IN B	5	I	Non-inverting input, channel B
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) supply voltage
V–	4	—	Negative (lowest) supply voltage

OPA4187: D and PW Packages
14-pin SOIC and 14-Pin TSSOP
Top View



Not to scale

OPA4187: RUM Package (Preview)
16-pin WQFN
Top View



Not to scale

Pin Functions: OPA4187

PIN			I/O	DESCRIPTION
NAME	D and PW	RUM		
+IN A	3	2	I	Non-inverting input, channel A
–IN A	2	1	I	Inverting input, channel A
+IN B	5	4	I	Non-inverting input, channel B
–IN B	6	5	I	Inverting input, channel B
+IN C	10	9	I	Non-inverting input, channel C
–IN C	9	8	I	Inverting input, channel C
+IN D	12	11	I	Non-inverting input, channel D
–IN D	13	12	I	Inverting input, channel D
OUT A	1	15	O	Output, channel A
OUT B	7	6	O	Output, channel B
OUT C	8	7	O	Output, channel C
OUT D	14	14	O	Output, channel D
V+	4	3	—	Positive (highest) supply voltage
V–	11	10	—	Negative (lowest) supply voltage
NC	—	13, 16	—	No internal connection (can be left floating)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, $V_S = (V^+) – (V^–)$		40	V
	Signal input pin(2)	$(V^–) – 0.5$	$(V^+) + 0.5$	
	Signal output pin(3)	$(V^–) – 0.5$	$(V^+) + 0.5$	
Current	Signal input pin(2)	–10	10	mA
	Signal output pin(3)	–55	55	mA
	Output short-circuit(4)	Continuous	Continuous	Continuous
Temperature	Operating range, T_A	–55	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to ±10 mA or less.
(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5 V beyond the supply rails should be current limited to ±55 mA or less.
(4) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$(V^+) – (V^–)$	Supply voltage	4.5 (±2.25)		36 (±18)	V
T_A	Operating temperature	–40		150	°C

6.4 Thermal Information: OPA187

THERMAL METRIC(1)		OPA187			UNIT
		5 PINS	8 PINS		
		DBV (SOT-23)	DGK (VSSOP)	D (SOIC)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	273.8	159	100.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	126.8	37	42.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.9	49	41.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.9	1.2	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	84.9	77.1	40.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information: OPA2187

THERMAL METRIC(1)		OPA2187		UNIT
		8 PINS		
		DGK (VSSOP)	D (SOIC)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	159	100.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37	42.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49	41.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.1	40.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Thermal Information: OPA4187

THERMAL METRIC(1)		OPA4187			UNIT
		14 PINS		16 PINS	
		PW (TSSOP)	D (SOIC)	RUM (WQFN)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.8	83.8	35.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.6	70.7	32.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	59.5	12.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	11.6	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.6	37.7	12.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.7 Electrical Characteristics: High-Voltage Operation

at T_A = +25°C, V_S = ±4 V to ±18 V (V_S = +8 V to +36 V), R_L = 10 kΩ connected to V_S / 2[(1)], and V_{CM} = V_{OUT} = V_S / 2[(1)] (unless otherwise noted)

PARAMETER			CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±1	±10	µV
			T_A = –40°C to +125°C		±0.001	±0.015	µV/°C
PSRR	Power-supply rejection ratio		V_S = 4.5 V to 36 V, T_A = –40°C to +125°C		±0.01	±1	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current		V_{CM} = V_S / 2		±100	±350	pA
			T_A = –40°C to +125°C			±7.5	nA
I_{OS}	Input offset current				±100	±500	pA
			T_A = –40°C to +125°C			±14.5	nA
NOISE							
e_n	Input voltage noise		f = 0.1 Hz to 10 Hz		0.4		μV_{PP}
			f = 0.1 Hz to 10 Hz		60		nVrms
	Input voltage noise density		f = 1 kHz		20		nV/√Hz
i_n	Input current noise density		f = 1 kHz		160		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) – 2	V
CMRR	Common-mode rejection ratio		(V–) – 0.1 V < V_{CM} < (V+) – 2 V, V_S = ±18 V	126	140		dB
			(V–) < V_{CM} < (V+) – 2 V, V_S = ±18 V, T_A = –40°C to +125°C	130	145		dB
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 6		MΩ || pF
Z_{IC}	Common-mode				6 || 4.2		10^{12} Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain		T_A = –40°C to +125°C, V_S = ±4 V to ±18 V, (V–) + 0.3 V < V_O < (V+) – 0.3 V, R_L = 10 kΩ	132	160		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				550		kHz
SR	Slew rate		V_O = 10-V step, G = +1		0.2		V/µs
t_S	Settling time	0.1%	V_S = ±18 V, G = 1, 10-V step		46		µs
		0.01%	V_S = ±18 V, G = 1, 10-V step		48		µs
t_{OR}	Overload recovery time		V_{IN} × G = V_S		8		µs
THD+N	Total harmonic distortion + noise		1 kHz, G = +1, V_{OUT} = 3.5 V_{RMS}, No Load		0.035%		
OUTPUT							
	Voltage output swing from rail		V_S = ±4 V to ±18 V, No Load		5	15	mV
			V_S = ±4 V to ±18 V, R_L = 10 kΩ		75	100	
			V_S = ±4 V to ±18 V, R_L = 10 kΩ, T_A = –40°C to +125°C		100	125	
I_{SC}	Short-circuit current		V_S = ±18 V, Sinking		–30		mA
			V_S = ±18 V, Sourcing		+30		mA
R_O	Open-loop output resistance		f = 550 kHz, I_O = 0, See Figure 21		1.4		kΩ
C_{LOAD}	Capacitive load drive					See *Typical Characteristics*	
POWER SUPPLY							
I_Q	Quiescent current (per amplifier)		V_S = ±4 V to V_S = ±18 V		100	145	µA
			I_O = 0 mA, T_A = –40°C to +125°C			150	µA

(1) V_S / 2 = midsupply.

6.8 Electrical Characteristics: Low-Voltage Operation

at T_A = +25°C, V_S = ±2.25 V to < ±4 V (V_S = +4.5 V to < +8 V), R_L = 10 kΩ connected to V_S / 2[(1)], and V_{CM} = V_{OUT} = V_S / 2[(1)] (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±1	±15	µV
		T_A = –40°C to +125°C		±0.001	±0.015	µV/°C
PSRR	Power-supply rejection ratio	V_S = 4.5 V to 36 V, T_A = –40°C to +125°C		±0.01	±1	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S / 2		±100	±350	pA
		T_A = –40°C to +125°C			±5	nA
I_{OS}	Input offset current			±100	±500	pA
		T_A = –40°C to +125°C			±5	nA
NOISE						
e_n	Input voltage noise	f = 0.1 Hz to 10 Hz		0.4		μV_{PP}
		f = 0.1 Hz to 10 Hz		60		nVrms
	Input voltage noise density	f = 1 kHz		20		nV/√Hz
i_n	Input current noise density	f = 1 kHz		160		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) – 2	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) – 2 V, V_S = ±2.25 V	114	130		dB
		(V–) < V_{CM} < (V+) – 2 V, V_S = ±2.25 V, T_A = –40°C to +125°C	120	137		dB
INPUT IMPEDANCE						
Z_{ID}	Differential			100 || 6		MΩ || pF
Z_{IC}	Common-mode			6 || 4.2		10^{12} Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	T_A = –40°C to +125°C, V_S = ±2.25 V to ±4 V, (V–) + 0.3 V < V_O < (V+) – 0.3 V, R_L = 10 kΩ	120	140		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			550		kHz
SR	Slew rate	V_O = 1-V step, G = +1		0.2		V/µs
t_{OR}	Overload recovery time	V_{IN} × G = V_S		8		µs
THD+N	Total harmonic distortion + noise	1 kHz, G = +1, V_{OUT} = 1 Vrms, No Load		0.05%		
OUTPUT						
	Voltage output swing from rail	V_S = ±2.25 V to ±4 V, No Load		5	15	mV
		V_S = ±2.25 V to ±4 V, R_L = 10 kΩ		15	25	
		V_S = ±2.25 V to ±4 V, R_L = 10 kΩ, T_A = –40°C to +125°C		15	30	
I_{SC}	Short-circuit current	V_S = ±2.25, Sinking		–20		mA
		V_S = ±2.25, Sourcing		+20		mA
R_O	Open-loop output resistance	f = 550 kHz, I_O = 0, See Figure 21		1.4		kΩ
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*	
POWER SUPPLY						
I_Q	Quiescent current (per amplifier)	V_S = ±2.25 V to V_S = ±4 V		100	145	µA
		I_O = 0 mA, T_A = –40°C to +125°C			150	µA

(1) V_S / 2 = midsupply.

6.9 Typical Characteristics

表 1. Typical Characteristic Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	图 1
Offset Voltage Drift Distribution	图 2
Offset Voltage vs Temperature	图 3
Offset Voltage vs Common-Mode Voltage	图 4
Offset Voltage vs Power Supply	图 5
Open-Loop Gain and Phase vs Frequency	图 6
Closed-Loop Gain vs Frequency	图 7
I_B vs Common-Mode Voltage	图 8
Input Bias Current vs Temperature	图 9
Output Voltage Swing vs Output Current	图 10
CMRR and PSRR vs Frequency (Referred-to-Input)	图 11
CMRR vs Temperature	图 12
PSRR vs Temperature	图 13
0.1-Hz to 10-Hz Noise	图 14
Input Voltage Noise Spectral Density vs Frequency	图 15
THD+N Ratio vs Frequency	图 16
THD+N vs Output Amplitude	图 17
Quiescent Current vs Supply Voltage	图 18
Quiescent Current vs Temperature	图 19
Open-Loop Gain vs Temperature	图 20
Open-Loop Output Impedance vs Frequency	图 21
Small-Signal Overshoot vs Capacitive Load (G = 1) (10-mV Output Step)	图 22
No Phase Reversal	图 23
Positive Overload Recovery	图 24
Negative Overload Recovery	图 25
Small-Signal Step Response (10 mV)	图 26, 图 27
Large-Signal Step Response	图 28, 图 29
Large-Signal Settling Time (10-V Positive Step)	图 30
Large-Signal Settling Time (10-V Negative Step)	图 31
Short-Circuit Current vs Temperature	图 32
Maximum Output Voltage vs Frequency	图 33
Crosstalk vs Frequency	图 34
EMIRR IN+ vs Frequency	图 35

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

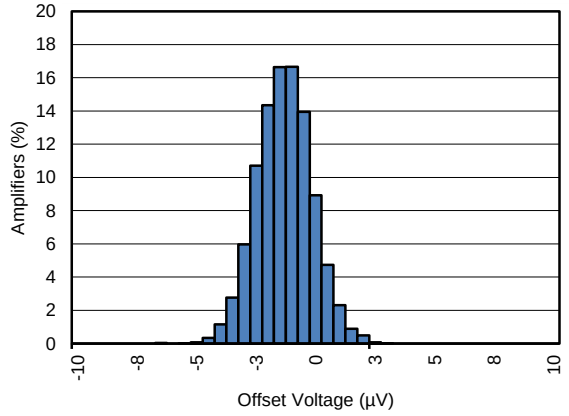


图 1. Offset Voltage Production Distribution

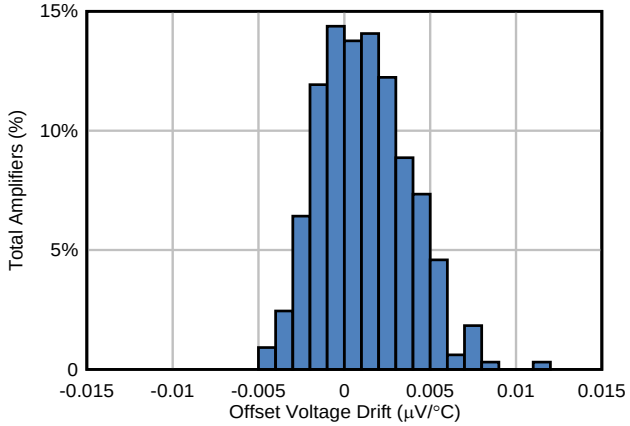


图 2. Offset Voltage Drift Distribution

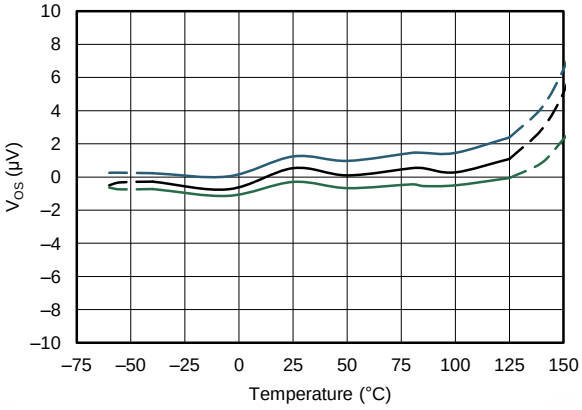


图 3. Offset Voltage vs Temperature

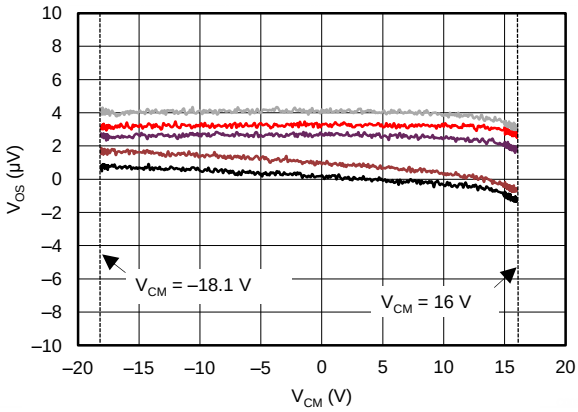


图 4. Offset Voltage vs Common-Mode Voltage

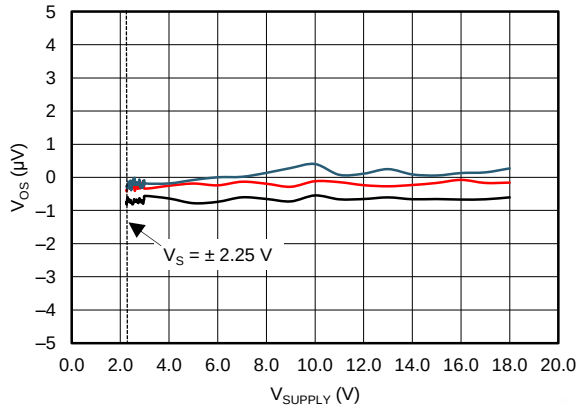


图 5. Offset Voltage vs Power Supply

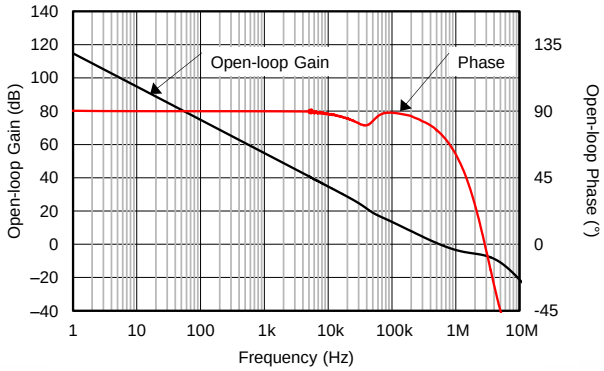


图 6. Open-Loop Gain and Phase vs Frequency

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

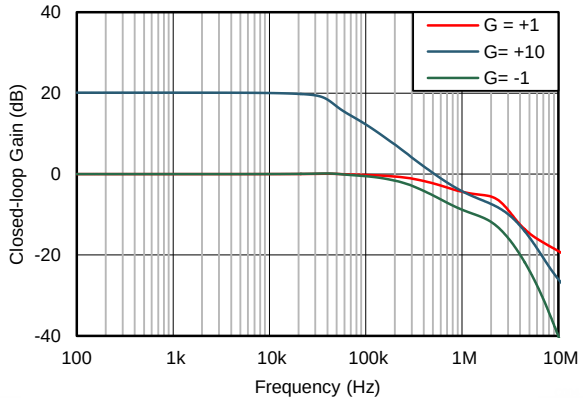


图 7. Closed-Loop Gain vs Frequency

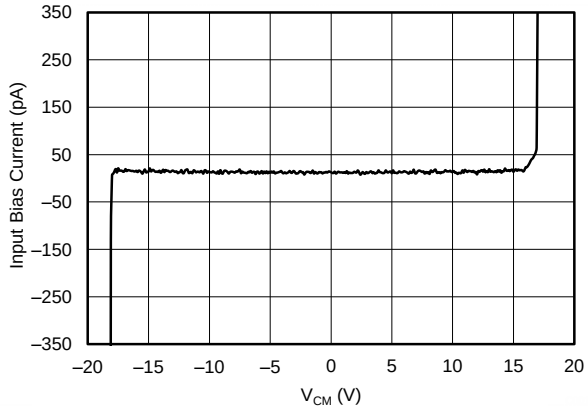


图 8. I_B vs Common-Mode Voltage

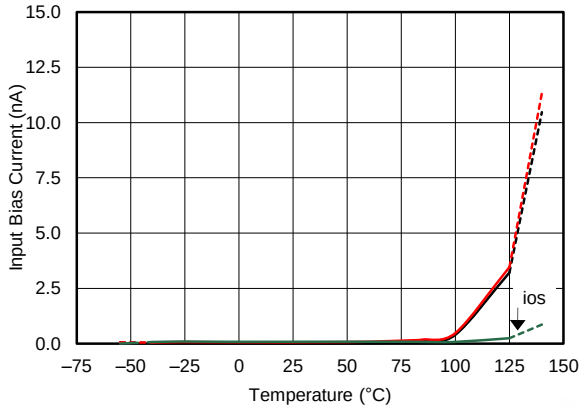


图 9. Input Bias Current vs Temperature

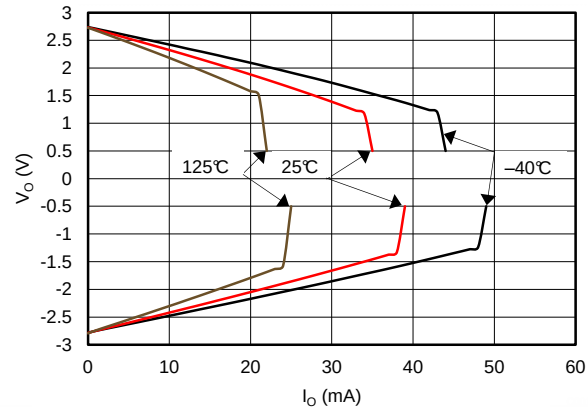


图 10. Output Voltage Swing vs Output Current

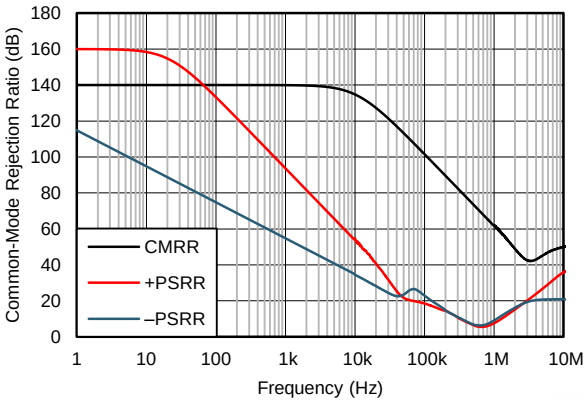


图 11. CMRR and PSRR vs Frequency (Referred-to-Input)

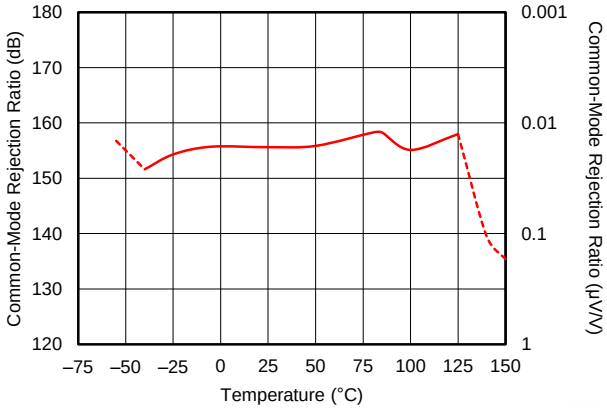


图 12. CMRR vs Temperature

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

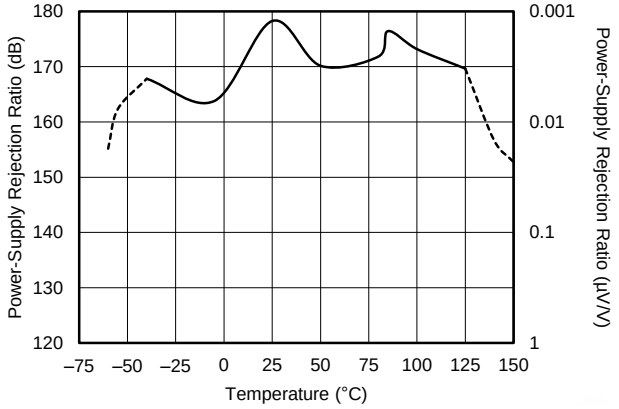


图 13. PSRR vs Temperature

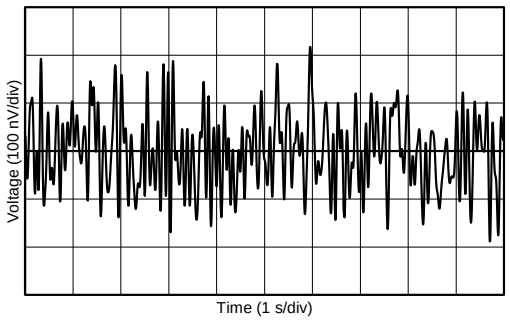


图 14. 0.1-Hz to 10-Hz Noise

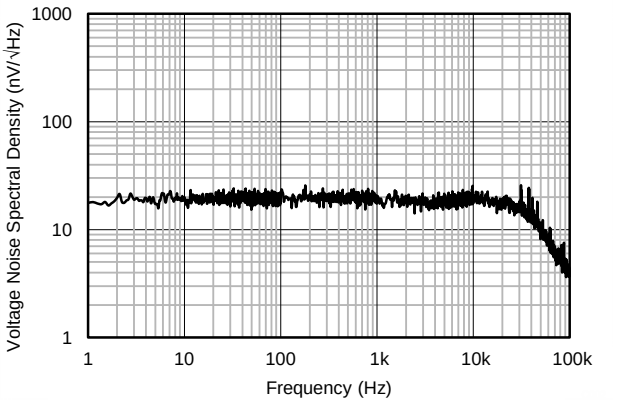


图 15. Input-Referred Voltage Noise Spectral Density vs Frequency (G = +101)

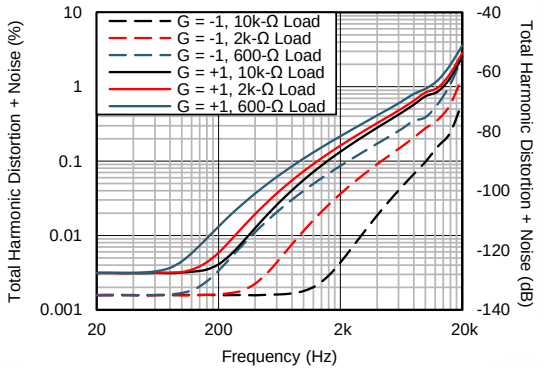


图 16. THD+N Ratio vs Frequency

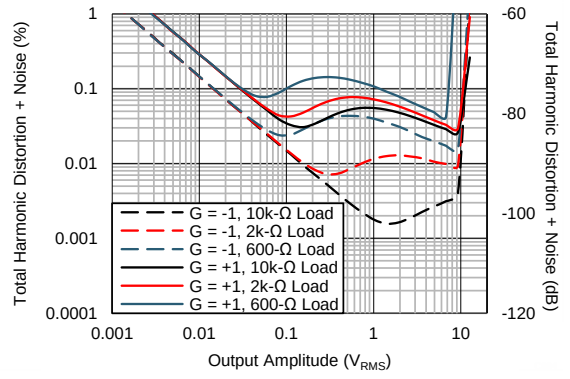


图 17. THD+N vs Output Amplitude

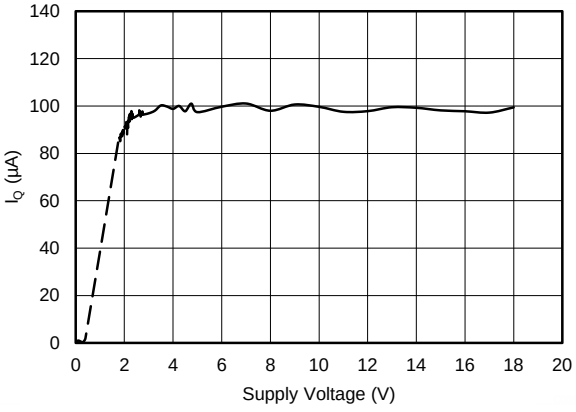


图 18. Quiescent Current vs Supply Voltage

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

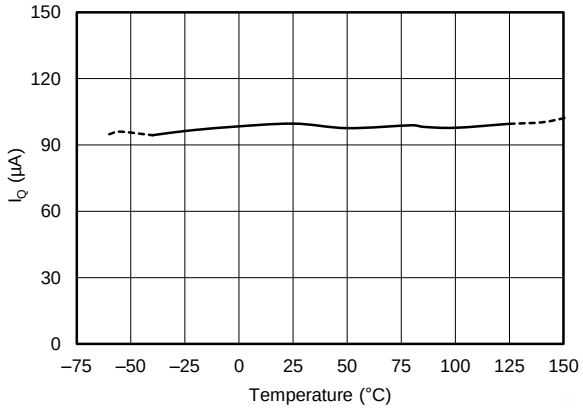


图 19. Quiescent Current vs Temperature

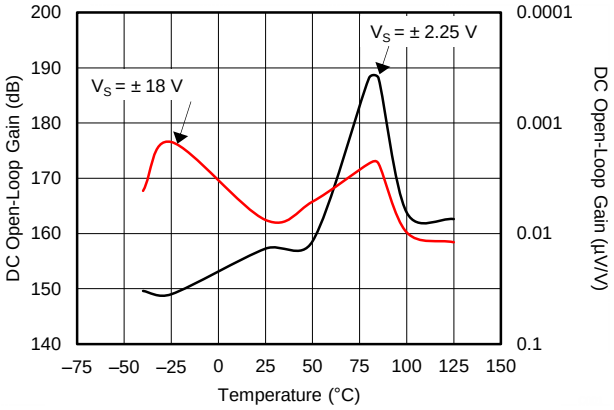


图 20. Open-Loop Gain vs Temperature

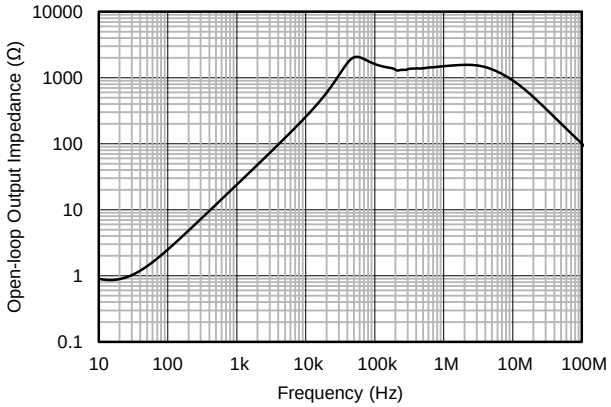


图 21. Open-Loop Output Impedance vs Frequency

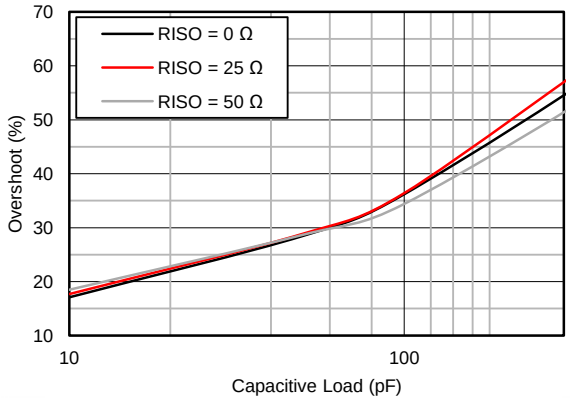


图 22. Small-Signal Overshoot vs Capacitive Load (G = +1) (10-mV Output Step)

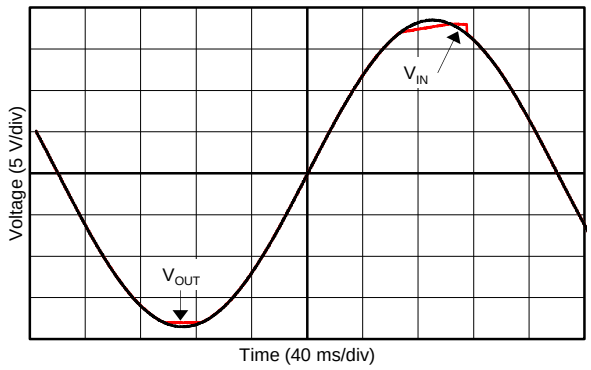


图 23. No Phase Reversal

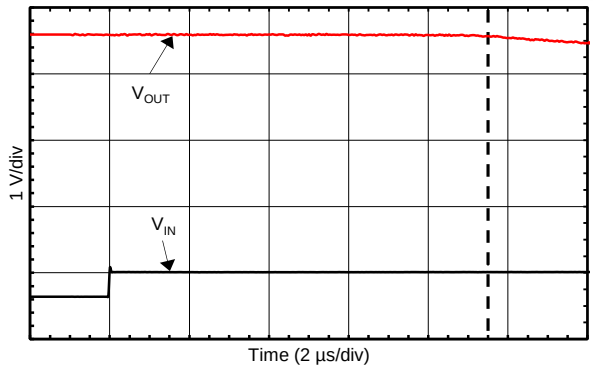


图 24. Positive Overload Recovery

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

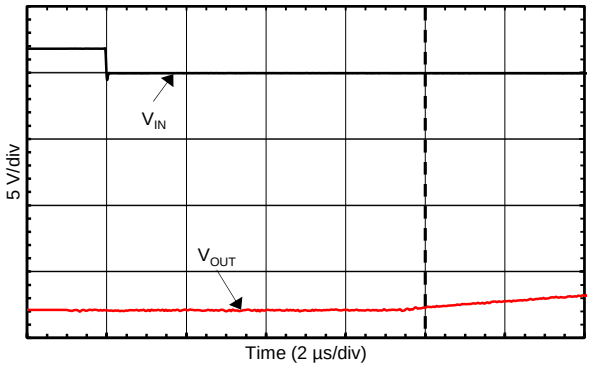


图 25. Negative Overload Recovery

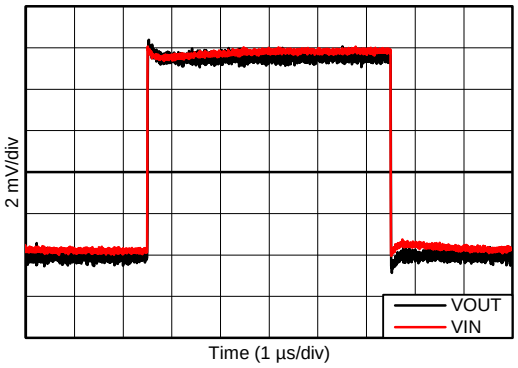


图 26. Small-Signal Step Response (100 mV)

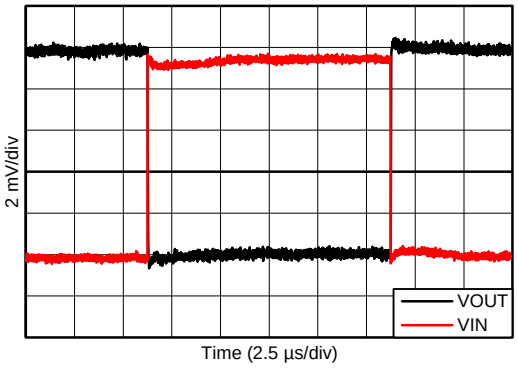


图 27. Small-Signal Step Response (100 mV)

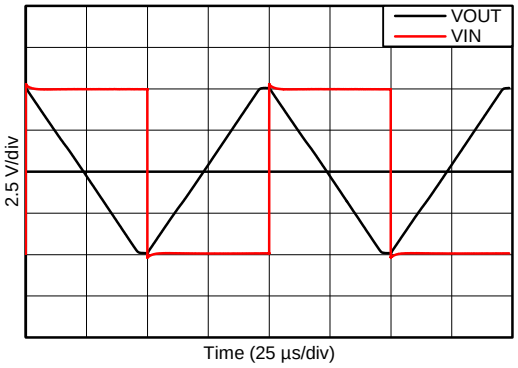


图 28. Large-Signal Step Response

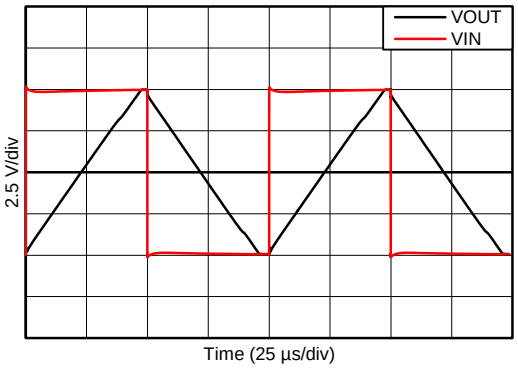


图 29. Large-Signal Step Response

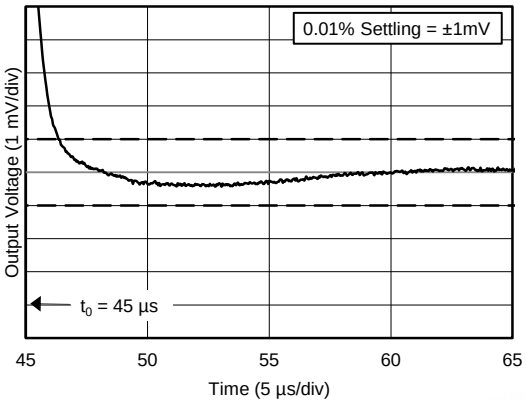


图 30. Large-Signal Settling Time (10-V Positive Step)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

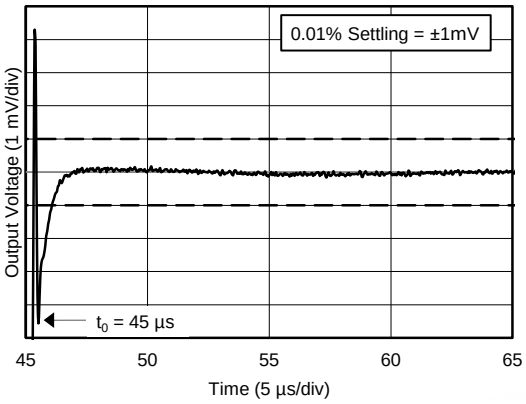


图 31. Large-Signal Settling Time (10-V Negative Step)

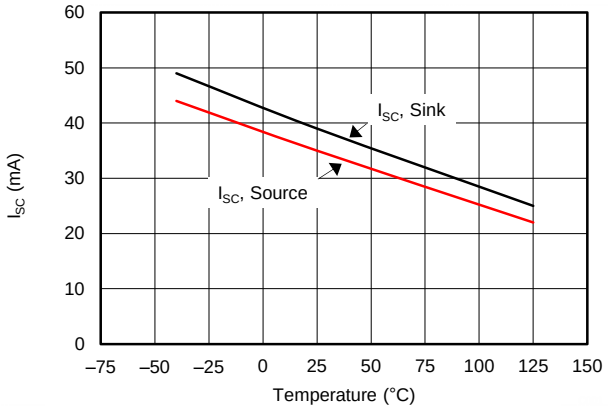


图 32. Short-Circuit Current vs Temperature

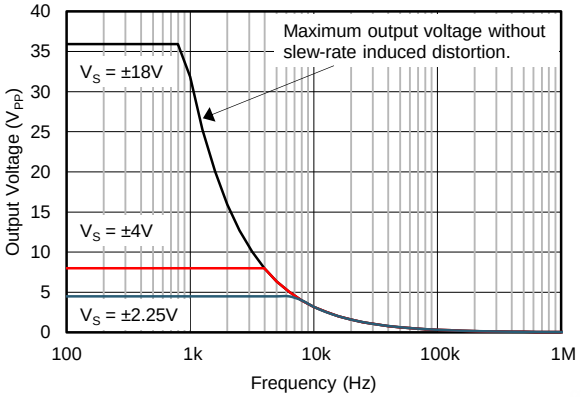


图 33. Maximum Output Voltage vs Frequency

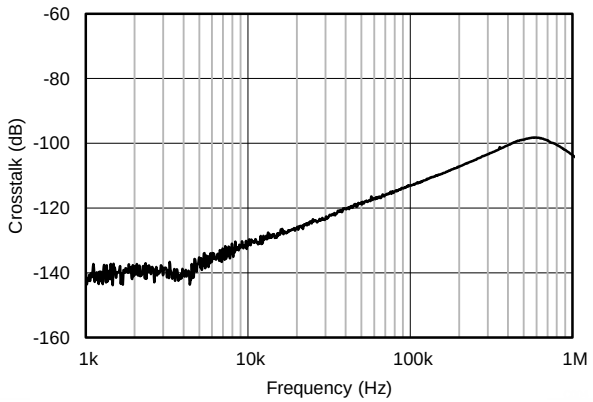


图 34. Crosstalk vs Frequency

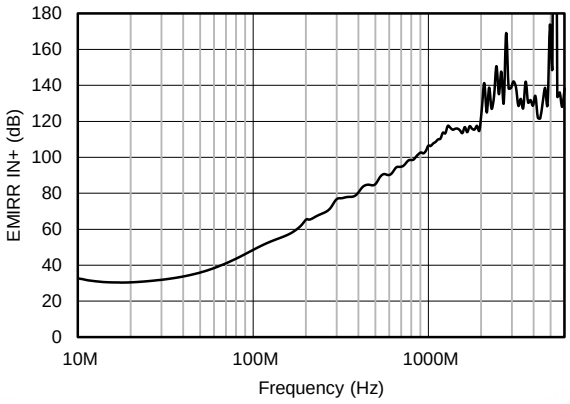


图 35. EMIRR IN+ vs Frequency

7 Detailed Description

7.1 Overview

The OPAx187 operational amplifier combines precision offset and drift with excellent overall performance, making the device ideal for many precision applications. The precision offset drift of only 0.001 µV/°C provides stability over the entire temperature range. In addition, this device offers excellent overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

The OPAx187 device is part of a family of zero-drift, low-power, rail-to-rail output operational amplifiers. These devices operate from 4.5 V to 36 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The zero-drift architecture provides ultra-low input offset voltage and near-zero input offset voltage drift over temperature and time. This choice of architecture also offers outstanding ac performance, such as ultra-low broadband noise and zero flicker noise.

7.2 Functional Block Diagram

图 36 shows a representation of the proprietary OPAx187 architecture. Functional blocks CHOP1 and CHOP2 operate such that the non-idealities of GM1 are cancelled while the input signal is left in-phase. The integrated notch filter of the OPAx187 family suppresses most of the auto-zero amplifier carrier.

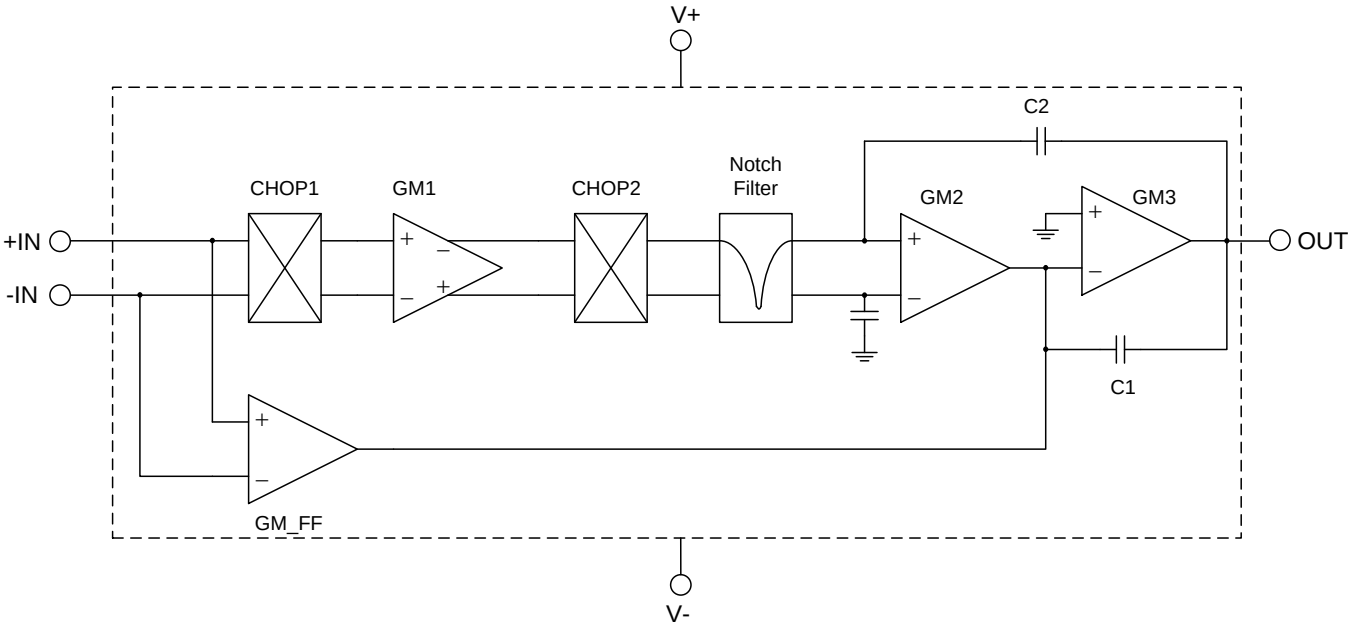


图 36. Functional Block Diagram

7.3 Feature Description

The OPAx187 is unity-gain stable and free from unexpected output phase reversal. This device uses a proprietary, periodic autocalibration technique to provide ultra-low input offset voltage and near zero input offset voltage drift over temp and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by making sure they are equal on both input pins. Other layout and design considerations include:

Use low thermoelectric-coefficient conditions (avoid dissimilar metals).

Thermally isolate components from power supplies or other heat sources.

Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Follow these guidelines to reduce the likelihood of junctions being at different temperatures, which may cause thermoelectric voltages of 0.1 µV/°C or higher, depending on the materials used.

7.3.1 Operating Characteristics

The OPAx187 device is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V). Many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

7.3.2 Phase-Reversal Protection

The OPAx187 device has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx187 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. 图 37 shows this performance.

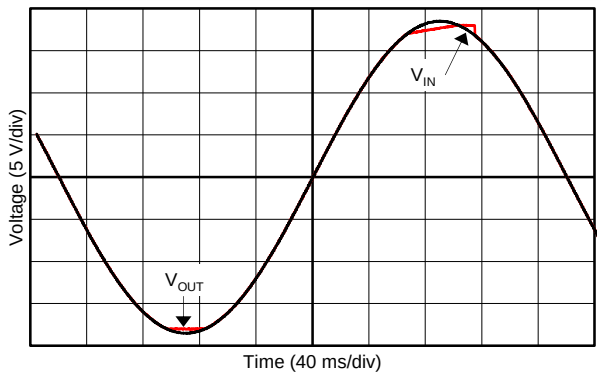


图 37. No Phase Reversal

7.3.3 Input Bias Current Clock Feedthrough

Zero-drift amplifiers, such as the OPAx187, use switching on their inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce very short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents them from being amplified, however they may be coupled to the output of the amplifier through the feedback network. The most effective method to prevent transients in the input bias current from producing additional noise at the amplifier output is to use a low-pass filter such as an RC network.

7.3.4 Internal Offset Correction

The OPAx187 op amp uses an auto-calibration technique with a time-continuous 125-kHz op amp in the signal path. This amplifier is zero-corrected every 22 µs using a proprietary technique. Upon power-up, the amplifier requires approximately 100 µs to achieve the specified V_{OS} accuracy. This design has no aliasing or flicker noise.

Feature Description (接下页)

7.3.5 EMI Rejection

The OPAx187 device uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx187 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 38 shows the results of this testing on the OPAx187. 表 2 lists the EMIRR IN+ values for the OPAx187 at particular frequencies commonly encountered in real-world applications. Applications listed in 表 2 may be centered on or operated near the particular frequency shown. Detailed information can also be found in *EMI Rejection Ratio of Operational Amplifiers*, available for download from www.ti.com.

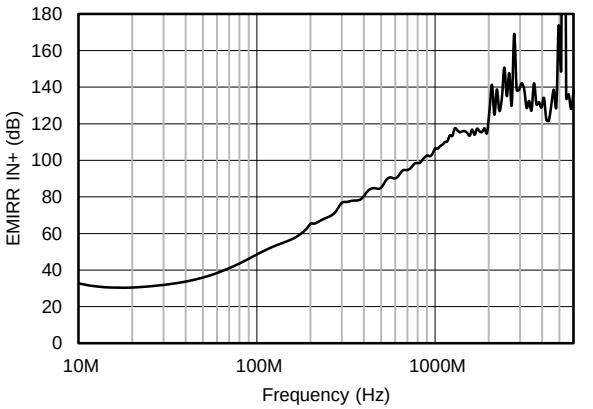


图 38. EMIRR Testing

表 2. OPAx187 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION/ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	81.8 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	102.7 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	115.4 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	150.7 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	142.0 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	173.8 dB

7.3.6 Capacitive Load and Stability

The device dynamic characteristics are optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the amplifier phase margin and can lead to gain peaking or oscillations. As a result, larger capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. 图 39 illustrates small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, for details of analysis techniques and application circuits, refer to *Feedback Plots Define Op Amp AC Performance*, available for download from www.ti.com.

G = 1, R_L = 10 kΩ, 10-mV Output Step

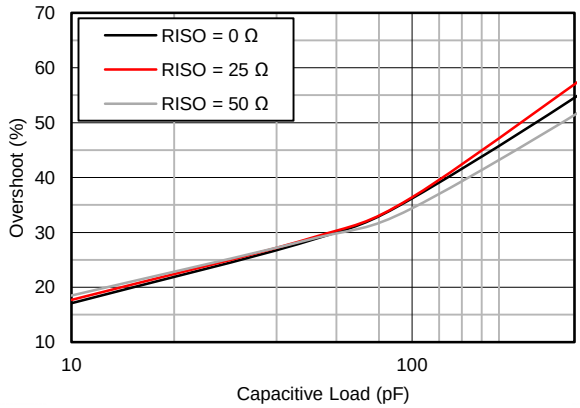


图 39. Small-Signal Overshoot Versus Capacitive Load

7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See 图 40 for an illustration of the ESD circuits contained in the OPAx187 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx187 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

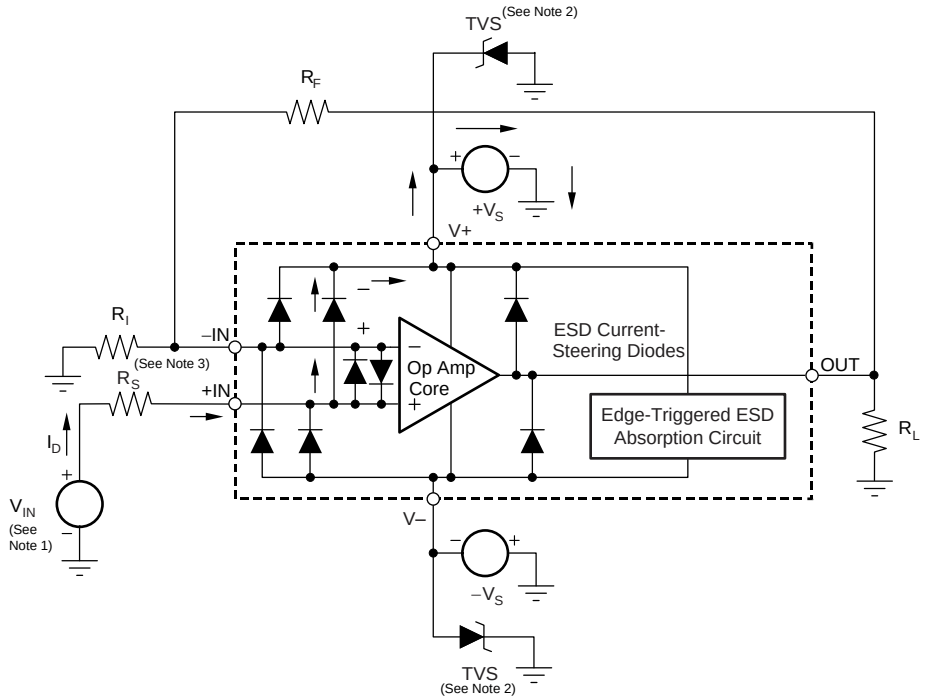
When the operational amplifier connects into a circuit (as shown in 图 40), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

图 40 shows a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current-steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, external TVS (Transient Voltage Suppressor) diodes may be added to the supply pins, as shown in 图 40. The TVS voltage must be selected such that the diode does not turn on during normal operation. However, the TVS voltage should be low enough so that the TVS diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



NOTE 1: $V_{IN} = +V_S + 500$ mV.

NOTE 2: TVS: $+V_{S(max)} > V_{TVSBR\ (min)} > +V_S$.

NOTE 3: Suggested value is approximately 1 kΩ.

图 40. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

The OPAx187 input terminals are protected from excessive differential voltage with back-to-back diodes, as shown in 图 40. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPAx187. 图 40 shows an example configuration that implements a current-limiting feedback resistor.

7.4 Device Functional Modes

The OPAx187 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx187 is 36 V (±18 V).

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx187 operational amplifier combines precision offset and drift with excellent overall performance, making it ideal for many precision applications. The precision offset drift of only 0.001 µV/°C provides stability over the entire temperature range. In addition, the device pairs excellent CMRR, PSRR, and A_{OL} dc performance with outstanding low-noise operation. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

The following application examples highlight only a few of the circuits where the OPAx187 can be used.

8.2 Typical Applications

8.2.1 High-Side Voltage-to-Current (V-I) Converter

The circuit shown in 图 41 is a high-side voltage-to-current (V-I) converter. The converter translates an input voltage of 0 V to 2 V into an output current of 0 mA to 100 mA. 图 42 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA2187 facilitate excellent dc accuracy for the circuit.

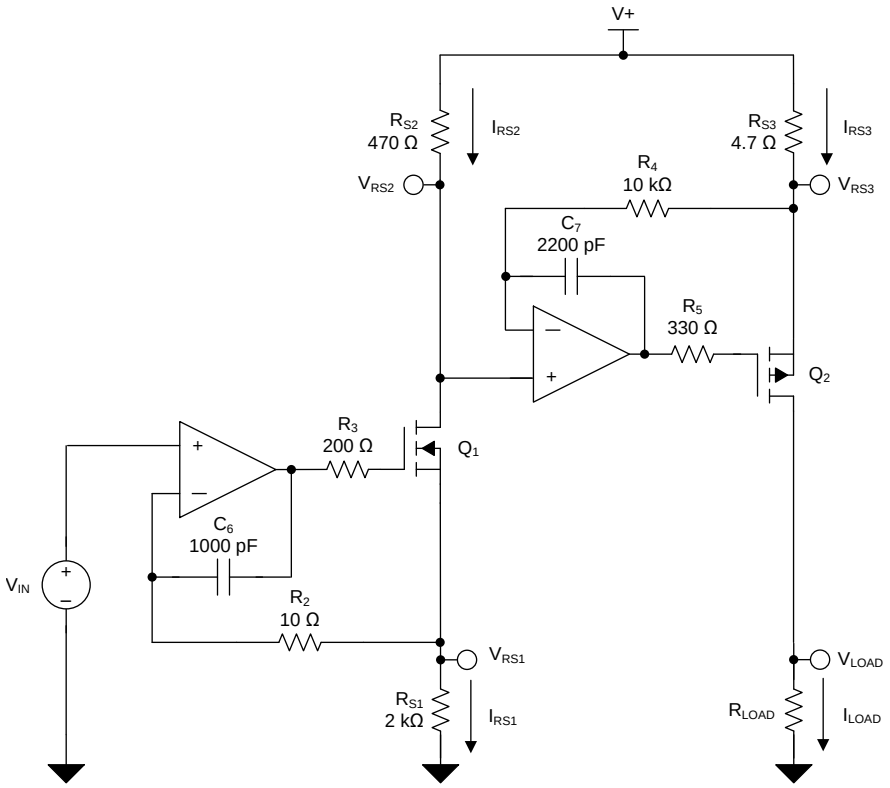


图 41. High-Side Voltage-to-Current (V-I) Converter

8.2.1.1 Design Requirements

The design requirements are:

Typical Applications (接下页)

- Supply voltage: 5 V DC
- Input: 0 V to 2 V DC
- Output: 0 mA to 100 mA DC

8.2.1.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors, R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

This application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPAx187 CMOS operational amplifier is a high-precision, ultra-low offset, ultra-low drift amplifier, optimized for wide-voltage, single-supply operation, with an output swing to within 5 mV of the positive rail. The OPAx187 family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making this device appropriate for precise dc control. The rail-to-rail output stage of the OPAx187 makes sure that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

A detailed error analysis, design procedure, and additional measured results are given in reference design TIPD102, a step-by-step process to design a *High-Side Voltage-to-Current (V-I) Converter*.

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIPD102, *High-Side Voltage-to-Current (V-I) Converter* (SLAU502).

8.2.1.3 Application Curve

图 42 shows the measured transfer function for the high-side voltage-to-current converter shown in 图 41.

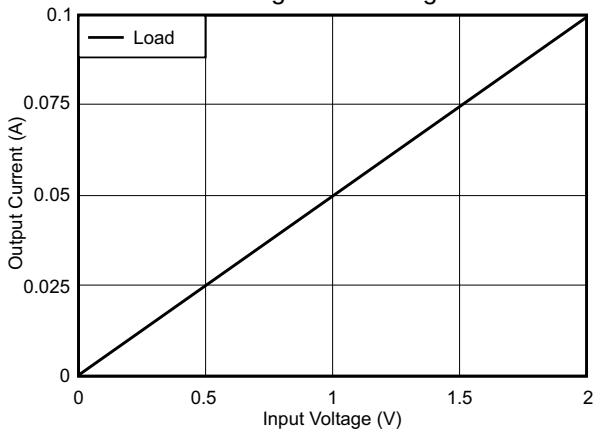


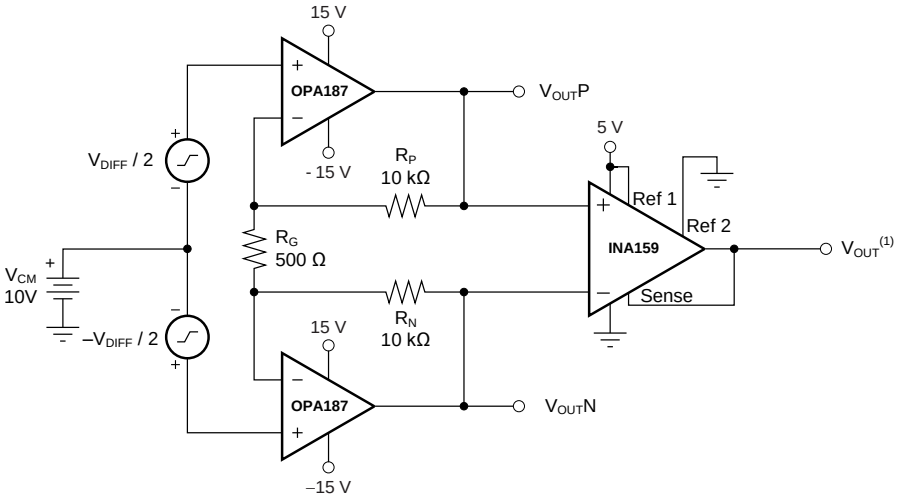
图 42. Measured Transfer Function for High-Side V-I Converter

8.2.2 Discrete INA + Attenuation for ADC With 3.3-V Supply

注

The TINA-TI files shown in the following sections require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

图 43 shows an example of how the OPAx187 is used as a high-voltage, high-impedance front-end for a precision, discreet instrumentation amplifier with attenuation. The INA159 provides the attenuation that allows this circuit to easily interface with 3.3-V or 5-V analog-to-digital converters (ADCs). Click the following link download the TINA-TI file: Discrete INA.



(1) $V_{OUT} = V_{DIFF} \times (41 / 5) + (Ref 1) / 2$.

图 43. Discrete INA + Attenuation for ADC With 3.3-V Supply

8.2.3 Bridge Amplifier

图 44 shows the basic configuration for a bridge amplifier. Click the following link to download the TINA-TI file: Bridge Amplifier Circuit.

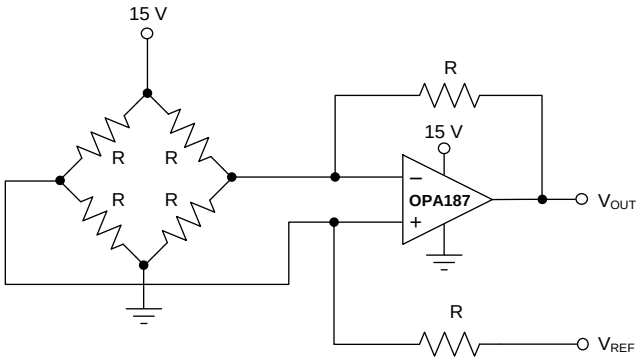


图 44. Bridge Amplifier

8.2.4 Low-Side Current Monitor

图 45 shows the OPAx187 configured in a low-side current-sensing application. The load current (I_{LOAD}) creates a voltage drop across the shunt resistor (R_{SHUNT}). This voltage is amplified by the OPAx187, with a gain of 201. The load current is set from 0 A to 500 mA, which corresponds to an output voltage range from 0 V to 10 V. The output range can be adjusted by changing the shunt resistor or gain of the configuration. Click the following link to download the TINA-TI file: Current-Sensing Circuit.

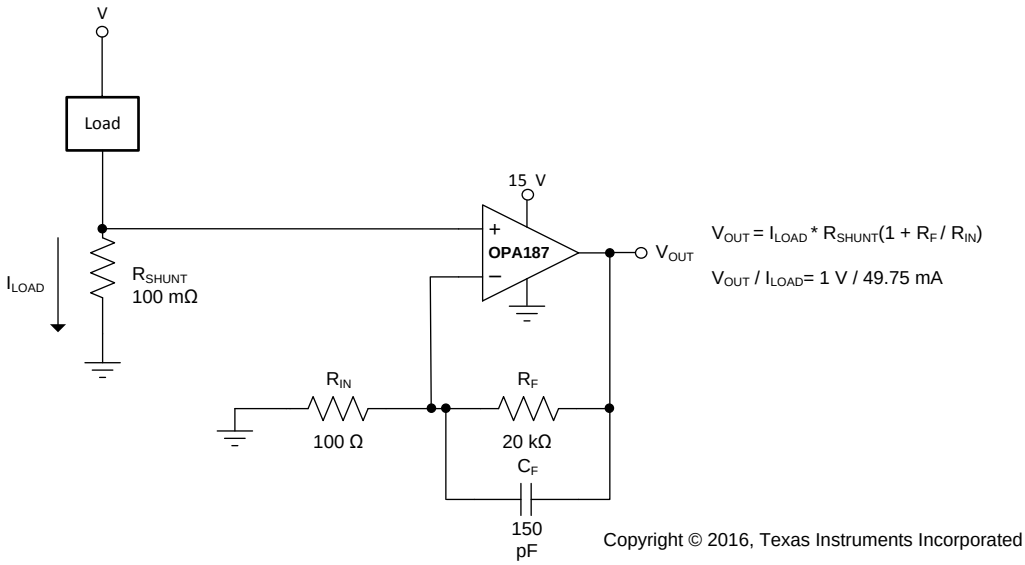


图 45. Low-Side Current Monitor

8.2.5 Programmable Power Supply

图 46 shows the OPAx187 configured as a precision programmable power supply using the 16-bit, voltage output DAC8581 and the OPA548 high-current amplifier. This application amplifies the digital-to-analog converter (DAC) voltage by a value of five, and handles a large variety of capacitive and current loads. The OPAx187 in the front-end provides precision and low drift across a wide range of inputs and conditions. Click the following link to download the TINA-TI file: Programmable Power-Supply Circuit.

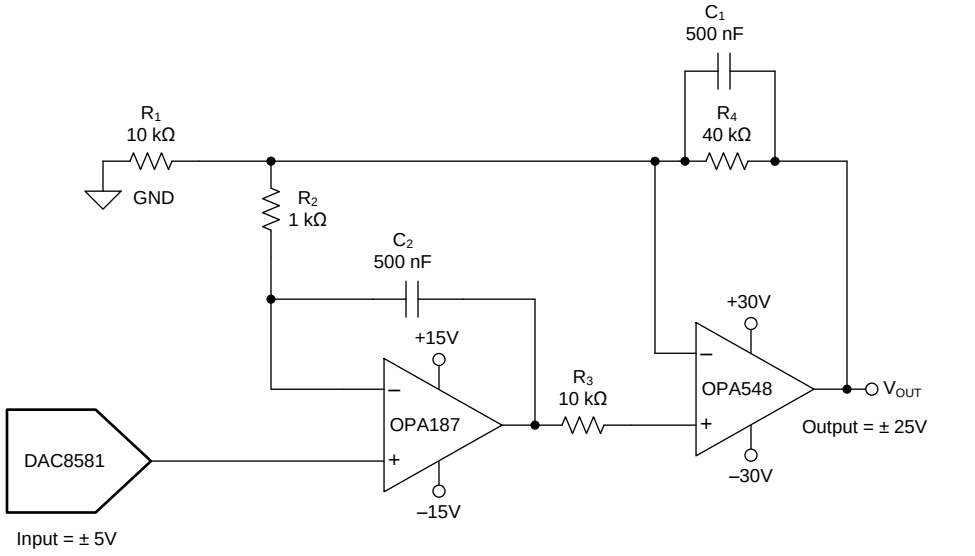
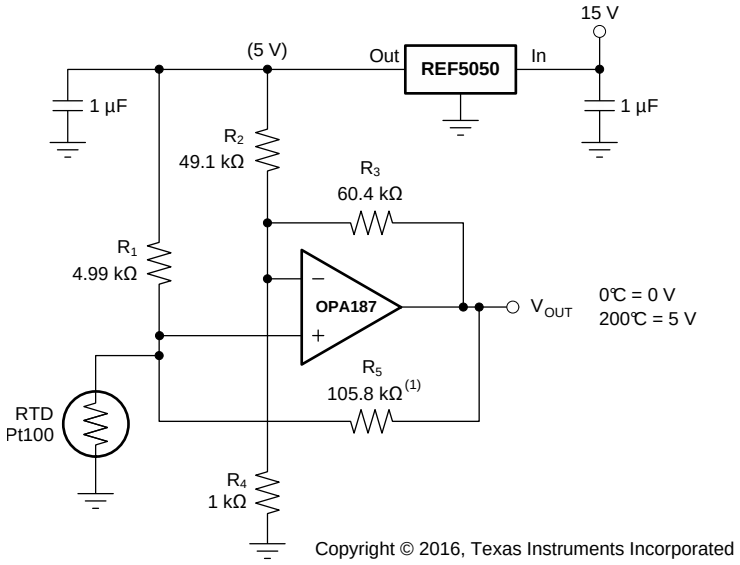


图 46. Programmable Power Supply

8.2.6 RTD Amplifier With Linearization

See *Analog Linearization Of Resistance Temperature Detectors*, for an in-depth analysis of 图 47. Click the following link to download the TINA-TI file: RTD Amplifier With Linearization.



(1) R_5 provides positive-varying excitation to linearize output.

图 47. RTD Amplifier With Linearization

9 Power Supply Recommendations

The OPAx187 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 40 V can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

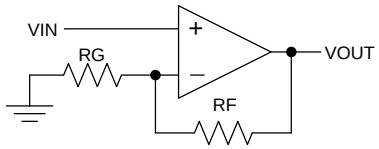
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Low-ESR, 0.1-µF ceramic bypass capacitors must be connected between each supply pin and ground; place the capacitors as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply lines as possible.
- A ground plane helps distribute heat and reduces EMI noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example



(Schematic Representation)

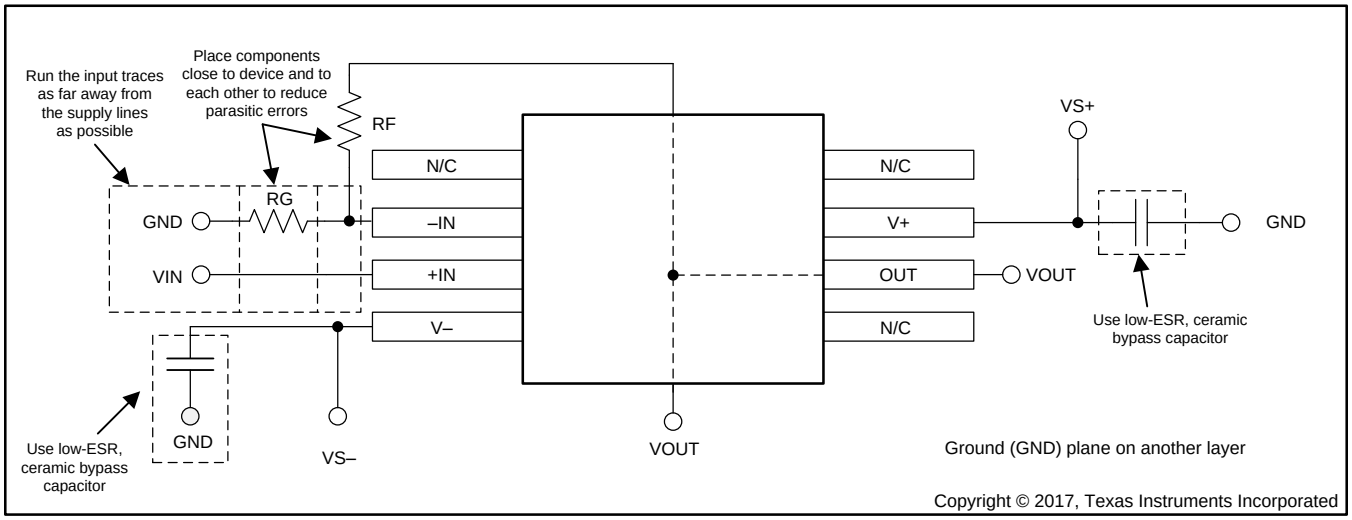


图 48. Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。 TINA-TI™是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流 (DC)、瞬态和频域分析以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器为用户提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

11.1.1.2 TI 高精度设计

TI 高精度设计的模拟设计方案是由 TI 公司高精度模拟实验室设计 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。欲获取 TI 高精度设计，请访问 http://www.ti.com.cn/ww/analog/precision-designs/。

11.1.1.3 WEBENCH® Filter Designer

WEBENCH® Filter Designer 是一款简单、功能强大且便于使用的有源滤波器设计程序。借助 WEBENCH 滤波设计器，用户可使用精选 TI 运算放大器和 TI 供应商合作伙伴提供的无源组件来打造最佳滤波器设计方案。

WEBENCH 设计中心以基于网络的工具形式提供 WEBENCH® Filter Designer，用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《运算放大器增益稳定性，第 3 部分：交流增益误差分析》*
- 德州仪器 (TI)，*《运算放大器增益稳定性，第 2 部分：直流增益误差分析》*
- 德州仪器 (TI)，*《在全差分有源滤波器中使用无限增益、MFB 滤波器拓扑》*
- 德州仪器 (TI)，*《运算放大器性能分析》*
- 德州仪器 (TI)，*《运算放大器的单电源运行》*
- 德州仪器 (TI)，*《放大器调优》*
- 德州仪器 (TI)，*《无铅组件涂层的储存寿命评估》*

11.3 相关链接

表 3 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具与软件，以及申请样片或购买产品的快速链接。

表 3. 相关链接

器件	产品文件夹	样片和购买	技术文档	工具与软件	支持和社区
OPA187	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA2187	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA4187	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.4 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 按钮注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.6 商标

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
DesignSoft, TINA are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.8 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA187ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA187	Samples
OPA187IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CUV	Samples
OPA187IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CUV	Samples
OPA187IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1D96	Samples
OPA187IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1D96	Samples
OPA187IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA187	Samples
OPA2187ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2187	Samples
OPA2187IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16TV	Samples
OPA2187IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16TV	Samples
OPA2187IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2187	Samples
OPA4187ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4187	Samples
OPA4187IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4187	Samples
OPA4187IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4187	Samples
OPA4187IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4187	Samples
OPA4187IRUMR	ACTIVE	WQFN	RUM	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 4187	Samples
OPA4187IRUMT	ACTIVE	WQFN	RUM	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA 4187	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

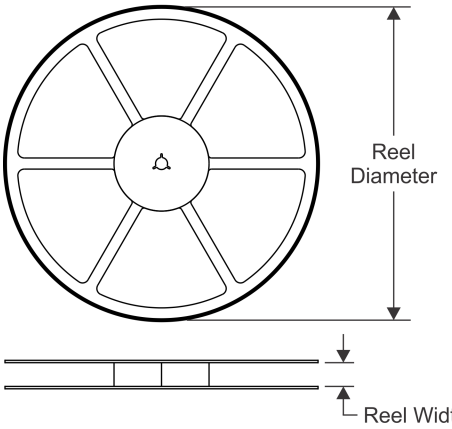
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

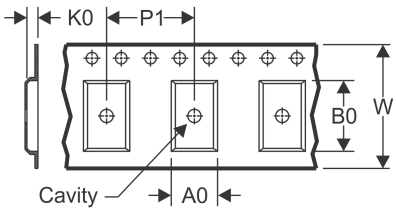
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

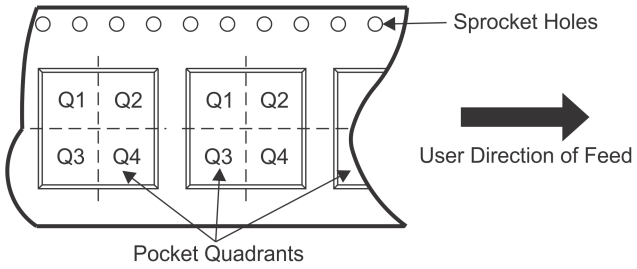


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

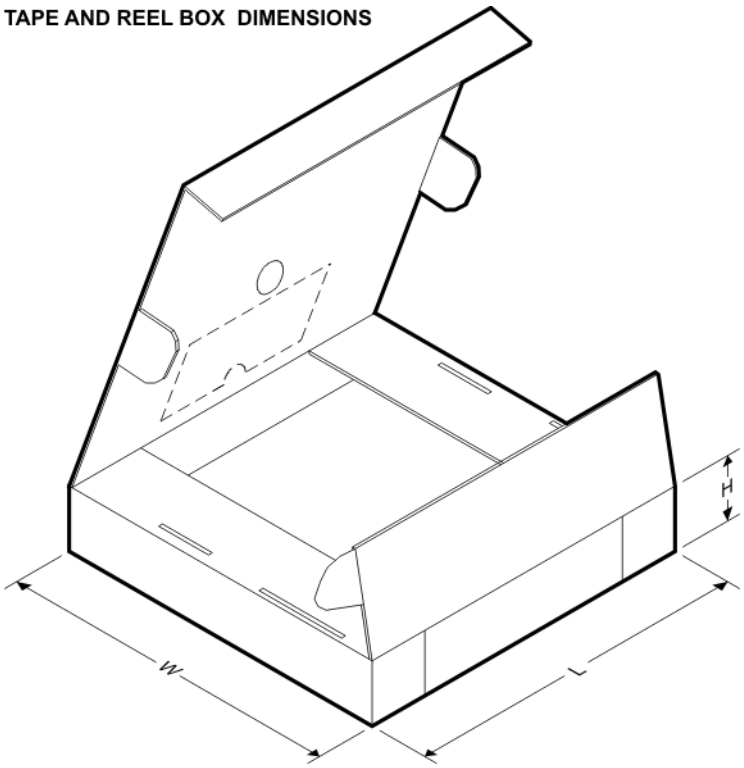
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA187IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA187IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA187IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA187IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA187IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2187IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2187IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2187IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4187IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4187IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4187IRUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA4187IRUMT	WQFN	RUM	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

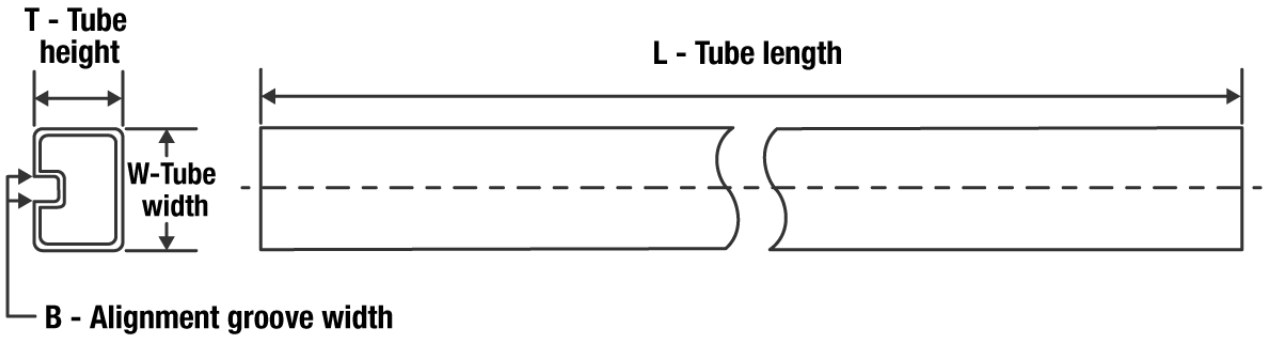
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA187IDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA187IDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA187IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA187IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA187IDR	SOIC	D	8	2500	853.0	449.0	35.0
OPA2187IDGKR	VSSOP	DGK	8	2500	853.0	449.0	35.0
OPA2187IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2187IDR	SOIC	D	8	2500	853.0	449.0	35.0
OPA4187IDR	SOIC	D	14	2500	853.0	449.0	35.0
OPA4187IPWR	TSSOP	PW	14	2000	853.0	449.0	35.0
OPA4187IRUMR	WQFN	RUM	16	3000	367.0	367.0	35.0
OPA4187IRUMT	WQFN	RUM	16	250	210.0	185.0	35.0

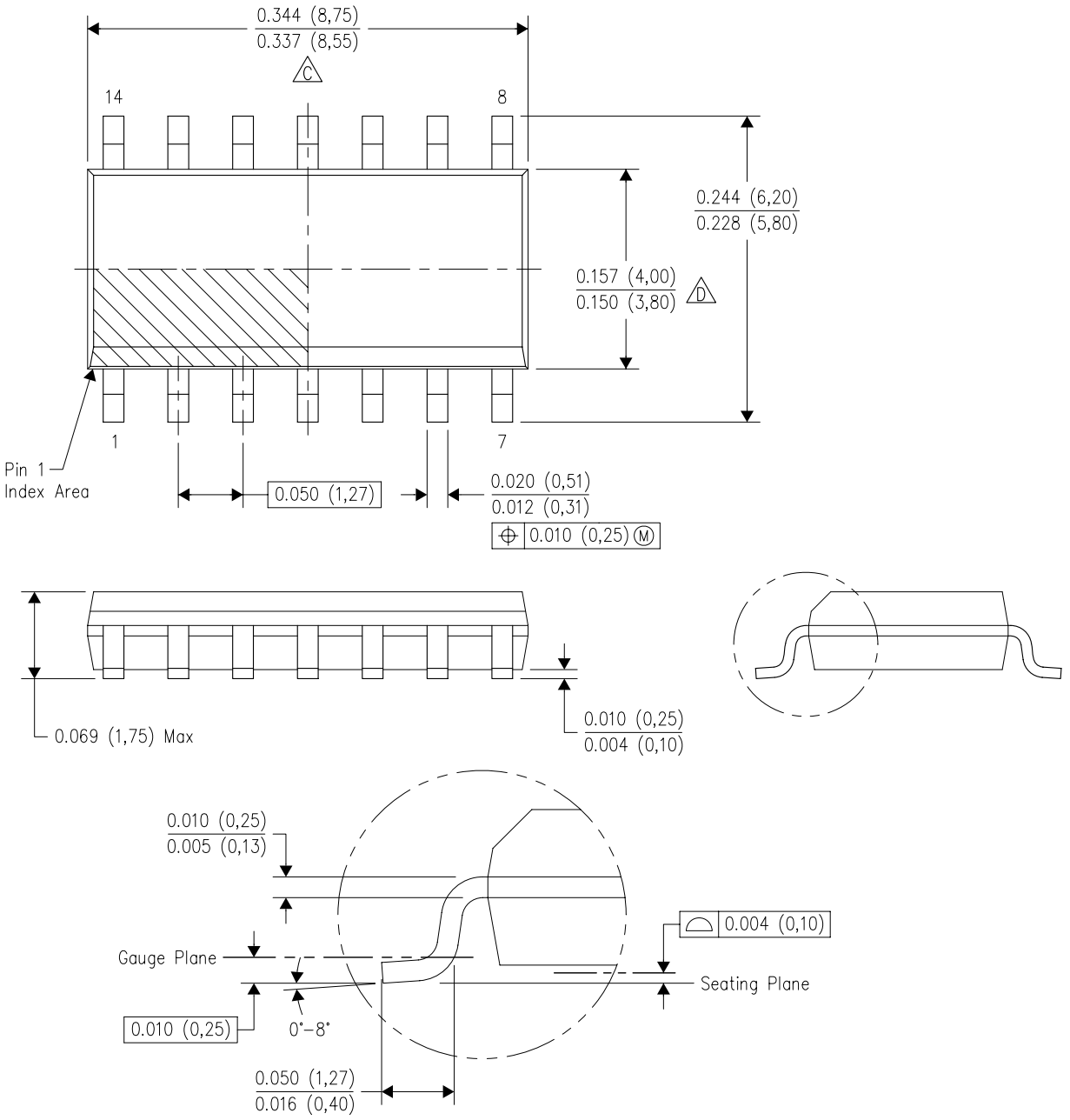
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA187ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2187ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA4187ID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4187IPW	PW	TSSOP	14	90	530	10.2	3600	3.5

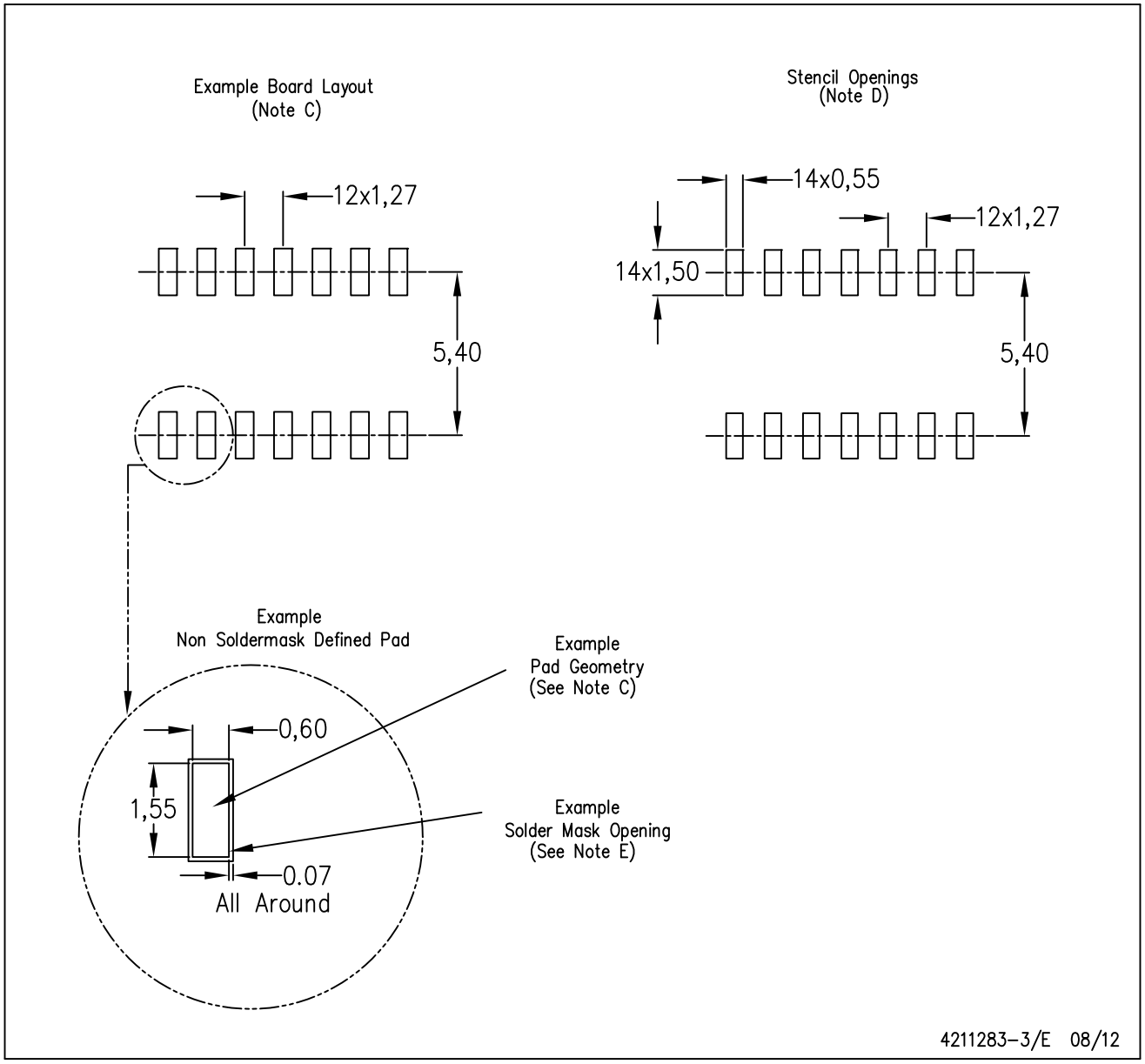
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

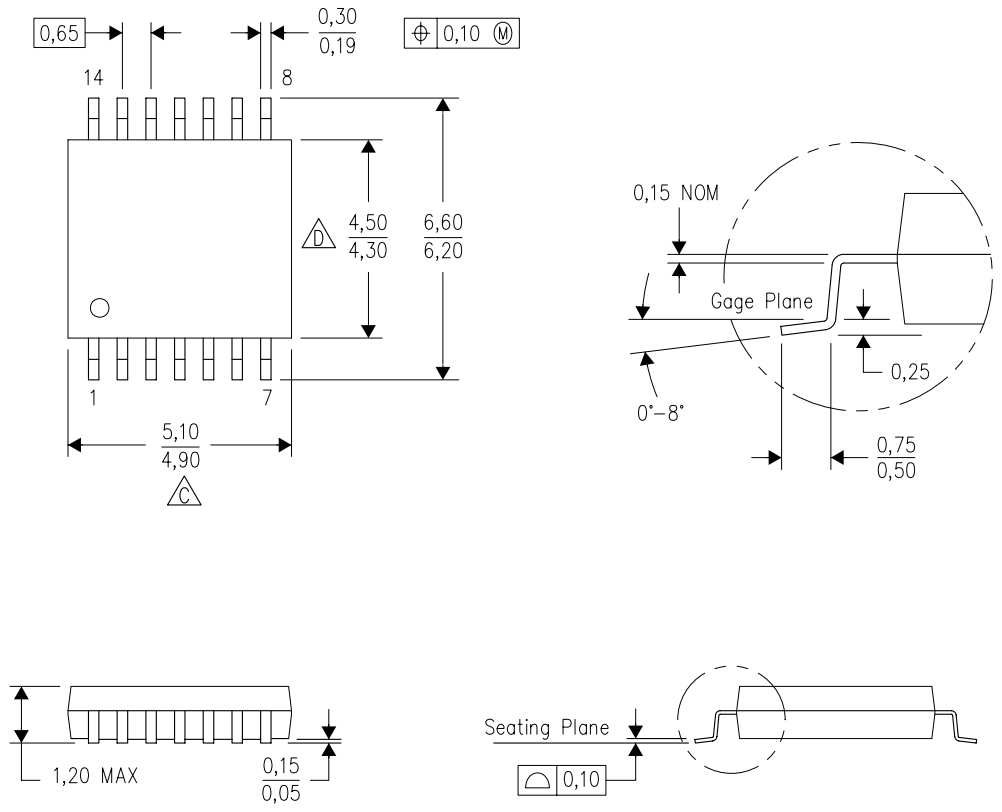
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

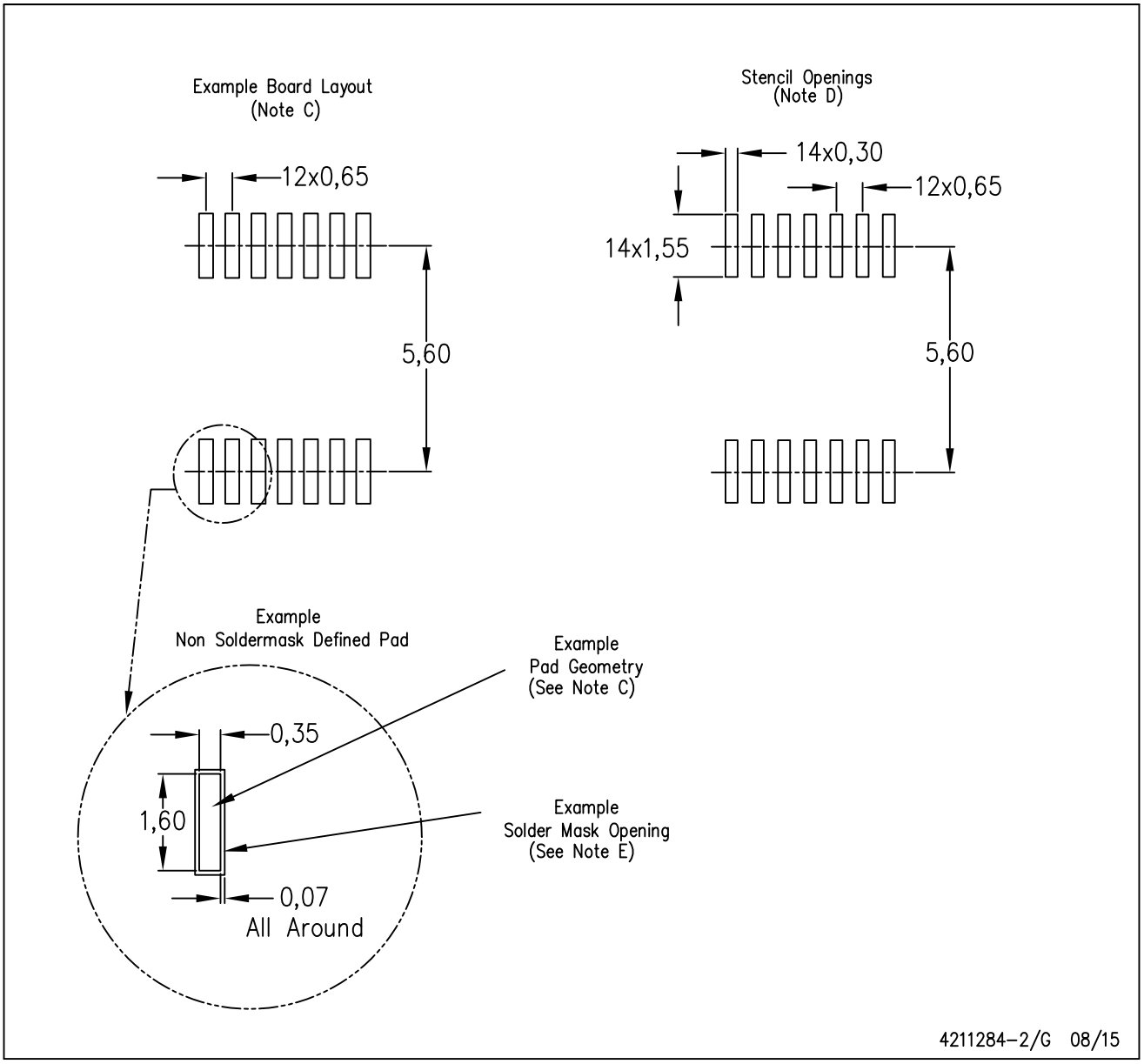
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



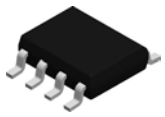
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

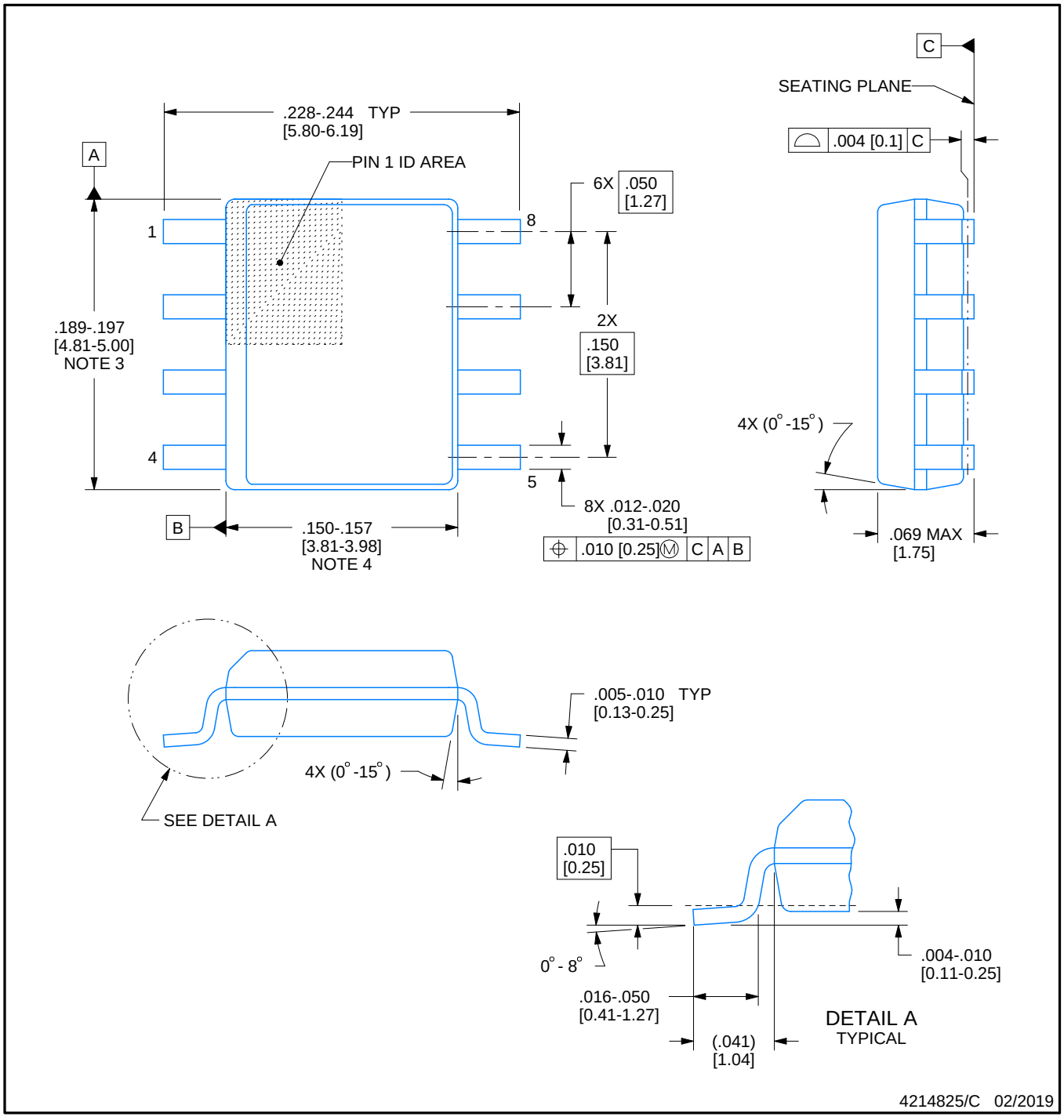


PACKAGE OUTLINE

D0008A

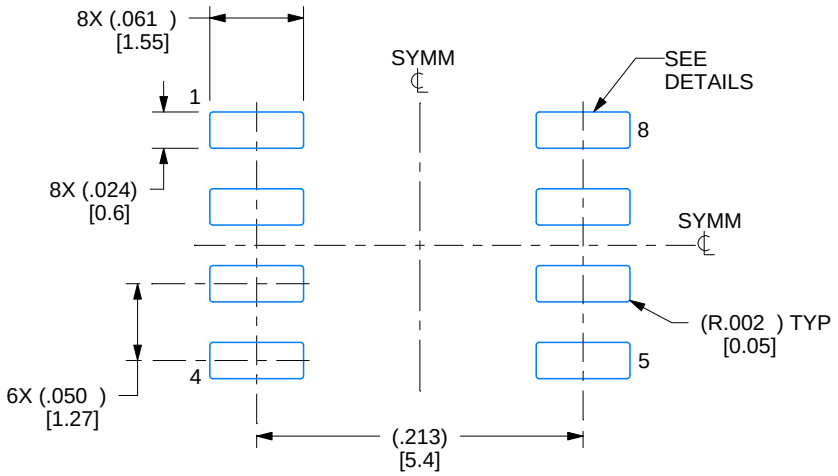
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

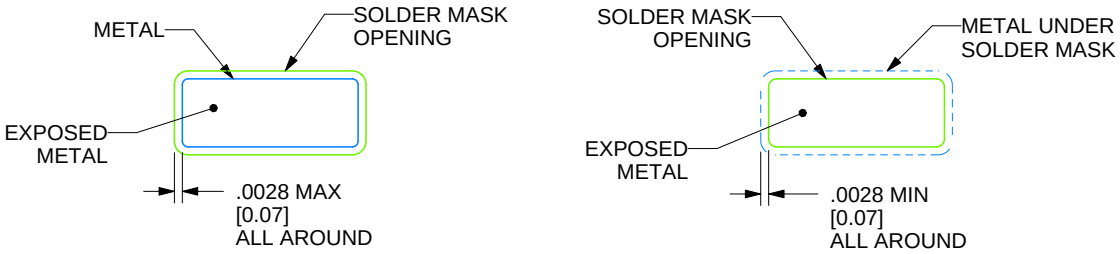


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

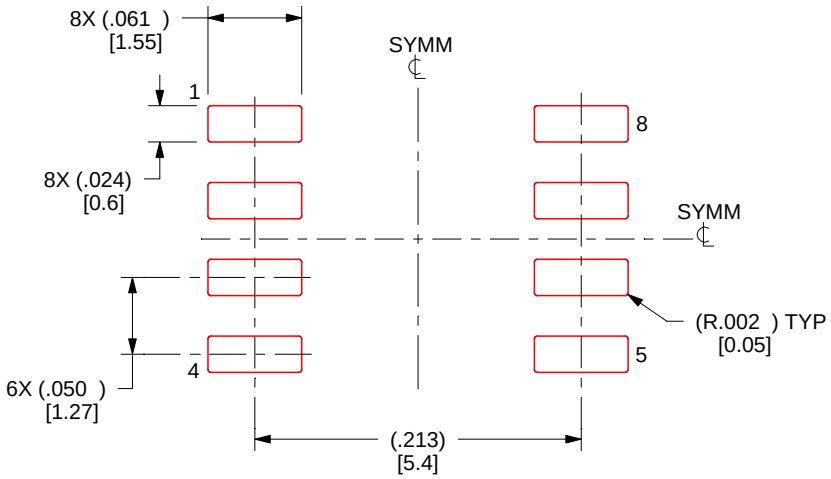
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



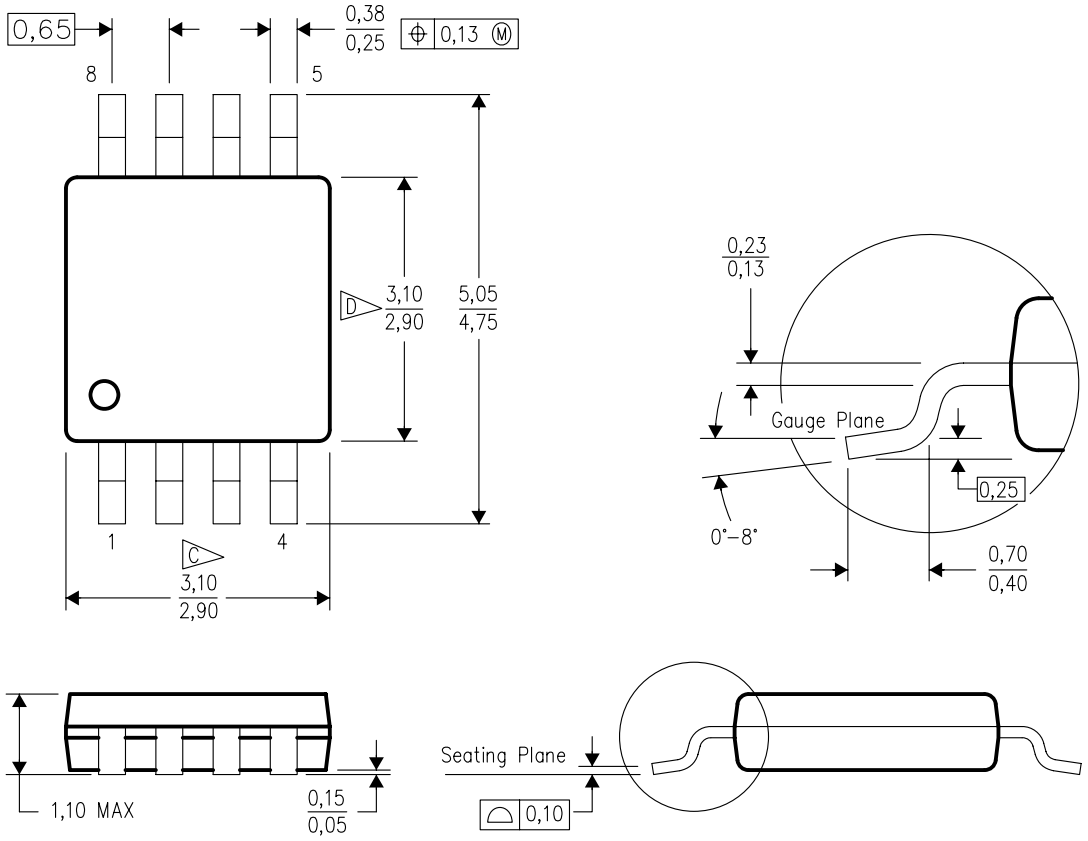
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

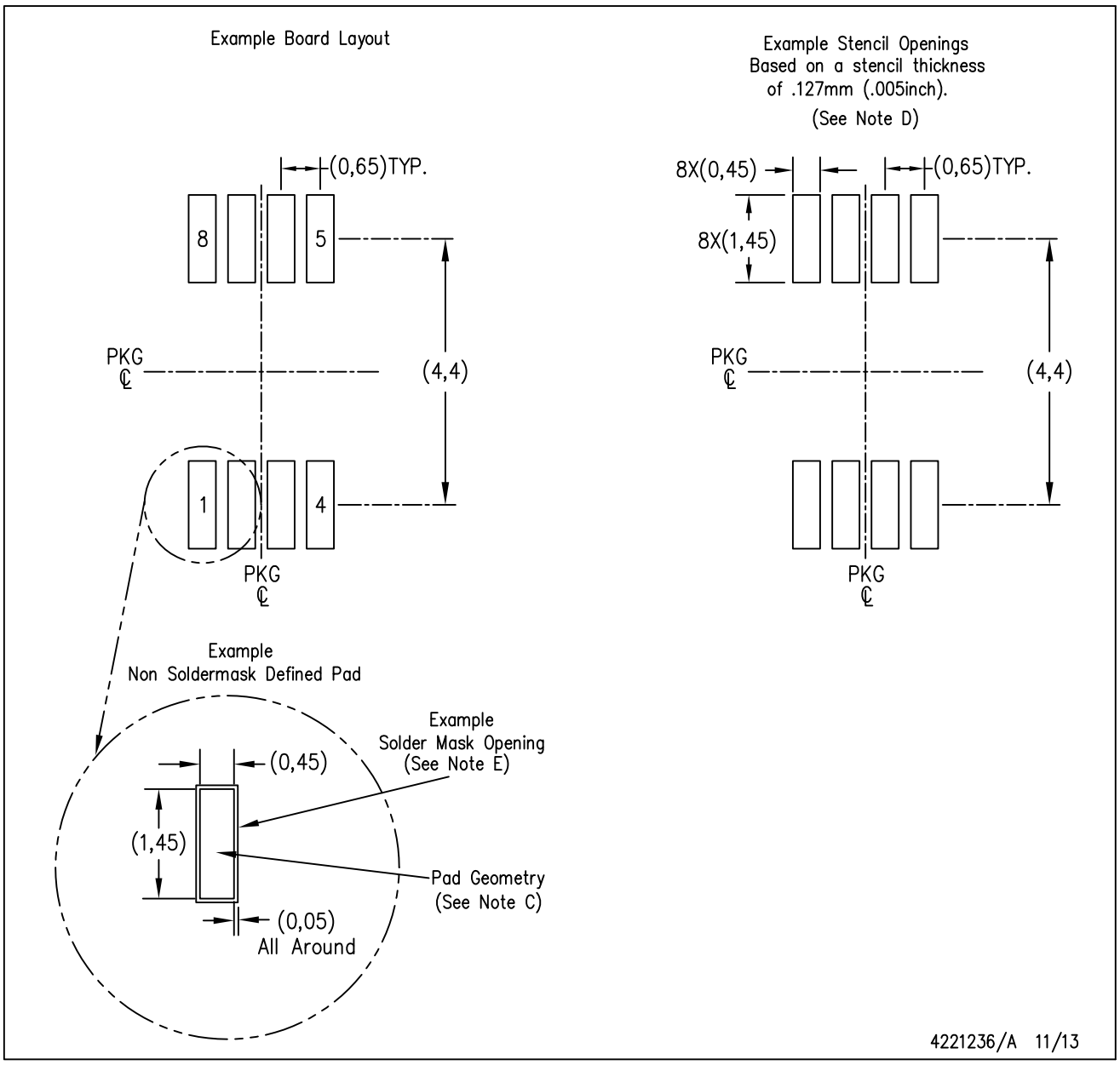
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



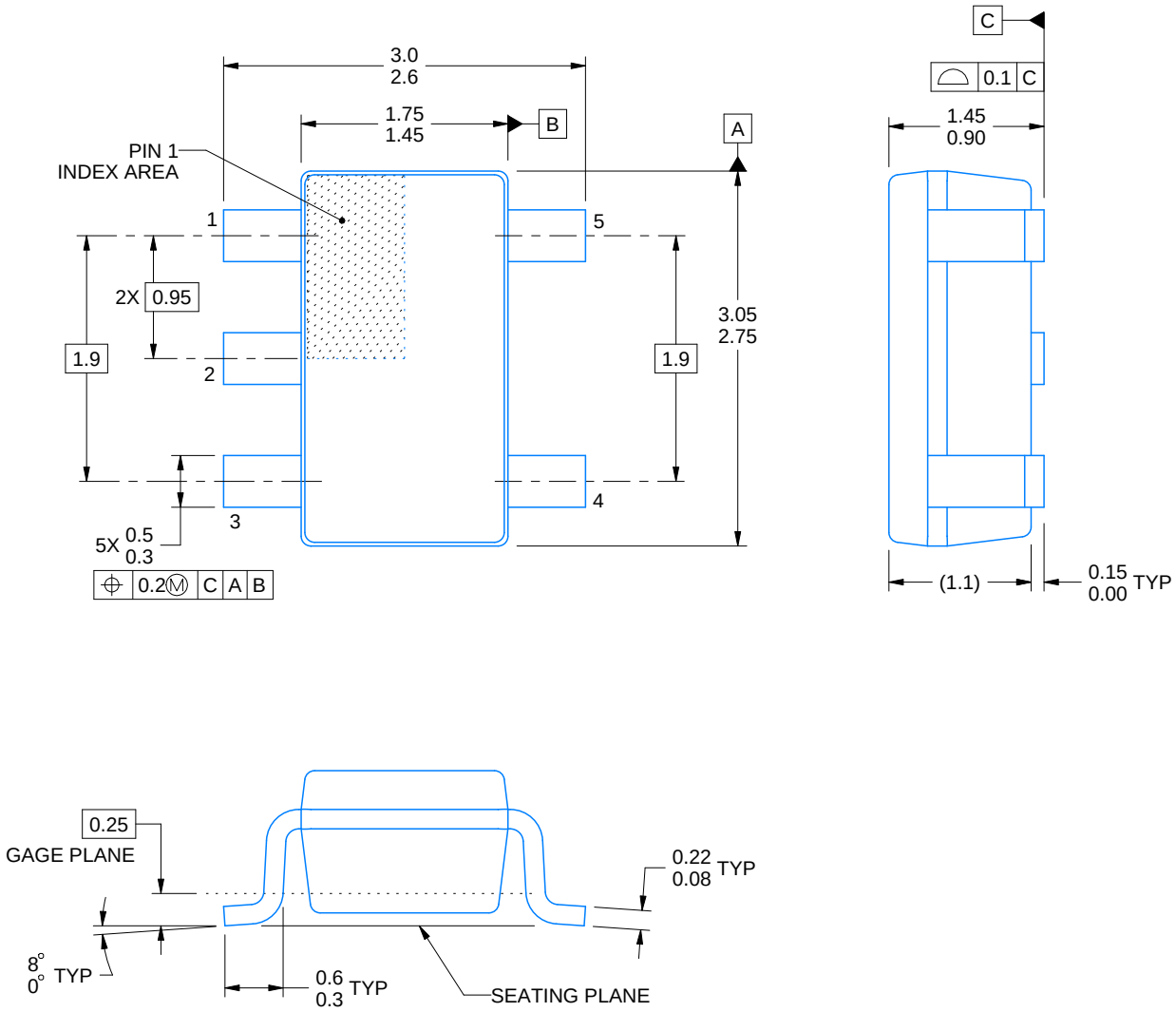
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

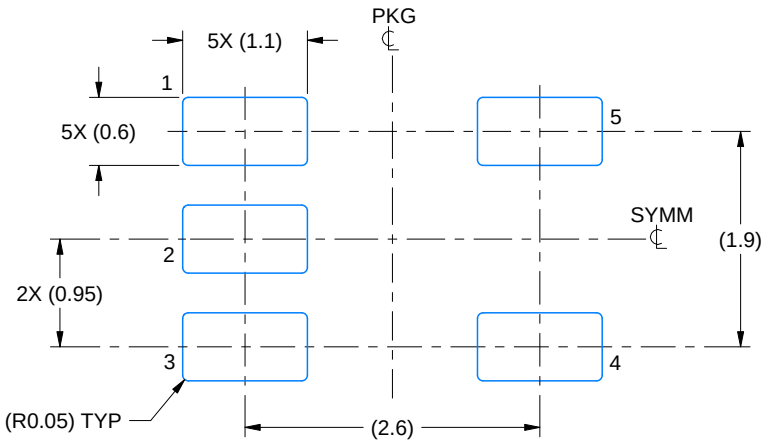
SMALL OUTLINE TRANSISTOR



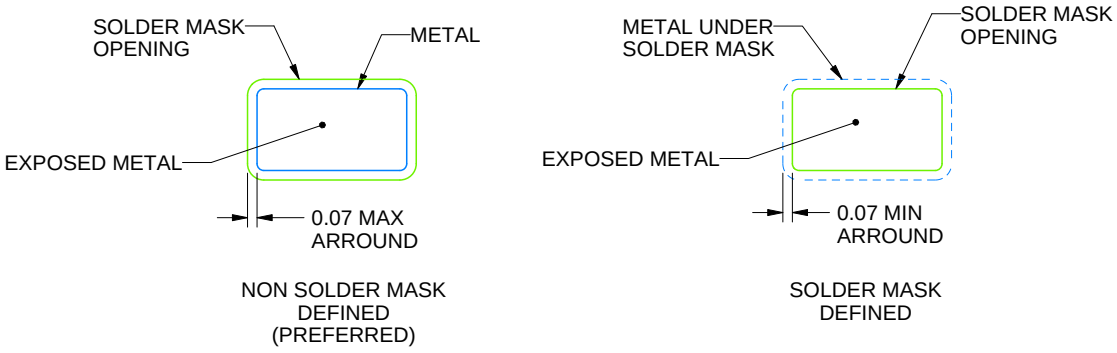
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

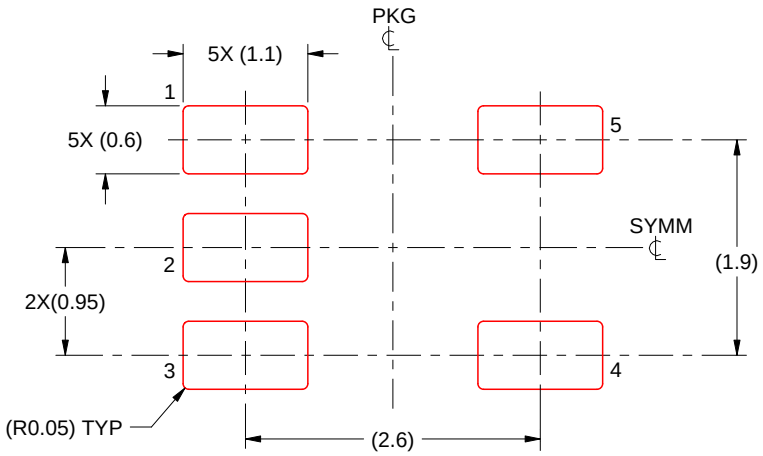


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

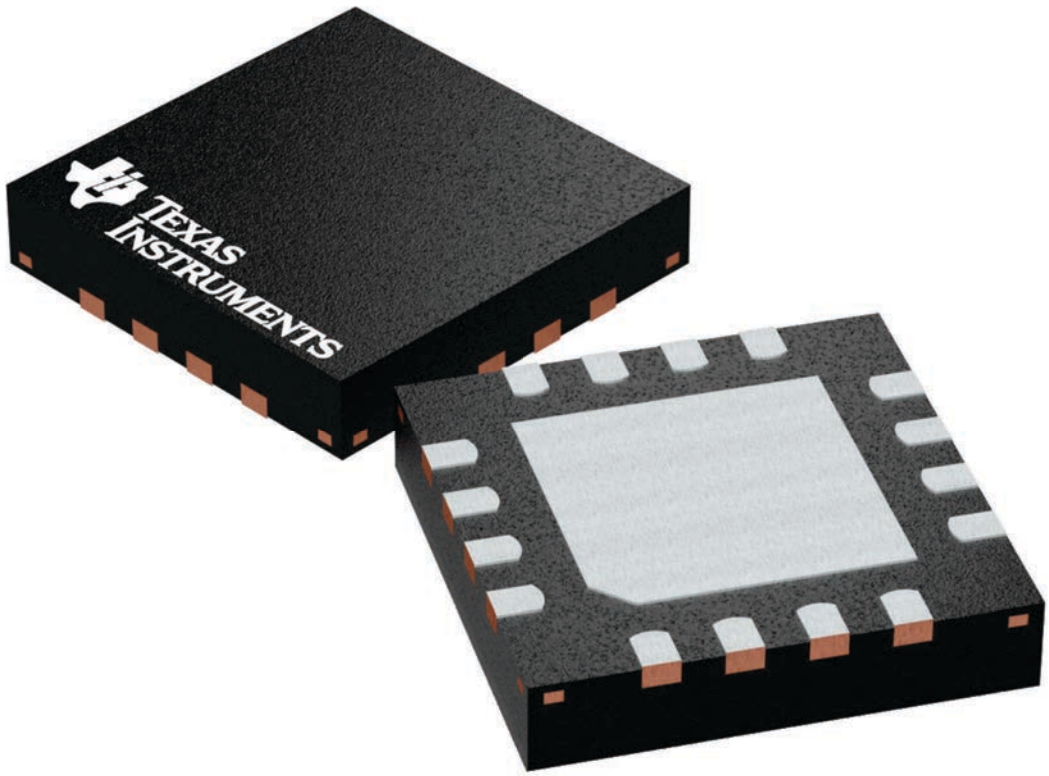
RUM 16

WQFN - 0.8 mm max height

4 x 4, 0.65 mm pitch

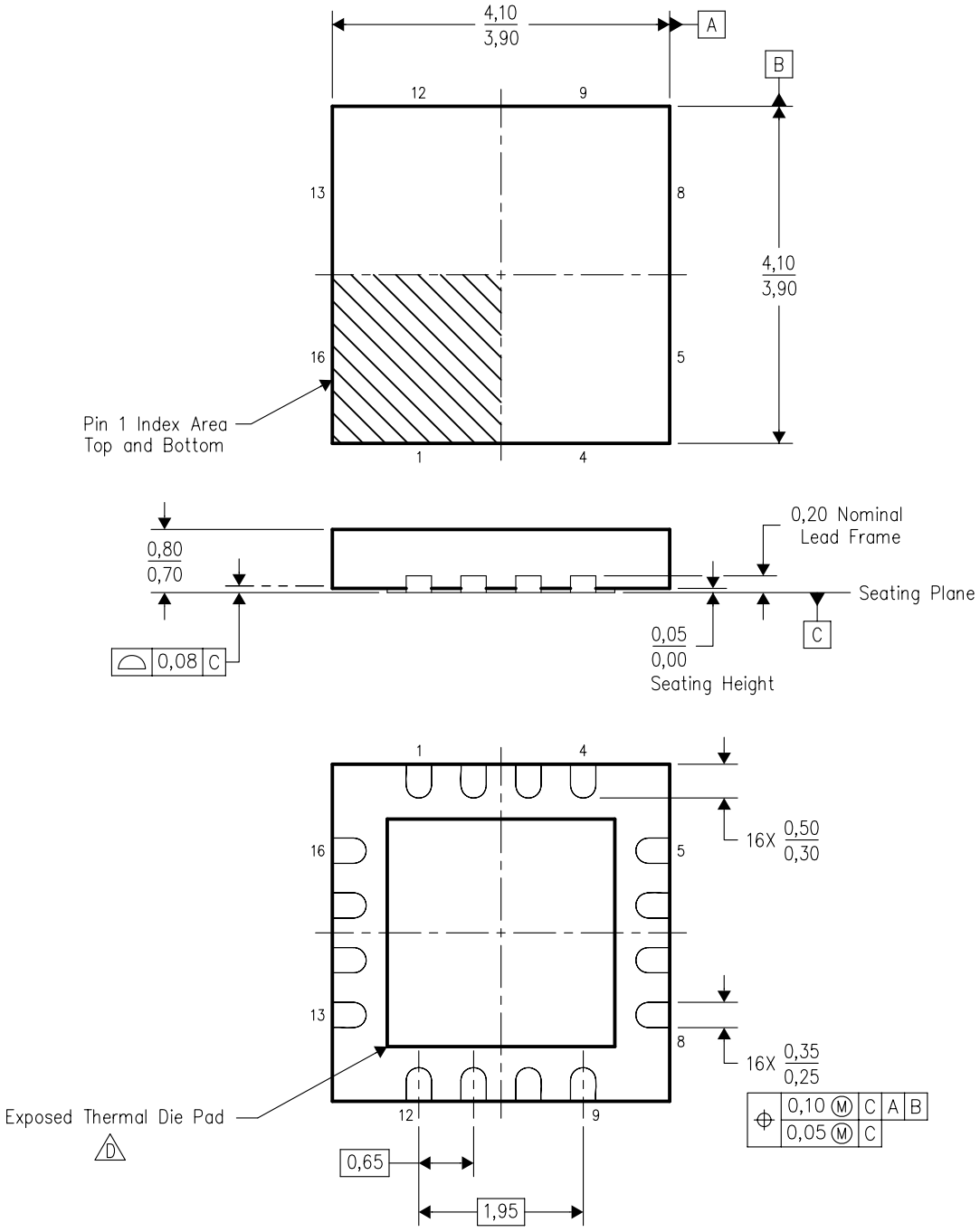
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224843/A

RUM (S–PQFP–N16) PLASTIC QUAD FLATPACK



4209092/A 10/2007

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220 variation WGGC–3.

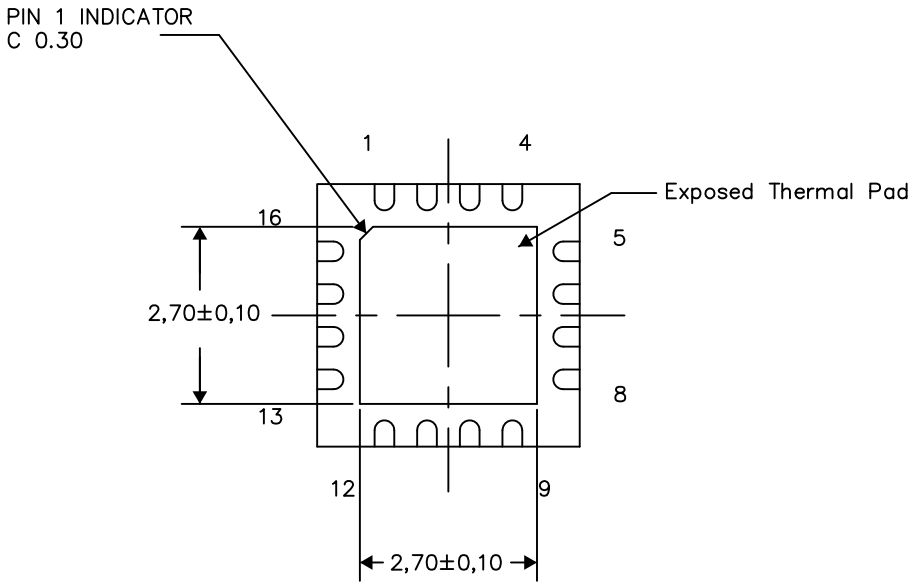
RUM (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



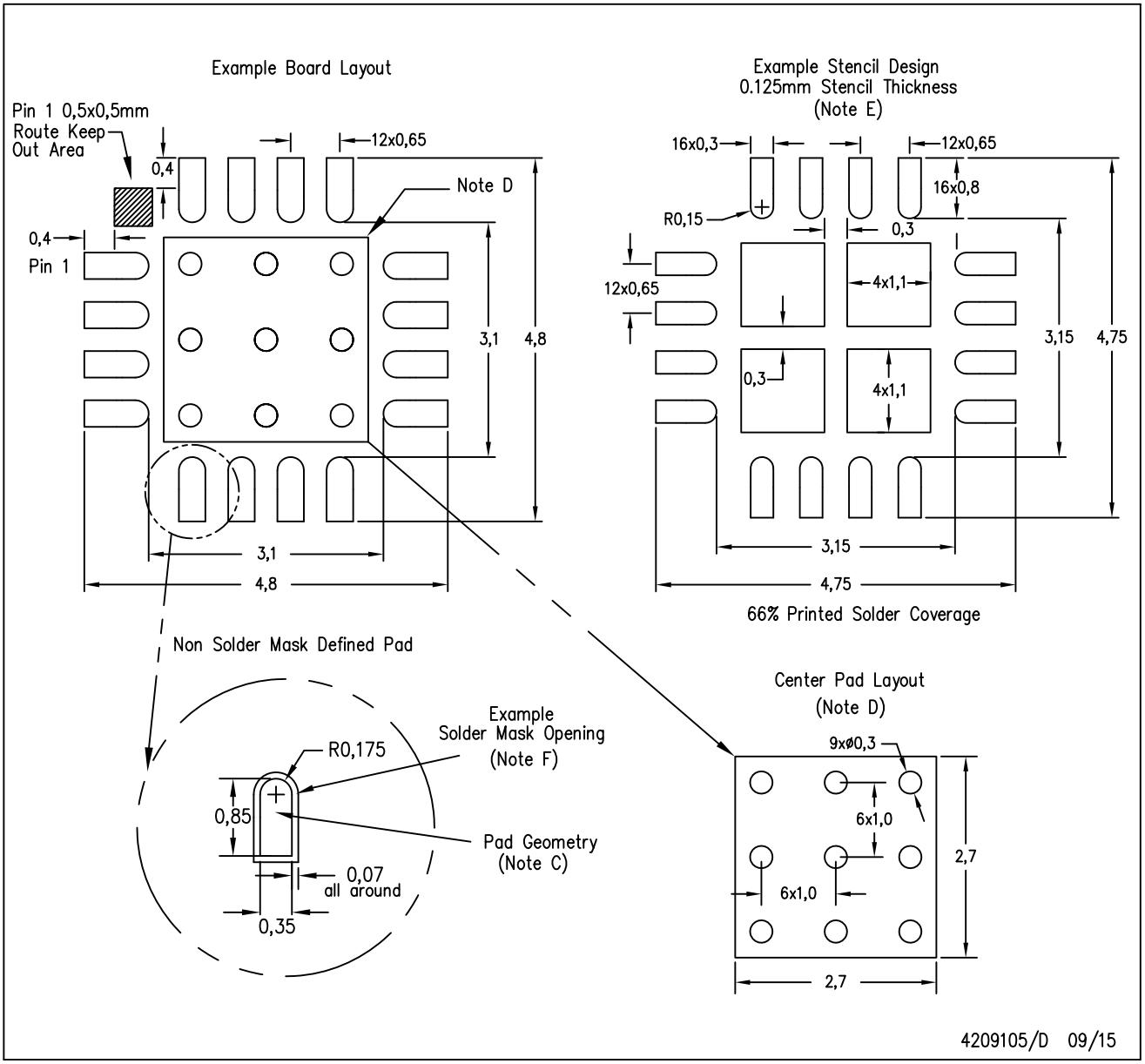
Bottom View

Exposed Thermal Pad Dimensions

4209093–2/F 09/15

NOTES: All linear dimensions are in millimeters

RUM (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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