TPS31xx
Ultralow Supply-Current Voltage Monitor With Optional Watchdog

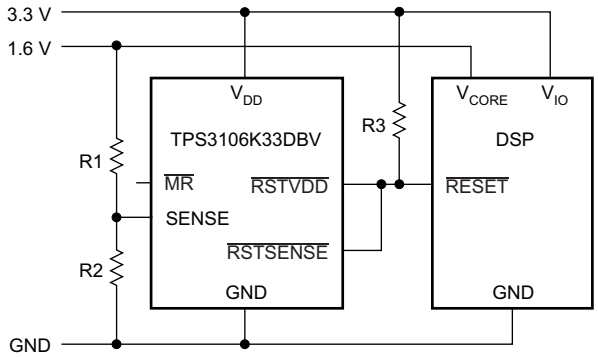
1 Features

- Precision Supply Voltage Supervision Range: 0.9 V, 1.2 V, 1.5 V, 1.6 V, 2 V, and 3.3 V
- High Trip-Point Accuracy: 0.75%
- Supply Current of 1.2 μA (Typical)
- $\overline{\text{RESET}}$ Defined With Input Voltages as Low as 0.4 V
- Power-On Reset Generator With a Delay Time of 130 ms
- Push/Pull or Open-Drain $\overline{\text{RESET}}$ Outputs
- Package Temperature Range: –40°C to 125°C

2 Applications

- Applications Using Low-Power DSPs, Microcontrollers, or Microprocessors
- Portable and Battery-Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Industrial Equipment
- Notebook and Desktop Computers

Typical Application Schematic



3 Description

The TPS310x and TPS311x families of supervisory circuits provide circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted low when the supply voltage (V_{DD}) becomes higher than 0.4 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps the $\overline{\text{RESET}}$ output low as long as V_{DD} remains below the threshold voltage (V_{IT-}). To ensure proper system reset, after V_{DD} surpasses the threshold voltage, an internal timer delays the transition of the $\overline{\text{RESET}}$ signal from low to high for the specified time. When V_{DD} drops below V_{IT-}, the output transitions low again.

All the devices of this family have a fixed-sense threshold voltage (V_{IT-}) set by an internal voltage divider.

The TPS3103 and TPS3106 devices have an active-low, open-drain $\overline{\text{RESET}}$ output and either an integrated power-fail input (PFI) or SENSE input with corresponding outputs for monitoring other voltages. The TPS3110 has an active-low push/pull $\overline{\text{RESET}}$ and a watchdog timer to monitor the operation of microprocessors. All three devices have a manual reset pin that can be used to force the outputs low regardless of the sensed voltages.

The product spectrum is designed for supply voltages of 0.9 V up to 3.6 V. The circuits are available in 6-pin SOT-23 packages. The TPS31xx family is characterized for operation over a temperature range of –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS3103xxx	SOT-23 (6)	2.90 mm × 1.60 mm
TPS3106xxx		
TPS3110xxx		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision F (November 2015) to Revision G — **Page**

- Changed Package Temperature Range Features bullet to extend to 125°C ... 1
- Changed supply voltage and temperature range in last paragraph of *Description* section ... 1
- Changed maximum specifications in *Supply voltage*, *All other pins*, and *Operating temperature* parameters in *Absolute Maximum Ratings* table ... 5
- Changed maximum specifications in V_{DD}, PFI, and T_J parameters of *Recommended Operating Conditions* table ... 5
- Added T_A = –40°C to 125°C rows to V_{IT-} parameter of *Electrical Characteristics* table ... 6
- Added second row to $V_{IT-(S)}$ parameter of *Electrical Characteristics* table ... 6
- Changed I_{DD} parameter of *Electrical Characteristics* table ... 7
- Changed Typical Characteristics curves *TPS3110E09 Supply Current vs Supply Voltage*, *TPS3110E09 Low-Level Output Voltage vs Low-Level Output Current*, *TPS3110E09 Low-Level Output Voltage vs Low-Level Output Current*, *TPS3110E09 High-Level Output Voltage vs High-Level Output Current*, and *TPS3110K33 High-Level Output Voltage vs High-Level Output Current* ... 11
- Changed *Normalized Threshold Voltage vs Free-Air Temperature* curve ... 12
- Changed supply voltage range in first sentence of *Overview* section ... 13
- Changed supply voltage range in description of *Application Information* section ... 18
- Changed *Normalized Threshold Voltage vs Free-Air Temperature* figure ... 19
- Changed supply voltage range in first sentence of *Power Supply Recommendations* section ... 20

Changes from Revision E (September 2007) to Revision F — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed title of document ... 1
- Deleted *Features* bullet for SOT23-6 package ... 1
- Changed front-page figure ... 1
- Changed second paragraph of *Description* section ... 1

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- Changed fourth paragraph of *Description* section 1
- Changed *Pin Configuration and Functions* section; updated table format 4
- Changed "free-air temperature" to "junction temperature" in *Absolute Maximum Ratings* condition statement 5
- Deleted *clamp current* from Absolute Maximum Ratings table; changed to *current* 5
- Deleted soldering temperature specification from *Absolute Maximum Ratings* table 5
- Changed "free-air temperature" to "junction temperature" in *Recommended Operating Conditions* condition statement 5
- Added *Thermal Information* table; deleted *Dissipation Ratings* table 6
- Changed "free-air temperature" to "junction temperature" in *Electrical Characteristics* condition statement 6
- Changed "free-air temperature" to "junction temperature" in *Electrical Characteristics* condition statement 7
- Changed *Switching Characteristics* table 8
- Changed Figure 1 title and timing drawing 8
- Changed Figure 2 title 9
- Changed Figure 3 9
- Changed Figure 4 10

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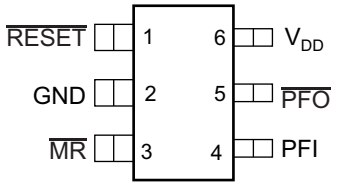
5 Available Options

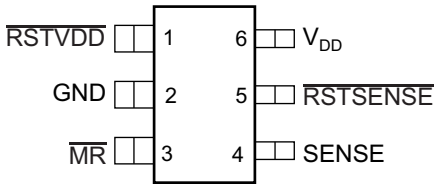
DEVICE	$\overline{\text{RESET}}$ OUTPUT	$\overline{\text{RSTSENSE}}$, $\overline{\text{RSTVDD}}$ OUTPUT	SENSE INPUT	WDI INPUT	$\overline{\text{PFO}}$ OUTPUT
TPS3103	Open-drain				Open-drain
TPS3106		Open-drain	✓		
TPS3110	Push-pull		✓	✓	

6 Pin Configuration and Functions

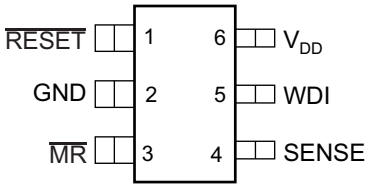
TPS3103 DBV Package
6-Pin SOT-23
Top View



TPS3106 DBV Package
6-Pin SOT-23
Top View



TPS3110 DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	TPS3103	TPS3106	TPS3110		
GND	2	2	2	—	GND
$\overline{\text{MR}}$	3	3	3	I	Manual-reset input. Pull low to force a reset. $\overline{\text{RESET}}$ remains low as long as $\overline{\text{MR}}$ is low and for the time-out period after $\overline{\text{MR}}$ goes high. Leave unconnected or connect to V_{DD} when unused.
PFI	4	—	—	I	Power-fail input compares to 0.551 V with no additional delay. Connect to V_{DD} if not used.
$\overline{\text{PFO}}$	5	—	—	O	Power-fail output. Goes high when voltage at PFI rises above 0.551 V.
$\overline{\text{RESET}}$	1	—	1	O	Active-low reset output. Either push-pull or open-drain output stage.
$\overline{\text{RSTSENSE}}$	—	5	—	O	Active-low reset output. Logic level at $\overline{\text{RSTSENSE}}$ only depends on the voltage at SENSE and the status of $\overline{\text{MR}}$.
$\overline{\text{RSTVDD}}$	—	1	—	O	Active-low reset output. Logic level at $\overline{\text{RSTVDD}}$ only depends on the voltage at V_{DD} and the status of $\overline{\text{MR}}$.
SENSE	—	4	4	I	A reset is asserted if the voltage at SENSE is lower than 0.551 V. Connect to V_{DD} if unused.
V_{DD}	6	6	6	I	Supply voltage. Powers the device and monitors its own voltage.
WDI	—	—	5	I	Watchdog timer input. If WDI remains high or low longer than the time-out period, then reset is triggered. The timer clears when reset is asserted or when WDI sees a rising edge or a falling edge.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage[2]	V_{DD}	–0.3	4	V
$\overline{MR}$ Pin, $\overline{RESET}$ (push-pull)	$V_{\overline{MR}}$, $V_{\overline{RESET}}$ (push-pull)	–0.3	V_{DD} + 0.3	V
All other pins[2]		–0.3	4	V
Maximum low output current	I_{OL}	–5	5	mA
Maximum high output current	I_{OH}	–5	5	mA
Input current	I_{IK} (V_{SENSE} < 0 V or V_{SENSE} > V_{DD})	–10	10	mA
Output current	I_{OK} (V_O < 0 V or V_O > V_{DD})[3]	–10	10	mA
Continuous total power dissipation		See *Thermal Information*		
Temperature	Operating, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation, the device must not be operated at 3.6 V for more than t = 1000h continuously.
(3) Output is clamped for push-pull outputs by the back gate diodes internal to the IC. No clamp exists for the open-drain outputs.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range, unless otherwise noted.

		MIN	NOM	MAX	UNIT
V_{DD}[1]	Supply voltage	0.9		3.6	V
V_{SENSE}	SENSE voltage	0		V_{DD}	V
WDI	High-level input voltage V_{IH} at $\overline{MR}$	0.7 × V_{DD}			V
WDI	Low-level input voltage V_{IL} at $\overline{MR}$			0.3 × V_{DD}	V
WDI	Input transition rise and fall rate at Δt/ΔV at $\overline{MR}$			100	ns/V
$\overline{MR}$	$\overline{MR}$ voltage	0		V_{DD}	V
PFI	PFI voltage	0		3.6	V
T_J	Operating temperature	–40		125	°C

(1) For proper operation of SENSE, PFI, and WDI functions: V_{DD} ≥ 0.8 V.

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7.4 Thermal Information

THERMAL METRIC[1]		TPS31xx DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	183.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	123.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating junction temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 3.3 V, I_{OH} = –3 mA	0.8 × V_{DD}			V
			V_{DD} = 1.8 V, I_{OH} = –2 mA				
			V_{DD} = 1.5 V, I_{OH} = –1 mA				
			V_{DD} = 0.9 V, I_{OH} = –0.4 mA				
			V_{DD} = 0.5 V, I_{OH} = –5 μA	0.7 × V_{DD}			
V_{OL}	Low-level output voltage		V_{DD} = 3.3 V, I_{OL} = 3 mA			0.3	V
			V_{DD} = 1.5 V, I_{OL} = 2 mA				
			V_{DD} = 1.2 V, I_{OL} = 1 mA				
			V_{DD} = 0.9 V, I_{OL} = 500 μA				
V_{OL}	Low-level output voltage	$\overline{RESET}$ only	V_{DD} = 0.4 V, I_{OL} = 5 μA			0.1	V
V_{IT-}	Negative-going input threshold voltage[1]	TPS31xxE09	T_A = 25°C	0.854	0.86	0.866	V
		TPS31xxE12		1.133	1.142	1.151	
		TPS31xxE15		1.423	1.434	1.445	
		TPS31xxE16		1.512	1.523	1.534	
		TPS31xxH20		1.829	1.843	1.857	
		TPS31xxK33		2.919	2.941	2.963	
		TPS31xxE09	T_A = –40°C to 125°C	0.817		0.903	
		TPS31xxE12		1.084		1.199	
		TPS31xxE15		1.362		1.505	
		TPS31xxK33		2.823		3.058	
$V_{IT-(S)}$	Negative-going input threshold voltage[1]	SENSE, PFI	V_{DD} ≥ 0.8 V, T_A = 25°C	0.542	0.551	0.559	V
			V_{DD} ≥ 0.8 V, T_A = –40°C to 125°C	0.5		0.58	
V_{HYS}	Hysteresis at V_{DD} input		0.8 V ≤ V_{IT-} < 1.5 V		20		mV
			1.6 V ≤ V_{IT-} < 2.4 V		30		
			2.5 V ≤ V_{IT-} < 3.3 V		50		
$T_{(K)}$	Temperature coefficient of V_{IT-}, PFI, SENSE		T_A = –40°C to 85°C		–0.012	–0.019	%/K
$V_{HYS(S)}$	Hysteresis at SENSE, PFI input		V_{DD} ≥ 0.8 V		15		mV
I_{IH}	High-level input current	$\overline{MR}$	$\overline{MR}$ = V_{DD}, V_{DD} = 3.3 V	–25		25	nA
		SENSE, PFI, WDI	SENSE, PFI, WDI = V_{DD}, V_{DD} = 3.3 V	–25		25	

(1) To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed close to the supply terminals.

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Electrical Characteristics (continued)

over operating junction temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Low-level input current	$\overline{MR}$	$\overline{MR}$ = 0 V, V_{DD} = 3.3 V	–47	–33	–25	µA
		SENSE, PFI, WDI	SENSE, PFI, WDI = 0 V, V_{DD} = 3.3 V	–25		25	nA
I_{OH}	High-level output current at $\overline{RESET}$ (2)	Open-drain	$V_{DD} = V_{IT-} + 0.2$ V, V_{OH} = 3.3 V			200	nA
I_{DD}	Supply current		T_A = –40°C to 85°C, $V_{DD} > V_{IT-}$ (average current), V_{DD} < 1.8 V		1.2	3	µA
			T_A = –40°C to 125°C, $V_{DD} > V_{IT-}$ (average current), V_{DD} < 1.8 V			3	
			T_A = –40°C to 85°C, $V_{DD} > V_{IT-}$ (average current), V_{DD} > 1.8 V		2	4.5	
			T_A = –40°C to 125°C, $V_{DD} > V_{IT-}$ (average current), V_{DD} > 1.8 V			5.5	
			T_A = –40°C to 85°C, $V_{DD} < V_{IT-}$, V_{DD} < 1.8 V			22	
			T_A = –40°C to 125°C, $V_{DD} < V_{IT-}$, V_{DD} < 1.8 V			27	
			T_A = –40°C to 85°C, $V_{DD} < V_{IT-}$, V_{DD} > 1.8 V			27	
			T_A = –40°C to 125°C, $V_{DD} < V_{IT-}$, V_{DD} > 1.8 V			32	
	Internal pullup resistor at $\overline{MR}$			70	100	130	kΩ
C_{IN}	Input capacitance at $\overline{MR}$, SENSE, PFI, WDI		V_{IN} = 0 V to V_{DD}		1		pF

(2) Also refers to $\overline{RSTVDD}$ and $\overline{RSTSENSE}$.

7.6 Timing Requirements

At R_L = 1 MΩ, C_L = 50 pF, and T_A = –40°C to 85°C, unless otherwise noted.

				MIN	TYP	MAX	UNIT
$t_{T(OUT)}$	Time-out period	at WDI	V_{DD} ≥ 0.85 V	0.55	1.1	1.65	s
t_W	Pulse duration	at V_{DD}	V_{IH} = 1.1 × $V_{IT–}$, V_{IL} = 0.9 × $V_{IT–}$, $V_{IT–}$ = 0.86 V	20			µs
		at $\overline{MR}$	V_{DD} ≥ $V_{IT–}$ + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}	0.1			
		at SENSE	V_{DD} ≥ $V_{IT–}$, V_{IH} = 1.1 × $V_{IT-(S)}$, V_{IL} = 0.9 × $V_{IT-(S)}$	20			
		at PFI	V_{DD} ≥ 0.85 V, V_{IH} = 1.1 × $V_{IT-(S)}$, V_{IL} = 0.9 × $V_{IT-(S)}$	20			
		at WDI	V_{DD} ≥ $V_{IT–}$, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}	0.3			

7.7 Switching Characteristics

At R_L = 1 MΩ, C_L = 50 pF, and T_A = –40°C to 85°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_D	Delay time		V_{DD} ≥ 1.1 × $V_{IT–}$, $\overline{MR}$ = 0.7 × V_{DD}. See *Timing Requirements*.	65	130	195	ms
$t_{PHL(VDD)}$	Propagation delay time, high-to-low level output	V_{DD} to $\overline{RESET}$ or $\overline{RSTVDD}$ delay	V_{IH} = 1.1 × $V_{IT–}$, V_{IL} = 0.9 × $V_{IT–}$			40	µs
$t_{PHL(SENSE)}$	Propagation delay time, high-to-low level output	SENSE to $\overline{RESET}$ or $\overline{RSTSENSE}$ delay	V_{DD} ≥ 0.8 V, V_{IH} = 1.1 × $V_{IT–}$, V_{IL} = 0.9 × $V_{IT–}$			40	µs
$t_{PHL(\overline{PFO})}$	Propagation delay time, high-to-low level output	PFI to $\overline{PFO}$ delay	V_{DD} ≥ 0.8 V, V_{IH} = 1.1 × $V_{IT–}$, V_{IL} = 0.9 × $V_{IT–}$			40	µs
$t_{PLH(\overline{PFO})}$	Propagation delay time, low-to-high level output	PFI to $\overline{PFO}$ delay	V_{DD} ≥ 0.8 V, V_{IH} = 1.1 × $V_{IT–}$, V_{IL} = 0.9 × $V_{IT–}$			300	µs
$t_{PHL(MR)}$	Propagation delay time, high-to-low level output	$\overline{MR}$ to $\overline{RESET}$. $\overline{RSTVDD}$, $\overline{RSTSENSE}$ delay	V_{DD} ≥ 1.1 × $V_{IT–}$, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}		1	5	µs

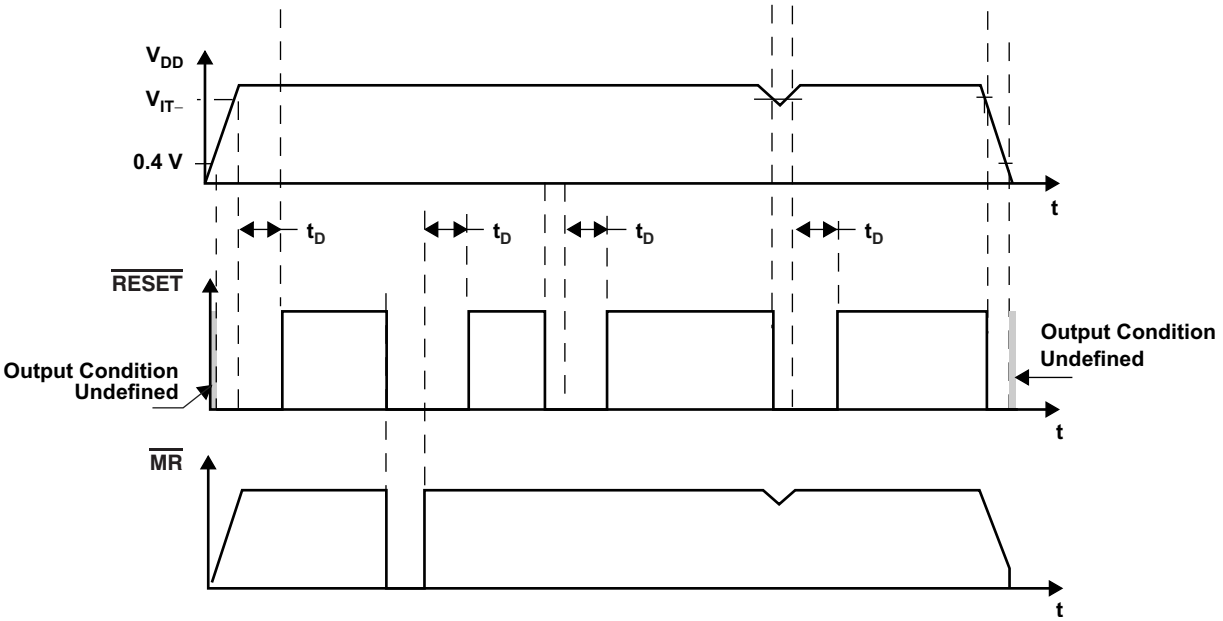

Figure 1. $\overline{RESET}$ Timing Diagram for TPS3103

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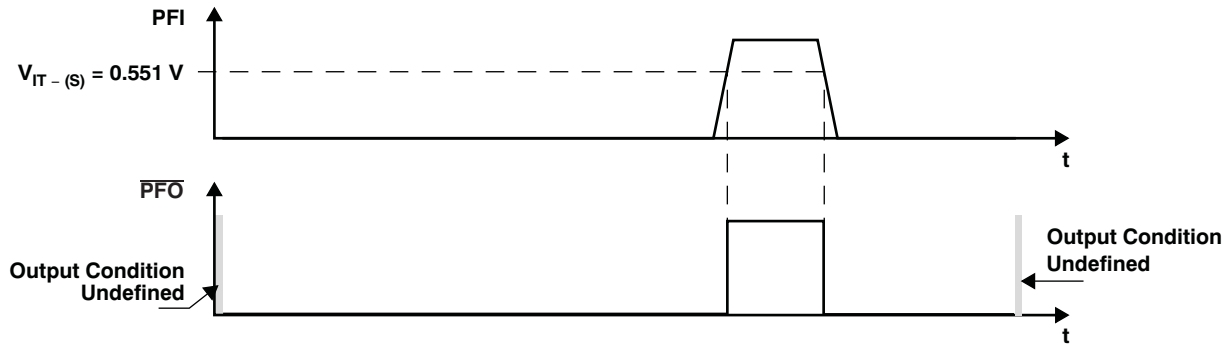

Figure 2. $\overline{PFO}$ Timing Diagram for TPS3103

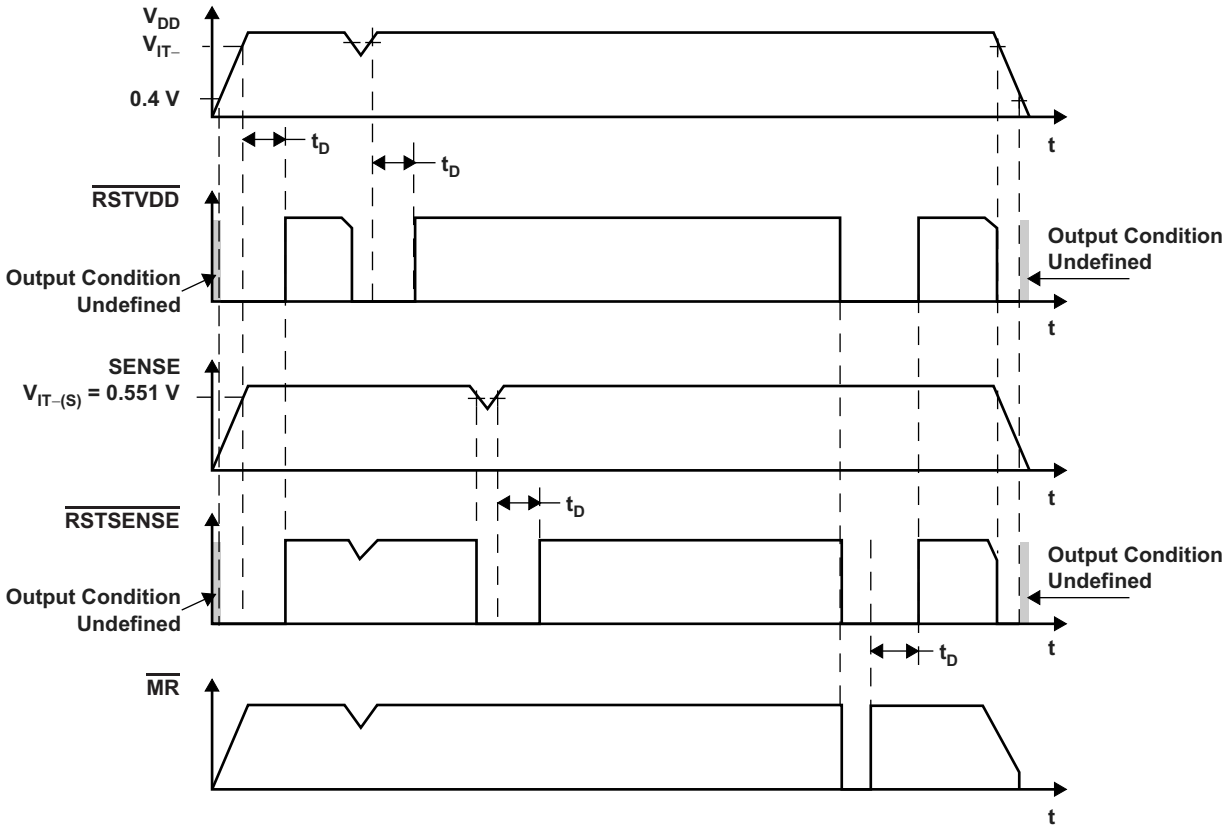

Figure 3. Timing Diagram for TPS3106

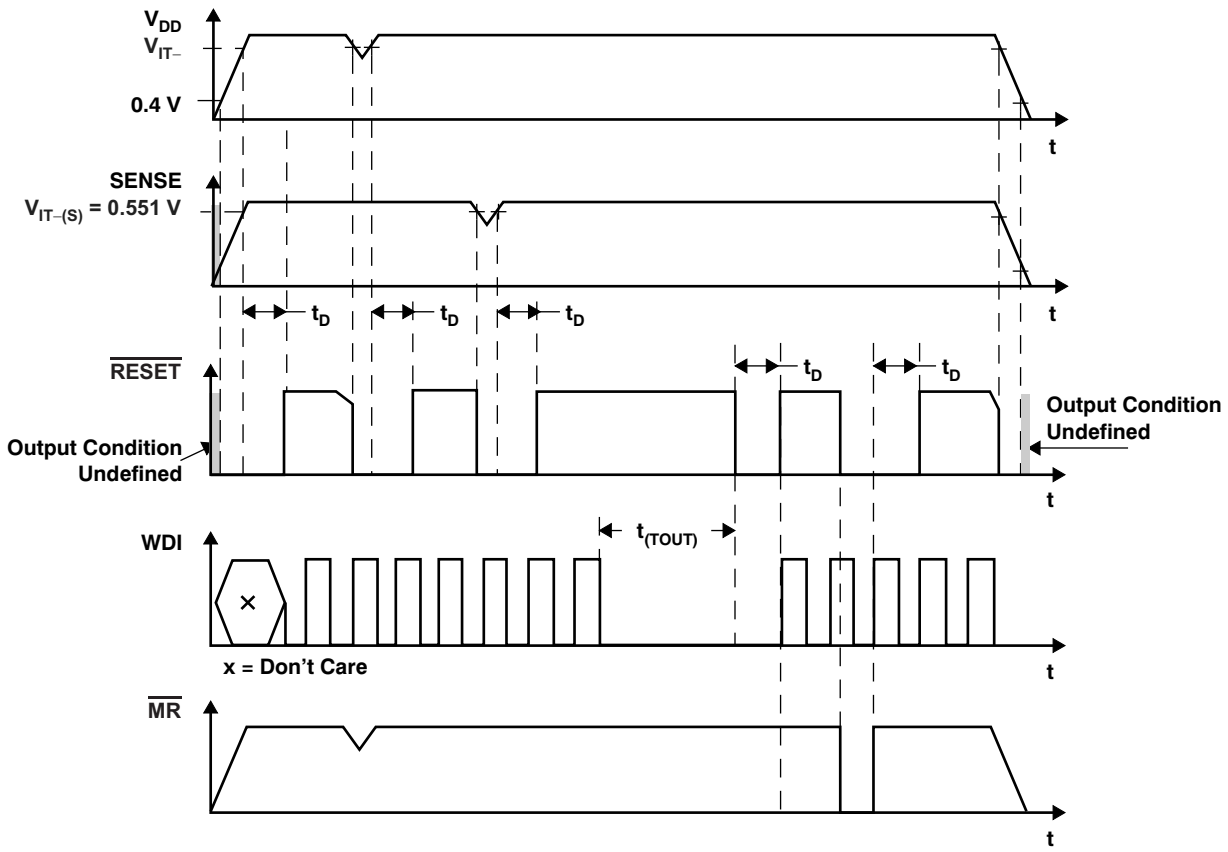

Figure 4. Timing Diagram for TPS3110

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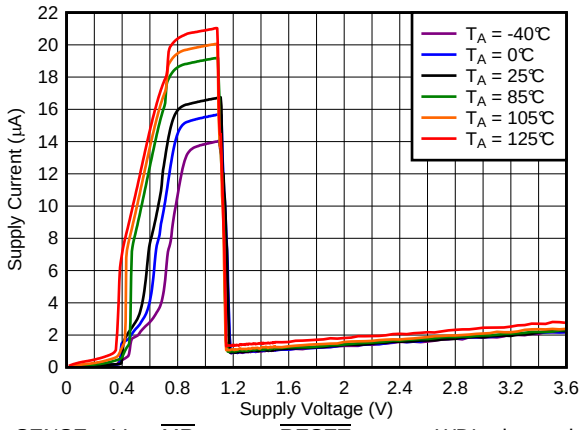
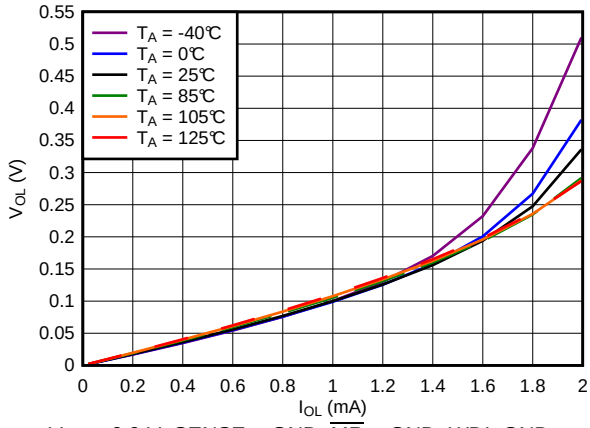
7.8 Typical Characteristics



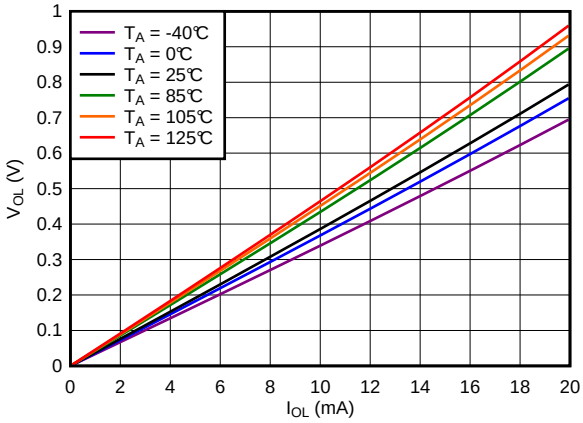
SENSE = V_{DD}, $\overline{MR}$ = open, $\overline{RESET}$ = open, WDI: triggered

Figure 5. TPS3110E09 Supply Current vs Supply Voltage



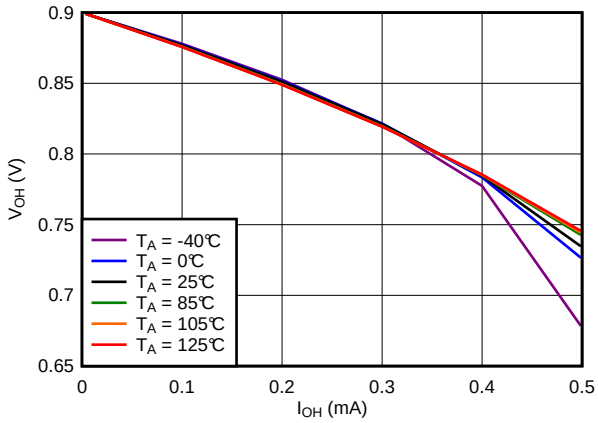
V_{DD} = 0.9 V, SENSE = GND, $\overline{MR}$ = GND, WDI: GND

Figure 6. TPS3110E09 Low-Level Output Voltage vs Low-Level Output Current



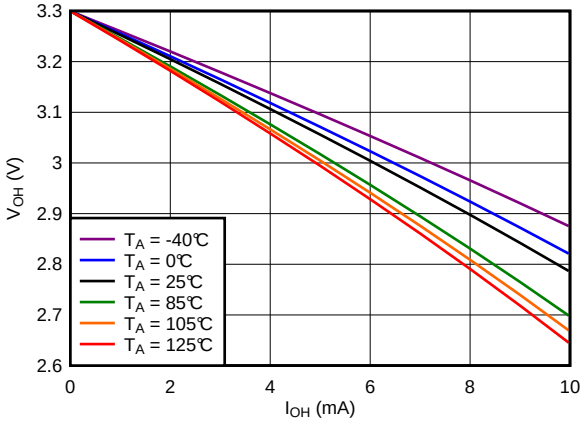
V_{DD} = 3.3 V, SENSE = GND, $\overline{MR}$ = GND, WDI: GND

Figure 7. TPS3110E09 Low-Level Output Voltage vs Low-Level Output Current



V_{DD} = 0.9 V, SENSE = V_{DD}, $\overline{MR}$ = V_{DD}, WDI: triggered

Figure 8. TPS3110E09 High-Level Output Voltage vs High-Level Output Current



V_{DD} = 3.3 V, SENSE = V_{DD}, $\overline{MR}$ = V_{DD}, WDI: triggered

Figure 9. TPS3110K33 High-Level Output Voltage vs High-Level Output Current

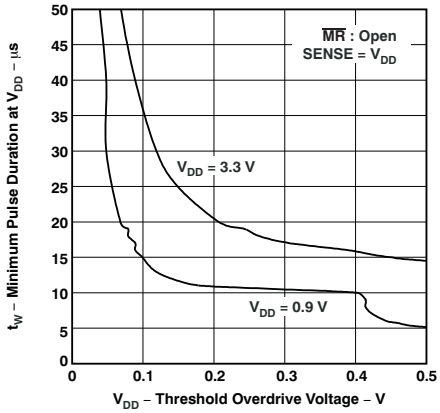


Figure 10. Minimum Pulse Duration at V_{DD} vs Threshold Overdrive Voltage

Typical Characteristics (continued)

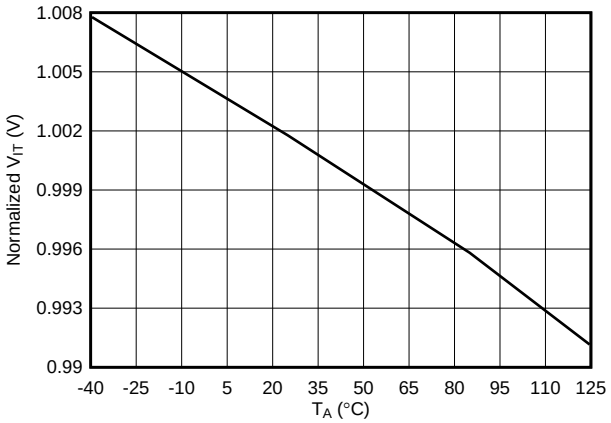


Figure 11. Normalized Threshold Voltage vs Free-Air Temperature

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8 Detailed Description

8.1 Overview

The TPS310x and TPS311x families of supervisory circuits operate from supply voltages from 0.9 V to 3.6 V and provide circuit initialization and timing supervision for DSP- and processor-based systems. During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage (V_{DD}) exceeds 0.4 V. The devices monitor V_{DD} and keep the $\overline{\text{RESET}}$ output low as long as V_{DD} remains below the threshold voltage (V_{IT-}). To ensure proper system reset, after V_{DD} surpasses the threshold voltage plus the hysteresis (V_{IT-} + V_{HYS}) an internal timer delays the transition of the $\overline{\text{RESET}}$ signal from low to high for the specified time. The delay time starts after V_{DD} has risen above (V_{IT-} + V_{HYS}). When V_{DD} drops below V_{IT-}, the output becomes active again.

All the devices of this family have a fixed-V_{DD} threshold voltage (V_{IT-}) set by an internal voltage divider. The TPS3103 and TPS3106 devices both have an active-low, open-drain $\overline{\text{RESET}}$ output. The TPS3103 device has an integrated power-fail input (PFI) and corresponding power-fail output ($\overline{\text{PFO}}$) that can be used for low-battery detection or for monitoring a power supply other than the input supply. The TPS3106 device has a SENSE input with a corresponding output ($\overline{\text{RSTSENSE}}$) for monitoring voltages other than the input supply. The TPS3110 device has an active-low push/pull $\overline{\text{RESET}}$ and a watchdog timer that is used for monitoring the operation of microprocessors. All three devices have manual reset pin ($\overline{\text{MR}}$) that can be used to force the outputs low regardless of the sensed voltages.

8.2 Functional Block Diagrams

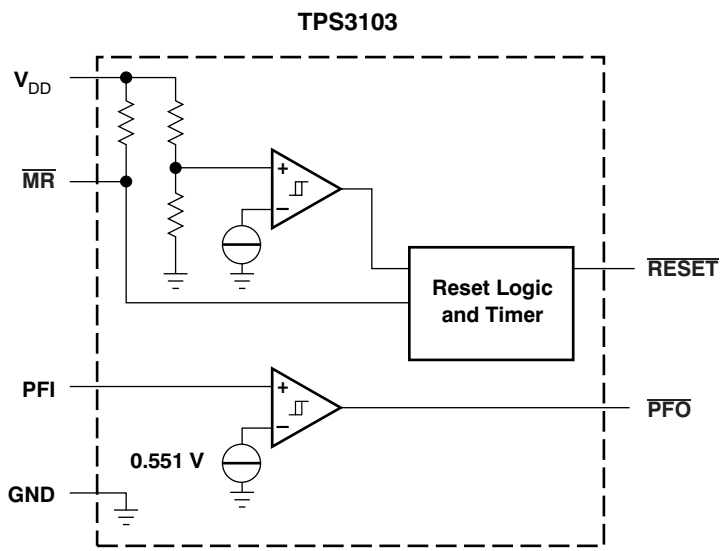

Figure 12. TPS3103 Functional Block Diagram

Functional Block Diagrams (continued)

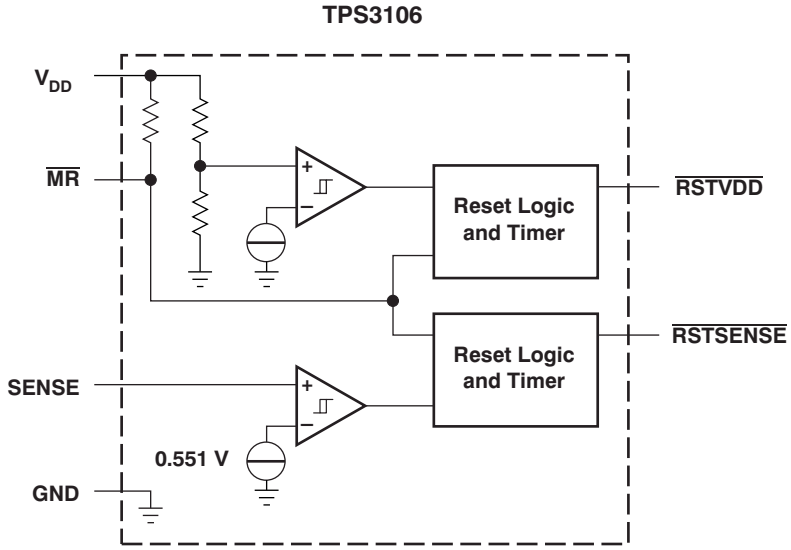

Figure 13. TPS3106 Functional Block Diagram

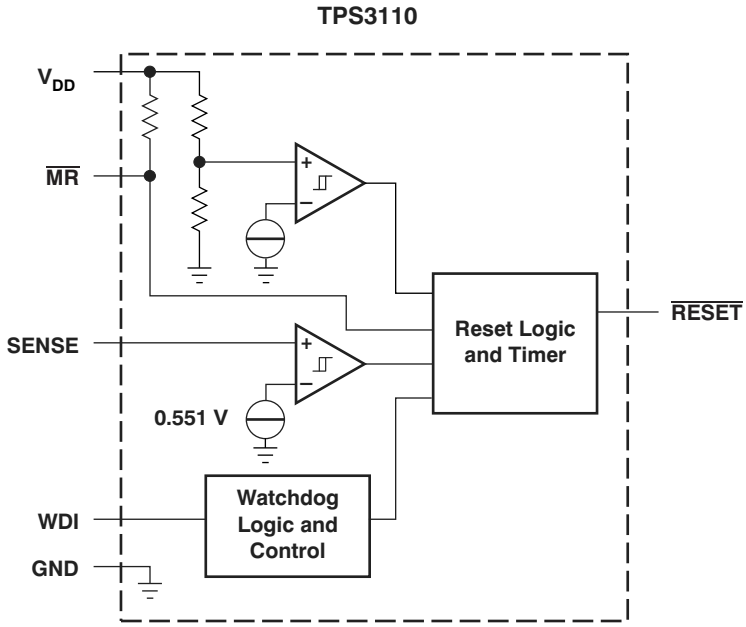

Figure 14. TPS3110 Functional Block Diagram

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8.3 Feature Description

8.3.1 Watchdog

The TPS3110 device integrates a watchdog timer that must be periodically triggered by a positive or negative transition of WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, $\overline{\text{RESET}}$ becomes active for the time period (t_D). This event also reinitializes the watchdog timer.

8.3.2 Manual Reset ($\overline{\text{MR}}$)

Many µC-based products require manual-reset capability, allowing an operator or logic circuitry to initiate a reset. Logic low at $\overline{\text{MR}}$ asserts reset. Reset remains asserted while $\overline{\text{MR}}$ is low and for a time period (t_D) after $\overline{\text{MR}}$ returns high. The input has an internal 100-kΩ pullup resistor, so it can be left open if it is unused.

Connect a normally open momentary switch from $\overline{\text{MR}}$ to GND to create a manual reset function. External debounce is not required. If $\overline{\text{MR}}$ is driven from long cables or if the device is used in noisy environments, connecting a 0.1-µF capacitor from $\overline{\text{MR}}$ to GND provides additional noise immunity.

If there is a possibility of transient or DC conditions causing $\overline{\text{MR}}$ to rise above V_{DD}, a diode should be used to limit $\overline{\text{MR}}$ to a diode drop above V_{DD}.

8.3.3 PFI, $\overline{\text{PFO}}$

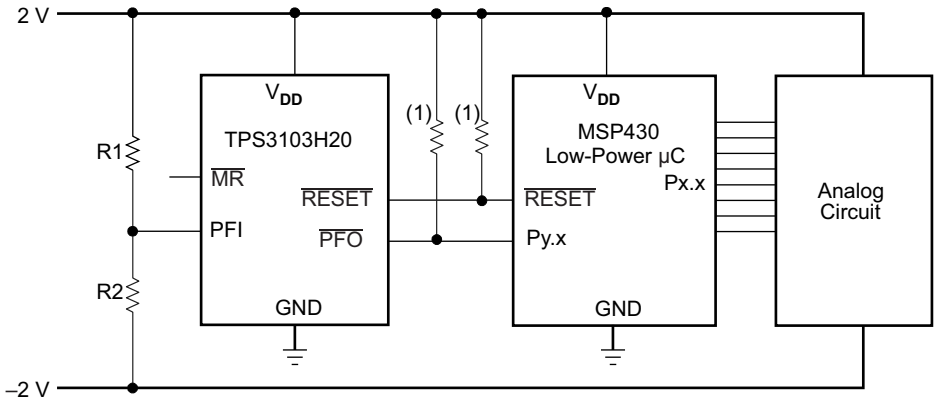
The TPS3103 has an integrated power-fail (PFI) comparator with a separate open-drain ($\overline{\text{PFO}}$) output. The PFI and $\overline{\text{PFO}}$ can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply, and has no effect on $\overline{\text{RESET}}$.

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail input (PFI) will be compared with an internal voltage reference of 0.551 V. If the input voltage falls below the power-fail threshold ($V_{IT-(S)}$), the power-fail output ($\overline{\text{PFO}}$) goes low. If it goes above 0.551 V plus approximately 15-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltage above 0.551 V. The sum of both resistors should be approximately 1 MΩ, to minimize power consumption and to assure that the current into the PFI pin can be neglected, compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, connect PFI to GND and leave $\overline{\text{PFO}}$ unconnected. For proper operation of the PFI-comparator, the supply voltage (V_{DD}) must be higher than 0.8 V.

8.3.4 SENSE

The voltage at the SENSE input is compared with a reference voltage of 0.551 V. If the voltage at SENSE falls below the sense-threshold ($V_{IT-(S)}$), reset is asserted. On the TPS3106 device, a dedicated $\overline{\text{RSTSENSE}}$ output is available. On the TPS3110 device, the logic signal from SENSE is OR-wired with the logic signal from V_{DD} or $\overline{\text{MR}}$. An internal timer delays the return of the output to the inactive state, once the voltage at SENSE goes above 0.551 V plus about 15 mV of hysteresis. For proper operation of the SENSE-comparator, the supply voltage must be higher than 0.8 V.

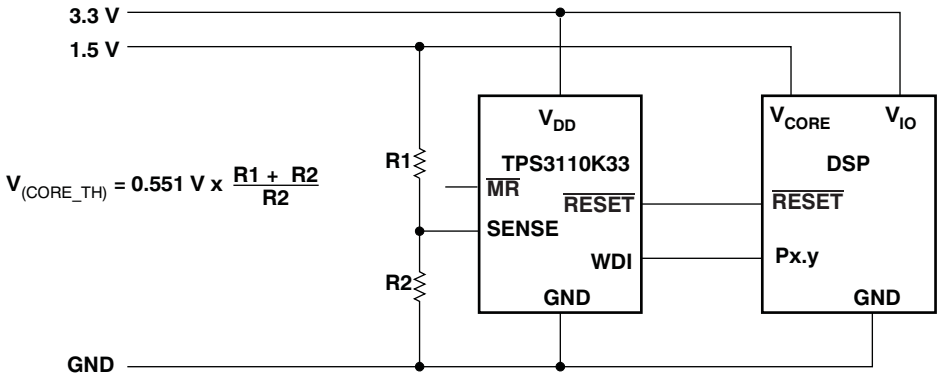
Feature Description (continued)



$$V_{(NEG_TH)} = 0.551\ V - \frac{R2}{R1}(V_{DD} - 0.551\ V)$$

(1) Resistor may be integrated in microcontroller.

Figure 15. TPS3103 Monitoring a Negative Voltage



$$V_{(CORE_TH)} = 0.551\ V \times \frac{R1 + R2}{R2}$$

Figure 16. TPS3110 in a DSP-System Monitoring Both Supply Voltages

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8.4 Device Functional Modes

Table 1. TPS3103 Function Table

$\overline{MR}$	$V_{(PFI)}$ > 0.551 V	$V_{DD} > V_{IT-}$	$\overline{RESET}$	$\overline{PFO}$
L	0	X(1)	L	L
L	1	X	L	H
H	0	0	L	L
H	0	1	H	L
H	1	0	L	H
H	1	1	H	H

(1) X = Don't care.

Table 2. TPS3106 Function Table

$\overline{MR}$	$V_{(SENSE)}$ > 0.551 V	$V_{DD} > V_{IT-}$	$\overline{RSTVDD}$	$\overline{RSTSENSE}$
L	X(1)	X	L	L
H	0	0	L	L
H	0	1	H	L
H	1	0	L	H
H	1	1	H	H

(1) X = Don't care.

Table 3. TPS3110 Function Table(1)

$\overline{MR}$	$V_{(SENSE)}$ > 0.551 V	$V_{DD} > V_{IT-}$	$\overline{RESET}$
L	X(2)	X	L
H	0	0	L
H	0	1	L
H	1	0	L
H	1	1	H

(1) Function of watchdog timer not shown.
(2) X = Don't care.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS310x and TPS311x families are supervisory circuits made to monitor the input supply and other external voltages greater than 0.551 V. These devices are made to operate from and monitor input supplies ranging from 0.9 V to 3.6 V, and all versions have a manual reset pin. The TPS3103 and TPS3106 both have an active-low, open-drain RESET output. The TPS3103 device has an integrated power-fail input (PFI) and corresponding power-fail output ($\overline{PFO}$) that can be used for low-battery detection or for monitoring a power supply other than the input supply and has a short delay time for more immediate triggering of the output. The TPS3106 device has a SENSE input with a corresponding output ($\overline{RSTSENSE}$) for monitoring voltages other than the input supply and a longer delay time than the TPS3103 device to minimize accidental triggering of the output. The TPS3110 device has an active-low push/pull $\overline{RESET}$ and a watchdog timer that is used for monitoring the operation of microprocessors.

9.2 Typical Application

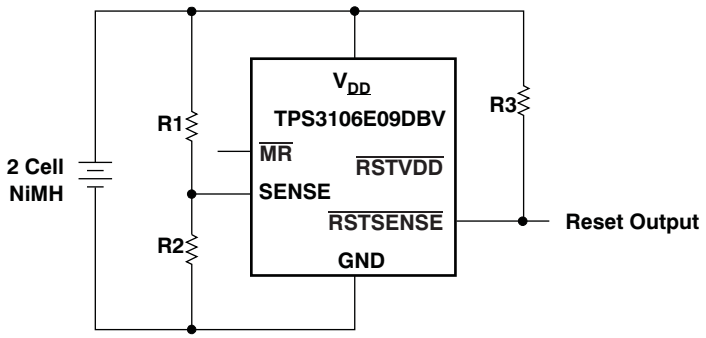

Figure 17. Battery Monitoring With 3-µA Supply Current for Device and Resistor Divider

9.2.1 Design Requirements

In some applications it is necessary to minimize the quiescent current even during the reset period. This is especially true when the voltage of a battery is supervised and the $\overline{RESET}$ is used to shut down the system or for an early warning. In this case the reset condition will last for a longer period of time. The current drawn from the battery should almost be zero, especially when the battery is discharged.

For this kind of application, either the TPS3103 or TPS3106 device is a good fit. To minimize current consumption, select a version where the threshold voltage is lower than the voltage monitored at V_{DD}. The TPS3106 device has two reset outputs. One output ($\overline{RSTVDD}$) is triggered from the voltage monitored at V_{DD}. The other output ($\overline{RSTSENSE}$) is triggered from the voltage monitored at SENSE. In the application shown in Figure 17, the TPS3106E09 device is used to monitor the input voltage of two NiCd or NiMH cells. The threshold voltage [$V_{(TH)}$ = 0.86 V] was chosen as low as possible to ensure that the supply voltage is always higher than the threshold voltage at V_{DD}. The voltage of the battery is monitored using the SENSE input.

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Typical Application (continued)

9.2.2 Detailed Design Procedure

The voltage divider was calculated to assert a reset using the $\overline{\text{RSTSENSE}}$ output at 2 × 0.8 V = 1.6 V, using Equation 1.

$$R_1 = R_2 \times \left(\frac{V_{TRIP}}{V_{IT-(S)}} - 1 \right)$$

where

- V_{TRIP} is the voltage of the battery at which a reset is asserted
- $V_{IT-(S)}$ is the threshold voltage at SENSE = 0.551 V
- R_1 was chosen for a resistor current in the 1-µA range
- With V_{TRIP} = 1.6 V
- $R_1 \equiv 1.9 \times R_2$
- R_1 = 820 kΩ, R_2 = 430 kΩ (1)

9.2.3 Application Curve

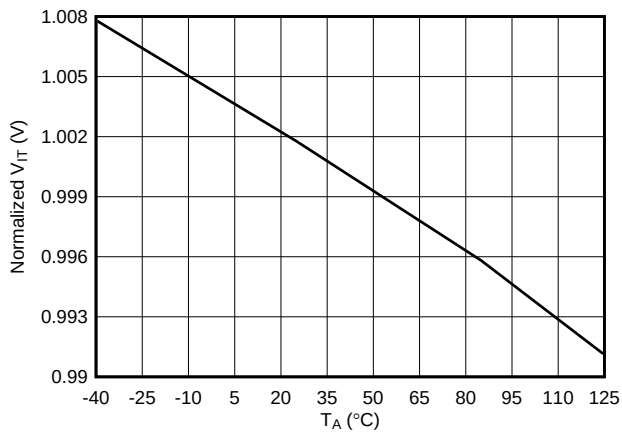

Figure 18. Normalized Threshold Voltage vs Free-Air Temperature

10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 0.9 V and 3.6 V.

Though not required, it is good analog design practice to place a 0.1-µF ceramic capacitor close to the VCC pin if the input supply is noisy.

11 Layout

11.1 Layout Guidelines

Follow these guidelines to lay out the printed-circuit-board (PCB) that is used for the TPS310x and TPS3110x family of devices.

- Place the V_{DD} decoupling capacitor close to the device.
- Avoid using long traces for the VCC supply node. The VCC capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum V_{DD} voltage.

11.2 Layout Example

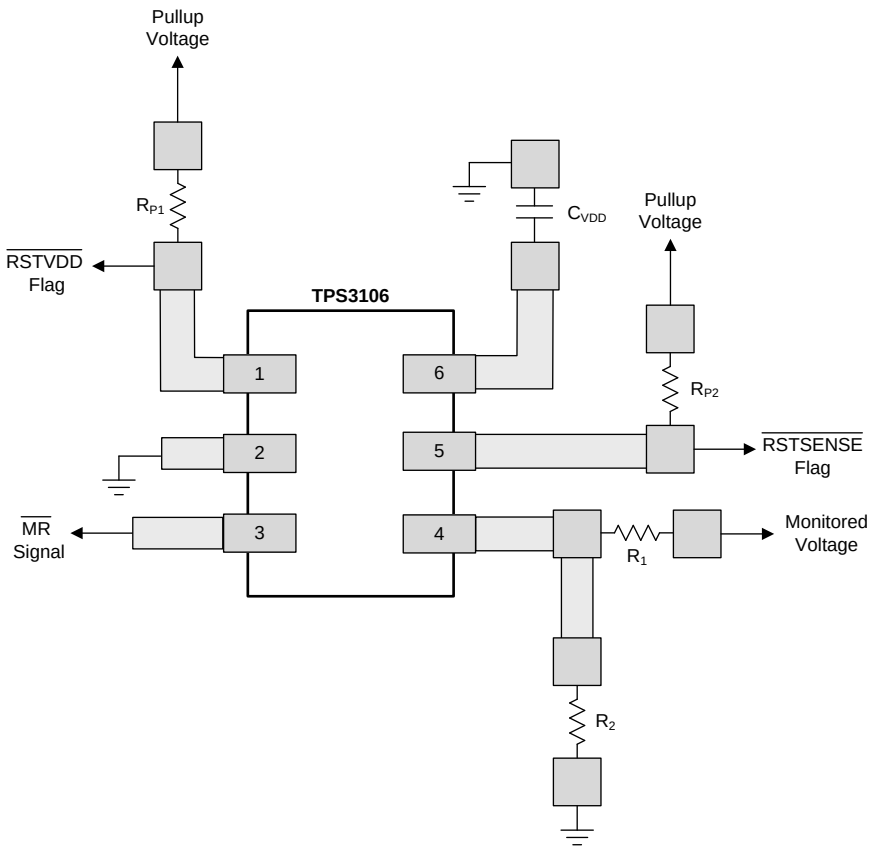

Figure 19. Example Layout (DBV Package)

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. SPICE models for the TPS310x and TPS311x are available through the respective product folders under *Tools & Software*.

12.1.2 Device Nomenclature

Table 4. Ordering Information(1)

PRODUCT	NOMINAL SUPPLY VOLTAGE	THRESHOLD VOLTAGE, V_{IT-}(2)
TPS3103E12DBVR	1.2 V	1.142 V
TPS3103E15DBVR	1.5 V	1.434 V
TPS3103H20DBVR	2.0 V	1.84 V
TPS3103K33DBVR	3.3 V	2.941 V
TPS3106E09DBVR	0.9 V	0.86 V
TPS3106E16DBVR	1.6 V	1.521 V
TPS3106K33DBVR	3.3 V	2.941 V
TPS3110E09DBVR	0.9 V	0.86 V
TPS3110E12DBVR	1.2 V	1.142 V
TPS3110E15DBVR	1.5 V	1.434 V
TPS3110K33DBVR	3.3 V	2.941 V

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Custom threshold voltages are available. Minimum order quantities apply. Contact factory for details and availability.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS3103	Click here	Click here	Click here	Click here	Click here
TPS3106	Click here	Click here	Click here	Click here	Click here
TPS3110	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3103E12DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFWI	Samples
TPS3103E12DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFWI	Samples
TPS3103E12DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFWI	Samples
TPS3103E12DBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFWI	Samples
TPS3103E15DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFXI	Samples
TPS3103E15DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFXI	Samples
TPS3103E15DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFXI	Samples
TPS3103E15DBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFXI	Samples
TPS3103H20DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFYI	Samples
TPS3103H20DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFYI	Samples
TPS3103K33DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGRI	Samples
TPS3103K33DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGRI	Samples
TPS3103K33DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGRI	Samples
TPS3103K33DBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGRI	Samples
TPS3106E09DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PFZI	Samples
TPS3106E09DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PFZI	Samples
TPS3106E09DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PFZI	Samples
TPS3106E09DBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PFZI	Samples
TPS3106E16DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGSI	Samples
TPS3106E16DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGSI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3106E16DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGSI	Samples
TPS3106E16DBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGSI	Samples
TPS3106K33DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGBI	Samples
TPS3106K33DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGBI	Samples
TPS3106K33DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGBI	Samples
TPS3106K33DBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGBI	Samples
TPS3110E09DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGII	Samples
TPS3110E12DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGJI	Samples
TPS3110E12DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGJI	Samples
TPS3110E15DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGKI	Samples
TPS3110E15DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGKI	Samples
TPS3110K33DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGLI	Samples
TPS3110K33DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGLI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3106 :

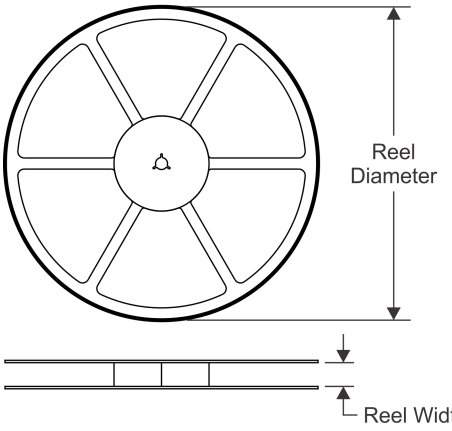
- Enhanced Product : TPS3106-EP

NOTE: Qualified Version Definitions:

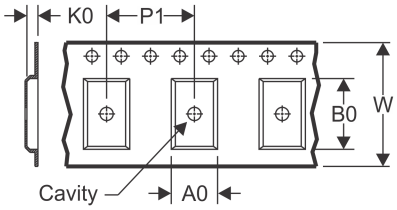
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

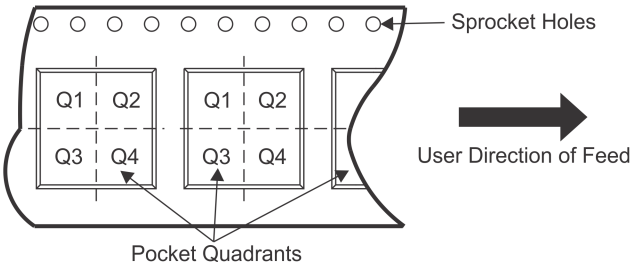


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

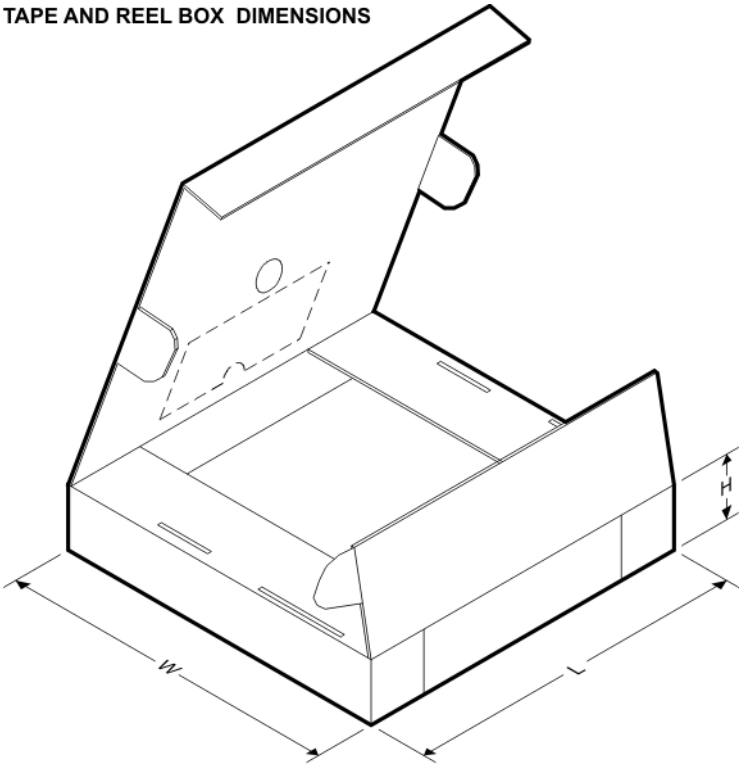


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3103E12DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3103E12DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3103E12DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3103E12DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3103E15DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3103E15DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3103H20DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3103H20DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3103H20DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3103H20DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3103K33DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3103K33DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3106E09DBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3106E09DBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3106E16DBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3106E16DBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3106K33DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3106K33DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3110E09DBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3110E12DBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3110E12DBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3110E15DBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3110E15DBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3110K33DBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3110K33DBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

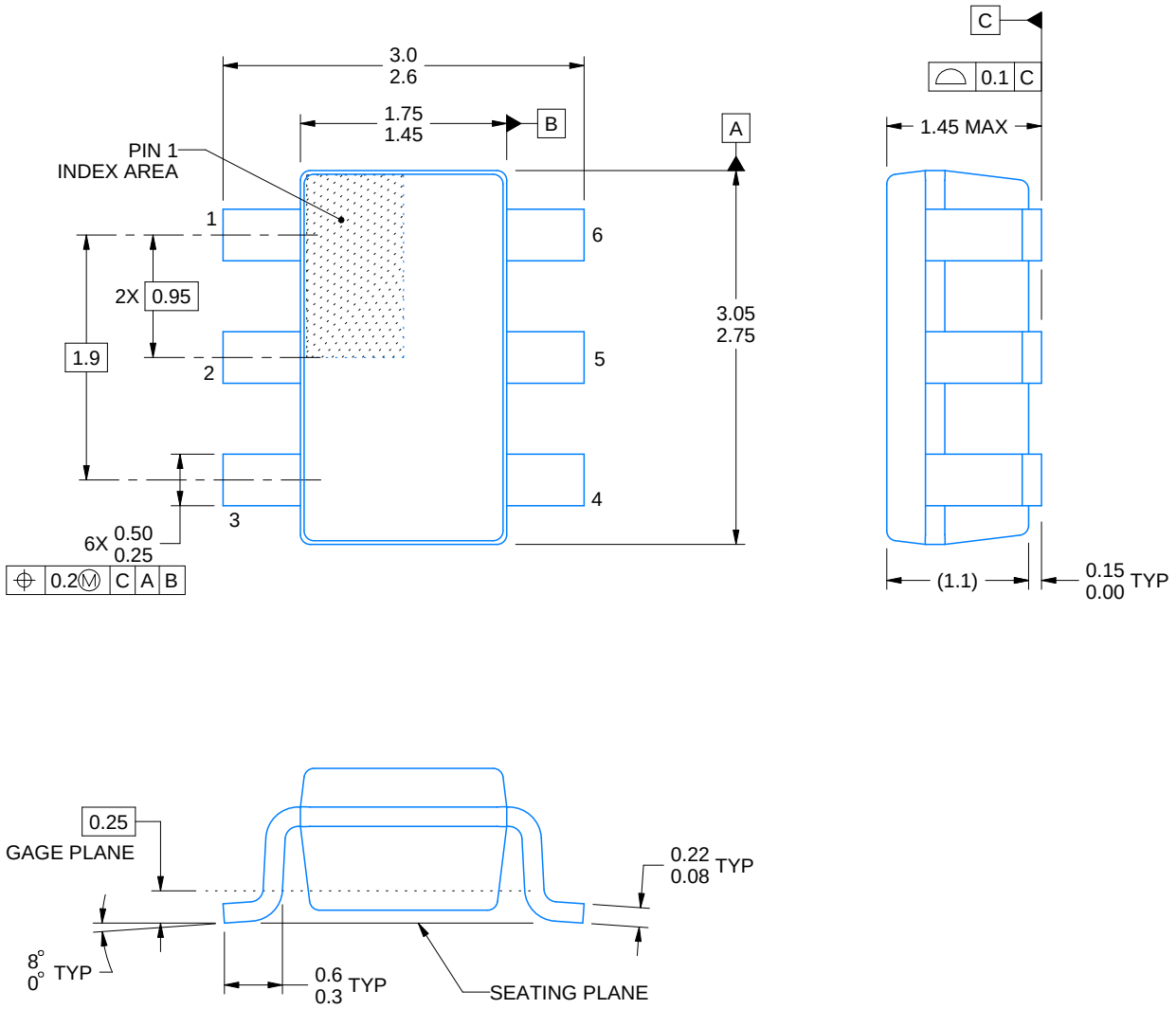
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3103E12DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3103E12DBVR	SOT-23	DBV	6	3000	200.0	183.0	25.0
TPS3103E12DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3103E12DBVT	SOT-23	DBV	6	250	200.0	183.0	25.0
TPS3103E15DBVR	SOT-23	DBV	6	3000	200.0	183.0	25.0
TPS3103E15DBVT	SOT-23	DBV	6	250	200.0	183.0	25.0
TPS3103H20DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3103H20DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3103H20DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3103H20DBVT	SOT-23	DBV	6	250	200.0	183.0	25.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3103K33DBVR	SOT-23	DBV	6	3000	200.0	183.0	25.0
TPS3103K33DBVT	SOT-23	DBV	6	250	200.0	183.0	25.0
TPS3106E09DBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS3106E09DBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TPS3106E16DBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS3106E16DBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TPS3106K33DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3106K33DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3110E09DBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS3110E12DBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS3110E12DBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TPS3110E15DBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS3110E15DBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TPS3110K33DBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS3110K33DBVT	SOT-23	DBV	6	250	182.0	182.0	20.0



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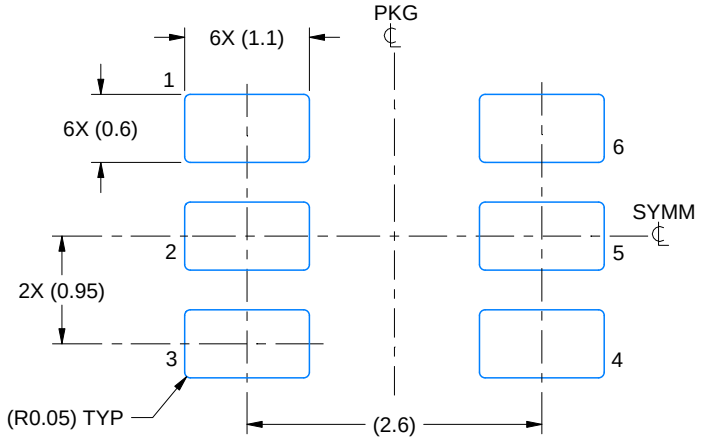
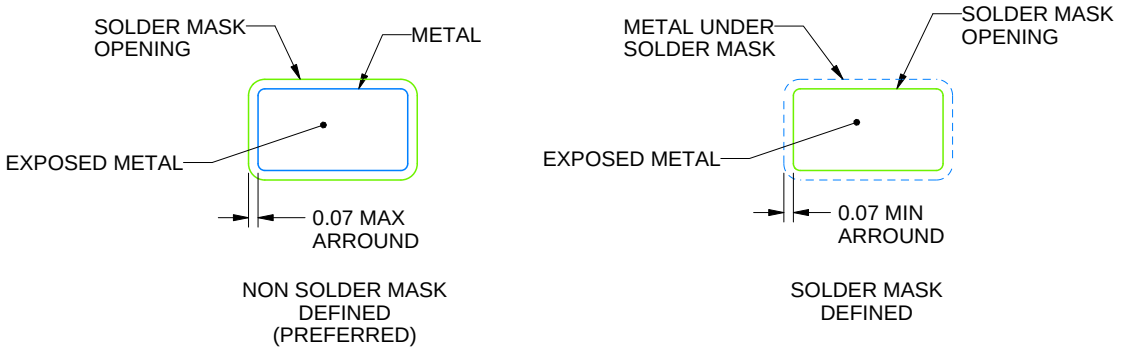
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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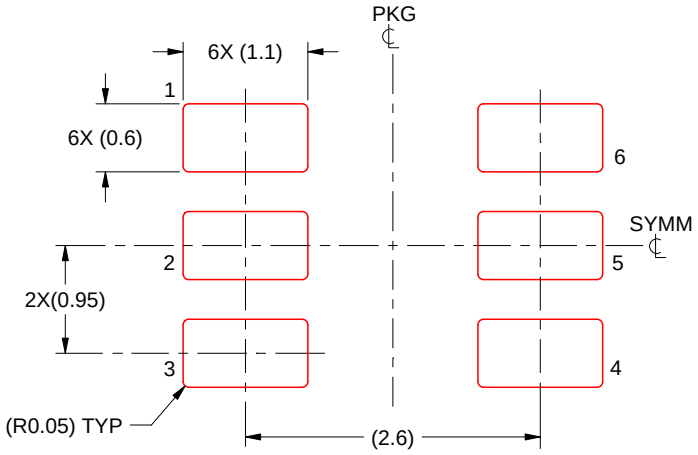
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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