DSLVDS1048 3.3V LVDS 四通道高速差动线路接收器

1 特性

- 旨在用于信号速率高达 400Mbps 的应用
- 直通引脚排列可简化 PCB 布局
- 150ps 通道到通道偏斜（典型值）
- 100ps 差动偏斜（典型值）
- 2.7ns 最大传播延迟
- 3.3V 电源设计
- 在断电模式下，LVDS 输入端具有高阻抗
- 低功耗设计（3.3V 静态条件下为 40mW）
- 能够与现有 5V LVDS 驱动器交互操作
- 接受小摆幅（350mV 典型值）差动信号电平
- 支持输入失效防护
  – 开路、短路及终止失效防护
- 0V 至 −100mV 阈值区域
- 工作温度范围：-40°C 至 +85°C
- 符合或超出 ANSI/TIA/EIA-644 标准
- 可采用 TSSOP 封装

2 应用

- 多功能打印机
- 板对板通信
- 测试和测量
- 打印机
- 数据中心互连
- 实验室仪表
- 超声波扫描仪

3 说明

DSLVDS1048 器件是一款四路 CMOS 直通差动线路接收器，专为需要超低功耗和高数据速率的 应用 而设计。该器件旨在使用低电压差动信号 (LVDS) 技术支持超过 400Mbps (200MHz) 的数据速率。

DSLVDS1048 接受低电压（350mV 典型值）差动输入信号，并将其转换为 3V CMOS 输出电平。该接收器支持 TRI-STATE 功能，可用于对输出进行多路复用。该接收器还支持开路、短路及终止 (100Ω) 输入失效防护。该接收器的输出在所有失效防护条件下均为高电平。DSLVDS1048 采用了直通引脚排列，可简化 PCB 布局。

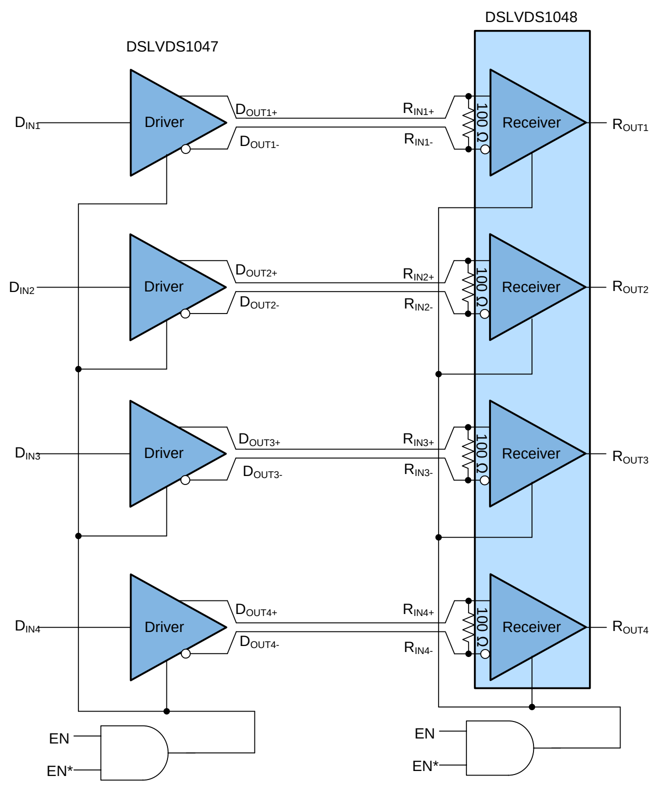
EN 和 EN* 输入将接受 AND 运算并控制 TRI-STATE 输出。这些使能端由四个接收器共用。DSLVDS1048 和配套的 LVDS 线路驱动器（例如 DSLVDS1047）为高速点对点接口应用提供了大功率 PECL/ECL 器件的替代 产品。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DSLVDS1048	TSSOP (16)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

图 1. 703A I2C



English Data Sheet: SNLS624

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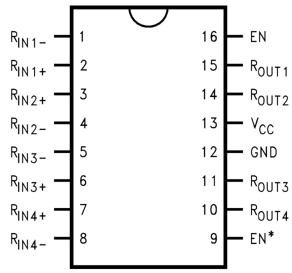
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2018 年 9 月	*	最初发布版本。

5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	16	I	Receiver enable pin: When EN is low, the receiver is disabled. When EN is high and EN* is low or open, the receiver is enabled. If both EN and EN* are open circuit, then the receiver is disabled.
EN*	9	I	Receiver enable pin: When EN* is high, the receiver is disabled. When EN* is low or open and EN is high, the receiver is enabled. If both EN and EN* are open circuit, then the receiver is disabled.
GND	12	—	Ground pin
R_{IN+}	2, 3, 6, 7	I	Noninverting receiver input pin
R_{IN-}	1, 4, 5, 8	I	Inverting receiver input pin
R_{OUT}	10, 11, 14, 15	O	Receiver output pin
V_{CC}	13	—	Power supply pin, +3.3V ± 0.3V

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)

			MIN	MAX	UNIT
Supply voltage (V_{CC})			–0.3	4	V
Input voltage (R_{IN+}, R_{IN-})			–0.3	3.6	V
Enable input voltage (EN, EN*)			–0.3	V_{CC} + 0.3	V
Output voltage (R_{OUT})			–0.3	V_{CC} + 0.3	V
Maximum package power dissipation at +25°C	PW0016A package			866	mW
	Derate PW0016A package	above +25°C		6.9	mW/°C
Lead temperature soldering	(4 s)			260	°C
Maximum junction temperature				150	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (1)	Human-body model (HBM)	±10000	V
		Machine model	±1200	

(1) ESD Rating:
HBM (1.5 kΩ, 100 pF)
EIAJ (0 Ω, 200 pF)

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Receiver input voltage	GND		3	V
Operating free air temperature, T_A	−40	25	85	°C

6.4 Thermal Information

THERMAL METRIC (1)		DSLVDS1048 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (1) (2)

PARAMETER		TEST CONDITIONS		PIN	MIN	TYP	MAX	UNIT
V_{TH}	Differential input high threshold	V_{CM} = +1.2 V, 0.05 V, 2.95 V (3)		R_{IN+}, R_{IN-}			100	mV
V_{TL}	Differential input low threshold				−100			mV
VCMR	Common-mode voltage range	VID = 200 mV peak to peak? (4)			0.1		2.3	V
I_{IN}	Input current	V_{IN} = +2.8 V	V_{CC} = 3.6 V or 0 V		−10	±5	10	μA
		V_{IN} = 0 V			−10	±1	10	
		V_{IN} = +3.6 V	V_{CC} = 0 V		–20	±1	20	
V_{OH}	Output high voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV, input terminated, input shorted		R_{OUT}	2.7	3.3		V
V_{OL}	Output low voltage	I_{OL} = 2 mA, V_{ID} = −200 mV					0.25	V
I_{OS}	Output short-circuit current	Enabled, V_{OUT} = 0 V (5)			−15	−47	−100	mA
I_{OZ}	Output TRI-STATE current	Disabled, V_{OUT} = 0 V or V_{CC}			−10	±1	10	μA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.
(2) All typicals are given for: V_{CC} = 3.3 V, T_A = 25°C.
(3) V_{CC} is always higher than R_{IN+} and R_{IN-} voltage. R_{IN-} and R_{IN+} are allowed to have a voltage range −0.2 V to V_{CC}− VID/2. However, to be compliant with AC specifications, the common voltage range is 0.1 V to 2.3 V.
(4) The VCMR range is reduced for larger VID. Example: if VID = 400 mV, the VCMR is 0.2 V to 2.2 V. The fail-safe condition with inputs shorted is not supported over the common-mode range of 0 V to 2.4 V, but is supported only with inputs shorted and no external common-mode voltage applied. A VID up to V_{CC} – 0 V may be applied to the R_{IN+}/ R_{IN-} inputs with the Common-Mode voltage set to V_{CC}/2. Propagation delay and Differential Pulse skew decrease when VID is increased from 200 mV to 400 mV. Skew specifications apply for 200 mV ≤ VID ≤ 800 mV over the common-mode range.
(5) Output short-circuit current (I_{OS}) is specified as magnitude only; minus sign indicates direction only. Only one output should be shorted at a time; do not exceed maximum junction temperature specification.

Electrical Characteristics (continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1)(2)

PARAMETER		TEST CONDITIONS	PIN	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		EN, EN*	2		V_{CC}	V
V_{IL}	Input low voltage		EN, EN*	GND		0.8	V
I_I	Input current	V_{IN} = 0 V or V_{CC}, other Input = V_{CC} or GND	EN, EN*	−10	±5	10	μA
V_{CL}	Input clamp voltage	I_{CL} = −18 mA	EN, EN*	−1.5	−0.8		V
I_{CC}	No load supply current receivers enabled	EN = V_{CC}, inputs open	V_{CC}		9	15	mA
I_{CCZ}	No load supply current receivers disabled	EN = GND, inputs open	V_{CC}		1	5	mA

6.6 Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1)(2)(3)(4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHLD}	Differential propagation delay high to low	C_L = 15 pF, V_{ID} = 200 mV (Figure 16 and Figure 17)	1.2	2	2.7	ns
t_{PLHD}	Differential propagation delay low to high	C_L = 15 pF, V_{ID} = 200 mV (Figure 16 and Figure 17)	1.2	2	2.7	ns
t_{SKD1}	Differential pulse skew $\|t_{PHLD} - t_{PLHD}\|$(5)	C_L = 15 pF, V_{ID} = 200 mV (Figure 16 and Figure 17)		0.1	0.4	ns
t_{SKD2}	Differential channel-to-channel skew; same device(3)	C_L = 15 pF, V_{ID} = 200 mV (Figure 16 and Figure 17)		0.15	0.5	ns
t_{SKD3}	Differential part-to-part skew(4)	C_L = 15 pF, V_{ID} = 200 mV (Figure 16 and Figure 17)			1	ns
t_{SKD4}	Differential part-to-part skew(6)	C_L = 15 pF, V_{ID} = 200 mV (Figure 16 and Figure 17)			1.5	ns
t_{TLH}	Rise time	C_L = 15 pF, V_{ID} = 200 mV (Figure 16 and Figure 17)		0.5	1	ns
t_{THL}	Fall time	C_L = 15 pF, V_{ID} = 200 mV (Figure 16 and Figure 17)		0.5	1	ns
t_{PHZ}	Disable time high to Z	R_L = 2 kΩ, C_L = 15 pF (Figure 18 and Figure 19)		8	14	ns
t_{PLZ}	Disable time low to Z	R_L = 2 kΩ, C_L = 15 pF (Figure 18 and Figure 19)		8	14	ns
t_{PZH}	Enable time Z to high	R_L = 2 kΩ, C_L = 15 pF (Figure 18 and Figure 19)		9	14	ns
t_{PZL}	Enable time Z to low	R_L = 2 kΩ, C_L = 15 pF (Figure 18 and Figure 19)		9	14	ns
f_{MAX}	Maximum operating frequency(7)	All channels switching	200	250		MHz

(1) All typicals are given for: V_{CC} = 3.3 V, T_A = 25°C.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, t_r and t_f (0% to 100%) ≤ 3 ns for R_{IN}.
(3) t_{SKD2}, channel-to-channel skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.
(4) t_{SKD3}, part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC}, and within 5°C of each other within the operating temperature range.
(5) t_{SKD1} is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel
(6) t_{SKD4}, part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max−Min| differential propagation delay.
(7) f_{MAX} generator input conditions: $t_r = t_f$ < 1 ns (0% to 100%), 50% duty cycle, differential (1.05-V to 1.35-V peak to peak). Output criteria: 60 / 40% duty cycle, V_{OL} (maximum 0.4 V), V_{OH} (minimum 2.7 V), Load = 15 pF (stray plus probes).

6.7 Typical Characteristics

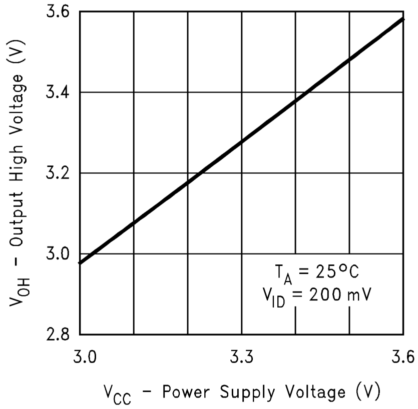


Figure 2. Output High Voltage vs Power Supply Voltage

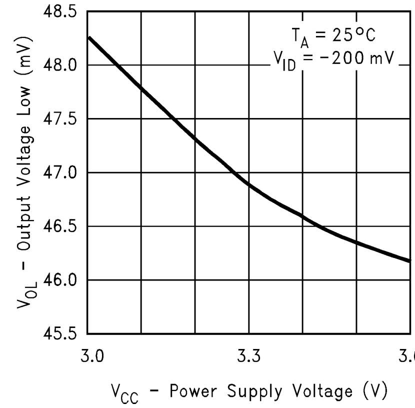


Figure 3. Output Low Voltage vs Power Supply Voltage

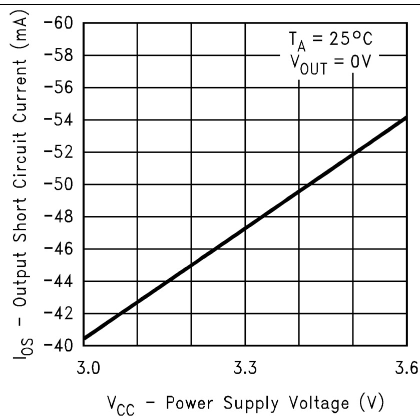


Figure 4. Output Short-Circuit Current vs Power Supply Voltage

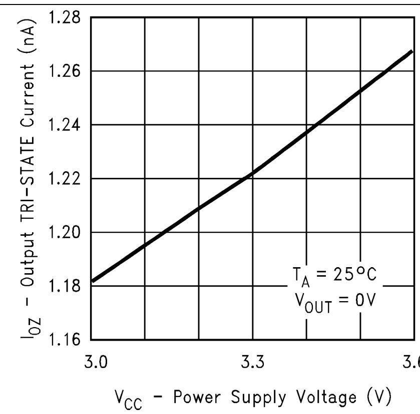


Figure 5. Output TRI-STATE Current vs Power Supply Voltage

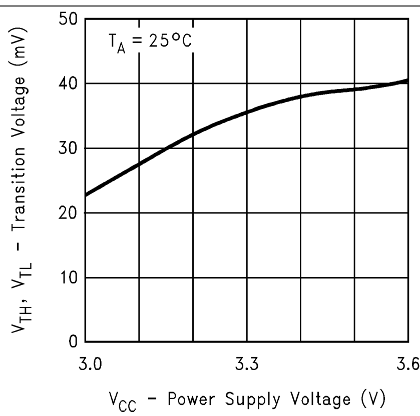


Figure 6. Differential Transition Voltage vs Power Supply Voltage

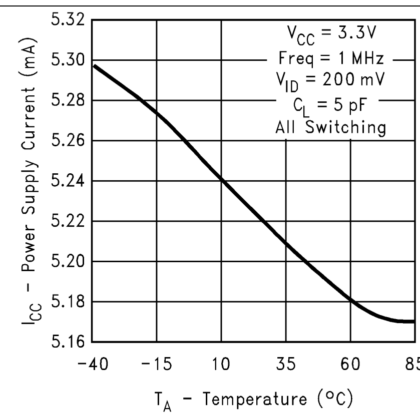


Figure 7. Power Supply Current vs Ambient Temperature

Typical Characteristics (continued)

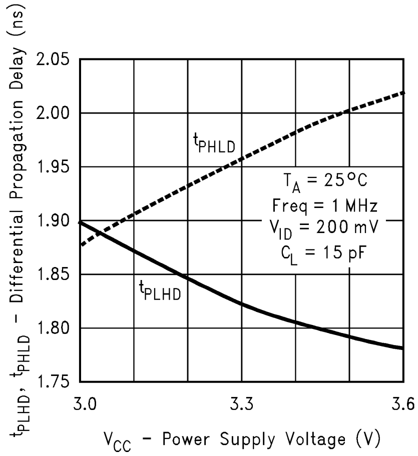


Figure 8. Differential Propagation Delay vs Power Supply Voltage

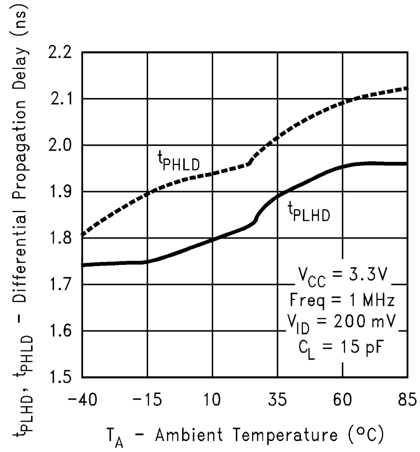


Figure 9. Differential Propagation Delay vs Ambient Temperature

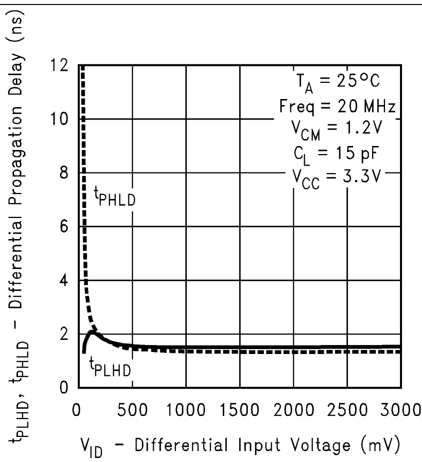


Figure 10. Differential Propagation Delay vs Differential Input Voltage

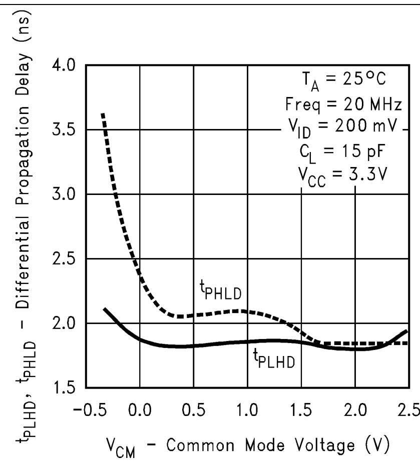


Figure 11. Differential Propagation Delay vs Common-Mode Voltage

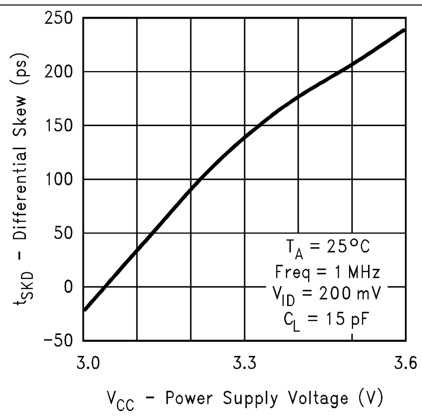


Figure 12. Differential Skew vs Power Supply Voltage

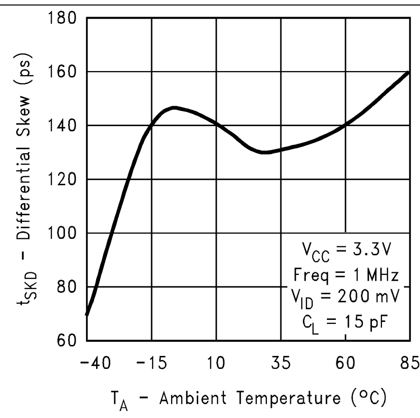


Figure 13. Differential Skew vs Ambient Temperature

Typical Characteristics (continued)

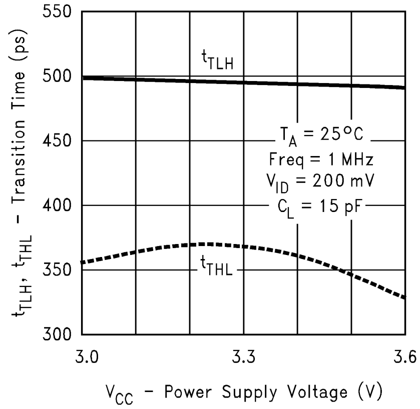


Figure 14. Transition Time vs Power Supply Voltage

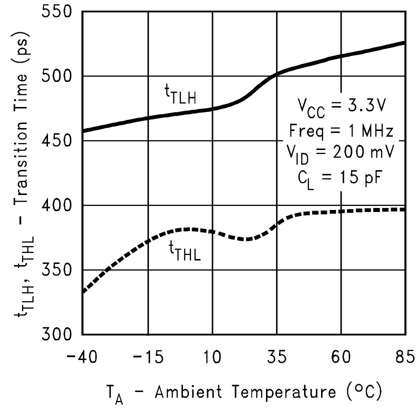


Figure 15. Transition Time vs Ambient Temperature

7 Parameter Measurement Information

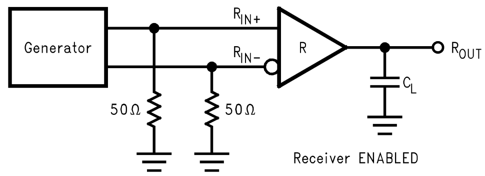


Figure 16. Receiver Propagation Delay and Transition Time Test Circuit

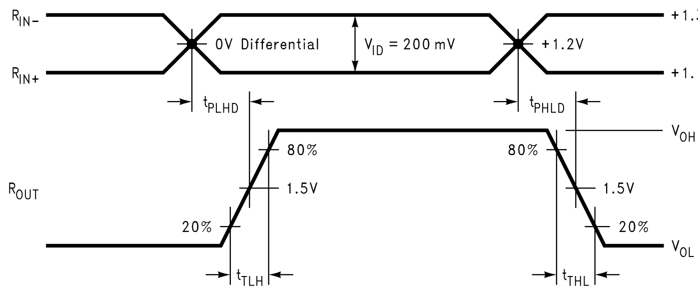
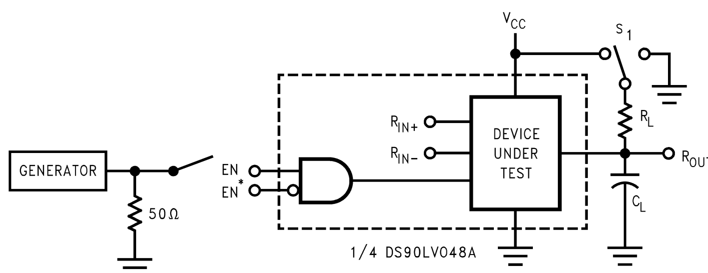


Figure 17. Receiver Propagation Delay and Transition Time Waveforms



C_L includes load and test jig capacitance.
S_1 = V_{CC} for t_{PZL} and t_{PLZ} measurements.
S_1 = GND for t_{PZH} and t_{PHZ} measurements.

Figure 18. Receiver TRI-STATE Delay Test Circuit

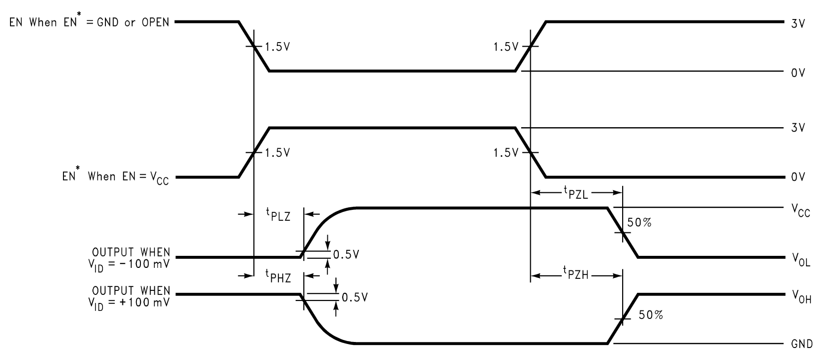


Figure 19. Receiver TRI-STATE Delay Waveforms

8 Detailed Description

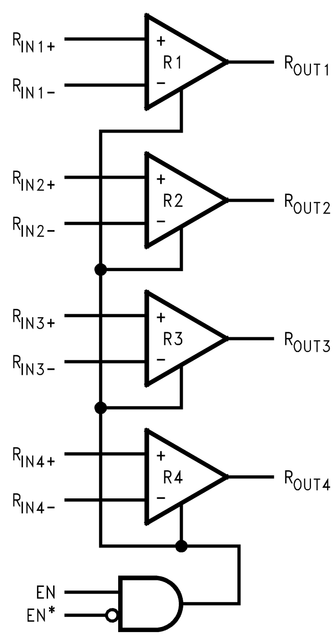
8.1 Overview

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as shown in Figure 20. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100 Ω. A termination resistor of 100 Ω (selected to match the media) is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be considered.

The DSLVDS1048 differential line receiver is capable of detecting signals as low as 100 mV, over a ±1-V common-mode range centered around +1.2 V. This is related to the driver offset voltage which is typically +1.2 V. The driven signal is centered around this voltage and may shift ±1 V around this center point. The ±1-V shifting may be the result of a ground potential difference between the ground reference of the driver and the ground reference of the receiver, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of 0 V to +2.4 V (measured from each pin to ground). The device operates for receiver input voltages up to V_{CC}, but exceeding V_{CC} turns on the ESD protection circuitry, which clamps the bus voltages.

The DSLVDS1048 has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device easily allows for matching electrical lengths of the differential pair trace lines between the driver and the receiver as well as allowing the trace lines to be close together to couple noise as common-mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Fail-Safe Feature

The LVDS receiver is a high-gain, high-speed device that amplifies a small differential signal (20 mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, take care to prevent noise from appearing as a valid signal.

The internal fail-safe circuitry of the receiver is designed to source or sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** The DSLVDS1048 is a quad receiver device, and if an application requires only 1, 2, or 3 receivers, the unused channel(s) inputs must be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pullup and pulldown resistors to set the output to a HIGH state. This internal circuitry ensures a HIGH, stable output state for open inputs.
2. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a TRI-STATE or power-off condition, the receiver output is again in a HIGH state, even with the end of cable 100-Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10 mV of differential noise, the receiver may see the noise as a valid signal and switch. To ensure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable offers better balance than flat ribbon cable.
3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0-V differential input voltage, the receiver output remains in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4 V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pullup and pulldown resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pullup and pulldown resistors must be in the 5-kΩ to 15-kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point must be set to approximately 1.2 V (less than 1.75 V) to be compatible with the internal circuitry.

Additional information on fail-safe biasing of LVDS devices may be found in *AN-1194 Failsafe Biasing of LVDS Interfaces* (SNLA051).

8.4 Device Functional Modes

Table 1 lists the functional modes of the DSLVDS1048.

Table 1. Truth Table

ENABLES		INPUT	OUTPUT
EN	EN*	$R_{IN+} - R_{IN-}$	R_{OUT}
H	L or Open	$V_{ID} \geq 0$ V	H
		$V_{ID} \leq -0.1$ V	L
		Full Fail-safe OPEN/SHORT or Terminated	H
All other combinations of ENABLE inputs		X	Z

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DSLVDS1048 has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device easily allows for matching electrical lengths of the differential pair trace lines between the driver and the receiver as well as allowing the trace lines to be close together to couple noise as common-mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

9.2 Typical Application

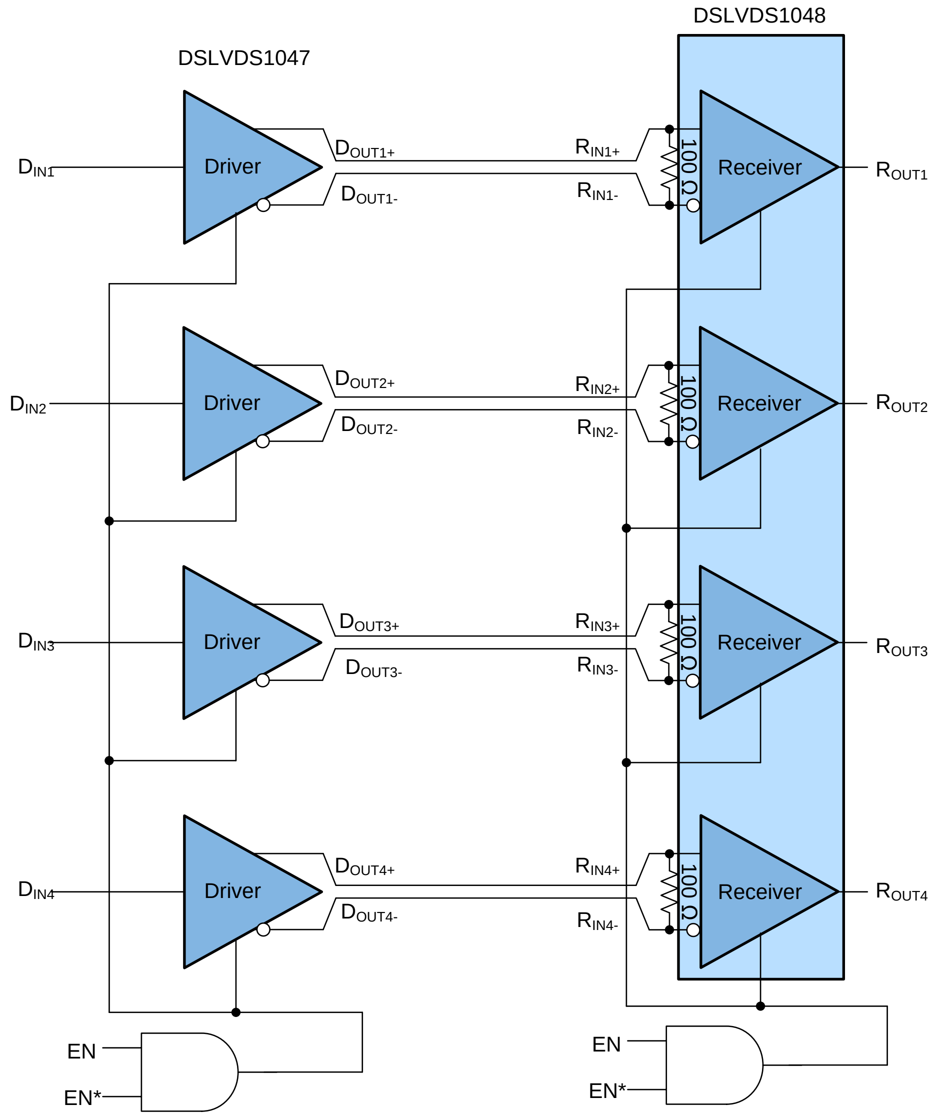

Figure 20. Balanced System Point-to-Point Application

Typical Application (continued)

9.2.1 Design Requirements

When using LVDS devices, it is important to remember to specify controlled impedance PCB traces, cable assemblies, and connectors. All components of the transmission media must have a matched differential impedance of about 100 Ω. They must not introduce major impedance discontinuities.

Balanced cables (for example, twisted pair) are usually better than unbalanced cables (ribbon cable) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential mode) noise which is rejected by the LVDS receiver.

For cable distances < 0.5 M, most cables can be made to work effectively. For distances 0.5 M ≤ d ≤ 10 M, CAT5 (Category 5) twisted pair cable works well, is readily available, and relatively inexpensive.

Table 2. Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Receiver Supply Voltage (V_{CC})	3.0 to 3.6 V
Receiver Output Voltage	0 to 3.6 V
Signaling Rate	0 to 400 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Receiver Nodes	1
Ground shift between driver and receiver	±1 V

9.2.2 Detailed Design Procedure

9.2.2.1 Probing LVDS Transmission Lines

Always use high impedance (> 100kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing gives deceiving results.

9.2.2.2 Threshold

The LVDS Standard (ANSI/TIA/EIA-644) specifies a maximum threshold of ±100 mV for the LVDS receiver. The DSLVDS1048 supports an enhanced threshold region of −100 mV to 0 V. This is useful for fail-safe biasing. The threshold region is shown in the Voltage Transfer Curve (VTC) in Figure 21. The typical DSLVDS1048 LVDS receiver switches at about −35 mV.

NOTE

With V_{ID} = 0 V, the output is in a HIGH state. With an external fail-safe bias of +25 mV applied, the typical differential noise margin is now the difference from the switch point to the bias point.

In the following example, this would be 60 mV of Differential Noise Margin (+25 mV − (−35 mV)). With the enhanced threshold region of −100 mV to 0 V, this small external fail-safe biasing of +25 mV (with respect to 0 V) gives a DNM of a comfortable 60 mV. With the standard threshold region of ±100 mV, the external fail-safe biasing would need to be +25 mV with respect to +100 mV or +125 mV, giving a DNM of 160 mV which is stronger fail-safe biasing than is necessary for the DSLVDS1048. If more DNM is required, then a stronger fail-safe bias point can be set by changing resistor values.

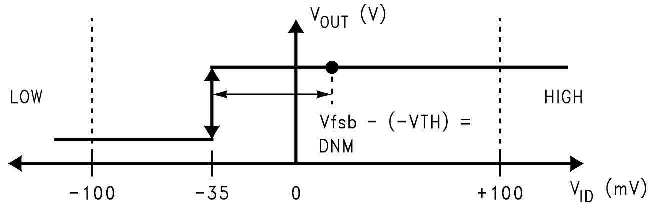

Figure 21. VTC of the DSLVDS1048 LVDS Receiver

9.2.3 Application Curve

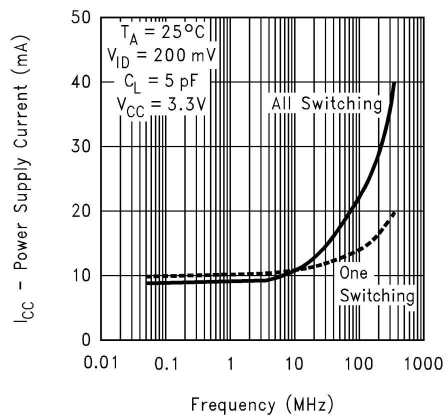

Figure 22. Power Supply Current vs Frequency

10 Power Supply Recommendations

Although the DSLVDS1047 draws very little power while at rest, its overall power consumption increases due to a dynamic current component. The DSLVDS1048 power supply connection must take this additional current consumption into consideration for maximum power requirements.

11 Layout

11.1 Layout Guidelines

- Use at least 4 PCB layers (top to bottom): LVDS signals, ground, power, and TTL signals.
- Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. Best practice is to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).
- Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

11.1.1 Power Decoupling Recommendations

Bypass capacitors must be used on power pins. Use high-frequency ceramic (surface mount is recommended) 0.1-µF and 0.001-µF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed-circuit board improves decoupling. Multiple vias must be used to connect the decoupling capacitors to the power planes. A 10-µF (35-V) or greater solid tantalum capacitor must be connected at the power entry point on the printed-circuit board between the supply and ground.

Layout Guidelines (continued)

11.1.2 Differential Traces

Use controlled impedance traces that match the differential impedance of your transmission medium (that is, cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs must be < 10 mm long). This helps eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1 mm apart radiate far less noise than traces 3 mm apart because magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals, which destroys the magnetic field cancellation benefits of differential signals and EMI, results. Remember the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997 mm/ps or 0.0118 in/ps.

Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number or vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed-circuit board, this distance must remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

11.1.3 Termination

Use a termination resistor that best matches the differential impedance or your transmission line. The resistor must be between 90 Ω and 130 Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS does not work without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs must be minimized. The distance between the termination resistor and the receiver must be < 10 mm (12 mm maximum).

11.2 Layout Example

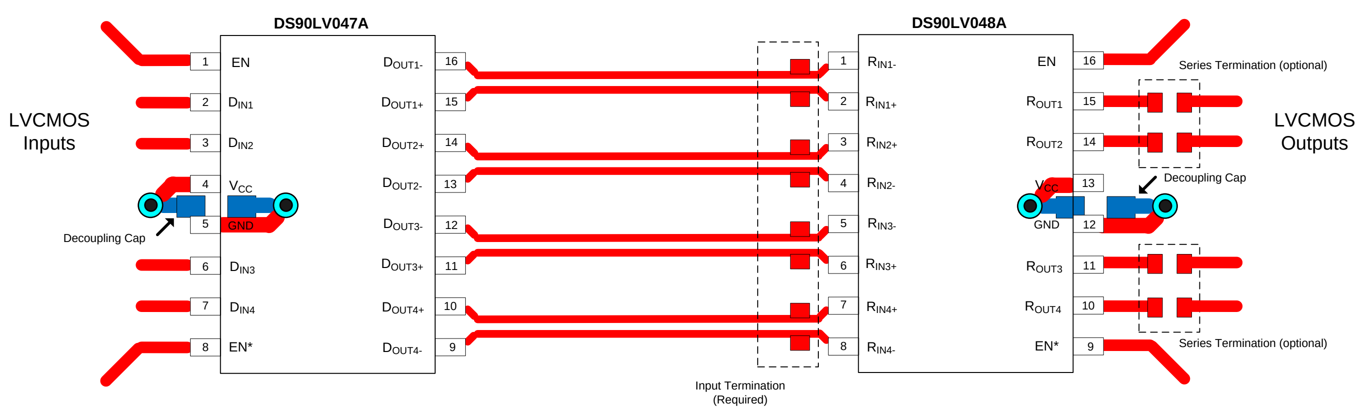

Figure 23. Layout Recommendation

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DSLVDS1048PWR	ACTIVE	TSSOP	PW	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DSLVDS 1048	Samples
DSLVDS1048PWT	ACTIVE	TSSOP	PW	16	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DSLVDS 1048	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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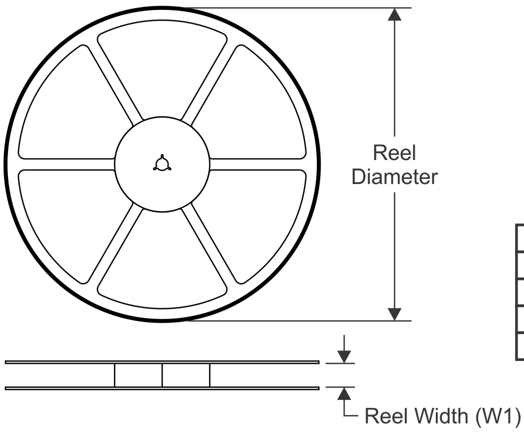
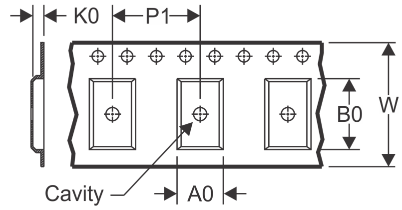
TAPE AND REEL INFORMATION

REEL DIMENSIONS

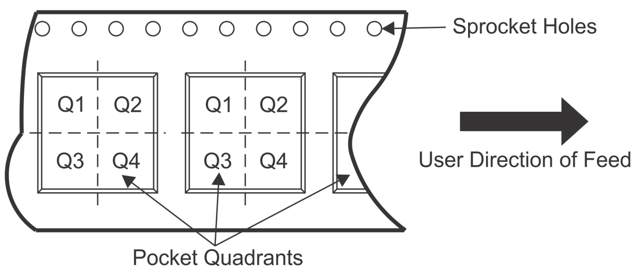


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

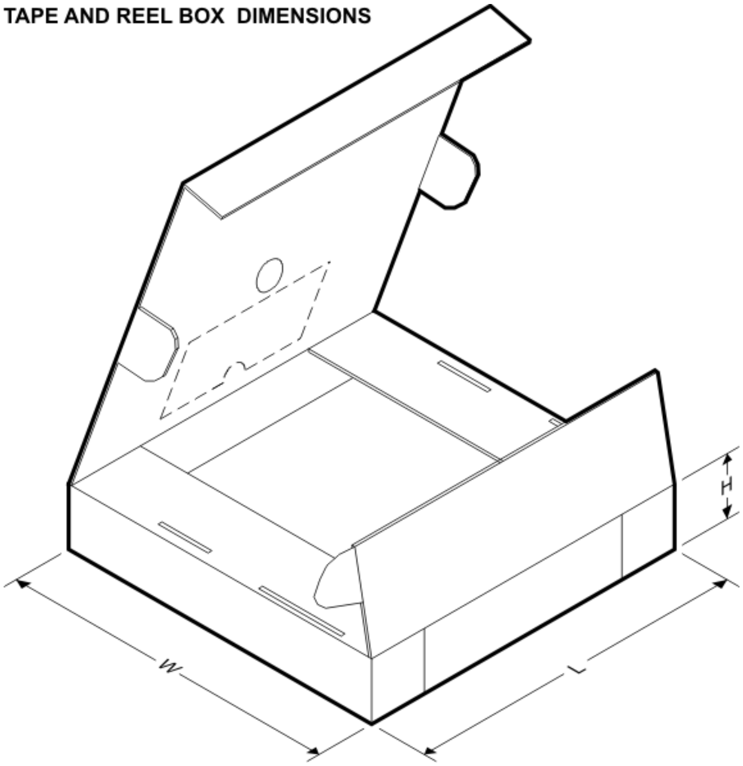
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

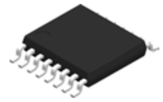
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DSLVDS1048PWR	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
DSLVDS1048PWT	TSSOP	PW	16	1000	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

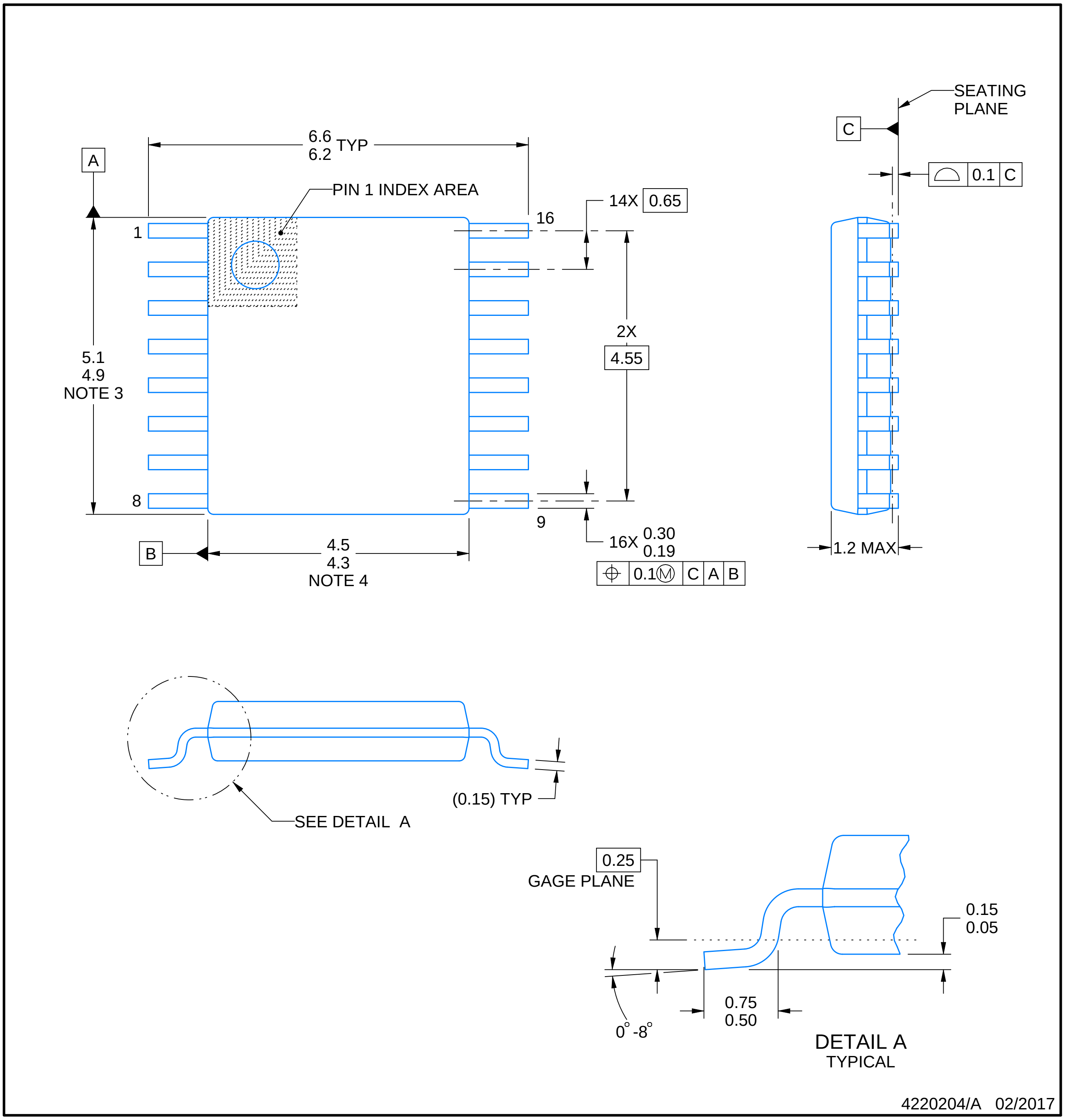
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DSLVDS1048PWR	TSSOP	PW	16	2500	367.0	367.0	35.0
DSLVDS1048PWT	TSSOP	PW	16	1000	367.0	367.0	35.0



PACKAGE OUTLINE

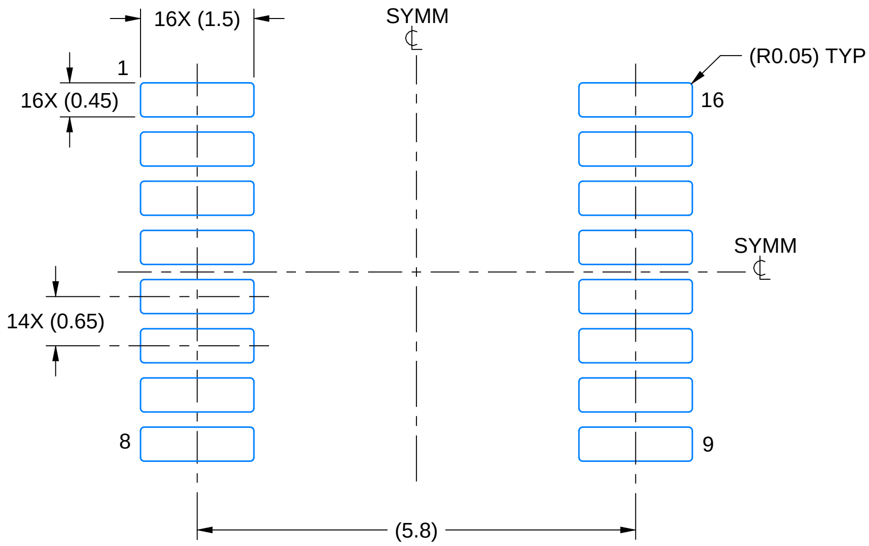
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

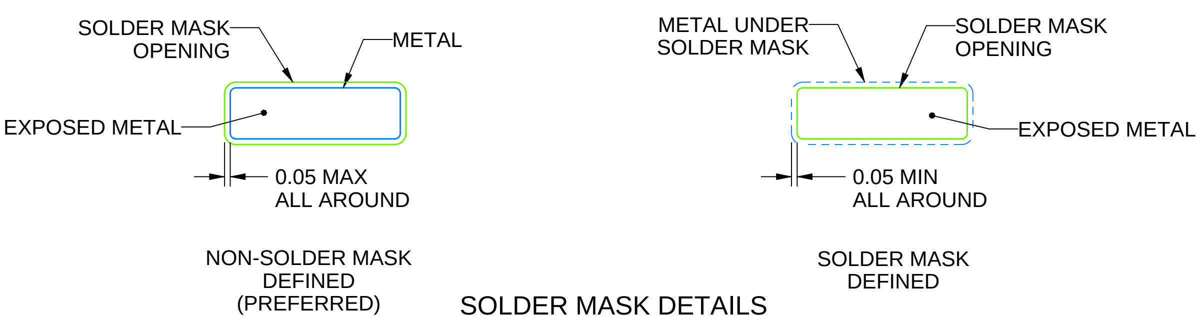


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

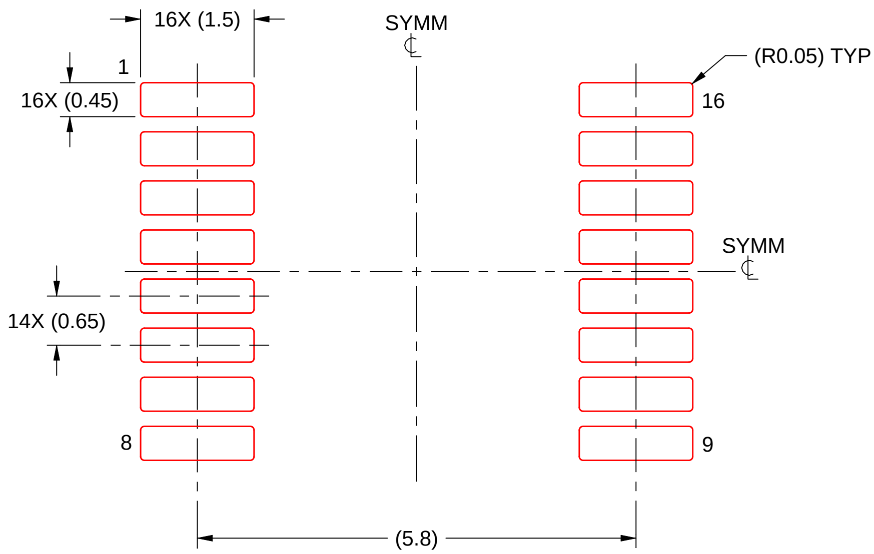


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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