500-mA DUAL DIFFERENTIAL LINE DRIVER

Check for Samples: THS6012

FEATURES

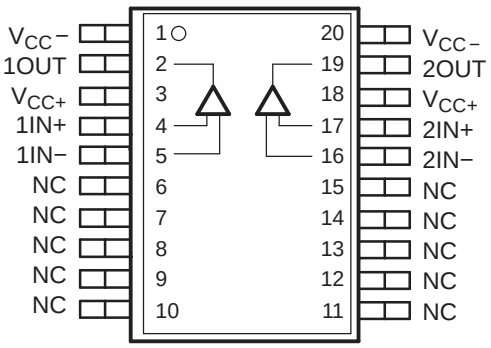
- **ADSL Differential Line Driver**
- **400 mA Minimum Output Current Into 25-Ω Load**
- **High Speed**
  - **140 MHz Bandwidth (-3dB) With 25-Ω Load**
  - **315 MHz Bandwidth (-3dB) With 100-Ω Load**
  - **1300 V/µs Slew Rate, G = 5**
- **Low Distortion**
  - **-72 dB 3rd Order Harmonic Distortion at f = 1 MHz, 25-Ω Load, and 20 V_{PP}**
- **Independent Power Supplies for Low Crosstalk**
- **Wide Supply Range ±4.5 V to ±16 V**
- **Thermal Shutdown and Short Circuit Protection**
- **Improved Replacement for AD815**
- **Evaluation Module Available**

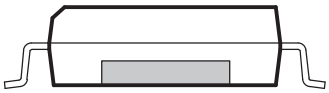
DESCRIPTION

The THS6012 contains two high-speed drivers capable of providing 400 mA output current (min) into a 25 Ω load. These drivers can be configured differentially to drive a 50-V_{PP} output signal over low-impedance lines. The drivers are current feedback amplifiers, designed for the high slew rates necessary to support low total harmonic distortion (THD) in xDSL applications. The THS6012 is ideally suited for asymmetrical digital subscriber line (ADSL) applications at the central office, where it supports the high-peak voltage and current requirements of this application.

Separate power supply connections for each driver are provided to minimize crosstalk. The THS6012 is available in the small surface-mount, thermally enhanced 20-pin PowerPAD™ package.

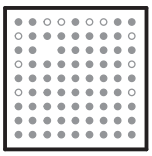
Thermally Enhanced SOIC (DWP) PowerPAD™ Package (TOP VIEW)





Cross Section View Showing PowerPAD

MicroStar™ Junior (GQE) Package (TOP VIEW)



(SIDE VIEW)

HIGH-SPEED xDSL LINE DRIVER/RECEIVER FAMILY

DEVICE	DRIVER	RECEIVER	DESCRIPTION
THS6002	•	•	Dual differential line drivers and receivers
THS6012	•		500-mA Dual differential line driver
THS6022	•		250-mA Dual differential line driver
THS6032	•		Low-power ADSL central office line driver
THS6062		•	Low-noise ADSL receiver
THS7002		•	Low-noise programmable gain ADSL receiver

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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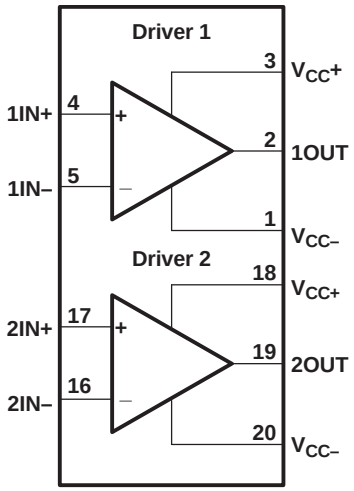
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 1. AVAILABLE OPTIONS

T_A	PACKAGED DEVICE		
	PowerPAD PLASTIC SMALL OUTLINE(1) (DWP)	MicroStar Junior (GQE)	EVALUATION MODULE
0°C to 70°C	THS6012CDWP	THS6012CGQE	THS6012EVM
-40°C to 85°C	THS6012IDWP	THS6012IGQE	—

(1) The PWP packages are available taped and reeled. Add an R suffix to the device type (i.e., THS6012CPWPR)

FUNCTIONAL BLOCK DIAGRAM



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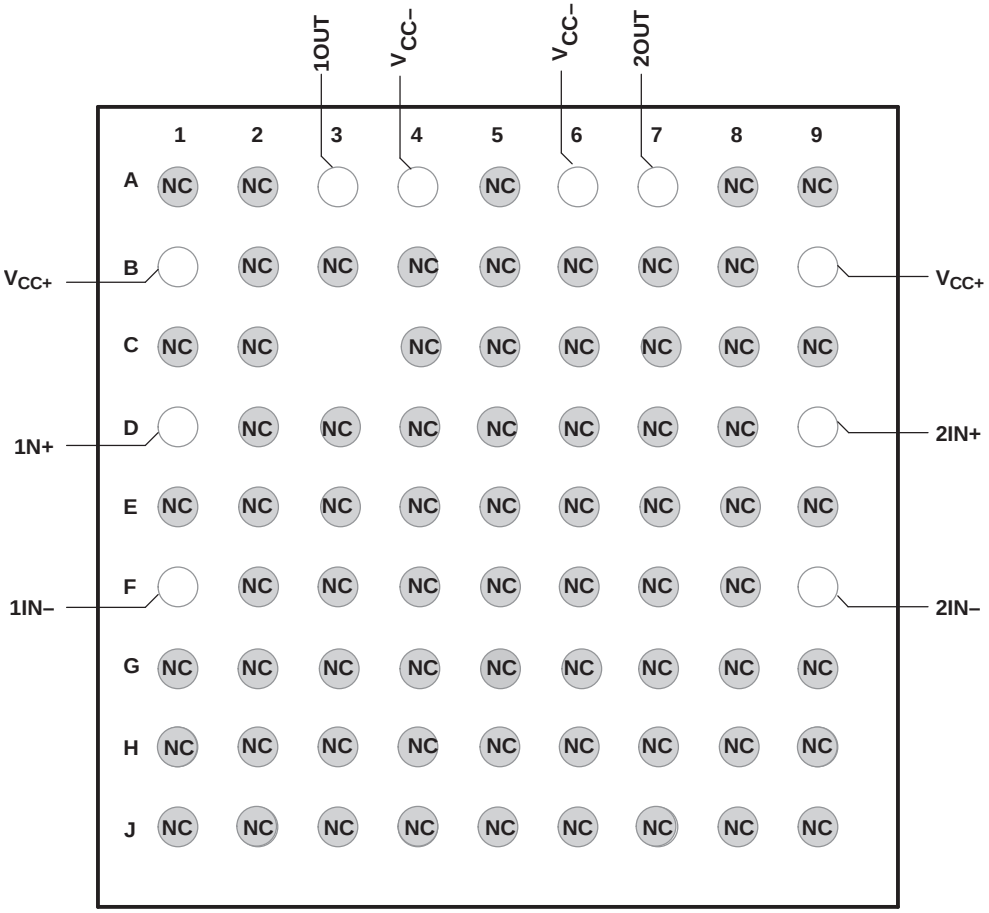
Terminal Functions

TERMINAL		
NAME	DWP PACKAGE NO.	GQE PACKAGE NO.
1OUT	2	A3
1IN-	5	F1
1IN+	4	D1
2OUT	19	A7
2IN-	16	F9
2IN+	17	D9
V_{CC+}	3, 18	B1, B9
V_{CC-}	1, 20	A4, A6
NC	6, 7, 8 ,9, 10, 11, 12, 13, 14, 15	NA

PIN ASSIGNMENTS

MicroStar™ Junior (GQE) Package
(TOP VIEW)



NOTE: Shaded terminals are used for thermal connection to the ground plane.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		UNIT
V_{CC}	Supply voltage, V_{CC+} to V_{CC-}	33 V
V_I	Input voltage (driver and receiver)	$\pm V_{CC}$
I_O	Output current (driver) (2)	800 mA
V_{ID}	Differential input voltage	6 V
	Continuous total power dissipation at (or below) T_A = 25°C (2)	5.8 W
T_A	Operating free air temperature	-40°C to 85°C
T_{stg}	Storage temperature	-65°C to 125°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The THS6012 incorporates a PowerPad on the underside of the chip. This acts as a heatsink and must be connected to a thermal dissipation plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature, which could permanently damage the device. See the *Thermal Information* section of this document for more information about PowerPad technology.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	Split supply	±4.5		±16	V
		Single supply	9		32	
T_A	Operating free-air temperature	C suffix	0		70	°C
		I suffix	–40		85	

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15 V, R_L = 25 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)			MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE								
BW	Small-signal bandwidth (-3 dB)	V_I = 200 mV, G = 1,	R_F = 680 Ω, R_L = 25 Ω	V_{CC} = ±15 V		140		MHz
		V_I = 200 mV, G = 1,	R_F = 1 kΩ, R_L = 25 Ω	V_{CC} = ±5 V		100		
		V_I = 200 mV, G = 2,	R_F = 620 Ω, R_L = 25 Ω	V_{CC} = ±15 V		120		
		V_I = 200 mV, G = 2,	R_L = 25 Ω, R_F = 820 Ω,	V_{CC} = ±5 V		100		
		V_I = 200 mV, G = 1,	R_F = 820 Ω, R_L = 100 Ω	V_{CC} = ±15 V		315		
		V_I = 200 mV, G = 2,	R_F = 560 Ω, R_L = 100 Ω	V_{CC} = ±15 V		265		
	Bandwidth for 0.1 dB flatness	V_I = 200 mV,	G = 1	V_{CC} = ±5 V, R_F = 820 Ω		30		MHz
				V_{CC} = ±15 V, R_F = 680 Ω		40		
	Full power bandwidth	V_{CC} = ±15 V,	$V_{O(PP)}$ = 20 V			20		MHz
		V_{CC} = ±5 V,	$V_{O(PP)}$ = 4 V			35		
SR	Slew rate	V_{CC} = ±15 V,	V_O = 20 $V_{(PP)}$,	G = 5		1300		V/µs
		V_{CC} = ±5 V,	V_O = 5 $V_{(PP)}$,	G = 2		900		
t_s	Settling time to 0.1%	0 V to 10 V Step,		G = 2		70		ns
NOISE/DISTORTION PERFORMANCE								

(1) Full range is 0°C to 70°C for the THS6012C and -40°C to 85°C for the THS6012I.

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = ±15 V, R_L = 25 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
THD	Total harmonic distortion		V_{CC} = ±15 V, G = 2,	R_F = 680 Ω, f = 1 MHz	$V_{O(PP)}$ = 20 V		-65		dBc
					$V_{O(PP)}$ = 2 V		-79		
			V_{CC} = ±5 V, G = 2,	R_F = 680 Ω, f = 1 MHz	$V_{O(PP)}$ = 2 V		-76		
V_n	Input voltage noise		V_{CC} = ±5 V or ±15 V, f = 10 kHz, G = 2, Single-ended				1.7		nV/√Hz
I_n	Input noise current	Positive (IN+)	V_{CC} = ±5 V or ±15 V, f = 10 kHz, G = 2				11.5		pA/√Hz
		Negative (IN-)					16		
A_D	Differential gain error		G = 2, R_L = 150 Ω,	NTSC, 40 IRE Modulation	V_{CC} = ±5 V		0.04%		
					V_{CC} = ±15 V		0.05%		
φ_D	Differential phase error		G = 2, R_L = 150 Ω,	NTSC, 40 IRE Modulation	V_{CC} = ±5 V		0.07°		
					V_{CC} = ±15 V		0.08°		
	Crosstalk	Driver to driver	V_I = 200 mV,	f = 1 MHz			-62		dB
DC PERFORMANCE									
	Open loop transresistance		V_{CC} = ±5 V				1.5		MΩ
			V_{CC} = ±15 V				5		
V_{IO}	Input offset voltage		V_{CC} = ±5 V or ±15 V		T_A = 25°C		2	5	mV
					T_A = full range			7	
	Input offset voltage drift		V_{CC} = ±5 V or ±15 V,		T_A = full range			20	μV/°C
	Differential input offset voltage		V_{CC} = ±5 V or ±15 V		T_A = 25°C		1.5	4	mV
					T_A = full range			5	
I_{IB}	Input bias current	Negative	V_{CC} = ±5 V or ±15 V		T_A = 25°C		3	9	μA
					T_A = full range			12	
		Positive			T_A = 25°C		4	10	μA
					T_A = full range			12	
		Differential			T_A = 25°C		1.5	8	μA
					T_A = full range			11	
	Differential input offset voltage drift		V_{CC} = ±5 V or ±15 V,		T_A = full range			10	μV/°C
INPUT CHARACTERISTICS									
V_{ICR}	Common-mode input voltage range		V_{CC} = ±5 V			±3.6	±3.7		V
			V_{CC} = ±15 V			±13.4	±13.5		
CMRR	Common-mode rejection ratio		V_{CC} = ±5 V or ±15 V,		T_A = full range	62	70		dB
	Differential common-mode rejection ratio						100		
R_I	Input resistance						300		kΩ
C_I	Differential input capacitance						1.4		pF
OUTPUT CHARACTERISTICS									
V_O	Output voltage swing	Single ended	R_L = 25 Ω	V_{CC} = ±5 V		3 to -2.8	3.2 to -3		V
				V_{CC} = ±15 V		11.8 to -11.5	12.5 to -12.2		
		Differential	R_L = 50 Ω	V_{CC} = ±5 V		6 to -5.6	6.4 to -6		V
				V_{CC} = ±15 V		23.6 to -23	25 to -24.4		
I_O	Output current[2]		R_L = 5 Ω,	V_{CC} = ±5 V			500		mA
			R_L = 25 Ω,	V_{CC} = ±15 V		400	500		

(2) A heat sink is required to keep the junction temperature below absolute maximum when an output is heavily loaded or shorted. See absolute maximum ratings and *Thermal Information* section.

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = ±15 V, R_L = 25 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
I_{OS}	Short-circuit output current[2]				800		mA
R_O	Output resistance	Open loop			13		Ω
POWER SUPPLY							
V_{CC}	Power supply operating range	Split supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Quiescent current (each driver)	V_{CC} = ±5 V,	T_A = full range			12	mA
		V_{CC} = ±15 V	T_A = 25°C		11.5	13	
			T_A = full range			15	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V	T_A = 25°C	-68	-74		dB
			T_A = full range	-65			
		V_{CC} = ±15 V	T_A = 25°C	-64	-72		dB
			T_A = full range	-62			

PARAMETER MEASUREMENT INFORMATION

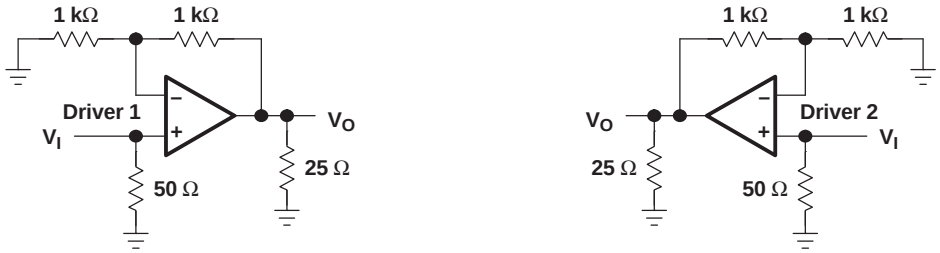

Figure 1. Input-to-Output Crosstalk Test Circuit

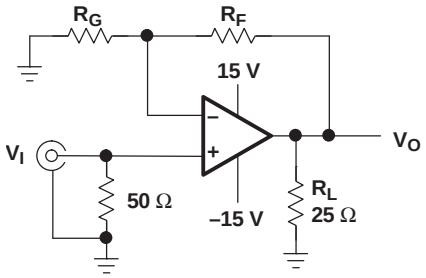

Figure 2. Test Circuit, Gain = 1 + (R_F/R_G)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$V_{O(PP)}$	Peak-to-peak output voltage	vs Supply voltage	3
		vs Load resistance	4
V_{IO}	Input offset voltage	vs Free-air temperature	5
I_{IB}	Input bias current	vs Free-air temperature	6
CMRR	Common-mode rejection ratio	vs Free-air temperature	7
	Input-to-output crosstalk	vs Frequency	8

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TYPICAL CHARACTERISTICS (continued)

			FIGURE
PSRR	Power supply rejection ratio	vs Free-air temperature	9
	Closed-loop output impedance	vs Frequency	10
I_{CC}	Supply current	vs Supply voltage	11
		vs Free-air temperature	12
SR	Slew rate	vs Output step	13, 14
V_n	Input voltage noise	vs Frequency	15
I_n	Input current noise	vs Frequency	
	Normalized frequency response	vs Frequency	16, 17
	Output amplitude	vs Frequency	18 - 21
	Normalized output response	vs Frequency	22 - 25
	Small and large frequency response		26, 27
	Single-ended harmonic distortion	vs Frequency	28, 29
		vs Output voltage	30, 31
	Differential gain	DC input offset voltage	32, 33
		Number of 150-Ω loads	34, 35
	Differential phase	DC input offset voltage	32, 33
		Number of 150-Ω loads	34, 35
	Output step response		36 - 38

PEAK-TO-PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

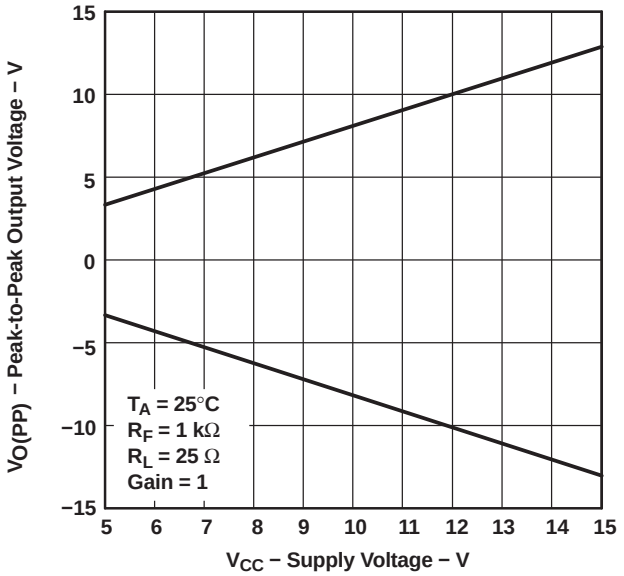

Figure 3.

PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

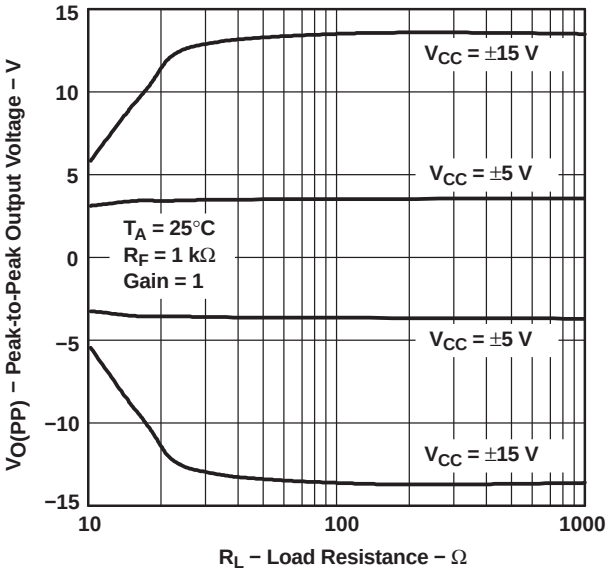

Figure 4.

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INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

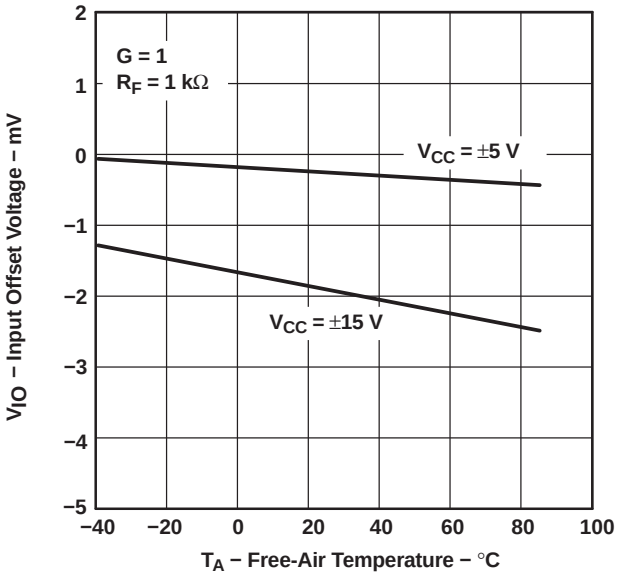

Figure 5.

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

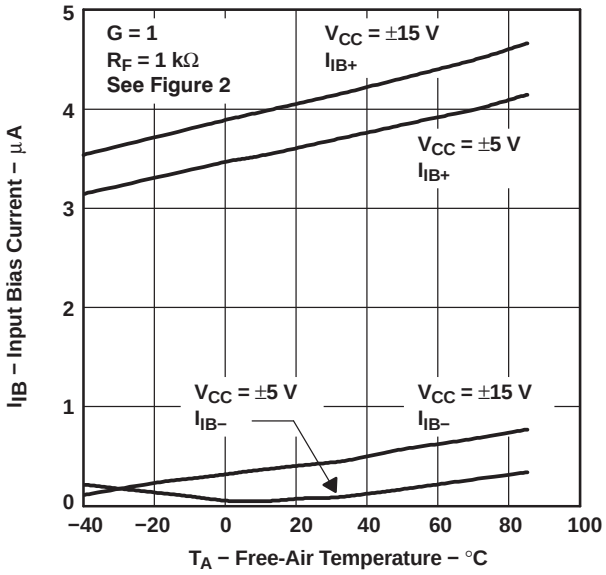

Figure 6.

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

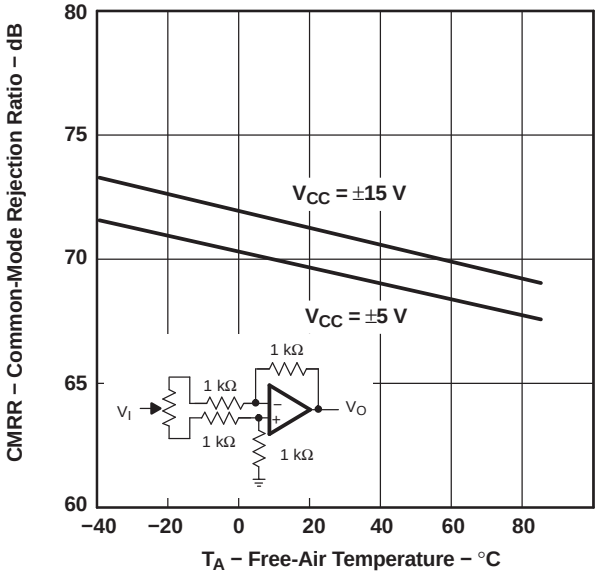

Figure 7.

INPUT-TO-OUTPUT CROSSTALK vs FREQUENCY

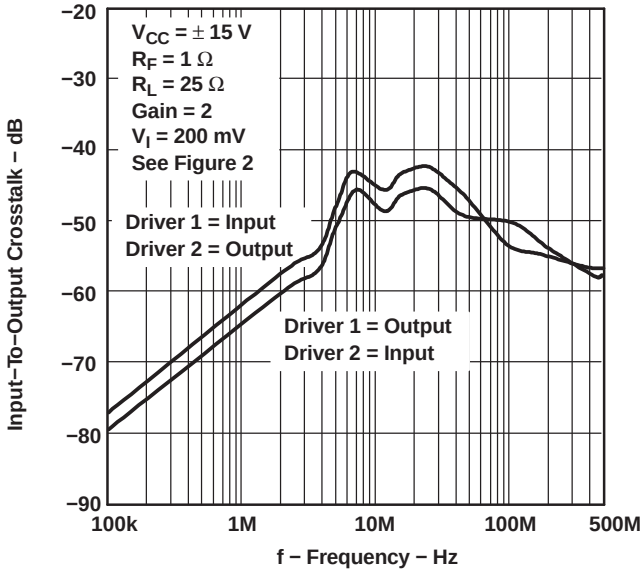

Figure 8.

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POWER SUPPLY REJECTION RATIO vs FREE-AIR TEMPERATURE

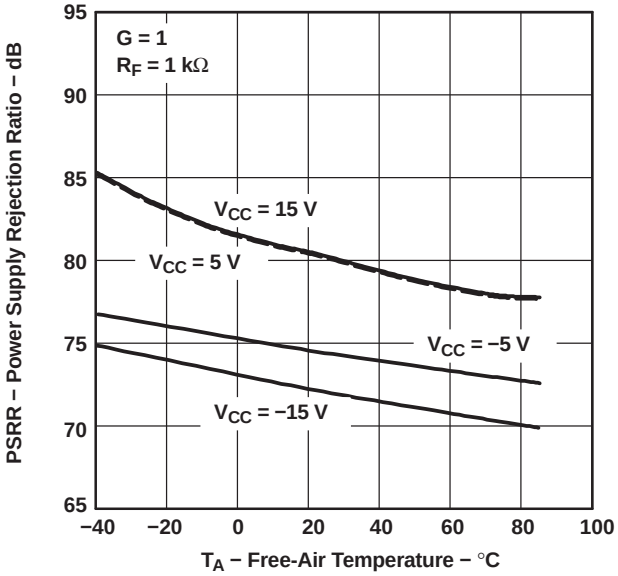

Figure 9.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

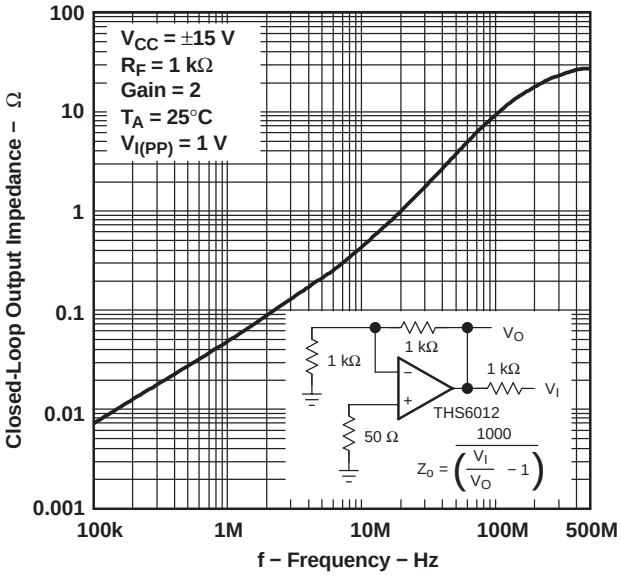

Figure 10.

SUPPLY CURRENT vs SUPPLY VOLTAGE

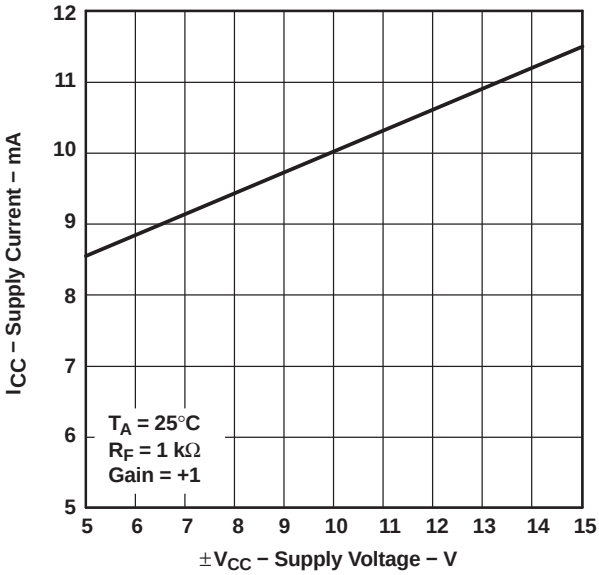

Figure 11.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

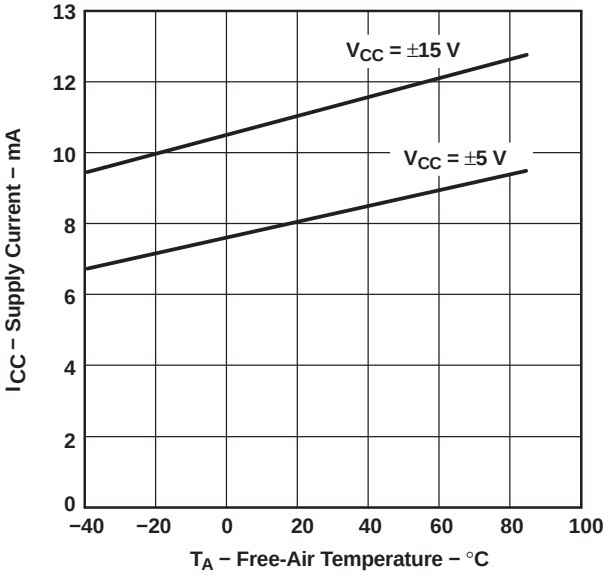

Figure 12.

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SLEW RATE vs OUTPUT STEP

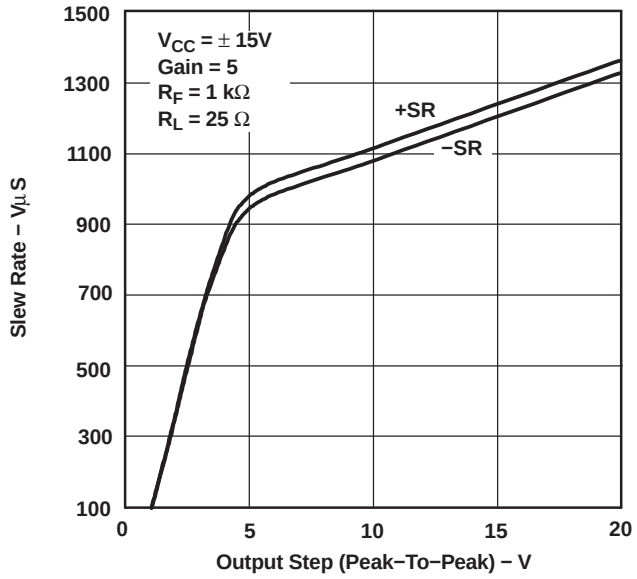

Figure 13.

SLEW RATE vs OUTPUT STEP

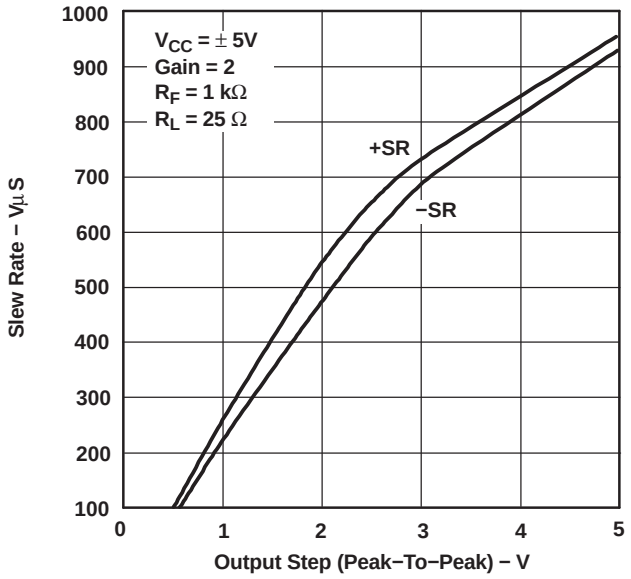

Figure 14.

INPUT VOLTAGE AND CURRENT NOISE vs FREQUENCY

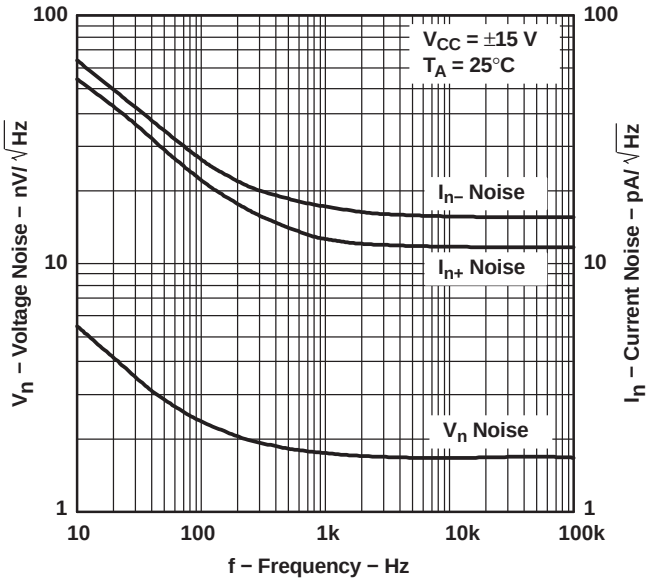

Figure 15.

NORMALIZED FREQUENCY RESPONSE vs FREQUENCY

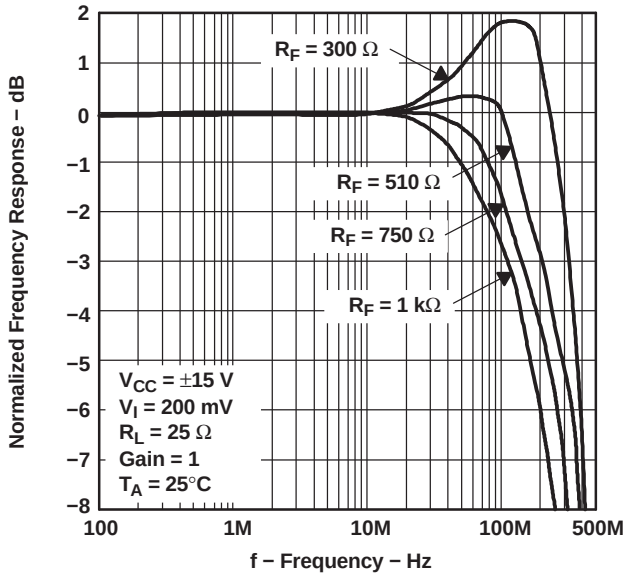

Figure 16.

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NORMALIZED FREQUENCY RESPONSE vs FREQUENCY

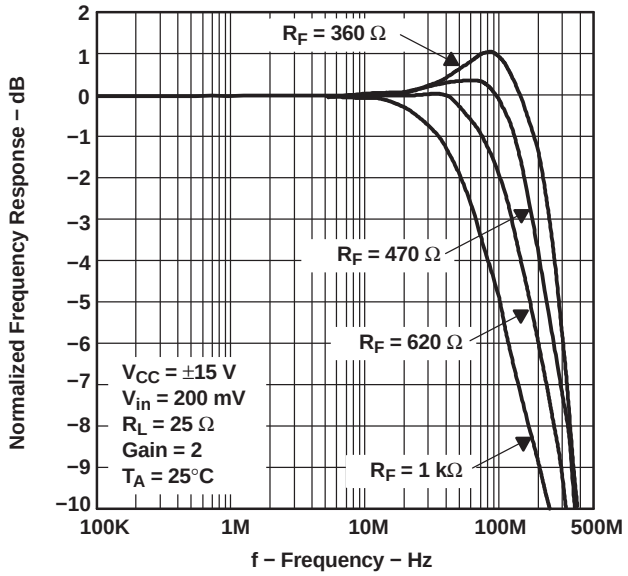

Figure 17.

OUTPUT AMPLITUDE vs FREQUENCY

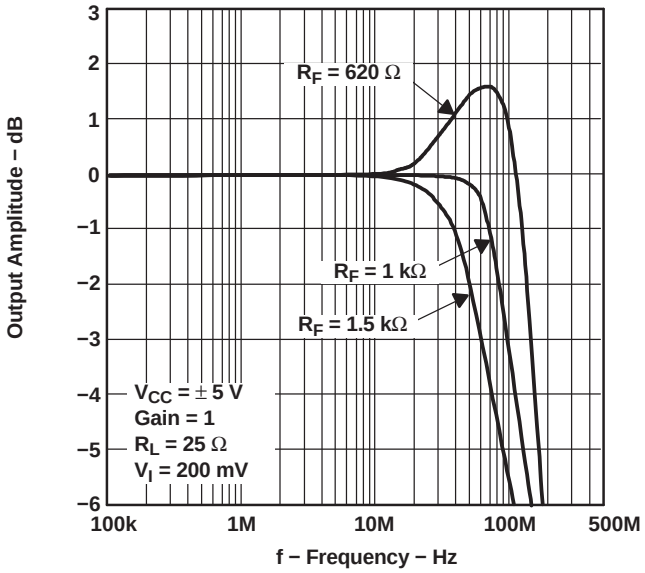

Figure 18.

OUTPUT AMPLITUDE vs FREQUENCY

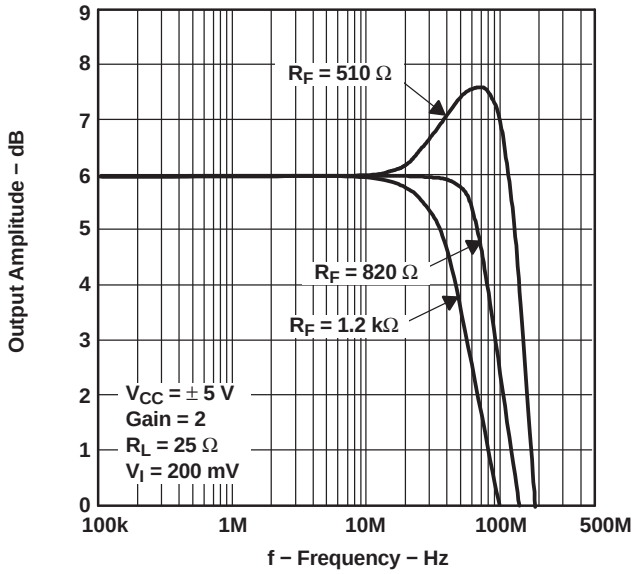

Figure 19.

OUTPUT AMPLITUDE vs FREQUENCY

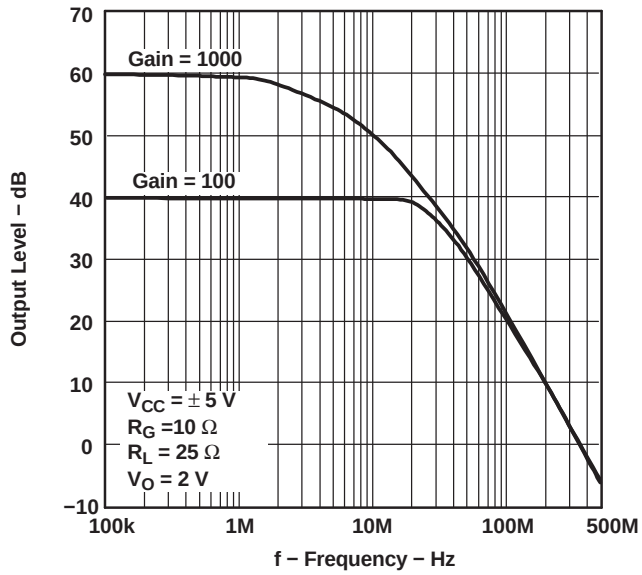

Figure 20.

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OUTPUT AMPLITUDE vs FREQUENCY

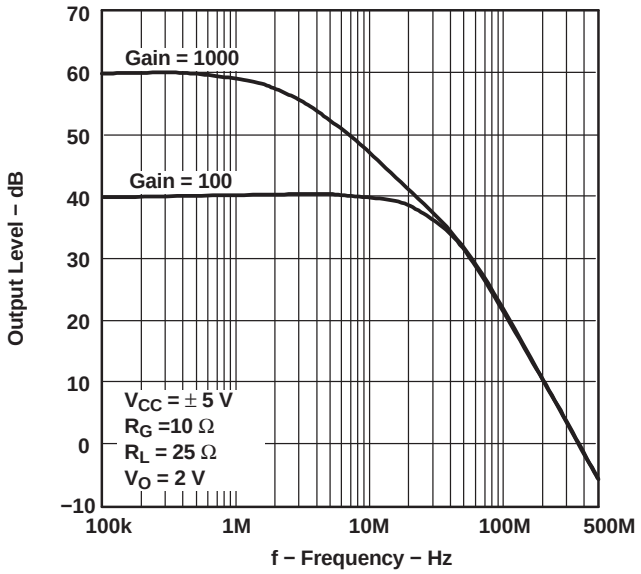

Figure 21.

NORMALIZED OUTPUT RESPONSE vs FREQUENCY

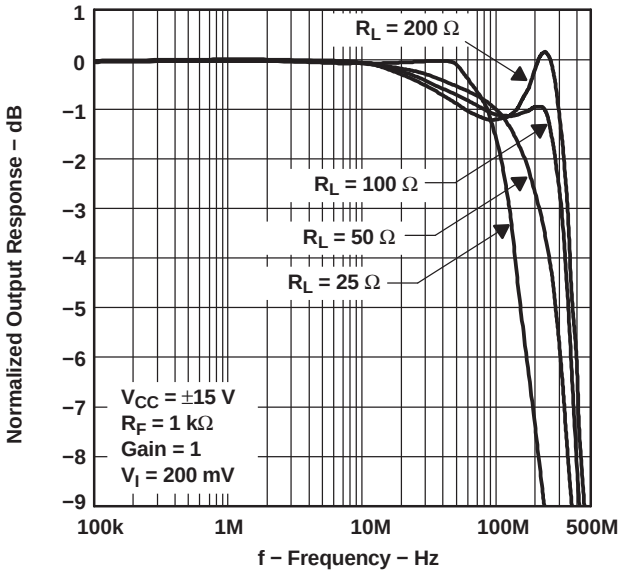

Figure 22.

NORMALILZED OUTPUT RESPONSE vs FREQUENCY

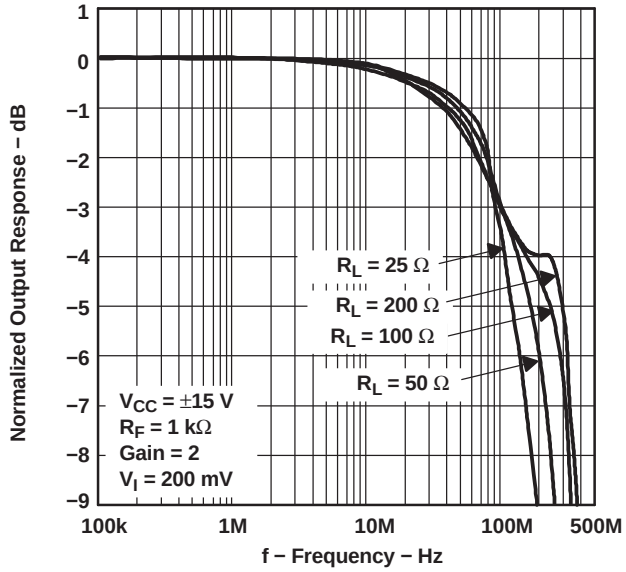

Figure 23.

NORMALIZFED OUTPUT RESPONSE vs FREQUENCY

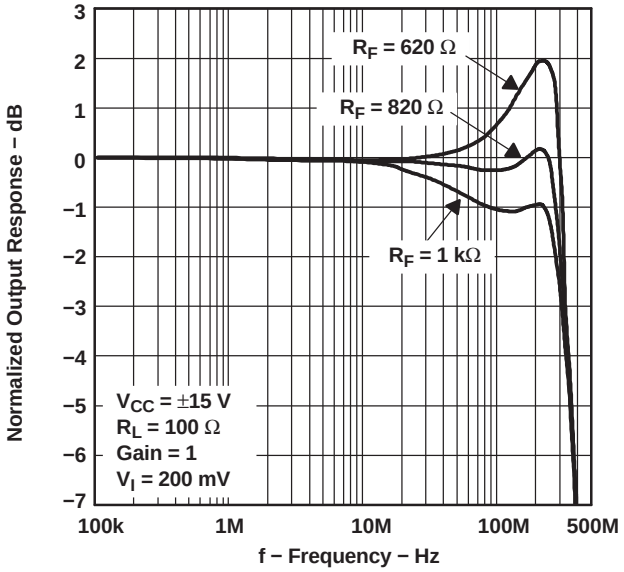

Figure 24.

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NORMALIZED OUTPUT RESPONSE vs FREQUENCY

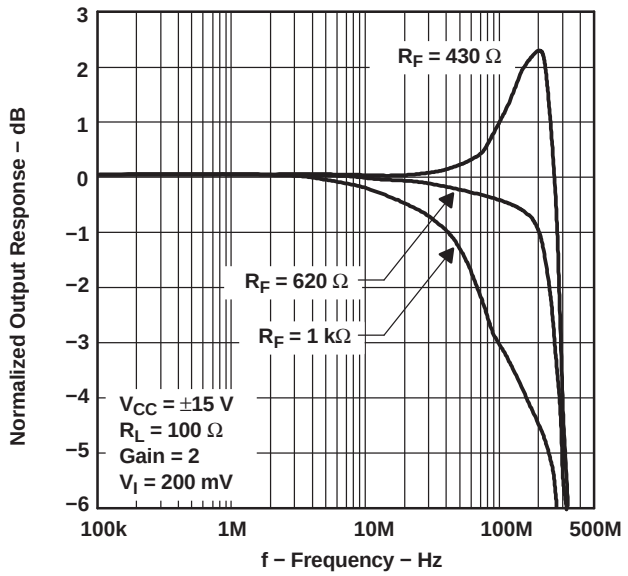

Figure 25.

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

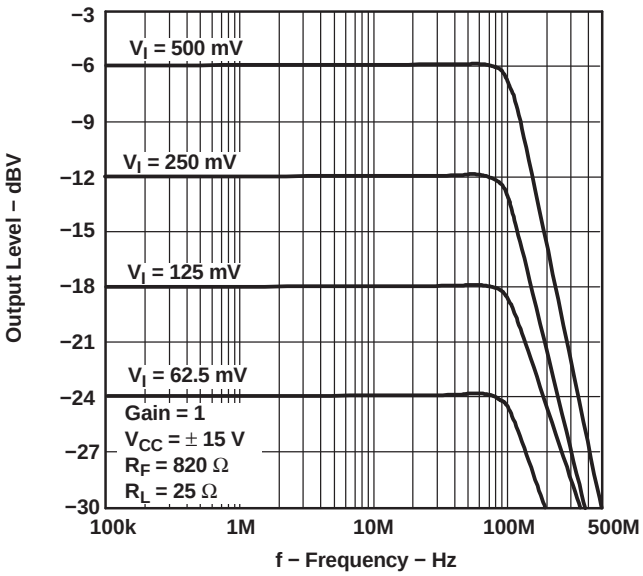

Figure 26.

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

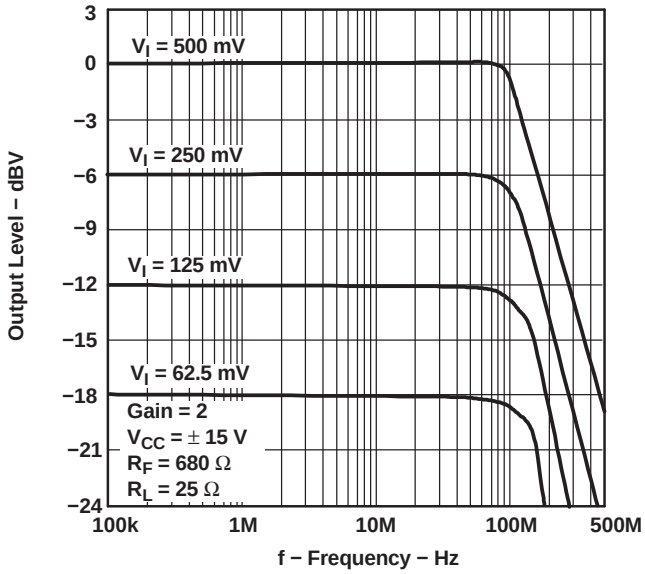

Figure 27.

SINGLE-ENDED HARMONIC DISTORTION vs FREQUENCY

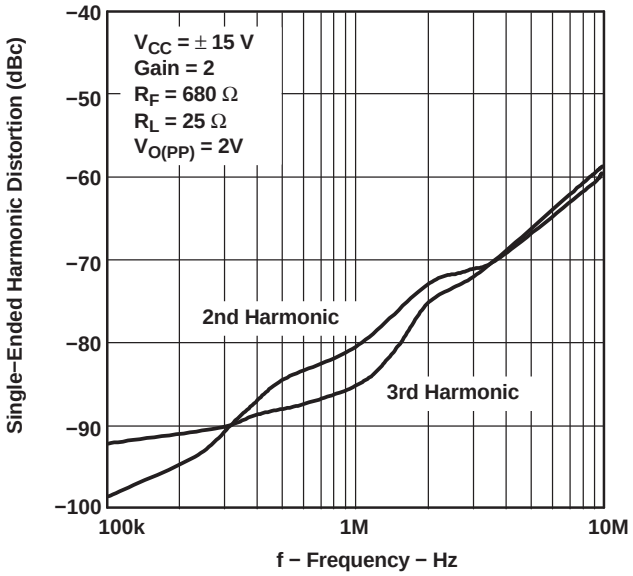

Figure 28.

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SINGLE-ENDED HARMONIC DISTORTION vs FREQUENCY

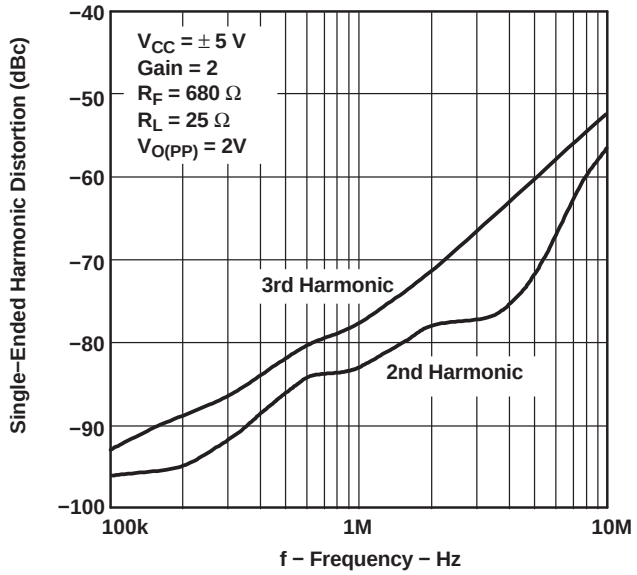

Figure 29.

SINGLE-ENDED HARMONIC DISTORTION vs OUTPUT VOLTAGE

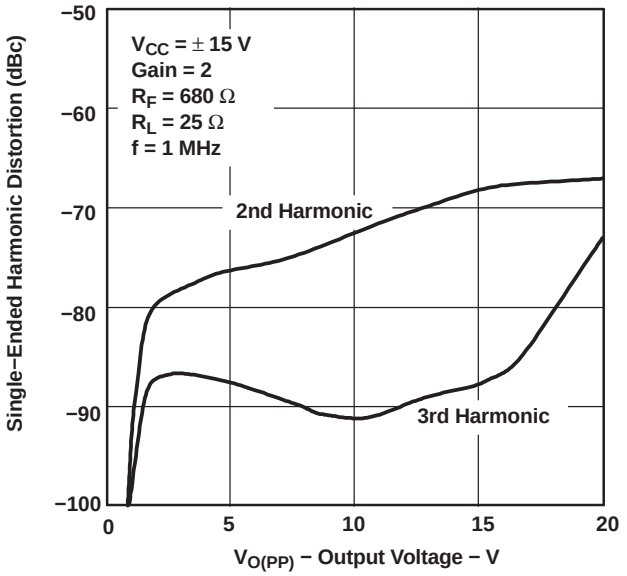

Figure 30.

SINGLE-ENDED HARMONIC DISTORTION vs OUTPUT VOLTAGE

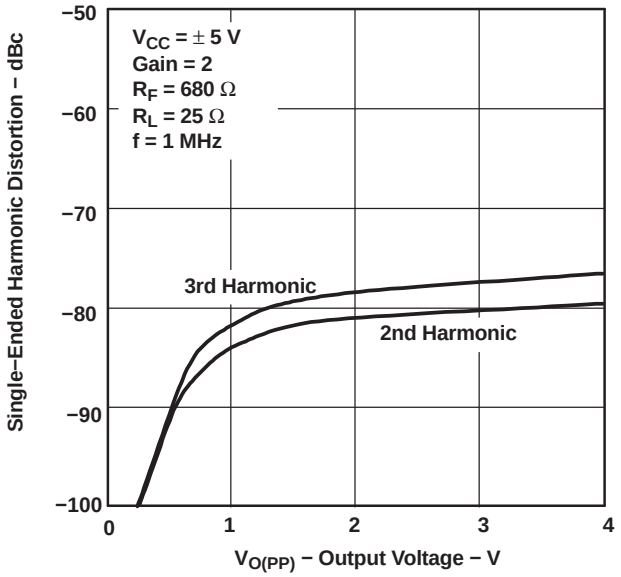

Figure 31.

DIFFERENTIAL GAIN AND PHASE vs DC INPUT OFFSET VOLTAGE

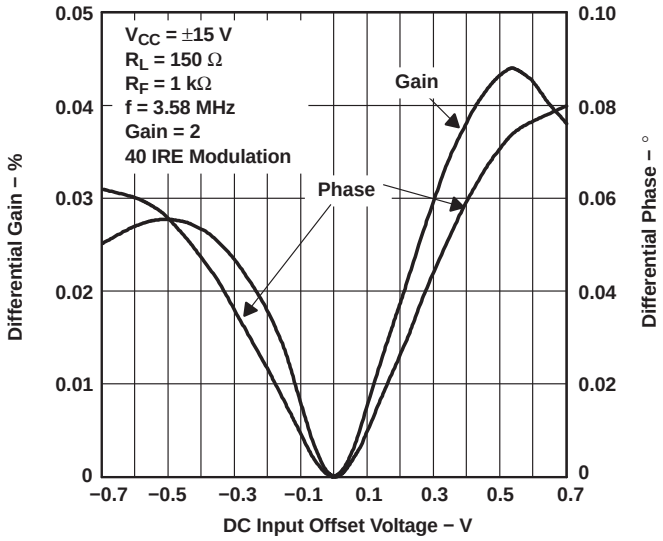

Figure 32.

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DIFFERENTIAL GAIN AND PHASE vs DC INPUT OFFSET VOLTAGE

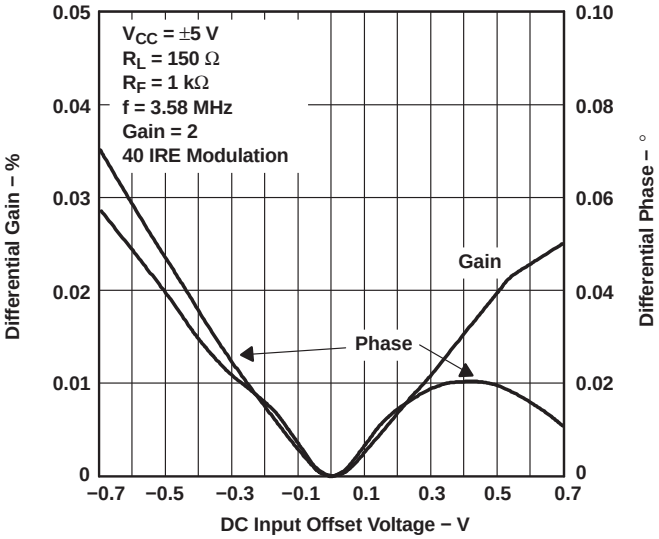

Figure 33.

DIFFERENTIAL GAIN AND PHASE vs NUMBER OF 150-Ω LOADS

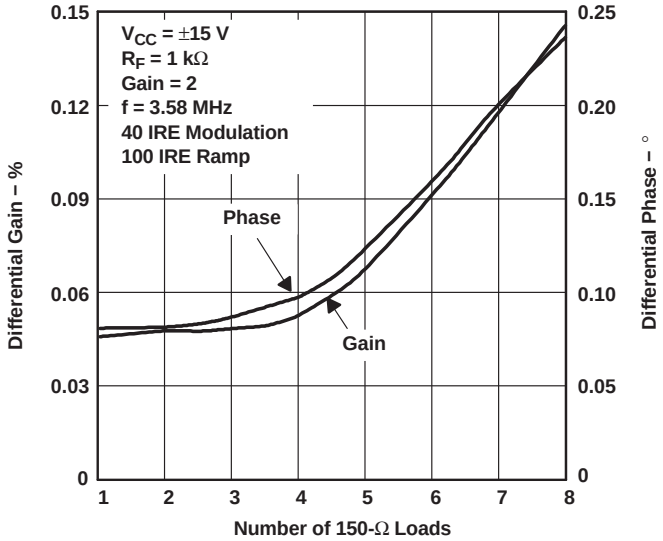

Figure 34.

DIFFERENTIAL GAIN AND PHASE vs NUMBER OF 150-Ω LOADS

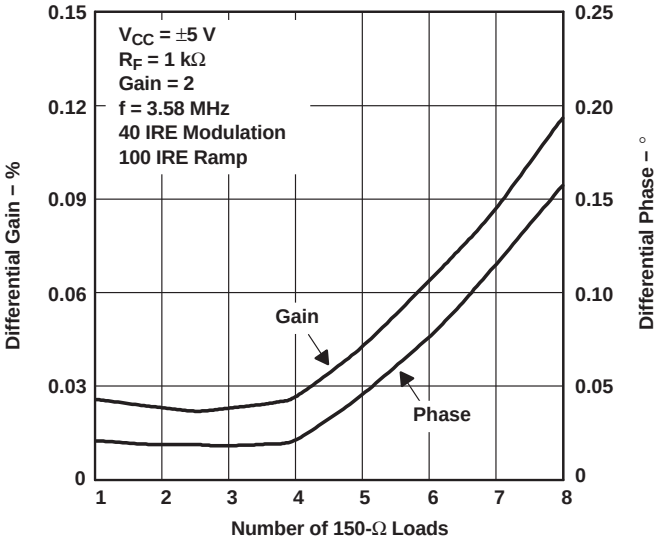

Figure 35.

400-mV STEP RESPONSE

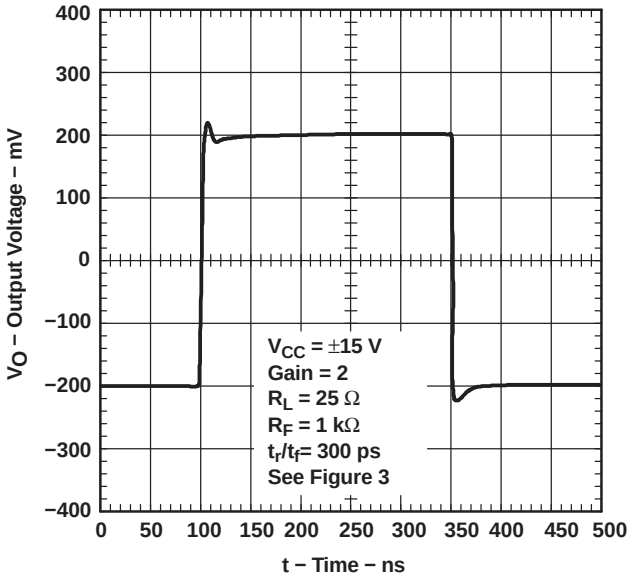

Figure 36.

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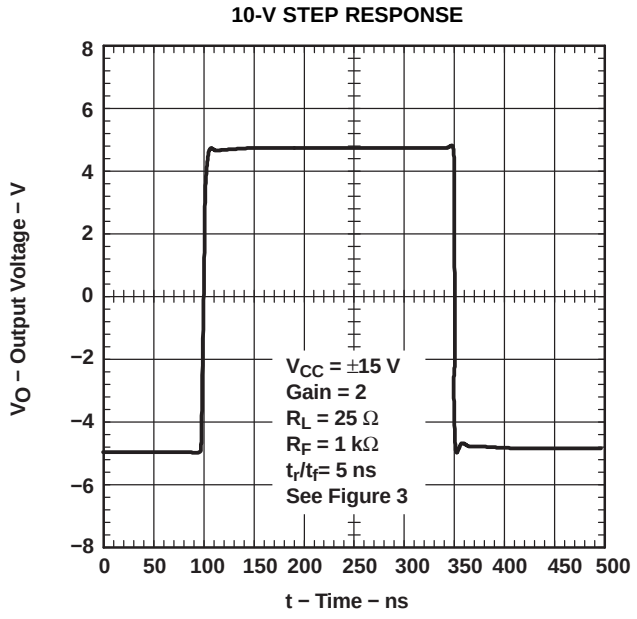

Figure 37.

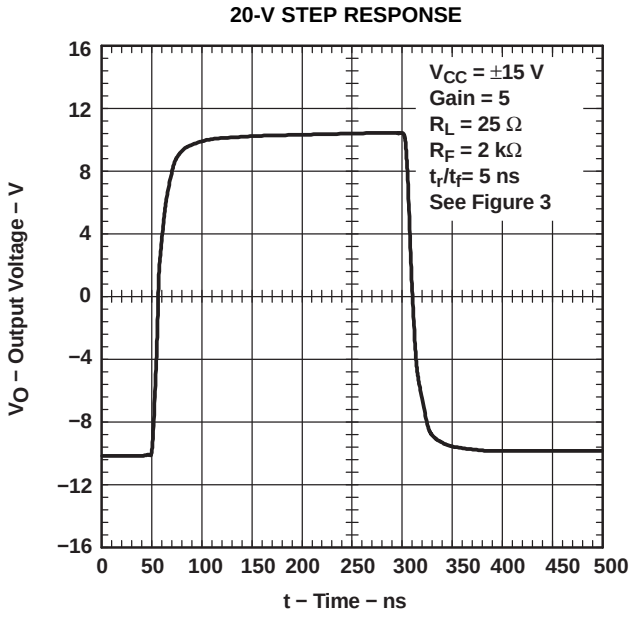

Figure 38.

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APPLICATION INFORMATION

The THS6012 contains two independent operational amplifiers. These amplifiers are current feedback topology amplifiers made for high-speed operation. They have been specifically designed to deliver the full power requirements of ADSL and therefore can deliver output currents of at least 400 mA at full output voltage.

The THS6012 is fabricated using Texas Instruments 30-V complementary bipolar process, HVBiCOM. This process provides excellent isolation and high slew rates that result in the device's excellent crosstalk and extremely low distortion.

INDEPENDENT POWER SUPPLIES

Each amplifier of the THS6012 has its own power supply pins. This was specifically done to solve a problem that often occurs when multiple devices in the same package share common power pins. This problem is crosstalk between the individual devices caused by currents flowing in common connections. Whenever the current required by one device flows through a common connection shared with another device, this current, in conjunction with the impedance in the shared line, produces an unwanted voltage on the power supply. Proper power supply decoupling and good device power supply rejection helps to reduce this unwanted signal. What is left is crosstalk.

However, with independent power supply pins for each device, the effects of crosstalk through common impedance in the power supplies is more easily managed. This is because it is much easier to achieve low common impedance on the PCB with copper etch than it is to achieve low impedance within the package with either bond wires or metal traces on silicon.

POWER SUPPLY RESTRICTIONS

Although the THS6012 is specified for operation from power supplies of ±5 V to ±15 V (or singled-ended power supply operation from 10 V to 30 V), and each amplifier has its own power supply pins, several precautions must be taken to assure proper operation.

1. The power supplies for each amplifier must be the same value. For example, if the driver 1 uses ±±15 volts, then the driver 2 must also use ±15 volts. Using ±15 volts for one amplifier and ±5 volts for another amplifier is not allowed.
2. To save power by powering down one of the amplifiers in the package, the following rules must be followed.
   - The amplifier designated driver 1 must always receive power. This is because the internal startup circuitry uses the power from the driver 1 device.
   - The $-V_{CC}$ pins from both drivers must always be at the same potential.
   - Driver 2 is powered down by simply opening the $+V_{CC}$ connection.

The THS6012 incorporates a standard Class A-B output stage. This means that some of the quiescent current is directed to the load as the load current increases. So under heavy load conditions, accurate power dissipation calculations are best achieved through actual measurements. For small loads, however, internal power dissipation for each amplifier in the THS6012 can be approximated by the following formula:

$$P_D \cong \left(2\,V_{CC}\,I_{CC}\right) + \left(V_{CC} - V_O\right) \times \left(\frac{V_O}{R_L}\right)$$

Where:

P_D = Power dissipation for one amplifier
V_{CC} = Split supply voltage
I_{CC} = Supply current for that particular amplifier
V_O = Output voltage of amplifier
R_L = Load resistance

To find the total THS6012 power dissipation, we simply sum up both amplifier power dissipation results. Generally, the worst case power dissipation occurs when the output voltage is one-half the V_{CC} voltage. One last note, which is often overlooked: the feedback resistor (R_F) is also a load to the output of the amplifier and should be taken into account for low value feedback resistors.

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DEVICE PROTECTION FEATURES

The THS6012 has two built-in protection features that protect the device against improper operation. The first protection mechanism is output current limiting. Should the output become shorted to ground the output current is automatically limited to the value given in the data sheet. While this protects the output against excessive current, the device internal power dissipation increases due to the high current and large voltage drop across the output transistors. Continuous output shorts are not recommended and could damage the device. Additionally, connection of the amplifier output to one of the supply rails ($\pm V_{CC}$) can cause failure of the device and is not recommended.

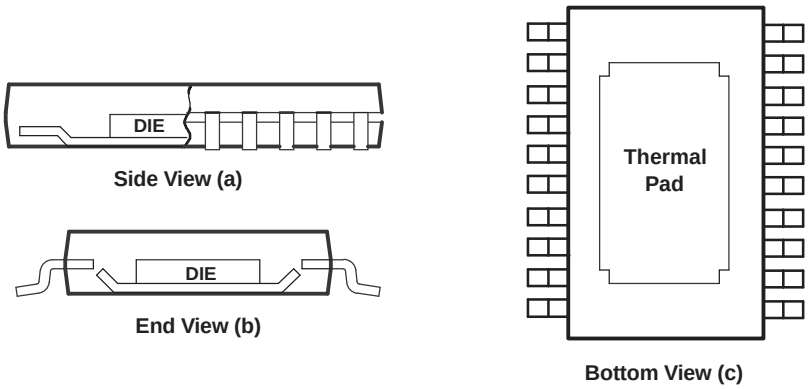
The second built-in protection feature is thermal shutdown. Should the internal junction temperature rise above approximately 180°C, the device automatically shuts down. Such a condition could exist with improper heat sinking or if the output is shorted to ground. When the abnormal condition is fixed, the internal thermal shutdown circuit automatically turns the device back on.

THERMAL INFORMATION

The THS6012 is packaged in a thermally-enhanced DWP package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 39(a) and Figure 39(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 39(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. This is discussed in more detail in the *PCB design considerations* section of this document.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.



A. The thermal pad is electrically isolated from all terminals in the package.

Figure 39. Views of Thermally Enhanced DWP Package

RECOMMENDED FEEDBACK AND GAIN RESISTOR VALUES

As with all current feedback amplifiers, the bandwidth of the THS6012 is an inversely proportional function of the value of the feedback resistor. This can be seen from Figure 17 through Figure 20. The recommended resistors with a ±15 V power supply for the optimum frequency response with a 25-Ω load system are 680-Ω for a gain = 1 and 620-Ω for a gain = 2 or -1. Additionally, using a ±5 V power supply, it is recommended that a 1-kΩ feedback resistor be used for a gain of 1 and a 820-Ω feedback resistor be used for a gain of 2 or -1. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics. Because there is a finite amount of output resistance of the operational amplifier, load resistance can play a major part in frequency response. This is especially true with these drivers, which tend to drive low-impedance loads. This can be seen in Figure 11, Figure 23, and Figure 24. As the load

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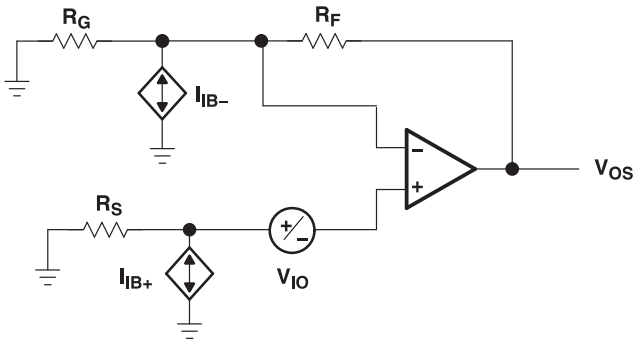
resistance increases, the output resistance of the amplifier becomes less dominant at high frequencies. To compensate for this, the feedback resistor should change. For 100-Ω loads, it is recommended that the feedback resistor be changed to 820 Ω for a gain of 1 and 560 Ω for a gain of 2 or -1. Although, for most applications, a feedback resistor value of 1 kΩ is recommended, which is a good compromise between bandwidth and phase margin that yields a very stable amplifier.

Consistent with current feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and internal dominant-pole capacitor. The ability to control the amplifier gain independently of the bandwidth constitutes a major advantage of current feedback amplifiers over conventional voltage feedback amplifiers. Therefore, once a frequency response is found suitable to a particular application, adjust the value of the gain resistor to increase or decrease the overall amplifier gain.

Finally, it is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third order harmonic distortion increases more than the second order harmonic distortion.

OFFSET VOLTAGE

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OS} = \left(\pm V_{IO} \pm I_{IB+} R_S\right)\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-} R_F$$

Figure 40. Output Offset Voltage Model

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NOISE CALCULATIONS AND NOISE FIGURE

Noise can cause errors on very small signals. This is especially true for the amplifying small signals. The noise model for current feedback amplifiers (CFB) is the same as voltage feedback amplifiers (VFB). The only difference between the two is that the CFB amplifiers generally specify different current noise parameters for each input while VFB amplifiers usually only specify one noise current parameter. The noise model is shown in Figure 41. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = Noninverting current noise (pA/$\sqrt{Hz}$)
- IN- = Inverting current noise (pA/$\sqrt{Hz}$)
- e_{RX} = Thermal voltage noise associated with each resistor (e_{RX} = 4 kTR_x)

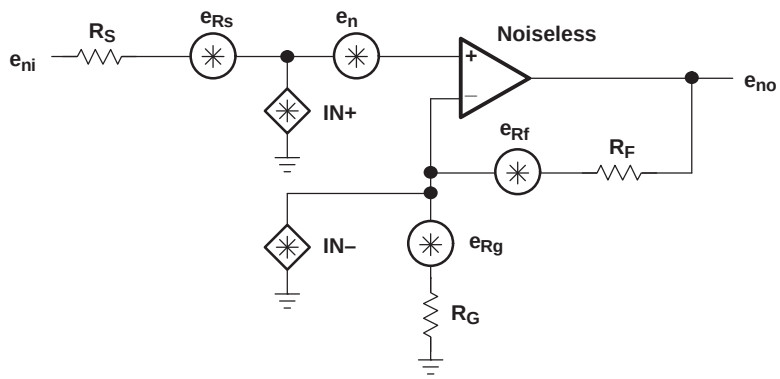

Figure 41. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\,kTR_S + 4\,kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni} A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

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$$NF = 10\log\left[\frac{e_{ni}^{2}}{\left(e_{Rs}\right)^{2}}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\,kTR_S}\right]$$

Figure 42 shows the noise figure graph for the THS6012.

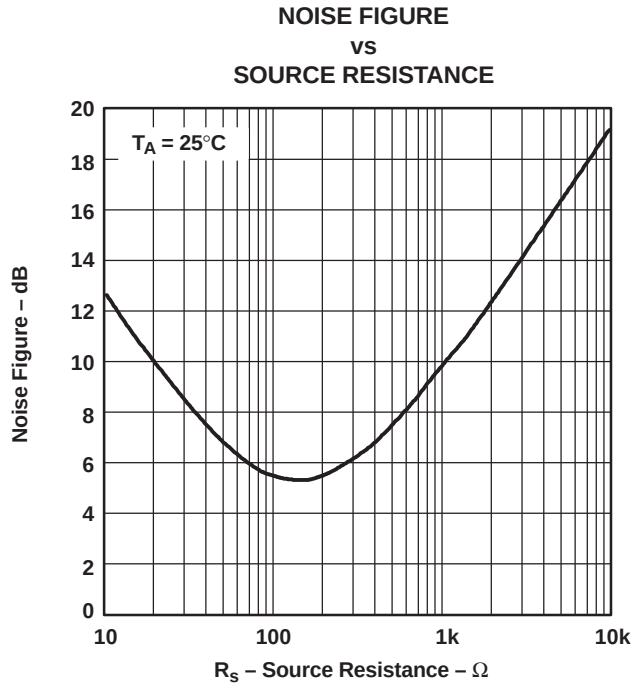

Figure 42. Noise Figure vs Source Resistance

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DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS6012 has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 43. A minimum value of 10 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

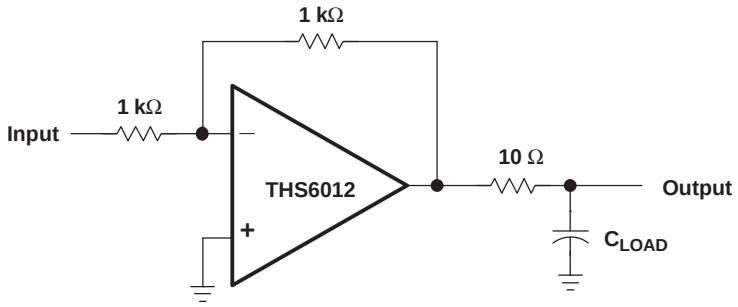

Figure 43. Driving a Capacitive Load

PCB DESIGN CONSIDERATIONS

Proper PCB design techniques in two areas are important to assure proper operation of the THS6012. These areas are high-speed layout techniques and thermal-management techniques. Because the THS6012 is a high-speed part, the following guidelines are recommended.

- Ground plane - It is essential that a ground plane be used on the board to provide all components with a low inductive ground connection. Although a ground connection directly to a terminal of the THS6012 is not necessarily required, it is recommended that the thermal pad of the package be tied to ground. This serves two functions. It provides a low inductive ground to the device substrate to minimize internal crosstalk and it provides the path for heat removal.
- Input stray capacitance - To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane must be removed under any etch runs connected to the inverting input, and external components should be placed as close as possible to the inverting input. This is especially true in the noninverting configuration. An example of this can be seen in Figure 44, which shows what happens when 1.8 pF is added to the inverting input terminal in the noninverting configuration. The bandwidth increases dramatically at the expense of peaking. This is because some of the error current is flowing through the stray capacitor instead of the inverting node of the amplifier. Although, in the inverting mode, stray capacitance at the inverting input has little effect. This is because the inverting node is at a *virtual ground* and the voltage does not fluctuate nearly as much as in the noninverting configuration.

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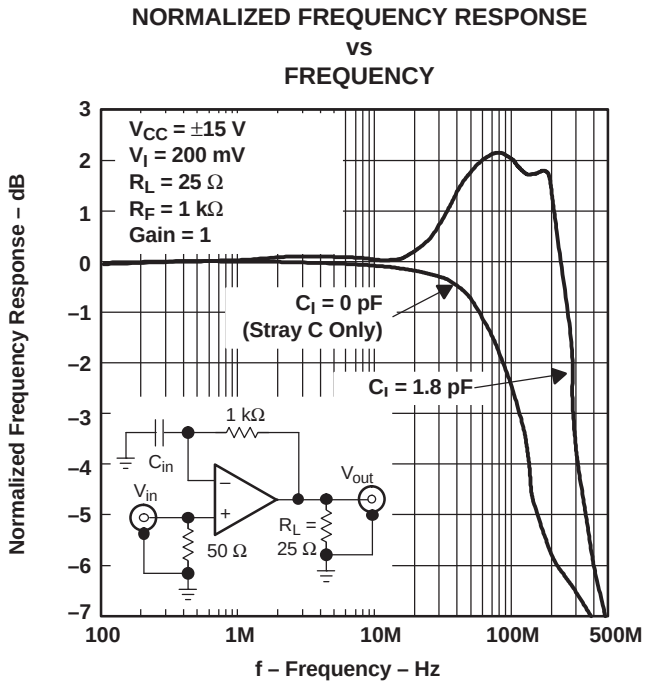

Figure 44. Driver Normalized Frequency Response vs Frequency

- Proper power supply decoupling - Use a minimum of a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminal and the ceramic capacitors.

Because of its power dissipation, proper thermal management of the THS6012 is required. Although there are many ways to properly heatsink this device, the following steps illustrate one recommended approach for a multilayer PCB with an internal ground plane.

1. Prepare the PCB with a top side etch pattern as shown in Figure 45. There should be etch for the leads as well as etch for the thermal pad.
2. Place 18 holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
3. It is recommended, but not required, to place six more holes under the package, but outside the thermal pad area. These holes are 25 mils in diameter. They may be larger because they are not in the area to be soldered so that wicking is not a problem.
4. Connect all 24 holes, the 18 within the thermal pad area and the 6 outside the pad area, to the internal ground plane.
5. When connecting these holes to the ground plane, do **not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6012 package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole.
6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area with its five holes. The four larger holes outside the thermal pad area, but still under the package, should be covered with solder mask.
7. Apply solder paste to the exposed thermal pad area and all of the operational amplifier terminals.
8. With these preparatory steps in place, the THS6012 is simply placed in position and run through the solder

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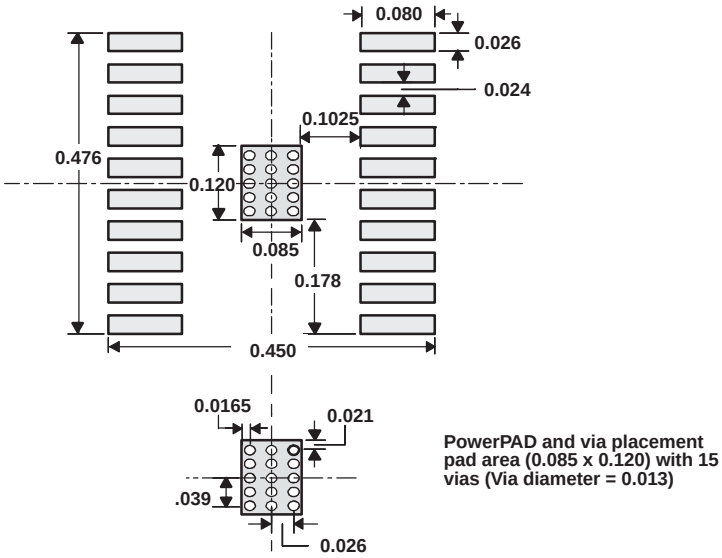
reflow operation as any standard surface-mount component. This results in a part that is properly installed.



Vias should go through the board connecting the top layer PowerPad to any and all ground planes. (The larger the ground plane, the larger the area to distribute the heat.) Solder resist should be used on the bottom side ground plane in order to prevent wicking of the solder through the vias during the reflow process.

All Units in Inches

Figure 45. PowerPAD PCB Etch and Via Pattern

The actual thermal performance achieved with the THS6012 in its PowerPAD package depends on the application. In the previous example, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, Θ_{JA}, is about 21.5°C/W. For a givenΘ_{JA}, the maximum power dissipation is shown in Figure 46 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of THS6012 (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = $\theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case (0.37°C/W)
θ_{CA} = Thermal coefficient from case to ambient

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

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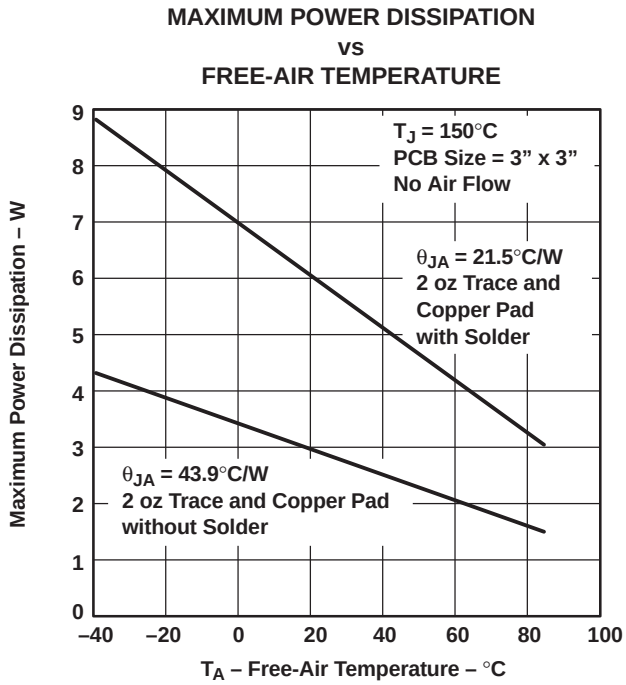

Figure 46. Maximum Power Dissipation vs Free-Air Temperature

ADSL

The THS6012 was primarily designed as a line driver and line receiver for ADSL (asymmetrical digital subscriber line). The driver output stage has been sized to provide full ADSL power levels of 20 dBm onto the telephone lines. Although actual driver output peak voltages and currents vary with each particular ADSL application, the THS6012 is specified for a minimum full output current of 400 mA at its full output voltage of approximately 12 V. This performance meets the demanding needs of ADSL at the central office end of the telephone line. A typical ADSL schematic is shown in Figure 47.

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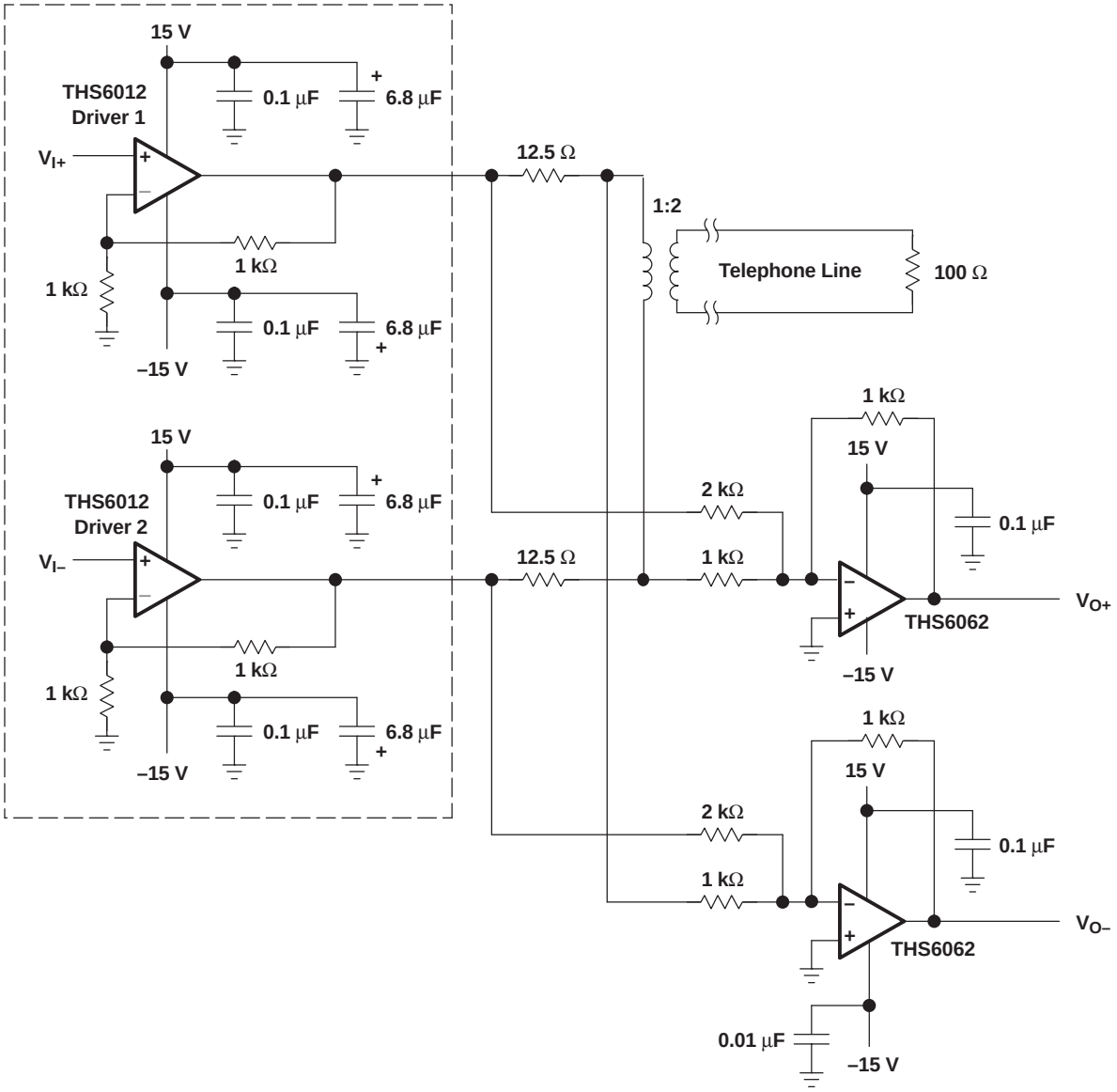

Figure 47. THS6012 ADSL Application

The ADSL transmit band consists of 255 separate carrier frequencies each with its own modulation and amplitude level. With such an implementation, it is imperative that signals put onto the telephone line have as low a distortion as possible. This is because any distortion either interferes directly with other ADSL carrier frequencies or it creates intermodulation products that interfere with ADSL carrier frequencies.

The THS6012 has been specifically designed for ultra low distortion by careful circuit implementation and by taking advantage of the superb characteristics of the complementary bipolar process. Driver single-ended distortion measurements are shown in Figure 28 through Figure 31. It is commonly known that in the differential driver configuration, the second order harmonics tend to cancel out. Thus, the dominant total harmonic distortion (THD) will be primarily due to the third order harmonics. For these tests the load was 25 Ω. Additionally, distortion should be reduced as the feedback resistance drops. This is because the bandwidth of the amplifier increases, which allows the amplifier to react faster to any nonlinearities in the closed-loop system.

Another significant point is the fact that distortion decreases as the impedance load increases. This is because the output resistance of the amplifier becomes less significant as compared to the output load resistance.

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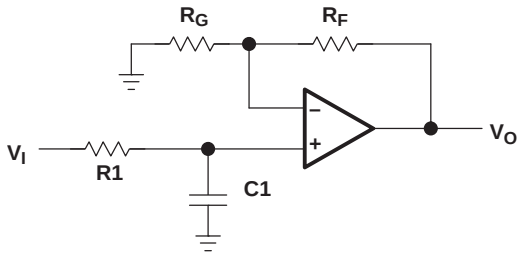
GENERAL CONFIGURATIONS

A common error for the first-time CFB user is to create a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration oscillates and is **not** recommended. The THS6012, like all CFB amplifiers, **must** have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 48).

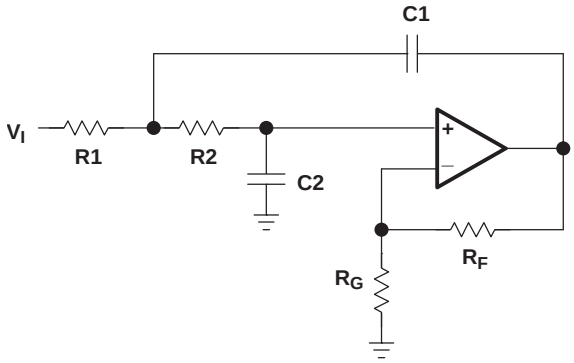


$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

Figure 48. Single-Pole Low-Pass Filter

If a multiple pole filter is required, the use of a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. An example is shown in Figure 49.



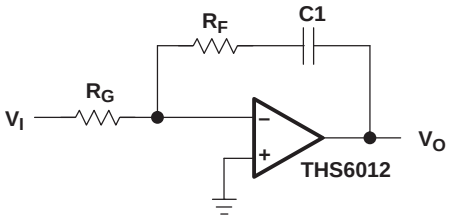
R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 49. 2-Pole Low-Pass Sallen-Key Filter

There are two simple ways to create an integrator with a CFB amplifier. The first one shown in Figure 50 adds a resistor in series with the capacitor. This is acceptable because at high frequencies, the resistor is dominant and the feedback impedance never drops below the resistor value. The second one shown in Figure 51 uses positive feedback to create the integration. Caution is advised because oscillations can occur because of the positive feedback.



$$\frac{V_O}{V_I} = \left(\frac{R_F}{R_G}\right)\left[\frac{S + \frac{1}{R_F C1}}{S}\right]$$

Figure 50. Inverting CFB Integrator

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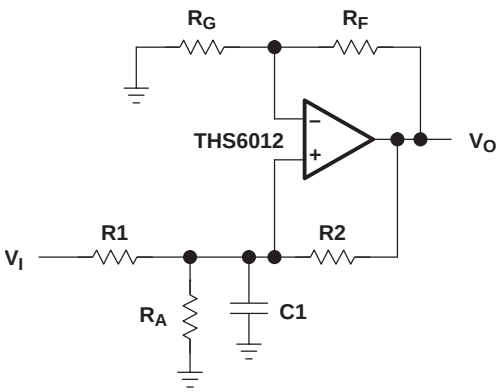

For Stable Operation:

$$\frac{R2}{R1 \parallel R_A} \geq \frac{R_F}{R_G}$$

$$V_O \cong V_I \left(\frac{1 + \frac{R_F}{R_G}}{sR1C1} \right)$$

Figure 51. Non-Inverting CFB Integrator

Another good use for the THS6012 amplifiers is as very good video distribution amplifiers. One characteristic of distribution amplifiers is the fact that the differential phase (DP) and the differential gain (DG) are compromised as the number of lines increases and the closed-loop gain increases. Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

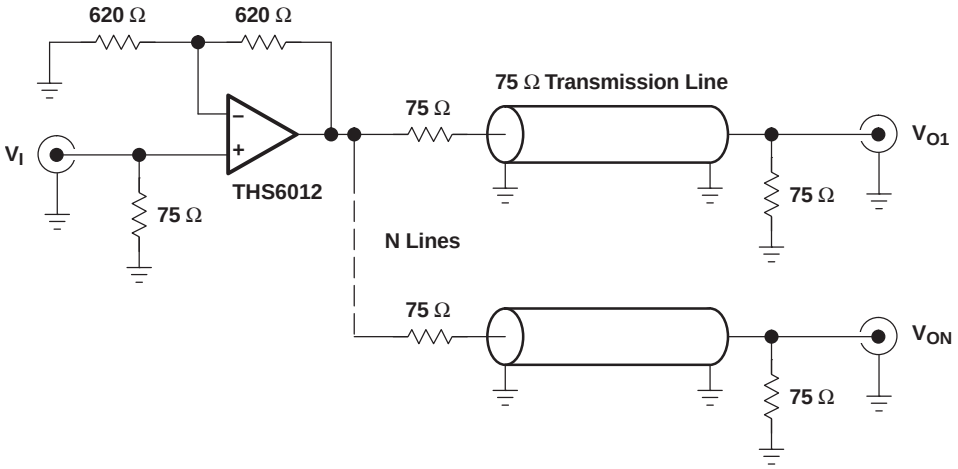

Figure 52. Video Distribution Amplifier Application

EVALUATION BOARD

An evaluation board is available for the THS6012 (literature number SLOP132). This board has been configured for proper thermal management of the THS6012. The circuitry has been designed for a typical ADSL application as shown previously in this document. For more detailed information, refer to the *THS6012EVM User's Manual* (literature number SLOU034). To order the evaluation board contact your local TI sales office or distributor.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS6012CDWP	ACTIVE	SO PowerPAD	DWP	20	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	THS6012C	Samples
THS6012CDWPR	ACTIVE	SO PowerPAD	DWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	THS6012C	Samples
THS6012IDWP	ACTIVE	SO PowerPAD	DWP	20	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS6012I	Samples
THS6012IDWPR	ACTIVE	SO PowerPAD	DWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS6012I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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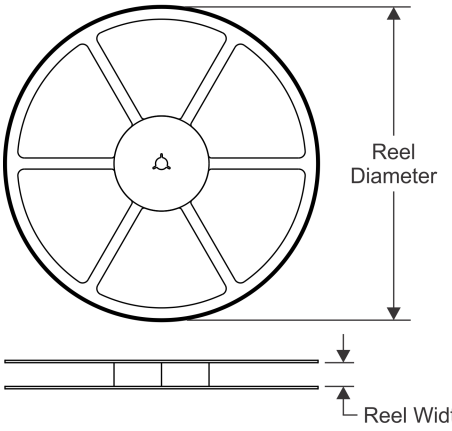
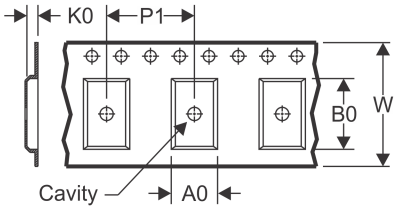
TAPE AND REEL INFORMATION

REEL DIMENSIONS

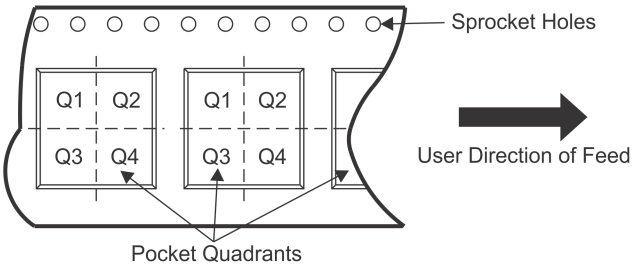


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

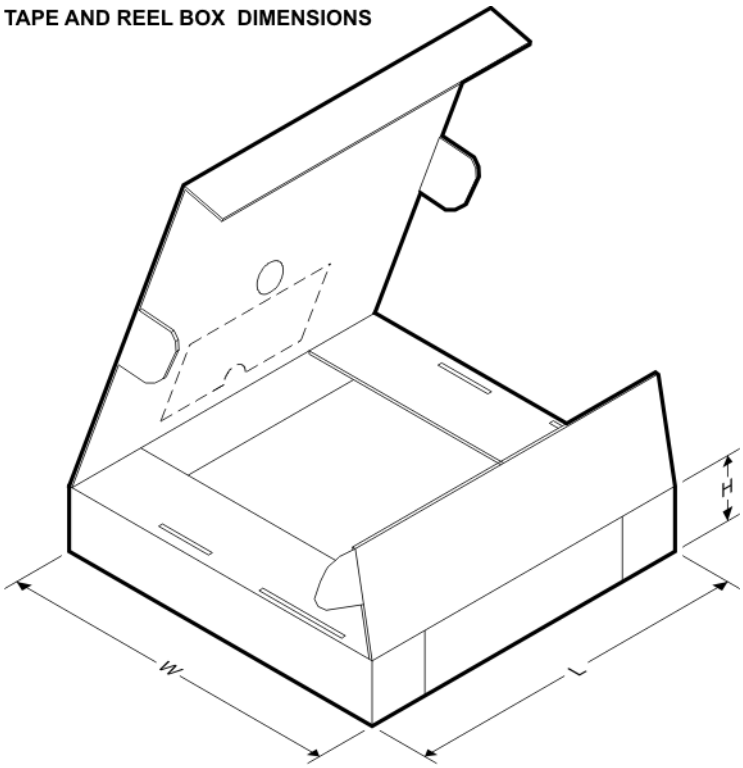
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6012CDWPR	SO Power PAD	DWP	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
THS6012IDWPR	SO Power PAD	DWP	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

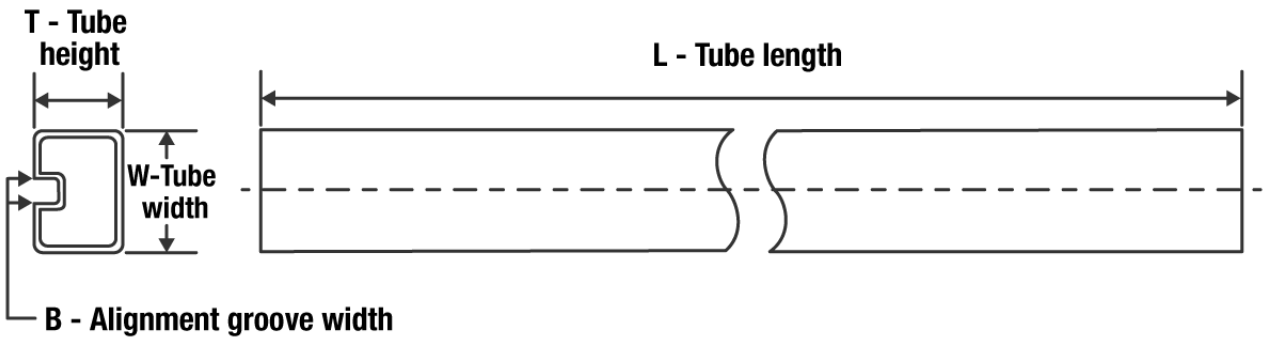
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6012CDWPR	SO PowerPAD	DWP	20	2000	350.0	350.0	43.0
THS6012IDWPR	SO PowerPAD	DWP	20	2000	350.0	350.0	43.0

TUBE

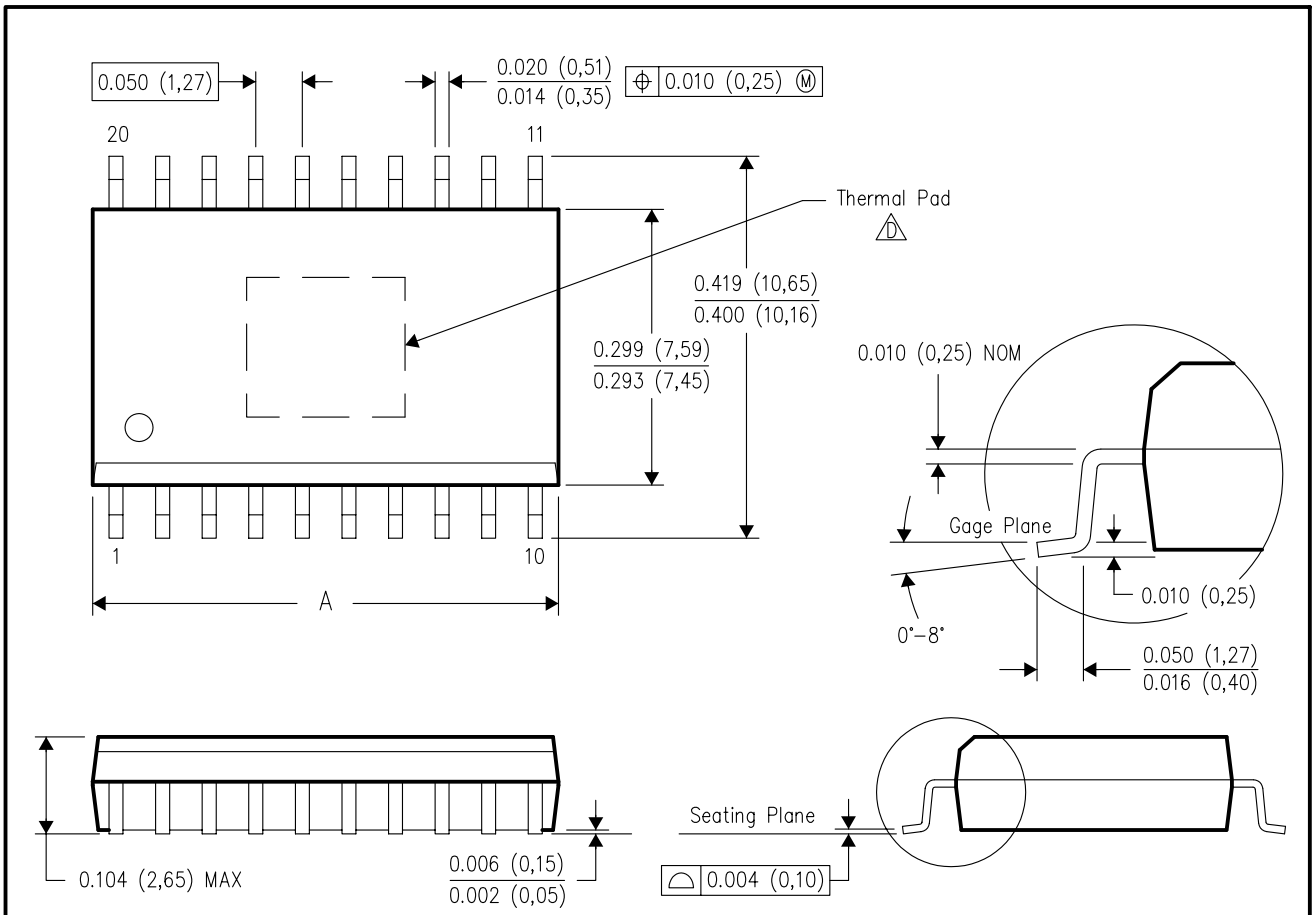


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS6012CDWP	DWP	HSOIC	20	25	506.98	12.7	4826	6.6
THS6012IDWP	DWP	HSOIC	20	25	506.98	12.7	4826	6.6

DWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4147575/C 02/05

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

PowerPAD is a trademark of Texas Instruments.

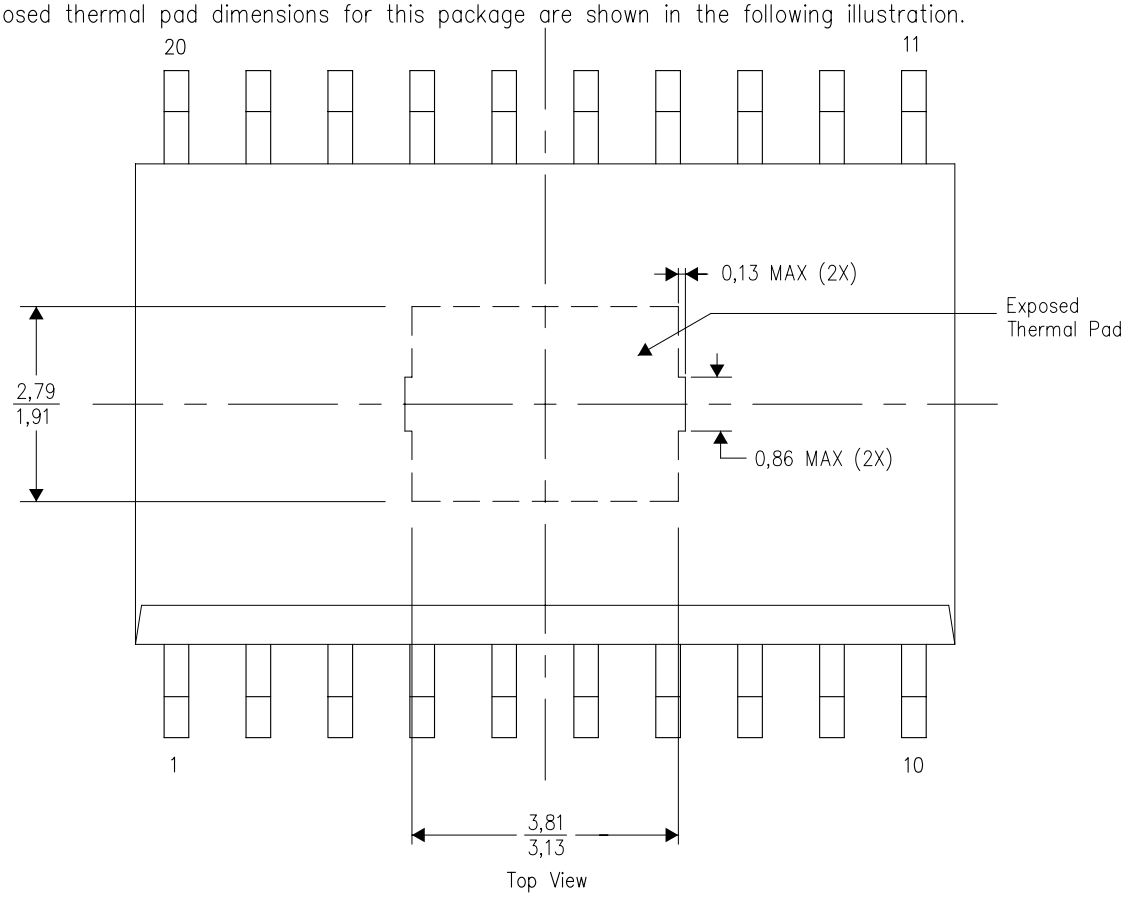
DWP (R-PDSO-G20) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

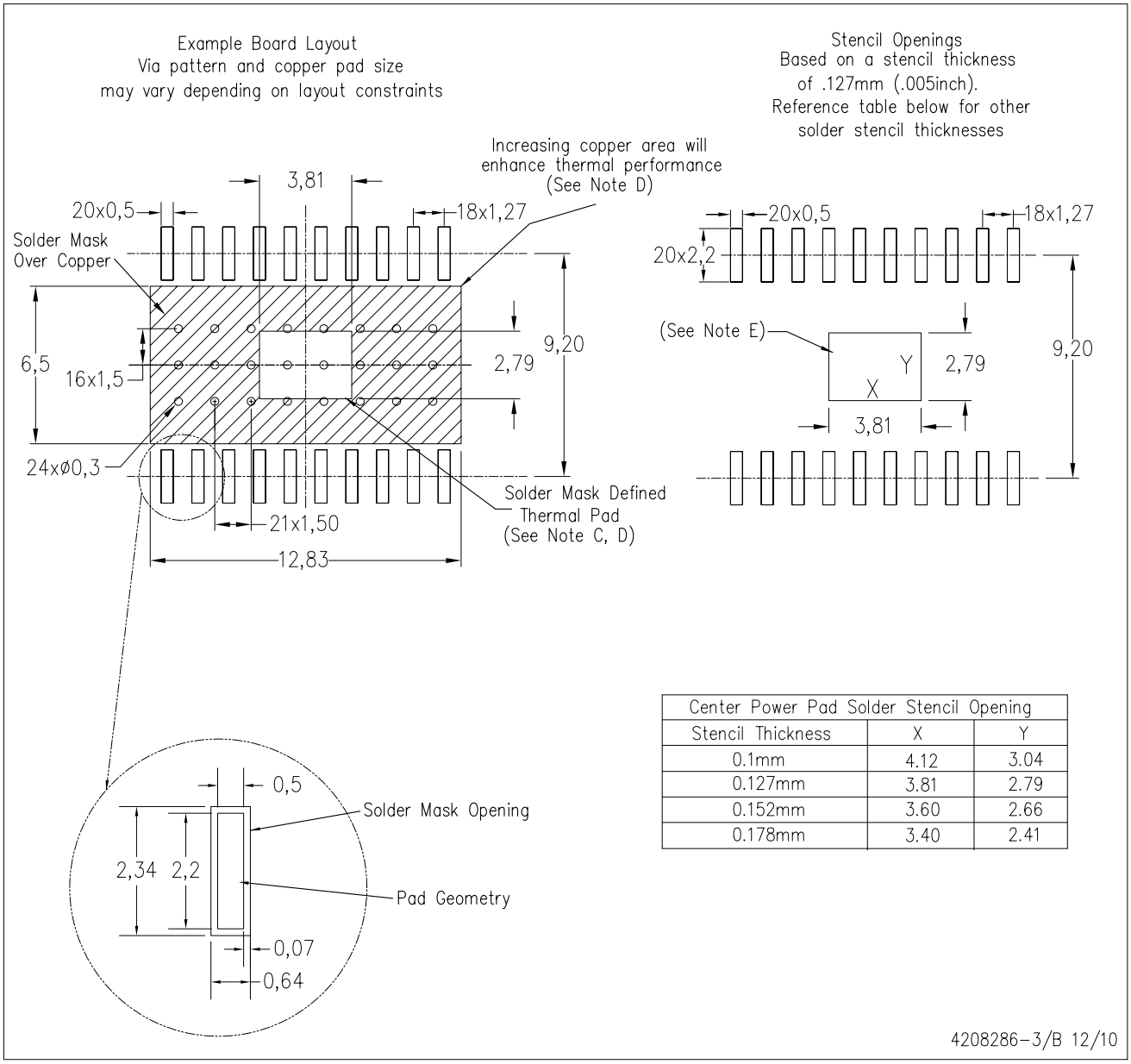


Exposed Thermal Pad Dimensions

4206325-4/E 12/10

NOTE: A. All linear dimensions are in millimeters

DWP (R-PDSO-G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.12	3.04
0.127mm	3.81	2.79
0.152mm	3.60	2.66
0.178mm	3.40	2.41

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste.

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