TLC59212 8-Bit Open-Collector Sink Driver with Latch

1 Features

- LBC3S (Lin BiCMOS) Process
- High Voltage Output (V_{OUT} = 24 V)
- Output Current (I_{OL} Maximum = 40 mA)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged Device Model (C101)

2 Applications

- Lamps and Displays (LED)
- Hammers
- Relay

3 Description

The TLC59212 device is an 8-bit open-collector driver with latch designed for 5-V V_{CC} operation.

These circuits are positive-edge-triggered D-type flip-flops with a direct clear ($\overline{CLR}$) input. Information at the data (D) input meeting the setup time requirements is transferred to the $\overline{Y}$ output on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D-input has no effect at the output.

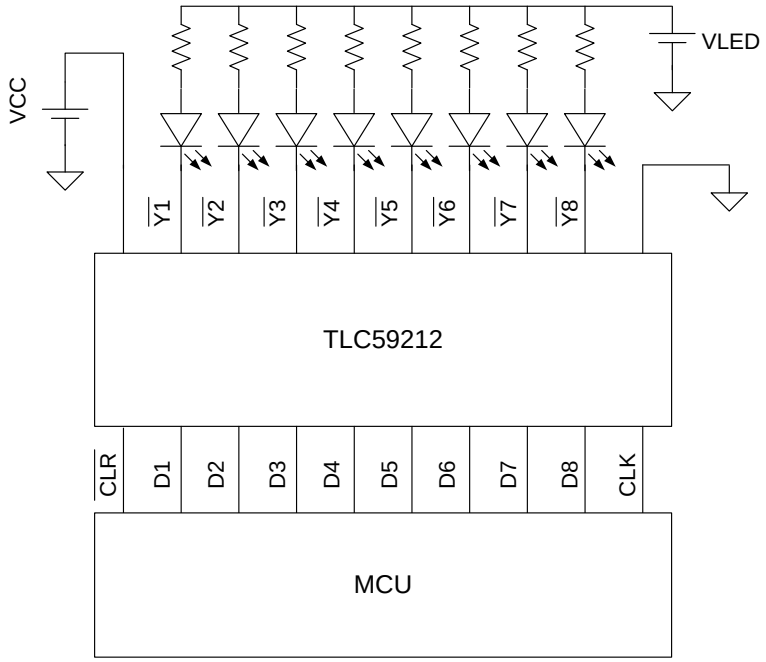
The TLC59212 is characterized for operation from –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC59212	PDIP (20)	24.33 mm × 6.35 mm
	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2009) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

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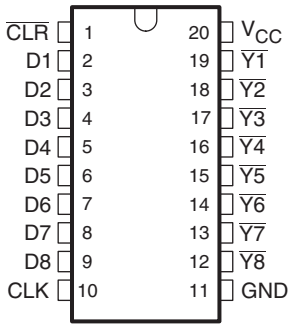
5 Pin Configuration and Functions

N or PW Package
20-Pin PDIP or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{CLR}$	1	I	Direct clear of output
D1	2	I	Input control to the current sink driver
D2	3	I	Input control to the current sink driver
D3	4	I	Input control to the current sink driver
D4	5	I	Input control to the current sink driver
D5	6	I	Input control to the current sink driver
D6	7	I	Input control to the current sink driver
D7	8	I	Input control to the current sink driver
D8	9	I	Input control to the current sink driver
CLK	10	I	Clock to positive edge triggered D flipflops
GND	11	—	Ground
$\overline{Y8}$	12	O	Output to load
$\overline{Y7}$	13	O	Output to load
$\overline{Y6}$	14	O	Output to load
$\overline{Y5}$	15	O	Output to load
$\overline{Y4}$	16	O	Output to load
$\overline{Y3}$	17	O	Output to load
$\overline{Y2}$	18	O	Output to load
$\overline{Y1}$	19	O	Output to load
V_{cc}	20	I	Supply voltage

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
D	Input voltage	D, CLK, $\overline{CLR}$	–0.5	7	V
V_O	Output voltage	H output	–0.5	30	V
I_O	Output current	1 bit for output low		40	mA
I_{IK}	Input clamp current	$V_I < 0$ V		–20	mA
T_A	Operating free-air temperature		–40	85	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

V_{CC} = 4.5 V to 5.5 V. Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} \times 0.7$	V_{CC}	V
V_{IL}	Low-level input voltage	0	$V_{CC} \times 0.3$	V
V_O	Output voltage	0	24	V
I_O	Output current, Duty cycle < 100%	0	40	mA
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		TLC59212		UNIT
		N (PDIP)	PW (TSSOP)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.8	96.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.4	29.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.8	47.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.3	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.6	46.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{t+}	Positive-going input threshold	D, $\overline{CLR}$, CLK				3.5	V
V_{t-}	Negative-going input threshold	D, $\overline{CLR}$, CLK		1.5			V
V_t	Hysteresis	D, $\overline{CLR}$, CLK		0.5		2	V
$V_{O(off)}$	Output tr sustain voltage	I_{ce} = 1 mA		24			V
I_{OZ}	Output tr leakage current	V_O = 24 V			0	5	μA
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = 5.5 V			0	1	μA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0 V			0	–1	μA
I_{off}	Leakage current	V_I = 0 to 5 V, V_O = 0 to 30 V, V_{CC} = 0			0	5	μA
I_{CC}	Supply current	V_I = 0 to 5 V, V_O = 0 to 30 V, V_{CC} = 0	Output = all OFF		0	5	μA
			Output = all ON		8	20	
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, I_O = 40 mA			0.32	0.55	V
r_{ON}	ON-state resistance	V_{CC} = 4.5 V, I_O = 10 mA			8	13	Ω
C_i	Input capacitance	V_I = V_{CC} or GND			5		pF

6.6 Timing Requirements

over T_A = –40°C to 85°C, V_{CC} = 4.5 V to 5.5 V, O/C to Y (unless otherwise noted)

				MIN	MAX	UNIT
t_{su}	Setup time	CLK	V_{DD} = 4.5 V to 5.5 V	5		ns
t_h	Hold time	CLK	V_{DD} = 4.5 V to 5.5 V	15		ns
t_w	Pulse width	CLK, $\overline{CLR}$	V_{DD} = 4.5 V to 5.5 V	20		ns

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted), see Figure 2

PARAMETER	TEST CONDITIONS	LOAD CAPACITANCE	T_A = 25°C			T_A = –40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{TLH}	Output = low to high	C_L = 50 pF, R_L = 500 Ω		60	185		185	ns
t_{THL}	Output = high to low	C_L = 50 pF, R_L = 500 Ω		10	185		185	ns
t_{PLH}	Output = low to high	C_L = 50 pF, R_L = 500 Ω		70	210		250	ns
t_{PHL}	Output = high to low	C_L = 50 pF, R_L = 500 Ω		45	210		250	ns
t_{PHLR}	$\overline{CLR}$-$\overline{Y}$	C_L = 50 pF, R_L = 500 Ω		70	210		250	ns

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6.8 Typical Characteristics

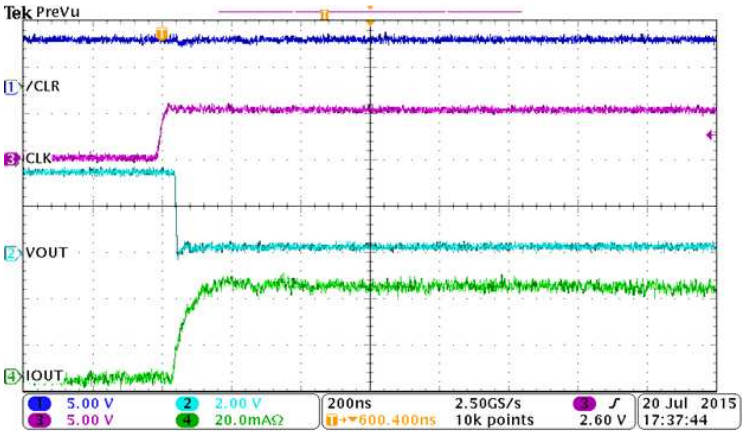

Figure 1. Output Voltage and Current Response

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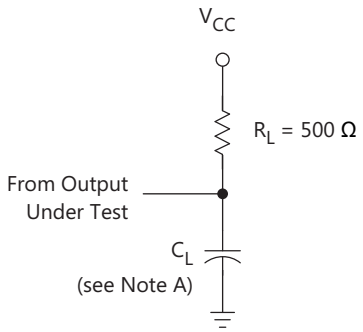
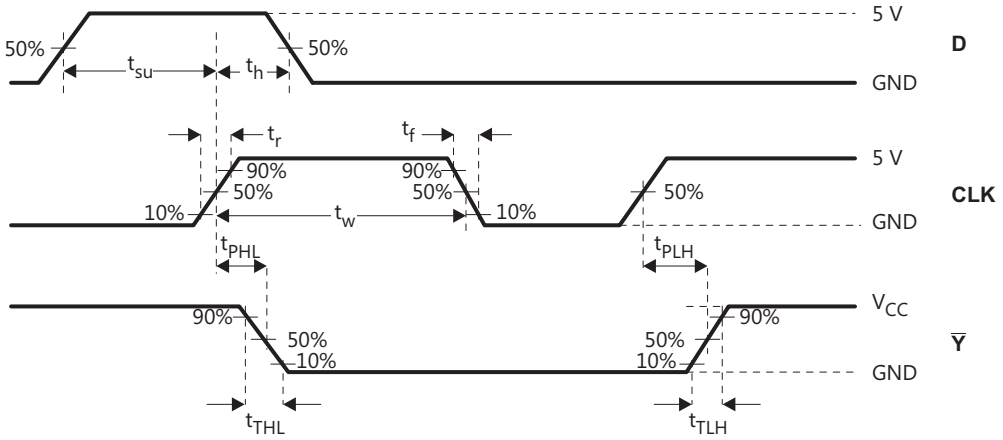
7 Parameter Measurement Information



LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUT



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, and t_f ≤ 3 ns.

C. The outputs are measured one at a time with one transition per measurement.

D. t_{PLH} and t_{PHL} are the same as t_{pd}.

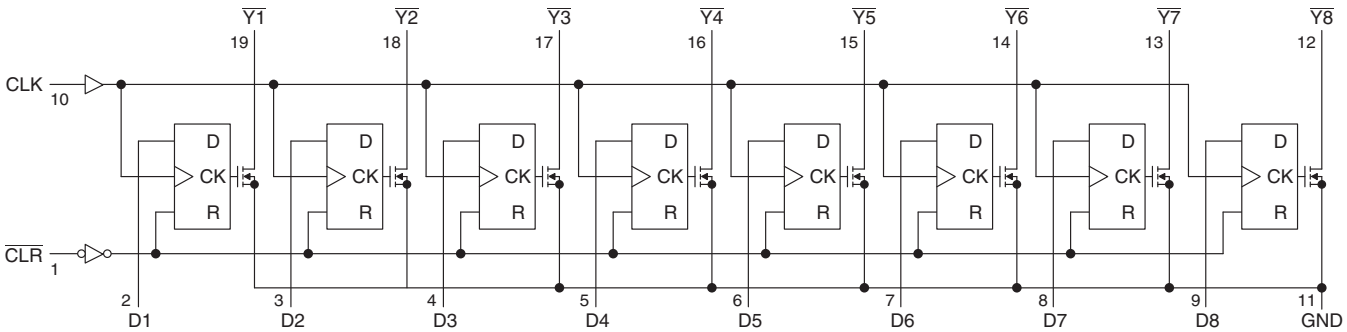
Figure 2. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The TLC59212 device is an 8-bit open-collector driver with latch designed for 5-V V_{CC} operation.

8.2 Functional Block Diagram



(1) This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

Figure 3. Logic Symbol

8.3 Feature Description

Each of the 8 channels is controlled by its input (Dn), a direct clear ($\overline{CLR}$), and clock (CLK) through a positive-edge-triggered D-type flip-flops. Information at the data (D) input meeting the setup time requirements is transferred to the output ($\overline{Y}$) on the positive-going edge of the clock (CLK) pulse. When CLK is at either the high or low level, the D-input has no effect at the output. When $\overline{CLR}$ is at low level, the D-input has no effect at the output.

8.4 Device Functional Modes

Table 1 lists the functional modes of the TLC59212.

Table 1. Function Table (Each Latch)(1)

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	$\overline{Y}$
L	X	X	H*
H	↑	L	H*
H	↑	H	L
H	L	X	Y_0
H	↓	X	Y_0

(1) L: Low-level
H: High-level
H*: with pullup resistor
X: Irrelevant
↑: Rising edge
↓: Falling edge
Z : High-impedance (OFF)

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In LED display application, TLC59212 is used to drive the current sink for 8 LEDs in parallel. LED display pattern can be created by providing different bit pattern. At every positive clock edge, new bit pattern will be transferred to LED display.

9.2 Typical Application

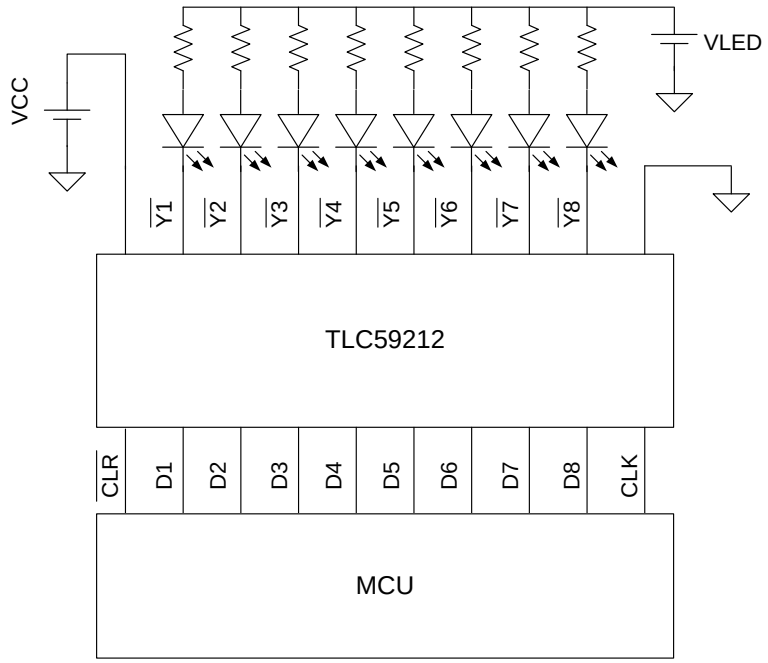

Figure 4. Typical Application Diagram

9.2.1 Design Requirements

For LED display application, LED is selected based on the application. The current level is determined by the required brightness. Given the available LED supply, the resistor value could be determined. The TCL59212 has a maximum current requirement less than 40mA for constant on application.

9.2.2 Detailed Design Procedure

The selection of supply voltage (VLED), LED, and resistor sets the current of the LED.

$$VR + VL + VOL = VLED \quad (1)$$

$$I = (VLED - VL - VOL) / R \quad (2)$$

VR is the voltage drop across the resistor, VL is the voltage drop across the LED when LED is on, VOL is the output voltage at the collector when the driver is enabled. For example, when VLED = 5 V, VL = 2.4 V, and VOL = 0.35 V, a 55-Ω resistor is used to obtain output current 40 mA.

Typical Application (continued)

9.2.3 Application Curve

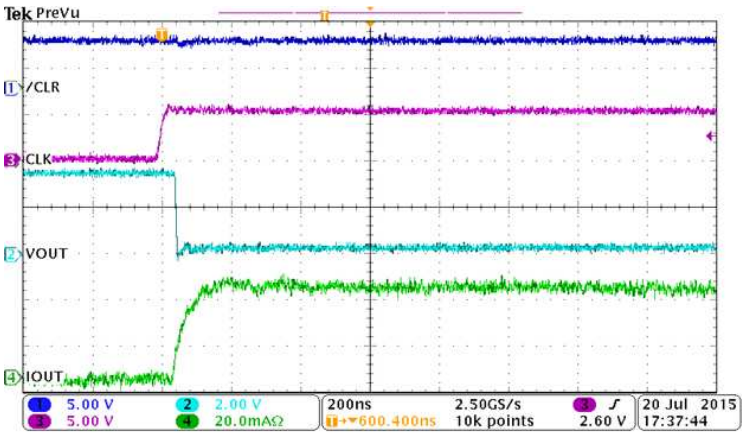

Figure 5. Output Voltage and Current Response

10 Power Supply Recommendations

The supply voltage to TLC59212 is from 4.5 V to 5.5 V. The voltage at output can be up to 24 V.

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11 Layout

11.1 Layout Guidelines

The traces that carry current from the LED cathodes to the output pins must be wide enough to support the current (up to 40 mA).

11.2 Layout Example

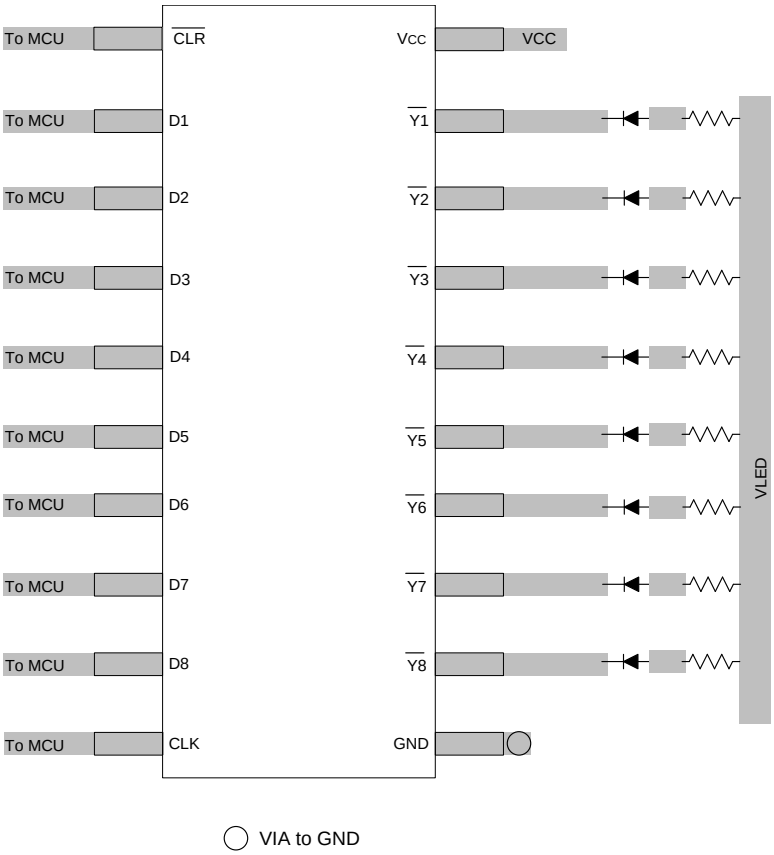

Figure 6. Layout Recommendation

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC59212IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59212	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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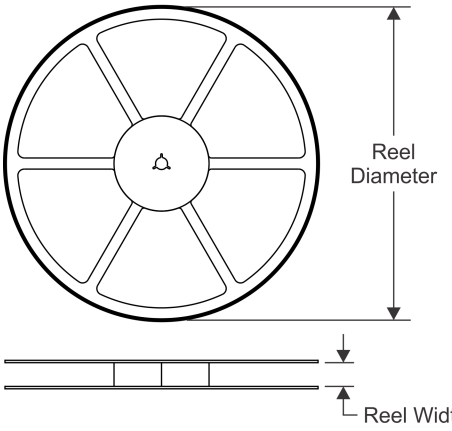
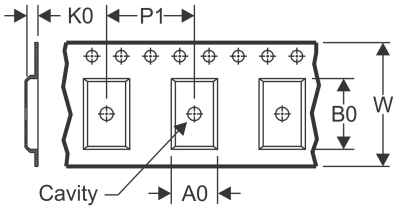
TAPE AND REEL INFORMATION

REEL DIMENSIONS

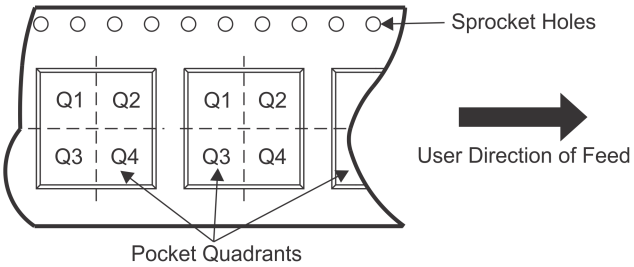


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

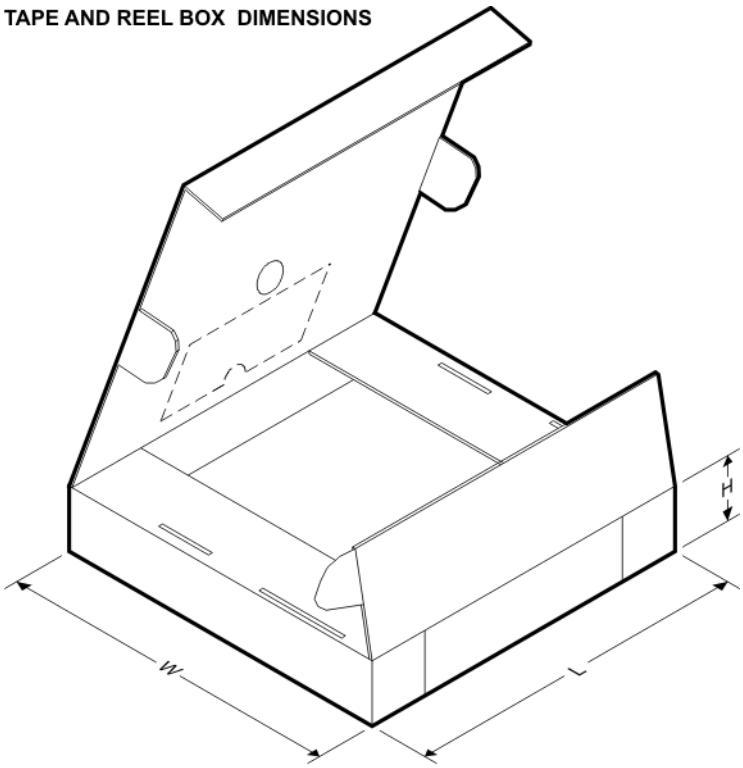
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

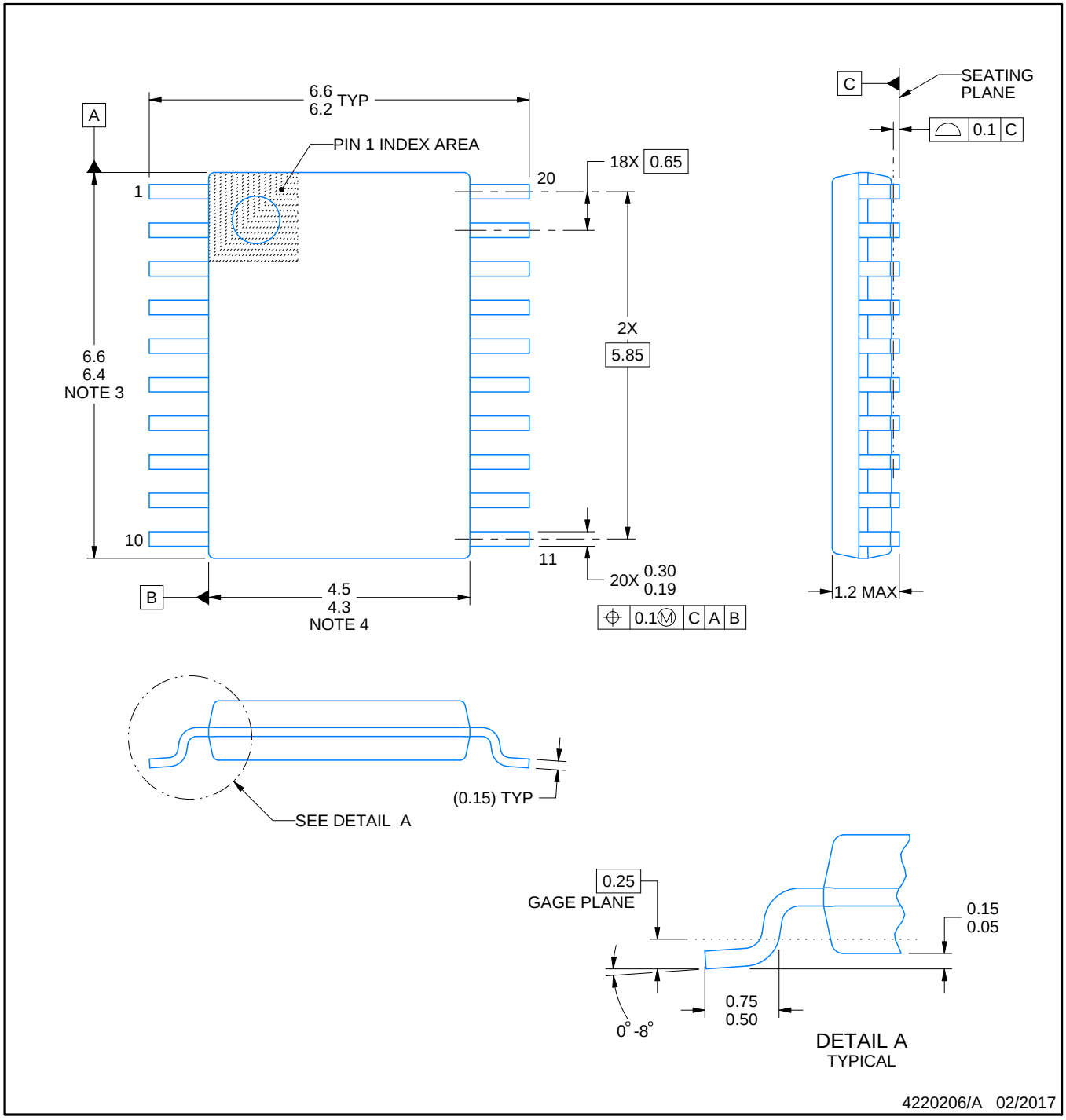
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59212IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



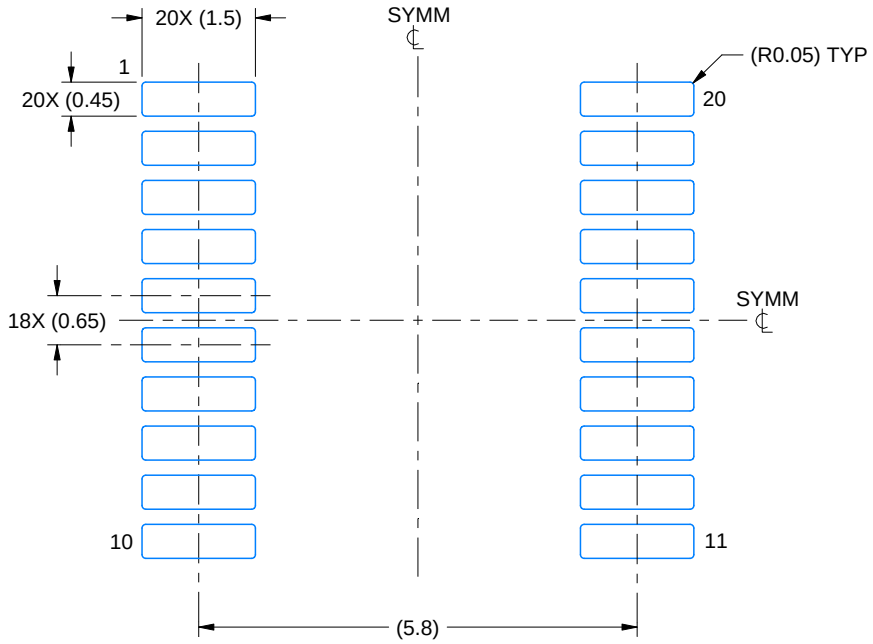
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59212IPWR	TSSOP	PW	20	2000	853.0	449.0	35.0



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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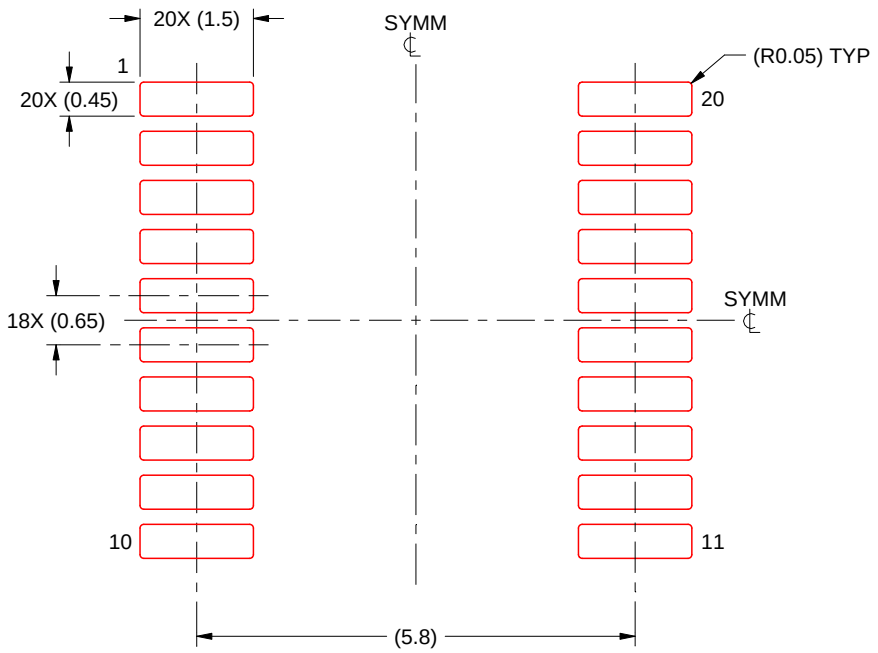
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



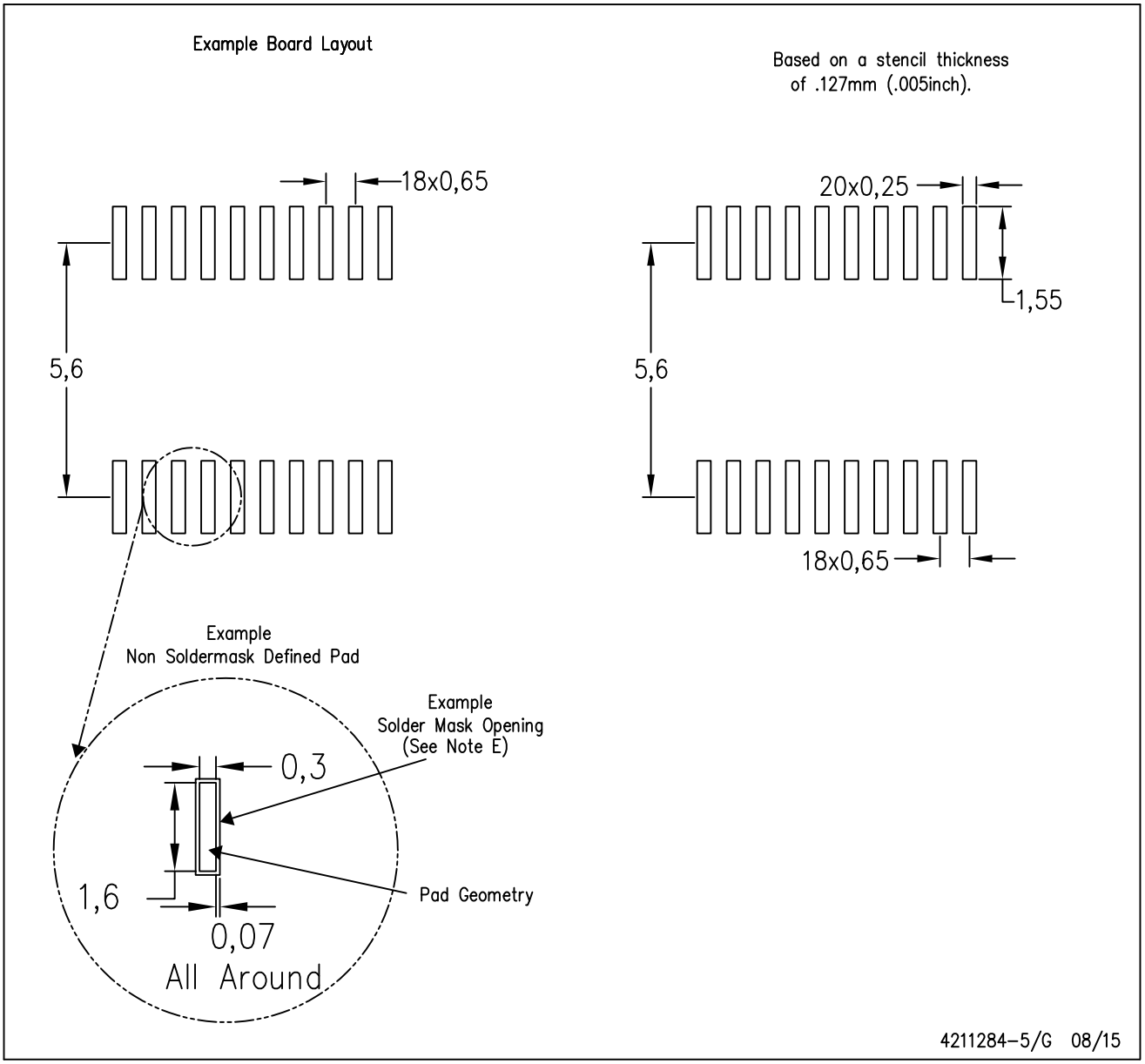
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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