LME49743 Quad High Performance, High Fidelity Audio Operational Amplifier

Check for Samples: LME49743

FEATURES

- **Easily Drives 600Ω Loads**
- **Optimized for Superior Audio Signal Fidelity**
- **Output Short Circuit Protection**
- **98dB (Typ) PSRR and 106dB (Typ) CMRR**
- **TSSOP Package**

APPLICATIONS

- **Audio Amplifiers and Preamplifiers**
- **Professional Audio**
- **Equalization and Crossover Networks**
- **Line Drivers and Receivers**
- **Active Filters**

DESCRIPTION

The LME49743 is a low distortion, low noise, high slew rate operational amplifier optimized and fully specified for high performance, high fidelity applications. The LME49743 audio operational amplifier delivers superior audio signal amplification for outstanding audio performance. The LME49743 combines low voltage noise density (3.5nV/$\sqrt{Hz}$) and THD+N (0.0001%) to easily satisfy demanding audio applications. To ensure that the most challenging loads are driven without compromise, the LME49743 has a slew rate of ±12V/µs and an output current capability of ±21mA.

The LME49743's outstanding CMRR(106dB), PSRR(98dB), and V_{OS} (±0.15mV) give the amplifier excellent operational amplifier DC performance.

The LME49743 has a wide supply range of ±4.0V to ±17V. Over this supply range the LME49743's input circuitry maintains excellent common-mode, power supply rejection, and low input bias current. The LME49743 is unity gain stable.

The LME49743 is available in 14–lead TSSOP.

Table 1. Key Specifications

		VALUE	UNIT
Power Supply Voltage Range		±4.0V to ±17	V
THD+N (A_V = 1, V_{OUT} = 3V_{RMS}, f_{IN} = 1kHz)	R_L = 2kΩ	0.0001	% (typ)
	R_L = 600Ω	0.0001	% (typ)
Input Noise Density		3.5	nV/$\sqrt{Hz}$ (typ)
Slew Rate		±12	V/µs (typ)
Gain Bandwidth Product		30	MHz (typ)
Open Loop Gain (R_L = 600Ω)		110	dB (typ)
Input Bias Current		190	nA (typ)
Input Offset Voltage		±0.15	mV (typ)

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Connection Diagram

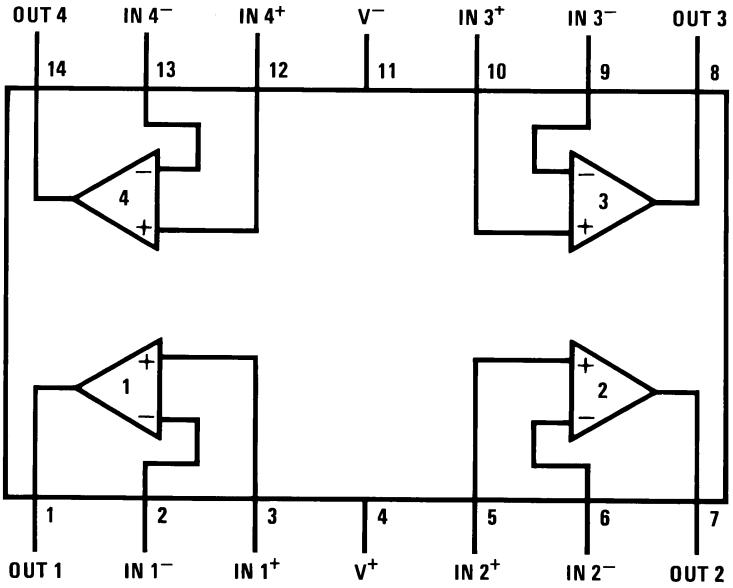


Figure 1. TSSOP Package
See Package Number PW0014A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

Power Supply Voltage	($V_S = V^+ - V^-$)	36V
Storage Temperature		−65°C to 150°C
Input Voltage		(V-) - 0.7V to (V+) + 0.7V
Output Short Circuit (4)		Continuous
Power Dissipation		Internally Limited
ESD Susceptibility (5)		750V
ESD Susceptibility (6)		175V
Junction Temperature		150°C
Thermal Resistance	θ_{JA} (MT)	140°C/W
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage Range		$\pm 4.0V \le V_S \le \pm 17V$

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur.
(2) Operating Ratings indicate conditions for which the device is functional, but do not specify specific performance limits. For specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specifications are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Amplifier output connected to GND, any number of amplifiers within a package.
(5) Human body model, 100pF discharged through a 1.5kΩ resistor.
(6) Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage and then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).

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Electrical Characteristics

The following specifications apply for V_S = ±15V, R_L = 2kΩ, f_{IN} = 1kHz, and T_A = 25C, unless otherwise specified.(1)(2)

Parameter		Test Conditions	LME49743		Units (Limits)
			Typ(3)	Limit (4)(5)	
THD+N	Total Harmonic Distortion + Noise	A_V = 1, V_{OUT} = 3V_{RMS} R_L = 2kΩ R_L = 600Ω	 0.0001 0.0001	 0.0002	 % (max)
IMD	Intermodulation Distortion	A_V = 1, V_{OUT} = 3V_{RMS} Two-tone, 60Hz & 7kHz 4:1	0.0005		% (max)
GBWP	Gain Bandwidth Product		30	25	MHz (min)
SR	Slew Rate		12	9.5	V/µs (min)
FPBW	Full Power Bandwidth	V_{OUT} = 1V_{P-P}, –3dB referenced to output magnitude at f = 1kHz	10		MHz
t_s	Settling time	A_V = 1, 10V step, C_L = 100pF 0.1% error range	 1.2		 µs
e_n	Equivalent Input Noise Voltage	f_{BW} = 20Hz to 20kHz	0.48	0.65	µV_{RMS}
	Equivalent Input Noise Density	f = 1kHz f = 10Hz	3.5 6.4	4.5	nV/√Hz (max) nV/√Hz
i_n	Current Noise Density	f = 1kHz f = 10Hz	1.6 3.1		pA/√Hz pA/√Hz
V_{OS}	Offset Voltage		±0.15	±1.0	mV (max)
$\Delta V_{OS}/\Delta Temp$	Average Input Offset Voltage Drift vs Temperature	40°C ≤ T_A ≤ 85°C	0.05		µV/°C
PSRR	Average Input Offset Voltage Shift vs Power Supply Voltage	ΔV_S = 20V(6)	98	94	dB (min)
ISO_{CH-CH}	Channel-to-Channel Isolation	f_{IN} = 1kHz f_{IN} = 20kHz	118 112		dB dB
I_B	Input Bias Current	V_{CM} = 0V	190	250	nA (max)
$\Delta I_{OS}/\Delta Temp$	Input Bias Current Drift vs Temperature	–40°C ≤ T_A ≤ 85°C	0.05		nA/°C
I_{OS}	Input Offset Current	V_{CM} = 0V	7	40	nA (max)
V_{IN-CM}	Common-Mode Input Voltage Range		±13.2	(V+)–2.0 (V-)+2.0	V (min) V (min)
CMRR	Common-Mode Rejection	–10V<V_{CM}<10V	106	98	dB (min)
Z_{IN}	Differential Input Impedance		30		kΩ
	Common Mode Input Impedance	–10V<V_{CM}<10V	1000		MΩ
A_{VOL}	Open Loop Voltage Gain	–10V<V_{OUT}<10V, R_L = 600Ω	110		dB (min)
		–10V<V_{OUT}<10V, R_L = 2kΩ	110		dB (min)
		–10V<V_{OUT}<10V, R_L = 10kΩ	110	100	dB (min)
V_{OUTMAX}	Maximum Output Voltage Swing	R_L = 600Ω	±12.4	±12.0	V (min)
		R_L = 2kΩ	±13.0		V (min)
		R_L = 10kΩ	±13.0		V (min)
I_{OUT}	Output Current	R_L = 600Ω, V_S = ±17V	±21	±20	mA (min)
I_{OUT-CC}	Short Circuit Current		+30 –38		mA mA

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur.
(2) Operating Ratings indicate conditions for which the device is functional, but do not specify specific performance limits. For specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) Typical specifications are specified at +25ºC and represent the most likely parametric norm.
(4) Tested limits are ensured to Texas Instrument's AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) PSRR is measured as follows: V_{OS} is measured at two supply voltages, ±5V and ±15V. PSRR = |20log($\Delta V_{OS}/\Delta V_S$)|.

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Electrical Characteristics (continued)

The following specifications apply for V_S = ±15V, R_L = 2kΩ, f_{IN} = 1kHz, and T_A = 25C, unless otherwise specified.(1)(2)

Parameter		Test Conditions	LME49743		Units (Limits)
			Typ(3)	Limit (4)(5)	
R_{OUT}	Output Impedance	f_{IN} = 10kHz Closed-Loop Open-Loop	 0.01 13		 Ω Ω
C_{LOAD}	Capacitive Load Drive Overshoot	100pF	16		%
I_S	Total Quiescent Current	I_{OUT} = 0mA	10	14	mA (max)

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Typical Performance Characteristics

THD+N vs Output Voltage V_S = ±15V, R_L = 2kΩ, f = 1kHz 30kHz BW

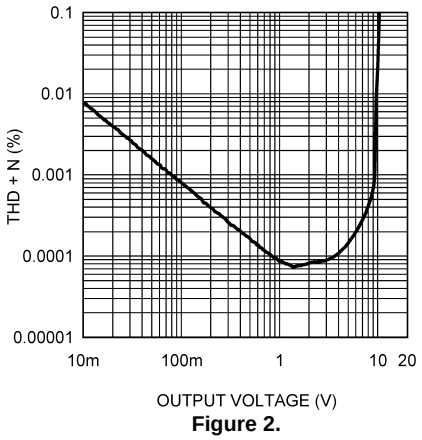


Figure 2.

THD+N vs Output Voltage V_S = ±15V, R_L = 10kΩ, f = 1kHz 30kHz BW

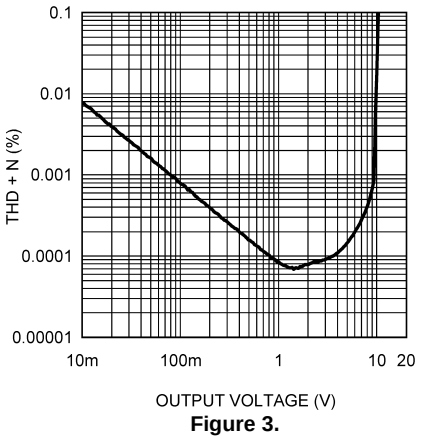


Figure 3.

THD+N vs Output Voltage V_S = ±15V, R_L = 600Ω, f = 1kHz 30kHz BW

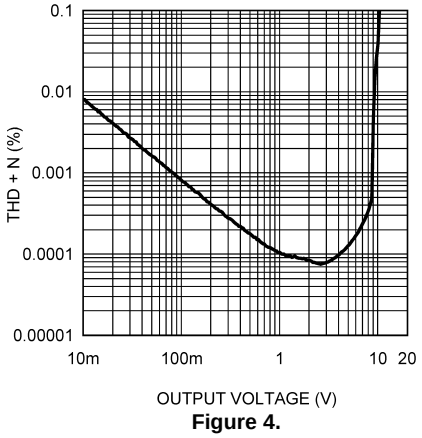


Figure 4.

THD+N vs Frequency V_S = ±15V, V_{OUT} = 3V_{RMS}, R_L = 2kΩ 80kHz BW

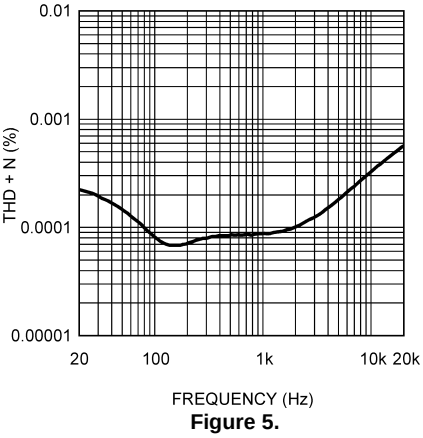


Figure 5.

THD+N vs Frequency V_S = ±15V, V_{OUT} = 3V_{RMS}, R_L = 10kΩ 80kHz BW

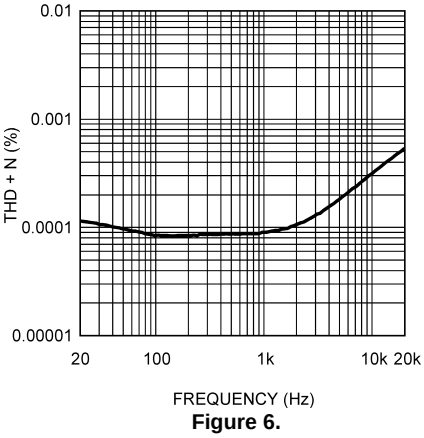


Figure 6.

THD+N vs Frequency V_S = ±15V, V_{OUT} = 3V_{RMS}, R_L = 600Ω 80kHz BW

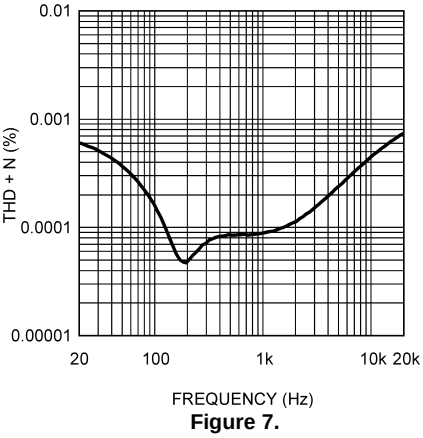


Figure 7.

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Typical Performance Characteristics (continued)

+PSRR vs Frequency
V_S = ±15V, R_L = 2kΩ, V_{RIPPLE} = 200mV_{PP}

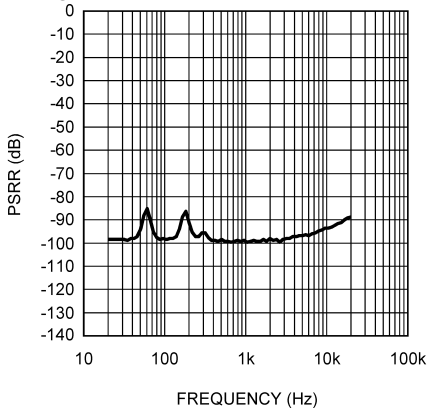


Figure 8.

+PSRR vs Frequency
V_S = ±15V, R_L = 10kΩ, V_{RIPPLE} = 200mV_{PP}

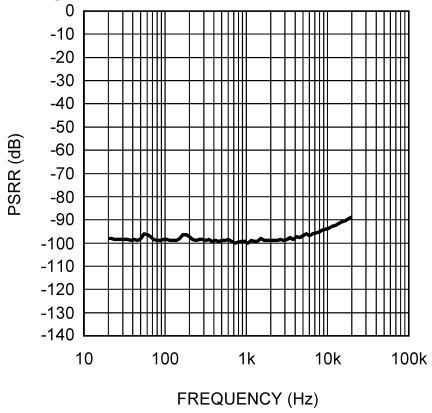


Figure 9.

+PSRR vs Frequency
V_S = ±15V, R_L = 600Ω, V_{RIPPLE} = 200mV_{PP}

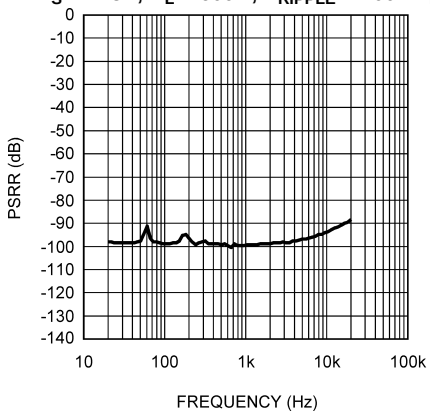


Figure 10.

−PSRR vs Frequency
V_S = ±15V, R_L = 2kΩ, V_{RIPPLE} = 200mV_{PP}

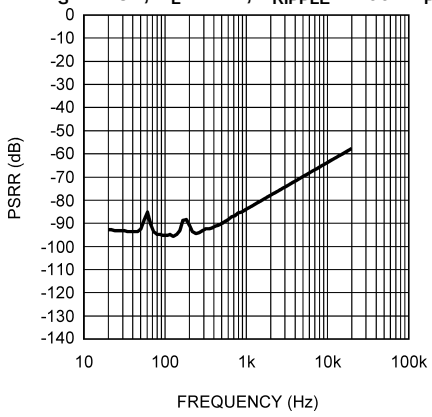


Figure 11.

−PSRR vs Frequency
V_S = ±15V, R_L = 10kΩ, V_{RIPPLE} = 200mV_{PP}

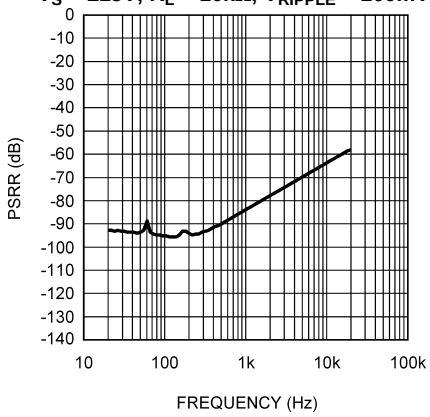


Figure 12.

−PSRR vs Frequency
V_S = ±15V, R_L = 600Ω, V_{RIPPLE} = 200mV_{PP}

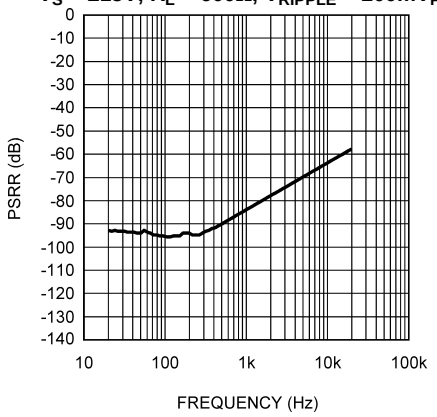


Figure 13.

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Typical Performance Characteristics (continued)

CMRR vs Frequency
V_S = ±15V, R_L = 2kΩ, V_{IN} = 200mV$_{PP}$

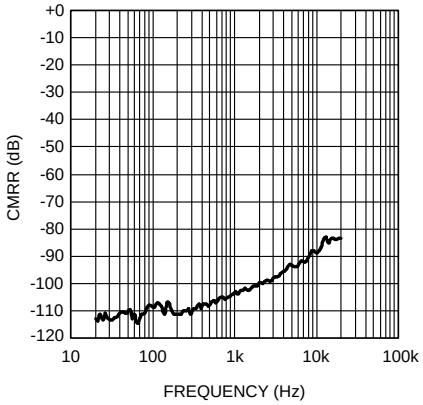


Figure 14.

CMRR vs Frequency
V_S = ±15V, R_L = 10kΩ, V_{IN} = 200mV$_{PP}$

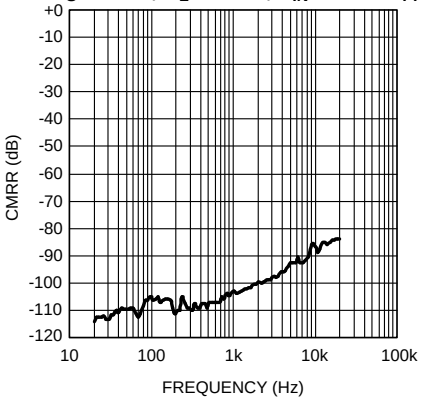


Figure 15.

CMRR vs Frequency
V_S = ±15V, R_L = 600Ω, V_{IN} = 200mV$_{PP}$

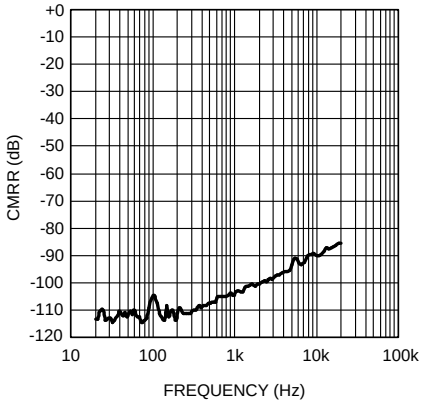


Figure 16.

Crosstalk vs Frequency
V_S = ±15V, V_{OUT} = 3V$_{RMS}$, R_L = 2kΩ

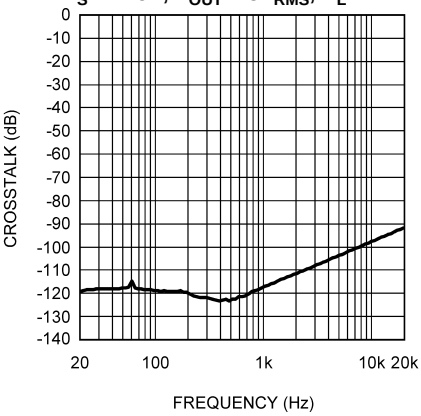


Figure 17.

Crosstalk vs Frequency
V_S = ±15V, V_{OUT} = 3V$_{RMS}$, R_L = 10kΩ

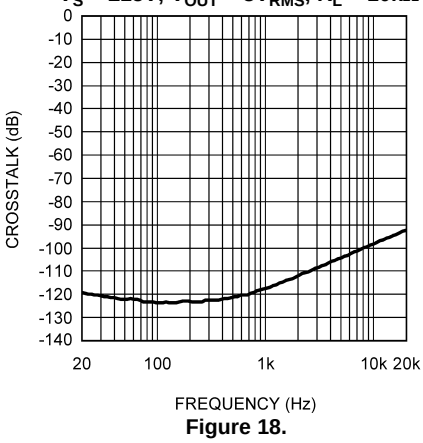


Figure 18.

Crosstalk vs Frequency
V_S = ±15V, V_{OUT} = 3V$_{RMS}$, R_L = 600Ω

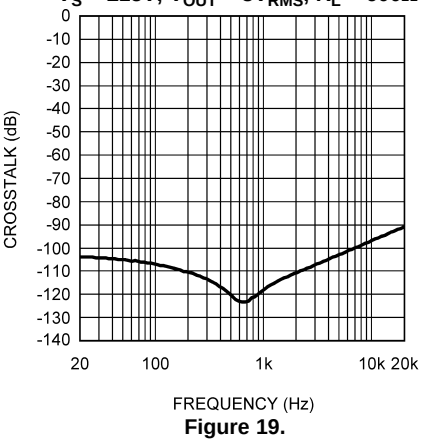


Figure 19.

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Typical Performance Characteristics (continued)

IMD vs Output Voltage V_S = ±5V, R_L = 2kΩ 7kHz/60Hz 4:1 SMPTE

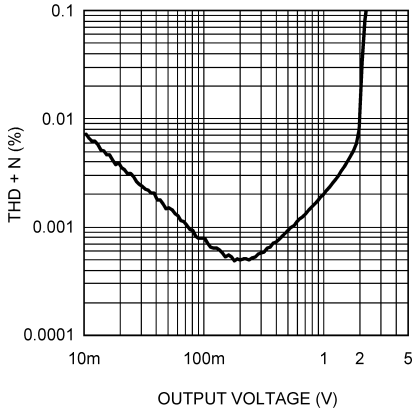


Figure 20.

IMD vs Output Voltage V_S = ±5V, R_L = 10kΩ 7kHz/60Hz 4:1 SMPTE

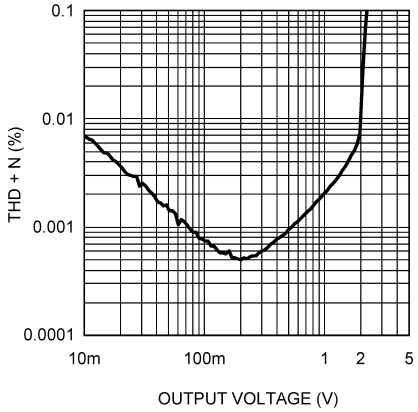


Figure 21.

IMD vs Output Voltage V_S = ±5V, R_L = 600Ω 7kHz/60Hz 4:1 SMPTE

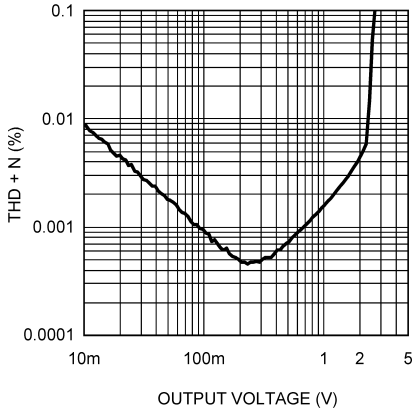


Figure 22.

Output Voltage vs Supply Voltage R_L = 2kΩ, THD+N = 0.1%

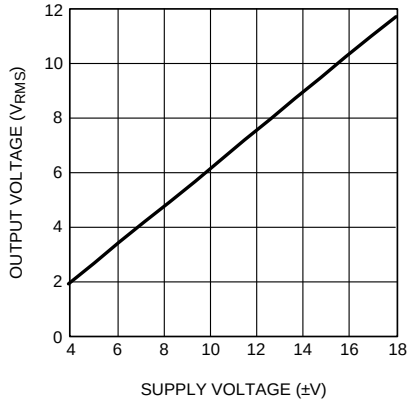


Figure 23.

Output Voltage vs Supply Voltage R_L = 10kΩ, THD+N = 0.1%

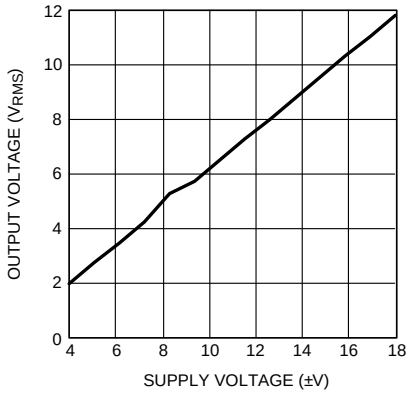


Figure 24.

Output Voltage vs Supply Voltage R_L = 600Ω, THD+N = 0.1%

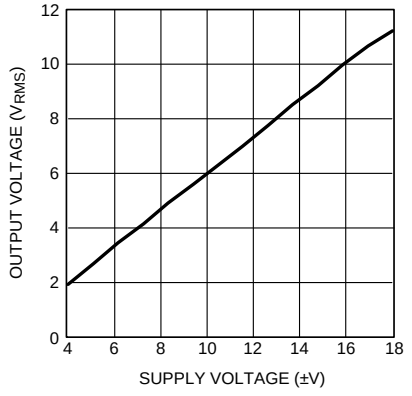


Figure 25.

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Typical Performance Characteristics (continued)

Supply Current vs Supply Voltage

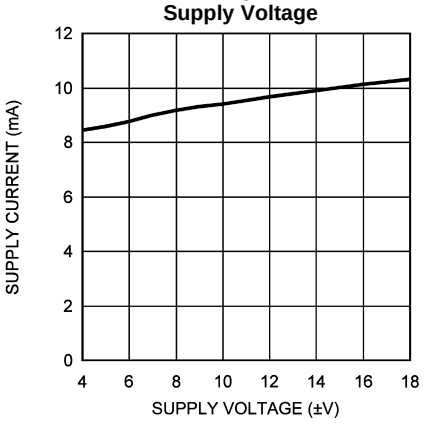


Figure 26.

Scope Photo Small Signal

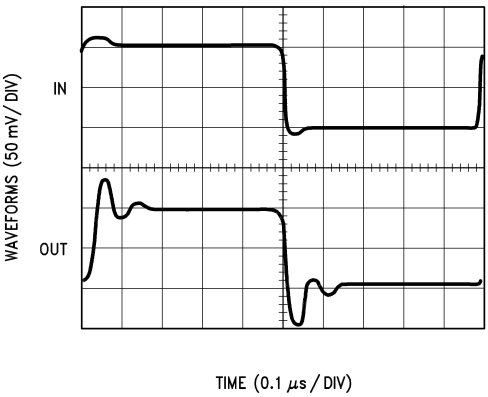


Figure 27.

Scope Photo Large Signal, Non-Inverting

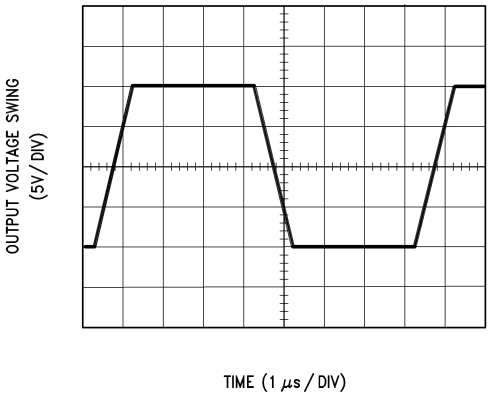


Figure 28.

Scope Photo Large Signal, Inverting

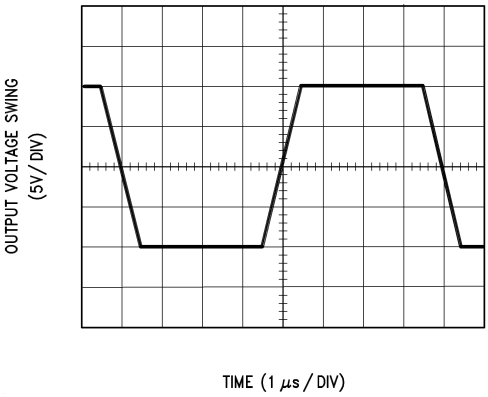


Figure 29.

Equivalent Input Noise vs Frequency

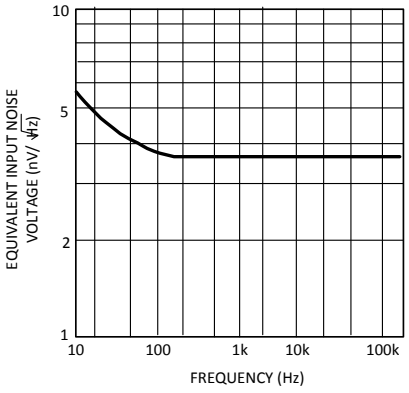


Figure 30.

Power Bandwidth

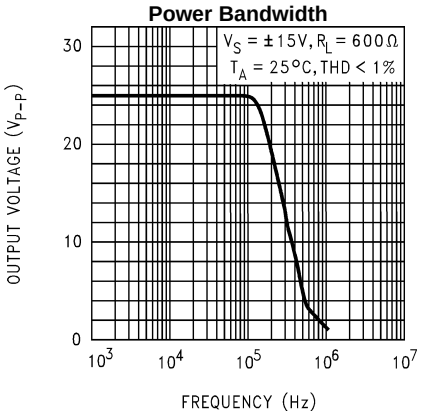


Figure 31.

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Typical Performance Characteristics (continued)

Open Loop Gain and Phase vs Frequency

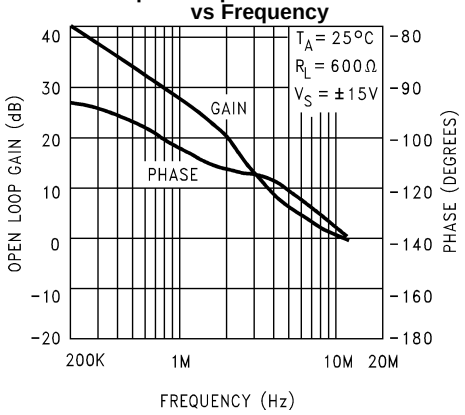


Figure 32.

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APPLICATION INFORMATION

DISTORTION MEASUREMENTS

The vanishingly low residual distortion produced by LME49743 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49743's low residual distortion is an input referred internal error. As shown in Figure 33, adding the 10Ω resistor connected between the amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101, which means that measurement resolution increases by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 33.

This technique is verified by duplicating the measurements with high closed loop gain and/or making the measurements at high frequencies. Doing so produces distortion components that are within the measurement equipment's capabilities. This datasheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

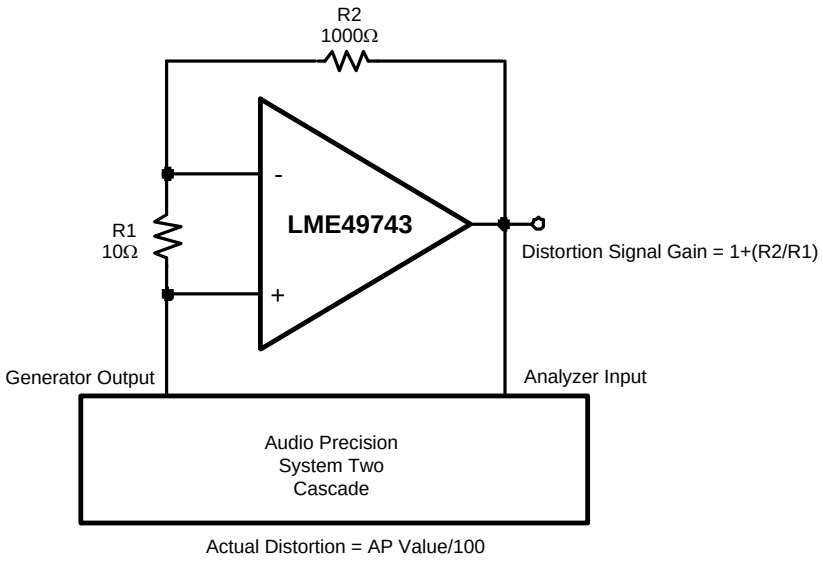


Figure 33. THD+N and IMD Distortion Test Circuit

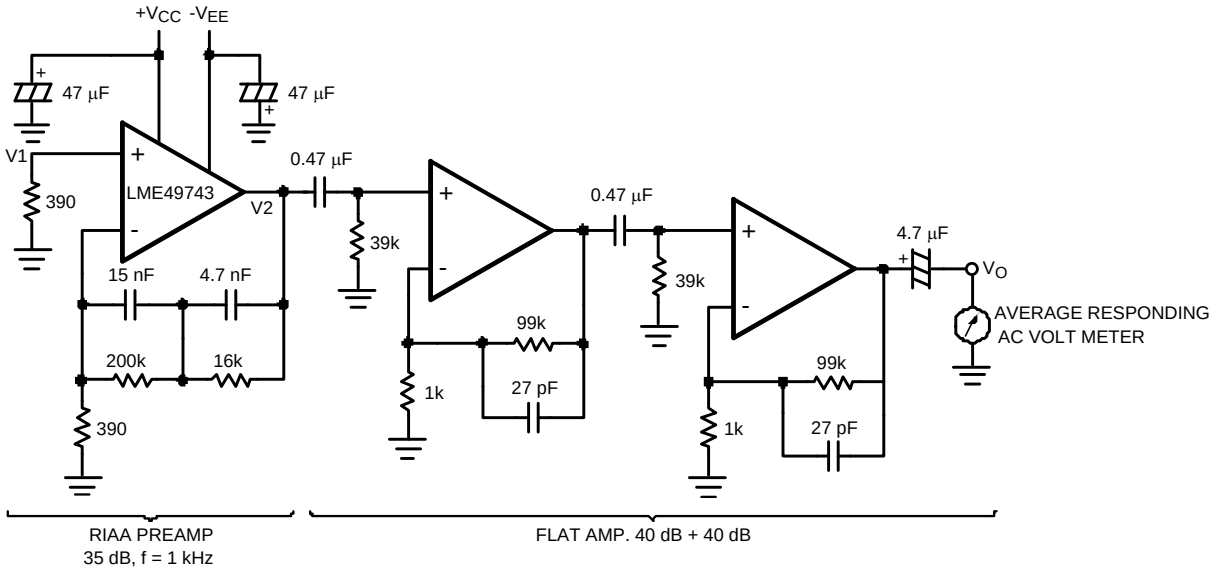
Application Hints

The LME49743 is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 100pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 100pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

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Noise Measurement Circuit



(1) Complete shielding is required to prevent induced pick up from external sources. Always check with oscilloscope for power line noise.

(2) Total Gain: 115 dB at f = 1 kHz

(3) Input Referred Noise Voltage: $e_n = V_O/560{,}000$ (V)

Figure 34.

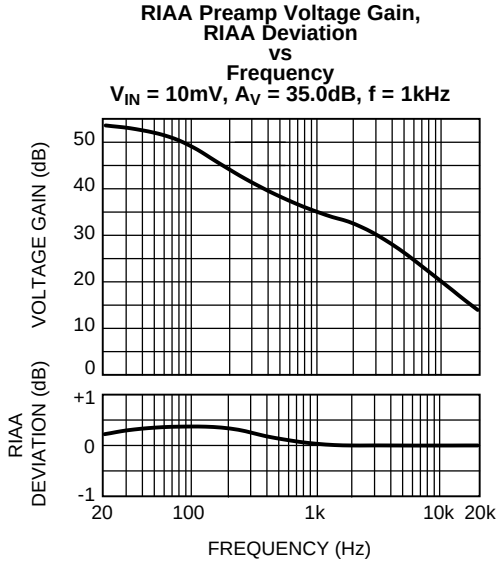


Figure 35.

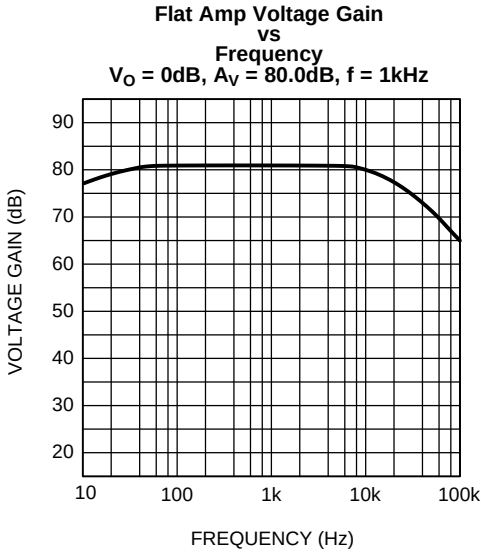
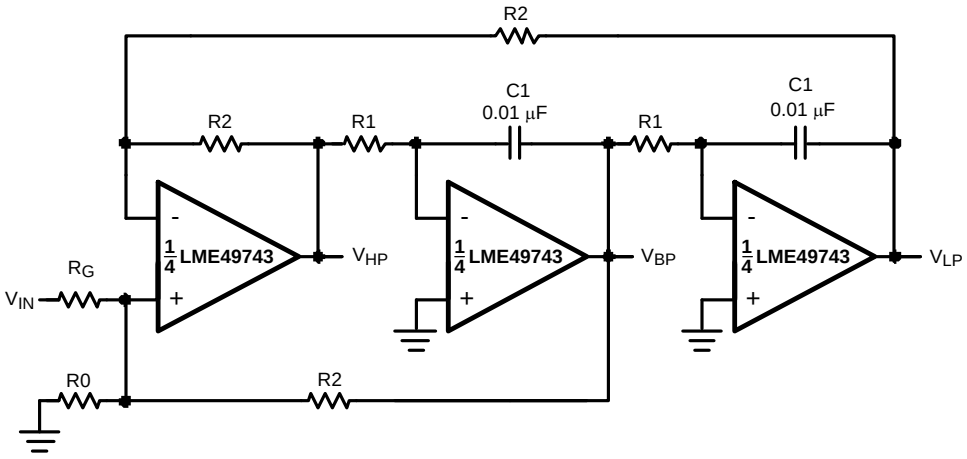


Figure 36.

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Typical Applications



$$f_0 = \frac{1}{2\pi C1R1}, Q = \frac{1}{2}\left(1 + \frac{R2}{R0} + \frac{R2}{RG}\right), A_{BP} = QA_{LP} = QA_{LH} = \frac{R2}{RG}$$

Figure 37. State Variable Filter

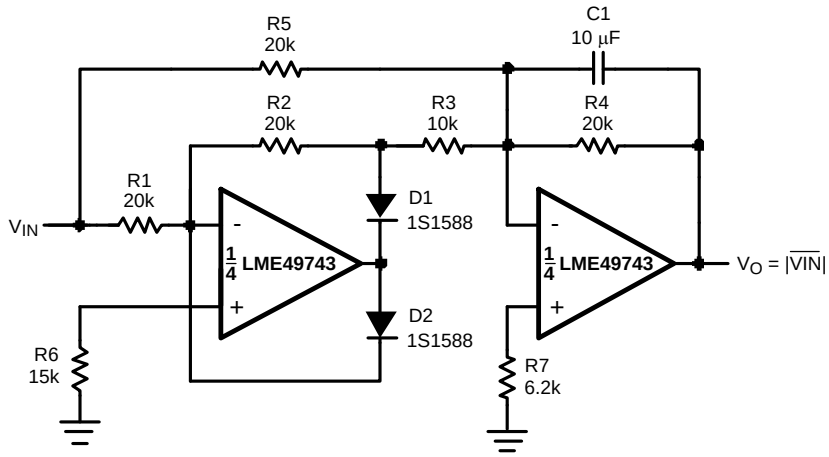


Figure 38. AC-DC Converter

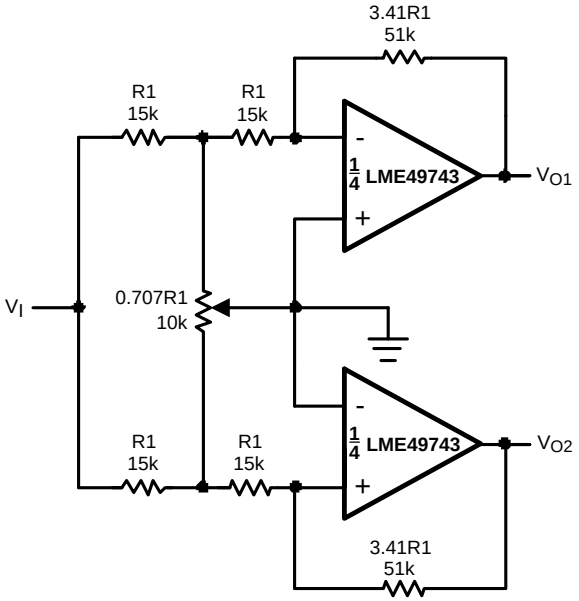


Figure 39. 2 Channel Panning Circuit (Pan Pot)

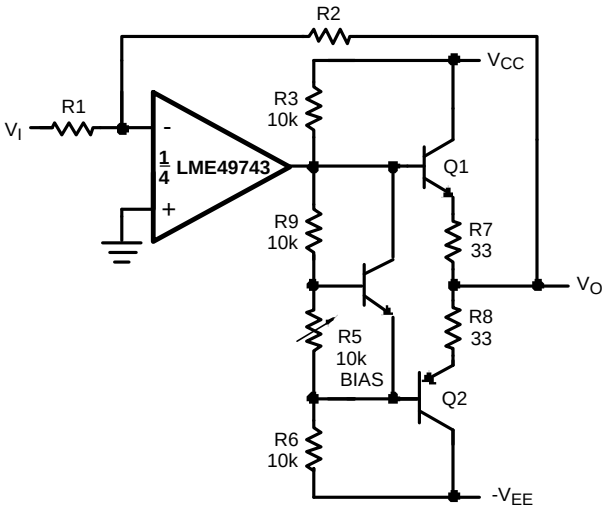
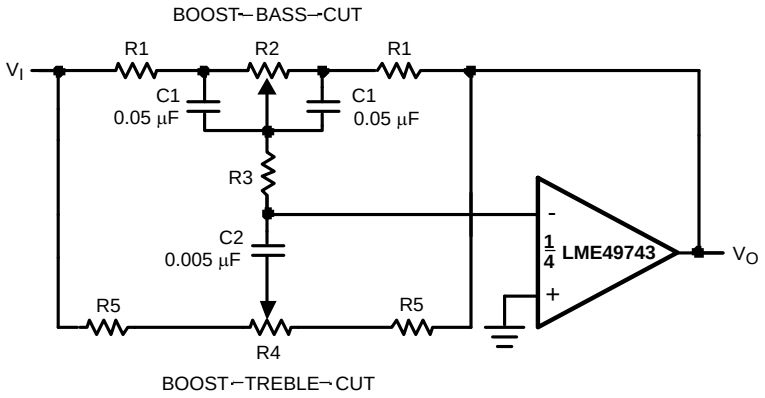


Figure 40. Line Driver

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$$f_L = \frac{1}{2\pi R2C1},\ f_{LB} = \frac{1}{2\pi R1C1}$$

$$f_H = \frac{1}{2\pi R5C2},\ f_{HB} = \frac{1}{2\pi(R1 + R5 + 2R3)C2}$$

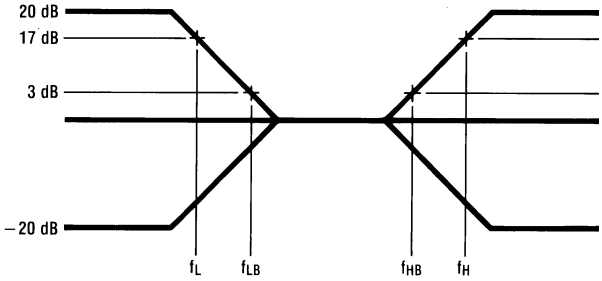
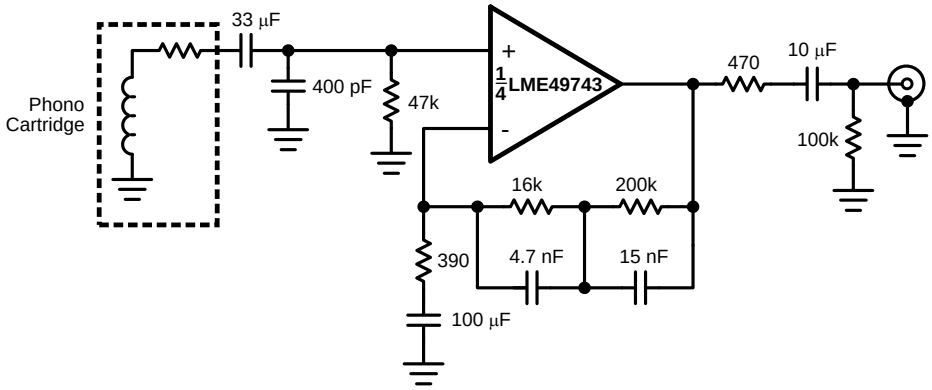
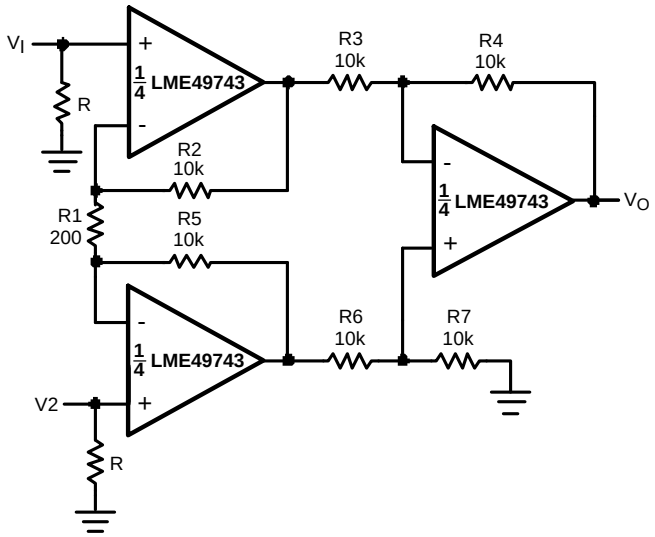


Figure 41. Tone Control



A_v = 35 dB
E_n = 0.33 µV
S/N = 90 dB
f = 1 kHz
A Weighted
A Weighted, V_{IN} = 10 mV
at f = 1 kHz

Figure 42. RIAA Preamp



If R2 = R5, R3 = R6, R4 = R7

$$V0 = \left(1 + \frac{2R2}{R1}\right)\frac{R4}{R3}(V2 - V1)$$

Illustration is:

V0 = 101(V2 − V1)

Figure 43. Balanced Input Mic Amp

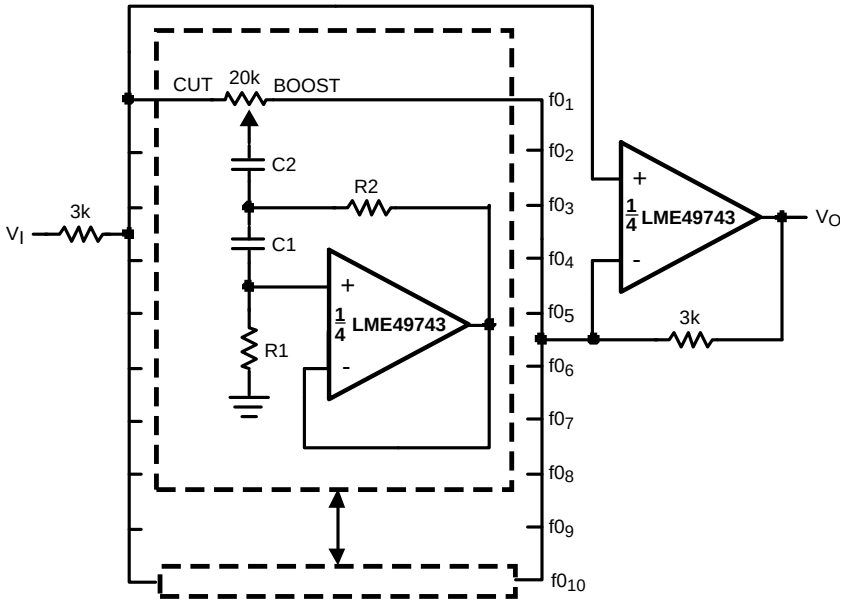


Figure 44. 10 Band Graphic Equalizer

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fo (Hz)	C_1	C_2	R_1	R_2
32	0.12µF	4.7µF	75kΩ	500Ω
64	0.056µF	3.3µF	68kΩ	510Ω
125	0.033µF	1.5µF	62kΩ	510Ω
250	0.015µF	0.82µF	68kΩ	470Ω
500	8200pF	0.39µF	62kΩ	470Ω
1k	3900pF	0.22µF	68kΩ	470Ω
2k	2000pF	0.1µF	68kΩ	470Ω
4k	1100pF	0.056µF	62kΩ	470Ω
8k	510pF	0.022µF	68kΩ	510Ω
16k	330pF	0.012µF	51kΩ	510Ω

NOTE

At volume of change = ±12 dB

Q = 1.7

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REVISION HISTORY

Rev	Date	Description
1.0	03/26/08	Initial release.
1.01	01/12/09	Fixed a typo.
B	04/04/13	Changed layout of National Data Sheet to TI format.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LME49743MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	L49743 MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

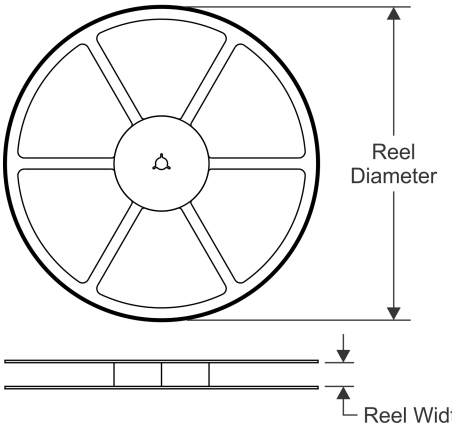
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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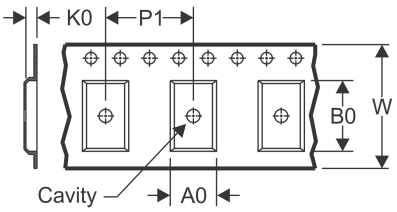
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

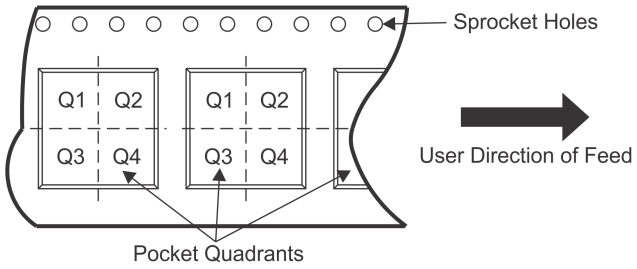


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

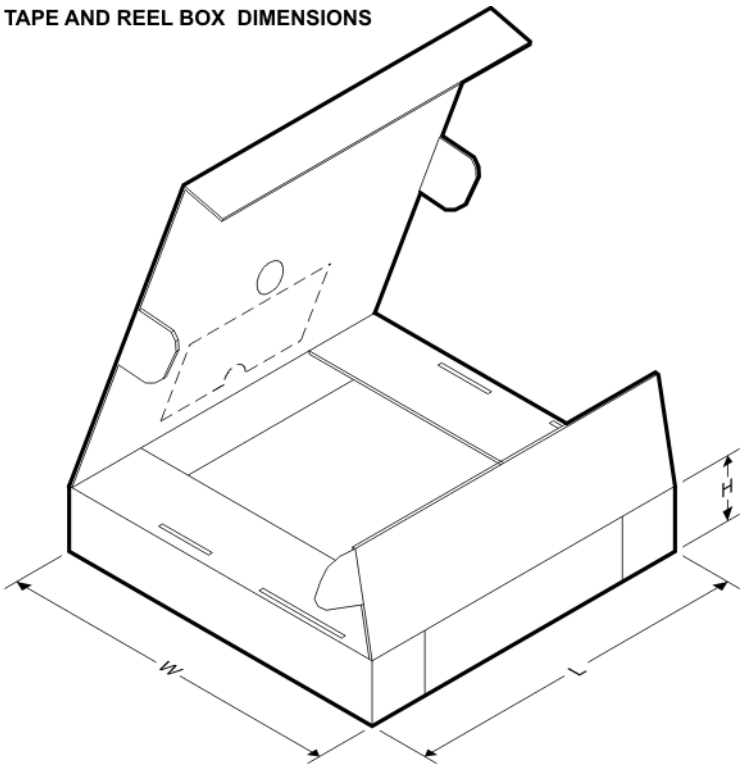
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LME49743MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

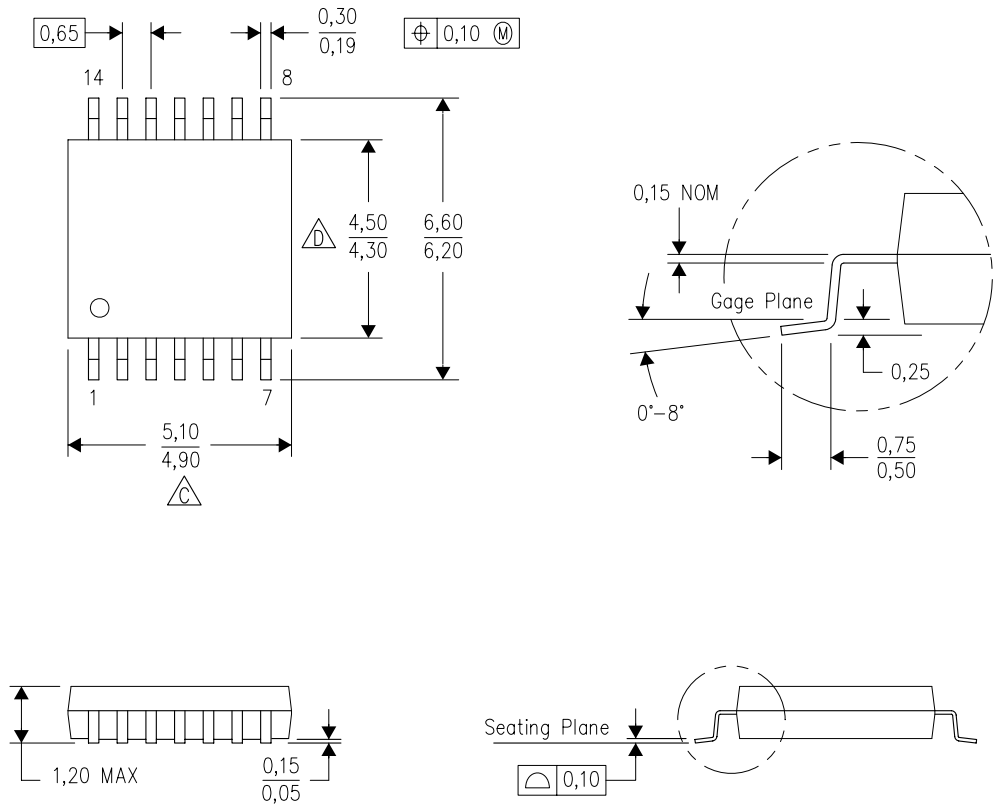
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LME49743MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

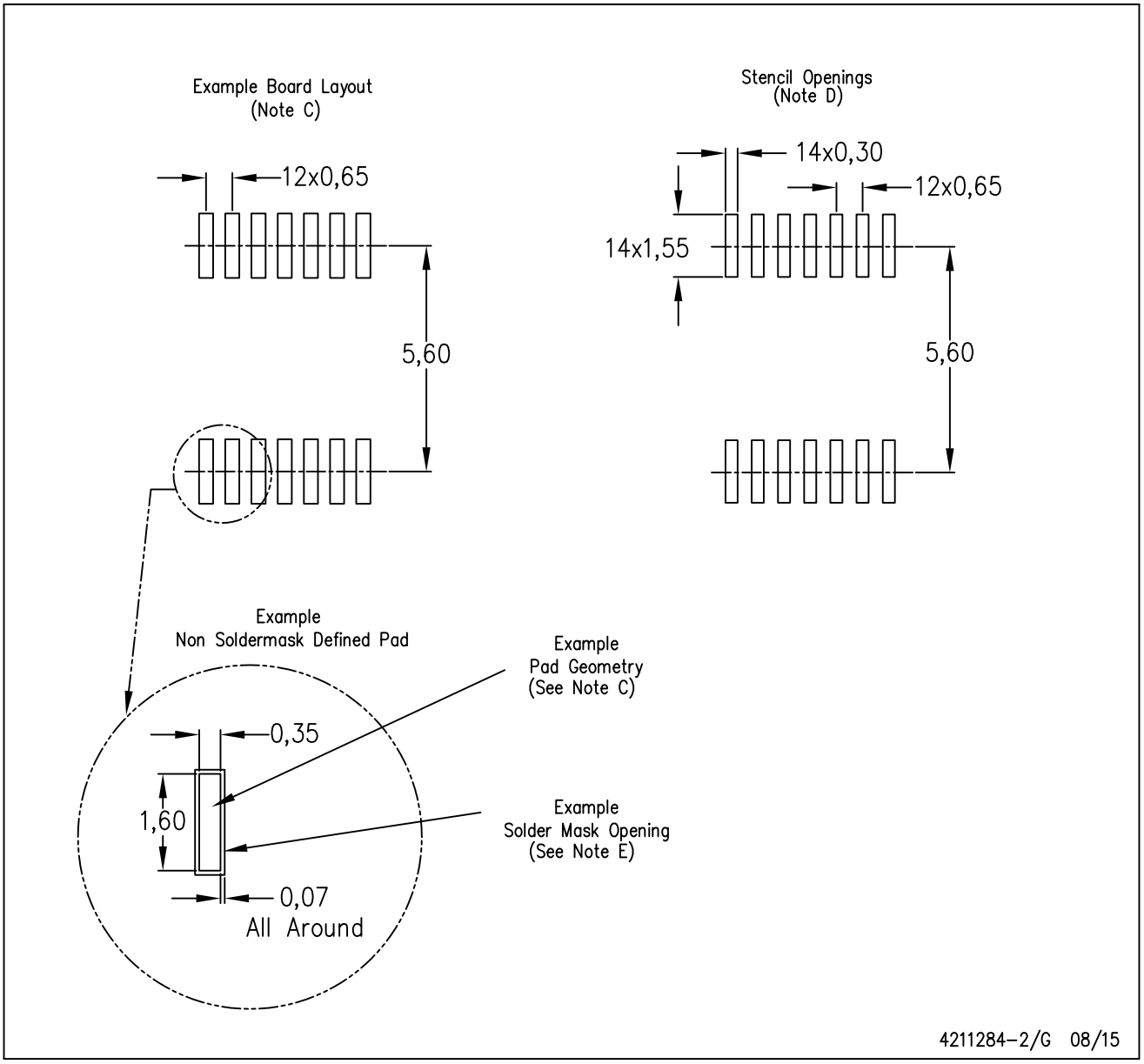
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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