# INAx180-Q1 汽车低侧和高侧电压输出电流感应放大器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1：–40°C ≤ $T_A$ ≤ +125°C
  - HBM ESD 分类等级 2
  - CDM ESD 分类等级 C6
- 共模范围 ($V_{CM}$)：–0.2V 至 +26V
- 高带宽：350kHz（A1 器件）
- 偏移电压：
  - ±150µV（最大值），$V_{CM}$ = 0V
  - ±500µV（最大值），$V_{CM}$ = 12V
- 输出压摆率：2V/µs
- 精度：
  - ±1% 增益误差（最大值）
  - 1µV/°C 温漂（最大值）
- 增益选项：
  - 20V/V（A1 器件）
  - 50V/V（A2 器件）
  - 100V/V（A3 器件）
  - 200V/V（A4 器件）
- 瞬态电流：最大为 260µA (INA180-Q1)

## 2 应用

- 电机控制
- 电池监控
- 电源管理
- 照明控制
- 过流检测

## 3 说明

INA180-Q1、INA2180-Q1 和 INA4180-Q1 (INAx180-Q1) 电流检测放大器专为经成本优化的 解决方案而设计。这些器件是一系列电流检测放大器（也称为电流分流监控器）的一部分，可在独立于电源电压的 –0.2V 至 +26V 范围内的共模电压中检测电流检测电阻器上的压降。INAx180-Q1 集成有一个匹配的电阻器增益网络，具有四个固定增益器件选项：20V/V、50V/V、100V/V 或 200V/V。该匹配增益电阻器网络可最大限度地减小增益误差并降低温漂。

所有这些器件由 2.7V 至 5.5V 单电源供电。单通道 INA180-Q1 消耗的最大电源电流为 260µA；而双通道 INA2180-Q1 消耗的最大电源电流为 500µA，四通道消耗的最大电源电流为 900µA。

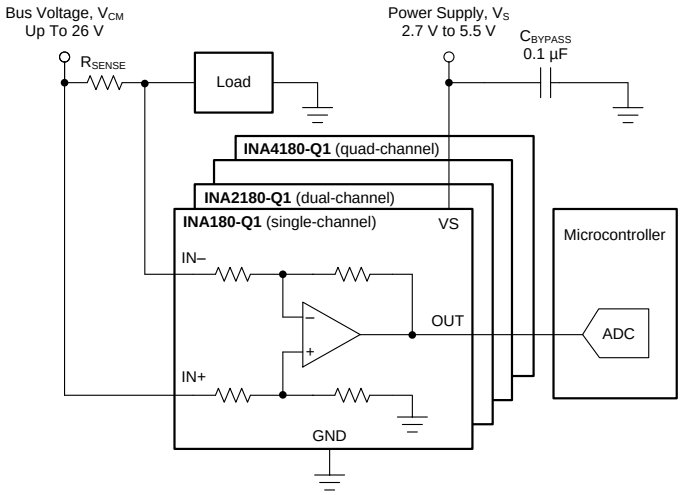
INA180-Q1 采用具有两种不同引脚配置的 5 引脚 SOT-23 封装。INA2180-Q1 采用 8 引脚 VSSOP 封装。INA4180-Q1 采用 14 引脚 TSSOP 封装。所有器件选项都具有 –40°C 至 +125°C 的扩展额定工作温度范围。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| INA180-Q1 | SOT-23 (5) | 2.90mm × 1.60mm |
| INA2180-Q1 | VSSOP (8) | 3.00mm × 3.00mm |
| INA4180-Q1 | TSSOP (14) | 5.00mm × 4.40mm |

(1) 如需了解所有可用封装，请参阅产品说明书末尾的封装选项附录。

典型应用电路




本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

# 目录

**1** 特性 ... 1
**2** 应用 ... 1
**3** 说明 ... 1
**4** 修订历史记录 ... 2
**5** **Device Comparison Table** ... 3
**6** **Pin Configuration and Functions** ... 3
**7** **Specifications** ... 5
7.1 Absolute Maximum Ratings ... 5
7.2 ESD Ratings ... 5
7.3 Recommended Operating Conditions ... 5
7.4 Thermal Information ... 5
7.5 Electrical Characteristics ... 6
7.6 Typical Characteristics ... 7
**8** **Detailed Description** ... 14
8.1 Overview ... 14
8.2 Functional Block Diagrams ... 14
8.3 Feature Description ... 16
8.4 Device Functional Modes ... 17
**9** **Application and Implementation** ... 19
9.1 Application Information ... 19
9.2 Typical Application ... 23
**10** **Power Supply Recommendations** ... 25
10.1 Common-Mode Transients Greater Than 26 V ... 25
**11** **Layout** ... 26
11.1 Layout Guidelines ... 26
11.2 Layout Examples ... 26
**12** 器件和文档支持 ... 29
12.1 文档支持 ... 29
12.2 相关链接 ... 29
12.3 接收文档更新通知 ... 29
12.4 社区资源 ... 29
12.5 商标 ... 29
12.6 静电放电警告 ... 29
12.7 术语表 ... 29
**13** 机械、封装和可订购信息 ... 29

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision A (July 2018) to Revision B** **Page**

- 已更改 将 INA180-Q1 器件从产品预览更改为生产数据（有效） ... 1
- 已添加 new paragraph regarding phase reversal to end of *Input Differential Overload* section ... 18

**Changes from Original (April 2018) to Revision A** **Page**

- 已更改 将 INA4180-Q1 器件从预览更改为生产数据（有效） ... 1


Copyright © 2018–2019, Texas Instruments Incorporated

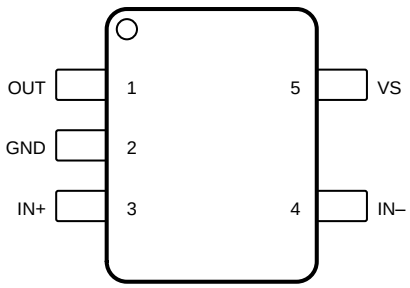
## 5 Device Comparison Table

| PRODUCT | NUMBER OF CHANNELS | GAIN (V/V) |
|---|---|---|
| INA180A1-Q1 (1) | 1 | 20 |
| INA180A2-Q1 (1) | 1 | 50 |
| INA180A3-Q1 (1) | 1 | 100 |
| INA180A4-Q1 (1) | 1 | 200 |
| INA180B1-Q1 (1) | 1 | 20 |
| INA180B2-Q1 (1) | 1 | 50 |
| INA180B3-Q1 (1) | 1 | 100 |
| INA180B4-Q1 (1) | 1 | 200 |
| INA2180A1-Q1 | 2 | 20 |
| INA2180A2-Q1 | 2 | 50 |
| INA2180A3-Q1 | 2 | 100 |
| INA2180A4-Q1 | 2 | 200 |
| INA4180A1-Q1 | 4 | 20 |
| INA4180A2-Q1 | 4 | 50 |
| INA4180A3-Q1 | 4 | 100 |
| INA4180A4-Q1 | 4 | 200 |

(1) INA180A devices use pinout A. INA180B devices use pinout B. See the *Pin Configuration and Functions* section for more information.

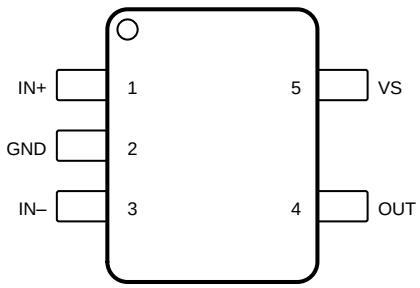
## 6 Pin Configuration and Functions

**INA180-Q1: DBV Package**
**5-Pin SOT-23 (Pinout A)**
**Top View**




Not to scale

**INA180-Q1: DBV Package**
**5-Pin SOT-23 (Pinout B)**
**Top View**



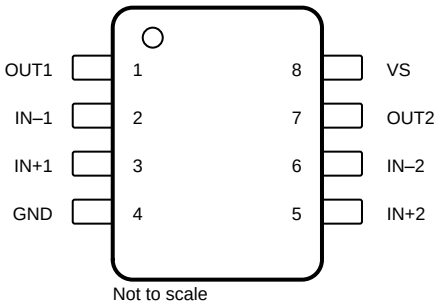

Not to scale

**Pin Functions: INA180-Q1 (Single Channel)**

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOT-23 Pinout A | SOT-23 Pinout B | | |
| GND | 2 | 2 | Analog | Ground |
| IN– | 4 | 3 | Analog input | Current-sense amplifier negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor. |
| IN+ | 3 | 1 | Analog input | Current-sense amplifier positive input. For high-side applications, connect to bus-voltage side of sense resistor. For low-side applications, connect to load side of sense resistor. |
| OUT | 1 | 4 | Analog output | Output voltage |
| VS | 5 | 5 | Analog | Power supply, 2.7 V to 5.5 V |

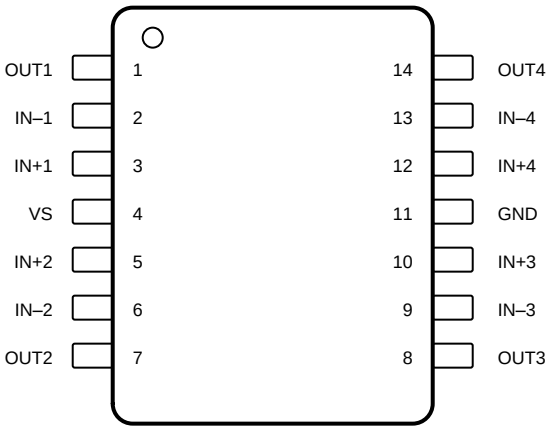
Copyright © 2018–2019, Texas Instruments Incorporated

**INA2180-Q1: DGK Package**
**8-Pin VSSOP**
**Top View**




Not to scale

**INA4180-Q1: PW Package**
**14-Pin TSSOP**
**Top View**




Not to scale

## Pin Functions: INA2180-Q1 (Dual Channel) and INA4180-Q1 (Quad Channel)

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | INA2180-Q1 | INA4180-Q1 | | |
| GND | 4 | 11 | Analog | Ground |
| IN–1 | 2 | 2 | Analog input | Current-sense amplifier negative input for channel 1. For high-side applications, connect to load side of channel-1 sense resistor. For low-side applications, connect to ground side of channel-1 sense resistor. |
| IN+1 | 3 | 3 | Analog input | Current-sense amplifier positive input for channel 1. For high-side applications, connect to bus-voltage side of channel-1 sense resistor. For low-side applications, connect to load side of channel-1 sense resistor. |
| IN–2 | 6 | 6 | Analog input | Current-sense amplifier negative input for channel 2. For high-side applications, connect to load side of channel-2 sense resistor. For low-side applications, connect to ground side of channel-2 sense resistor. |
| IN+2 | 5 | 5 | Analog input | Current-sense amplifier positive input for channel 2. For high-side applications, connect to bus-voltage side of channel-2 sense resistor. For low-side applications, connect to load side of channel-2 sense resistor. |
| IN–3 | — | 9 | Analog input | Current-sense amplifier negative input for channel 3. For high-side applications, connect to load side of channel-3 sense resistor. For low-side applications, connect to ground side of channel-3 sense resistor. |
| IN+3 | — | 10 | Analog input | Current-sense amplifier positive input for channel 3. For high-side applications, connect to bus-voltage side of channel-3 sense resistor. For low-side applications, connect to load side of channel-3 sense resistor. |
| IN–4 | — | 13 | Analog input | Current-sense amplifier negative input for channel 4. For high-side applications, connect to load side of channel-4 sense resistor. For low-side applications, connect to ground side of channel-4 sense resistor. |
| IN+4 | — | 12 | Analog input | Current-sense amplifier positive input for channel 4. For high-side applications, connect to bus-voltage side of channel-4 sense resistor. For low-side applications, connect to load side of channel-4 sense resistor. |
| OUT1 | 1 | 1 | Analog output | Channel 1 output voltage |
| OUT2 | 7 | 7 | Analog output | Channel 2 output voltage |
| OUT3 | — | 8 | Analog output | Channel 3 output voltage |
| OUT4 | — | 14 | Analog output | Channel 4 output voltage |
| VS | 8 | 4 | Analog | Power supply, 2.7 V to 5.5 V |


Copyright © 2018–2019, Texas Instruments Incorporated

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_S$ | | | 6 | V |
| Analog inputs, IN+, IN–(2)(3) | Differential ($V_{IN+}$) – ($V_{IN–}$) | –28 | 28 | V |
| | Common-mode(4) | GND – 0.3 | 28 | |
| Output voltage | | GND – 0.3 | $V_S$ + 0.3 | V |
| Maximum output current, $I_{OUT}$ | | | 8 | mA |
| Operating free-air temperature, $T_A$ | | –55 | 150 | °C |
| Junction temperature, $T_J$ | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) $V_{IN+}$ and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.
(3) Sustained operation between 26 V and 28 V for more than a few minutes may cause permanent damage to the device.
(4) Input voltage at any pin can exceed the voltage shown if the current at that pin is limited to 5 mA.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±3000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CM}$ | Common-mode input voltage (IN+ and IN–) | –0.2 | 12 | 26 | V |
| $V_S$ | Operating supply voltage | 2.7 | 5 | 5.5 | V |
| $T_A$ | Operating free-air temperature | –40 | | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC (1) | | INA180-Q1 DBV (SOT-23) 6 PINS | INA2180-Q1 DGK (VSSOP) 8 PINS | INA4180-Q1 PW (TSSOP) 20 PINS | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 197.1 | 177.9 | 115.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 95.8 | 65.6 | 44.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 53.1 | 99.3 | 59.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 23.4 | 10.5 | 4.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 52.7 | 97.9 | 58.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Copyright © 2018–2019, Texas Instruments Incorporated

## 7.5 Electrical Characteristics

at $T_A$ = 25°C, $V_S$ = 5 V, $V_{IN+}$ = 12 V, and $V_{SENSE}$ = $V_{IN+}$ – $V_{IN–}$ (unless otherwise noted)

| PARAMETER | | CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | |
| CMRR | Common-mode rejection ratio, RTI(1) | $V_{IN+}$ = 0 V to 26 V, $V_{SENSE}$ = 10 mV, $T_A$ = –40°C to +125°C | | 84 | 100 | | dB |
| $V_{OS}$ | Offset voltage(2), RTI | | | | ±100 | ±500 | µV |
| | | $V_{IN+}$ = 0 V | | | ±25 | ±150 | |
| $dV_{OS}/dT$ | Offset drift, RTI | $T_A$ = –40°C to +125°C | | | 0.2 | 1 | µV/°C |
| PSRR | Power-supply rejection ratio, RTI | $V_S$ = 2.7 V to 5.5 V, $V_{SENSE}$ = 10 mV | | | ±8 | ±40 | µV/V |
| $I_{IB}$ | Input bias current | $V_{SENSE}$ = 0 mV, $V_{IN+}$ = 0 V | | | 0.1 | | µA |
| | | $V_{SENSE}$ = 0 mV | | | 80 | | |
| $I_{IO}$ | Input offset current | $V_{SENSE}$ = 0 mV | | | ±0.05 | | µA |
| **OUTPUT** | | | | | | | |
| G | Gain | A1 devices | | | 20 | | V/V |
| | | A2 devices | | | 50 | | |
| | | A3 devices | | | 100 | | |
| | | A4 devices | | | 200 | | |
| $E_G$ | Gain error | $V_{OUT}$ = 0.5 V to $V_S$ – 0.5 V, $T_A$ = –40°C to +125°C | | | ±0.1% | ±1% | |
| | Gain error vs temperature | $T_A$ = –40°C to +125°C | | | 1.5 | 20 | ppm/°C |
| | Nonlinearity error | $V_{OUT}$ = 0.5 V to $V_S$ – 0.5 V | | | ±0.01% | | |
| | Maximum capacitive load | No sustained oscillation | | | 1 | | nF |
| **VOLTAGE OUTPUT(3)** | | | | | | | |
| $V_{SP}$ | Swing to $V_S$ power-supply rail(4) | $R_L$ = 10 kΩ to GND, $T_A$ = –40°C to +125°C | | | ($V_S$) – 0.02 | ($V_S$) – 0.03 | V |
| $V_{SN}$ | Swing to GND(4) | $R_L$ = 10 kΩ to GND, $T_A$ = –40°C to +125°C | | | ($V_{GND}$) + 0.0005 | ($V_{GND}$) + 0.005 | V |
| **FREQUENCY RESPONSE** | | | | | | | |
| BW | Bandwidth | A1 devices, $C_{LOAD}$ = 10 pF | | | 350 | | kHz |
| | | A2 devices, $C_{LOAD}$ = 10 pF | | | 210 | | |
| | | A3 devices, $C_{LOAD}$ = 10 pF | | | 150 | | |
| | | A4 devices, $C_{LOAD}$ = 10 pF | | | 105 | | |
| SR | Slew rate | | | | 2 | | V/µs |
| **NOISE, RTI** | | | | | | | |
| | Voltage noise density | | | | 40 | | nV/√Hz |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current | INA180-Q1 | $V_{SENSE}$ = 10 mV | | 197 | 260 | µA |
| | | | $V_{SENSE}$ = 10 mV, $T_A$ = –40°C to +125°C | | | 300 | |
| | | INA2180-Q1 | $V_{SENSE}$ = 10 mV | | 355 | 500 | |
| | | | $V_{SENSE}$ = 10 mV, $T_A$ = –40°C to +125°C | | | 520 | |
| | | INA4180-Q1 | $V_{SENSE}$ = 10 mV | | 690 | 900 | |
| | | | $V_{SENSE}$ = 10 mV, $T_A$ = –40°C to +125°C | | | 1000 | |

(1) RTI = referred-to-input.
(2) Offset voltage is obtained by linear extrapolation to $V_{SENSE}$ = 0 V with $V_{SENSE}$ = 10% to 90% of full-scale-range.
(3) See 图 19.
(4) Swing specifications are tested with an overdriven input condition.


版权 © 2018–2019, Texas Instruments Incorporated

## 7.6 Typical Characteristics

at $T_A$ = 25°C, $V_S$ = 5 V, and $V_{IN+}$ = 12 V (unless otherwise noted)

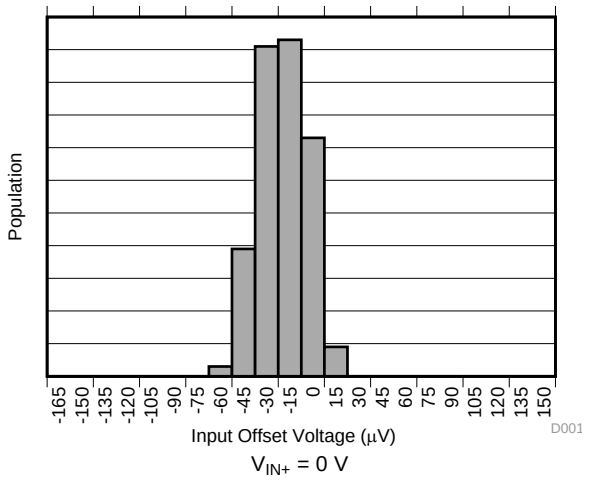



**图 1. Input Offset Voltage Production Distribution A1**

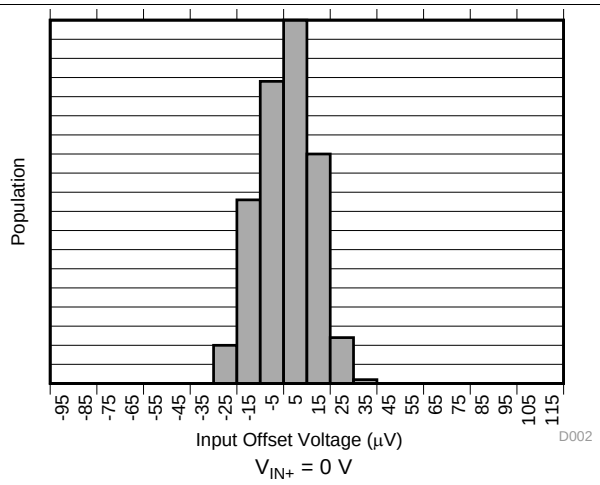



**图 2. Input Offset Voltage Production Distribution A2**

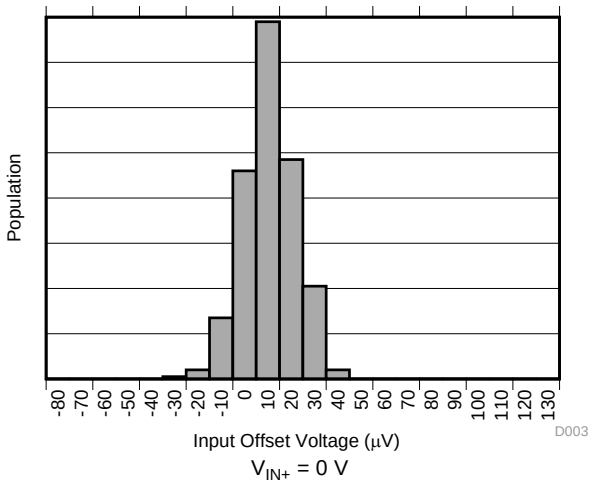



**图 3. Input Offset Voltage Production Distribution A3**

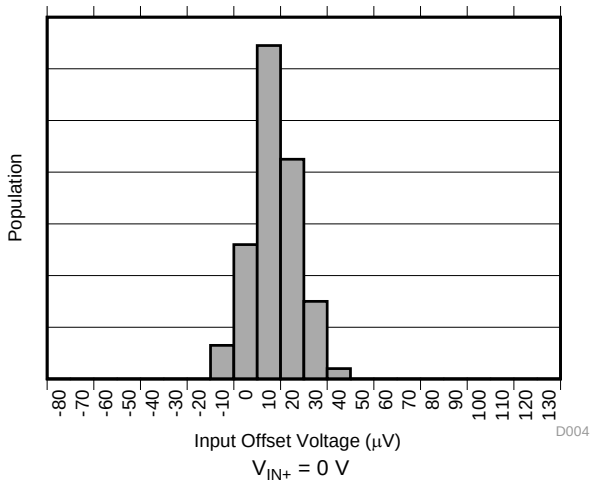



**图 4. Input Offset Voltage Production Distribution A4**

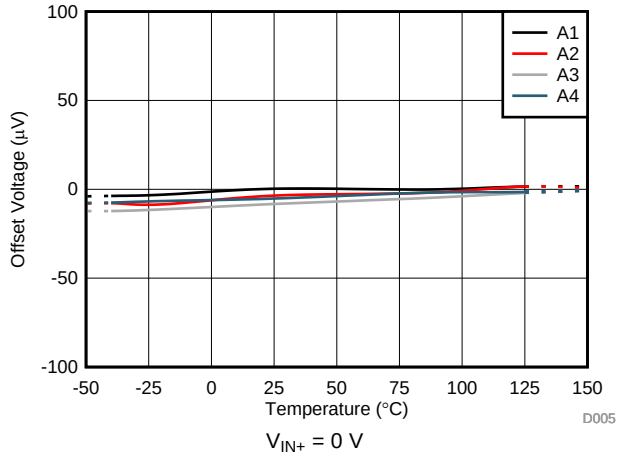



**图 5. Offset Voltage vs Temperature**

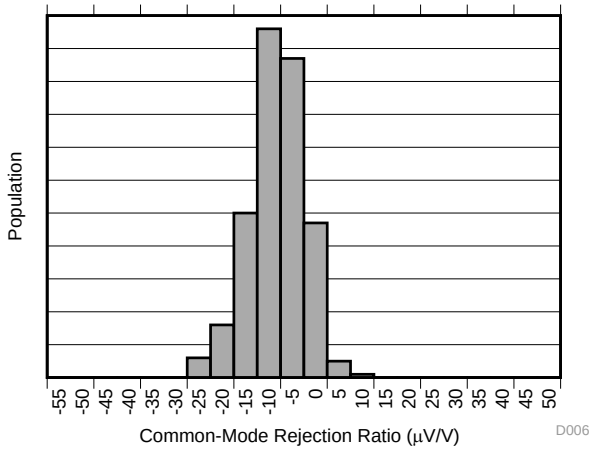



**图 6. Common-Mode Rejection Production Distribution A1**

## Typical Characteristics (接下页)

at $T_A$ = 25°C, $V_S$ = 5 V, and $V_{IN+}$ = 12 V (unless otherwise noted)

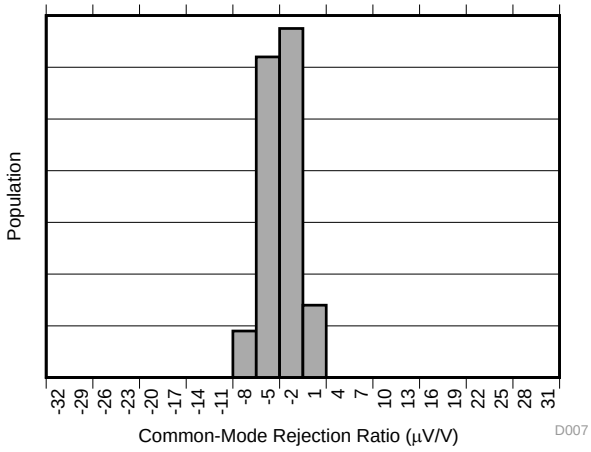



图 7. Common-Mode Rejection Production Distribution A2

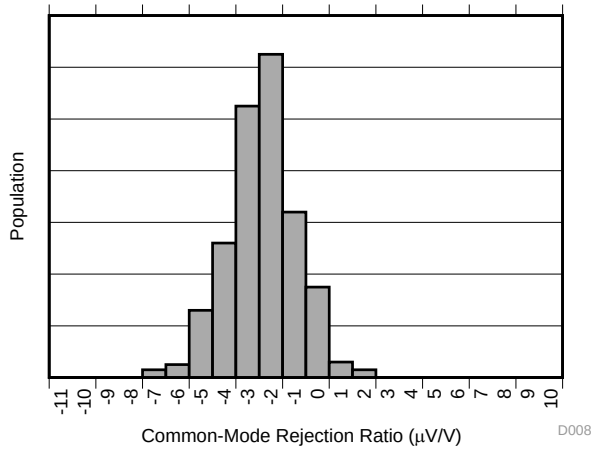



图 8. Common-Mode Rejection Production Distribution A3

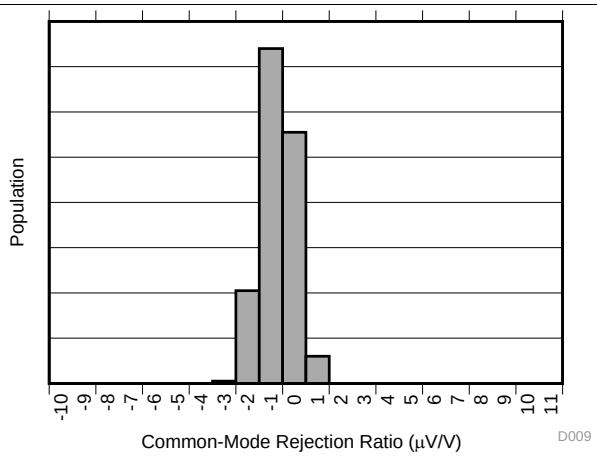



图 9. Common-Mode Rejection Production Distribution A4

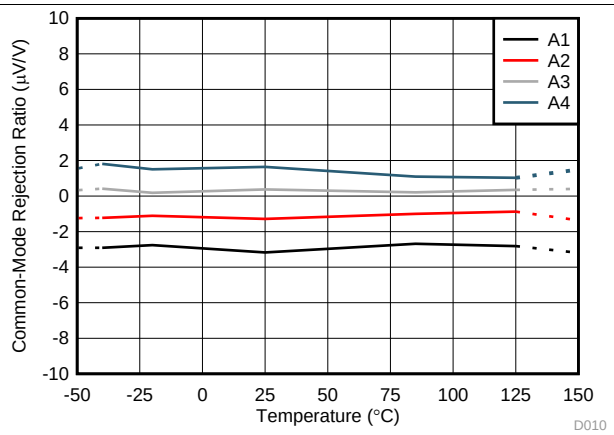



图 10. Common-Mode Rejection Ratio vs Temperature

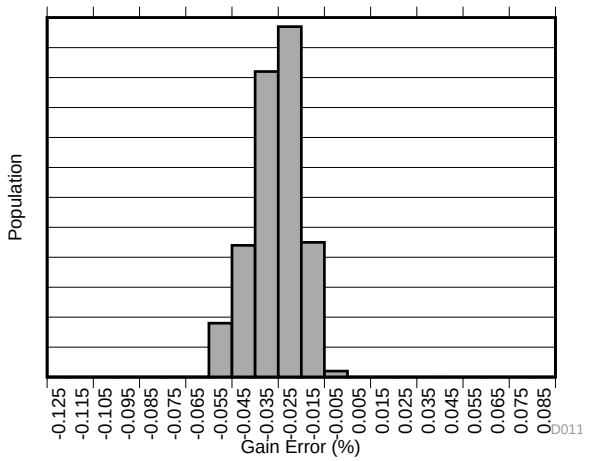



图 11. Gain Error Production Distribution A1

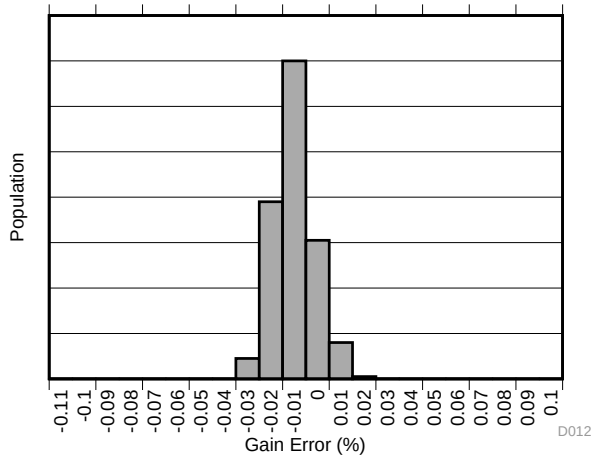



图 12. Gain Error Production Distribution A2


版权 © 2018–2019, Texas Instruments Incorporated

## Typical Characteristics (接下页)

at $T_A$ = 25°C, $V_S$ = 5 V, and $V_{IN+}$ = 12 V (unless otherwise noted)

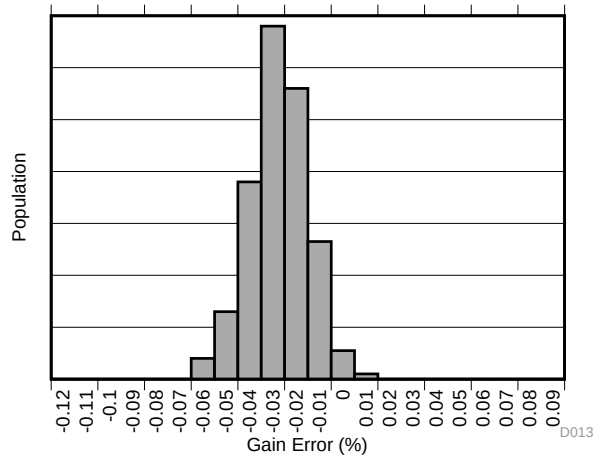



图 13. Gain Error Production Distribution A3

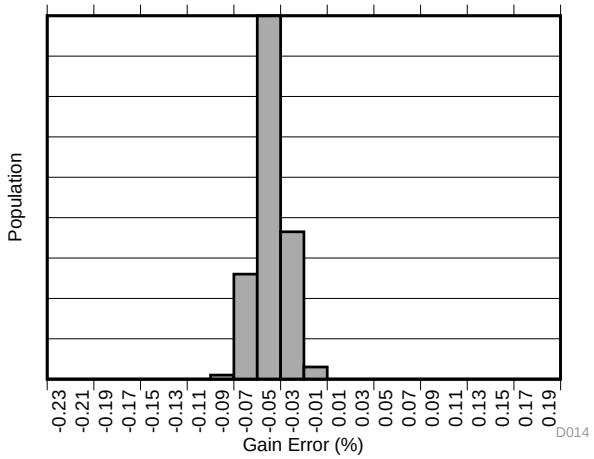



图 14. Gain Error Production Distribution A4

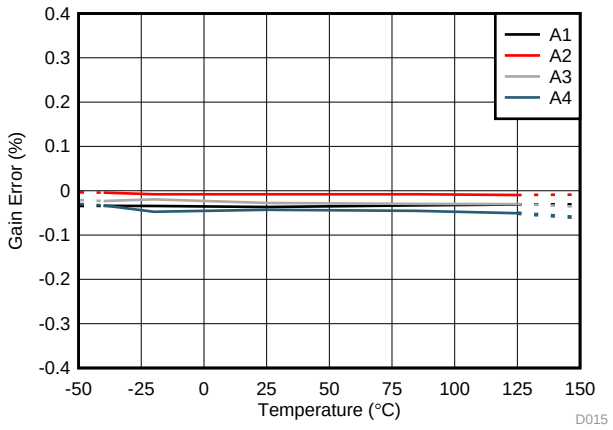



图 15. Gain Error vs Temperature

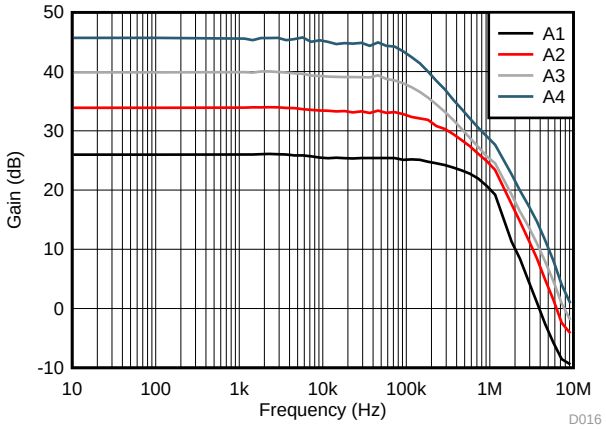



图 16. Gain vs Frequency

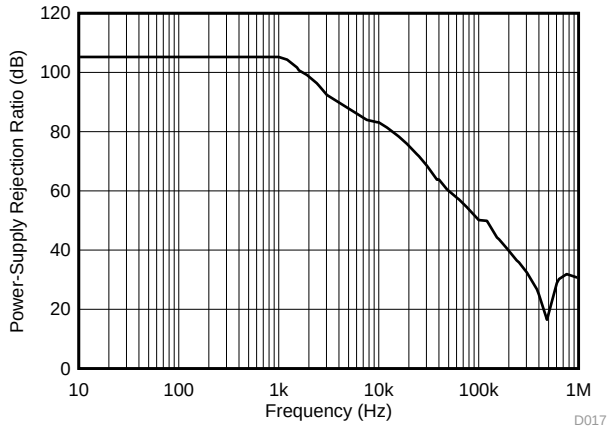



图 17. Power-Supply Rejection Ratio vs Frequency

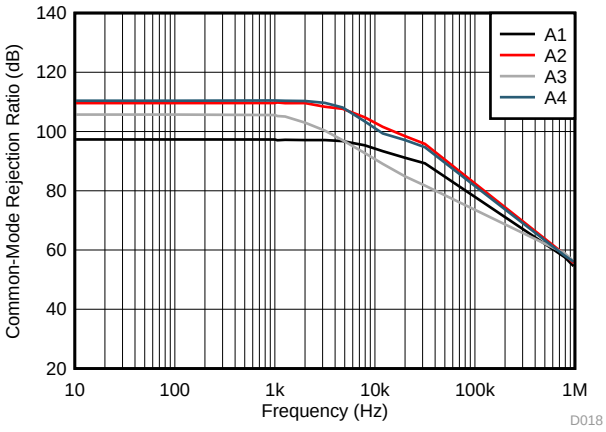



图 18. Common-Mode Rejection Ratio vs Frequency

## Typical Characteristics (接下页)

at $T_A$ = 25°C, $V_S$ = 5 V, and $V_{IN+}$ = 12 V (unless otherwise noted)

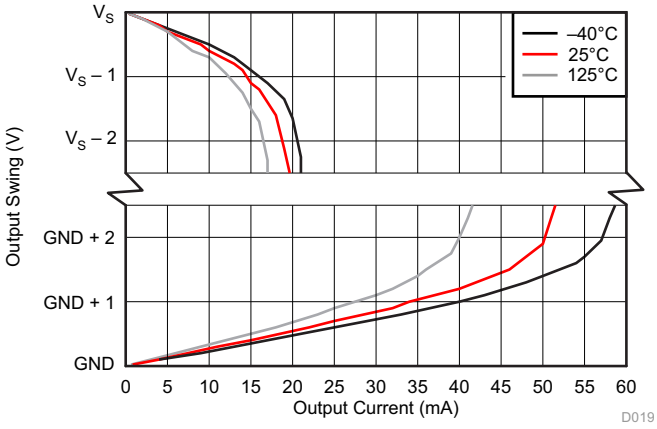



图 19. Output Voltage Swing vs Output Current

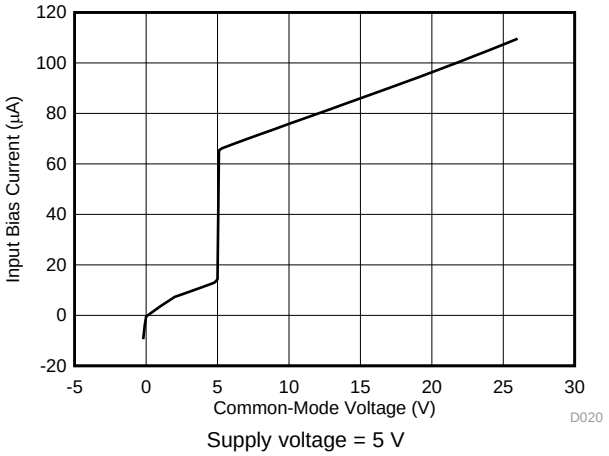



图 20. Input Bias Current vs Common-Mode Voltage

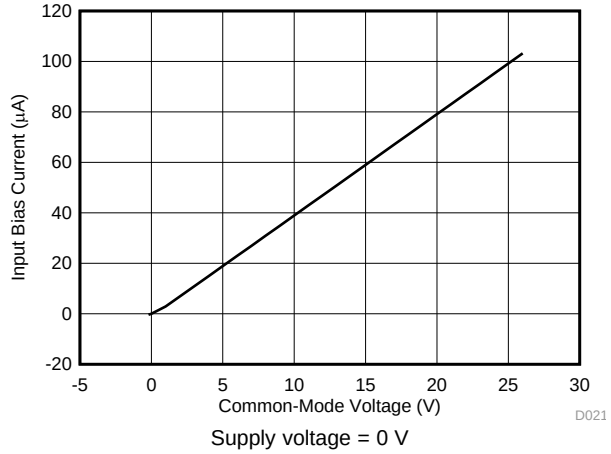



图 21. Input Bias Current vs Common-Mode Voltage (Both Inputs, Shutdown)

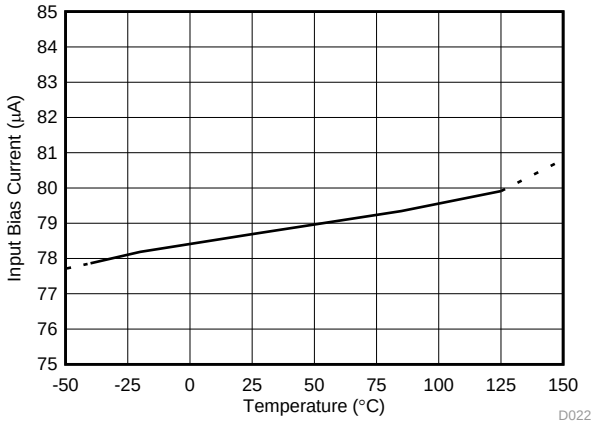



图 22. Input Bias Current vs Temperature

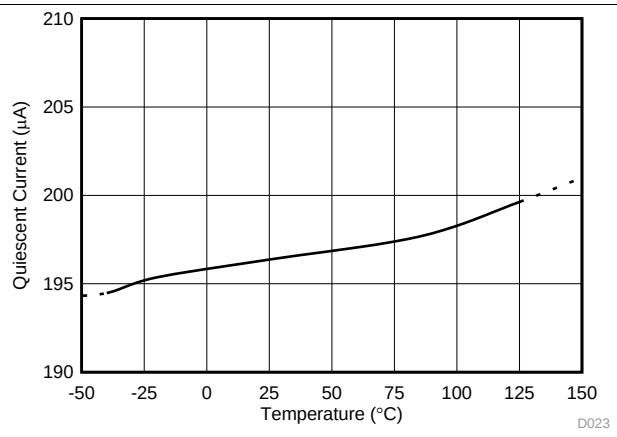



图 23. Quiescent Current vs Temperature (INA180-Q1)

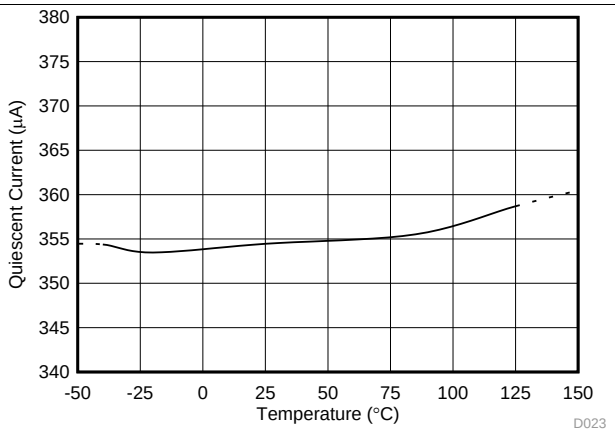



图 24. Quiescent Current vs Temperature (INA2180-Q1)


版权 © 2018–2019, Texas Instruments Incorporated

## Typical Characteristics (接下页)

at $T_A$ = 25°C, $V_S$ = 5 V, and $V_{IN+}$ = 12 V (unless otherwise noted)

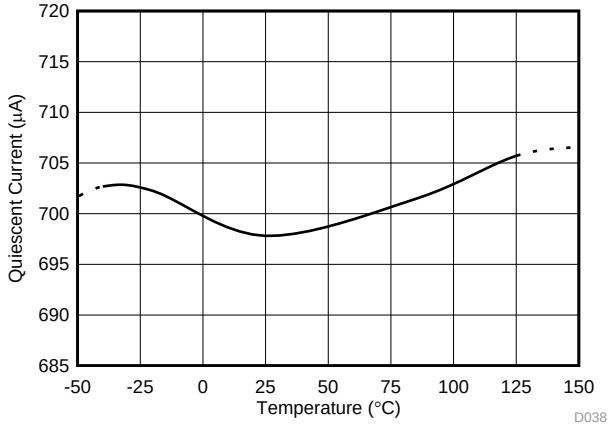



**图 25. Quiescent Current vs Temperature (INA4180-Q1)**

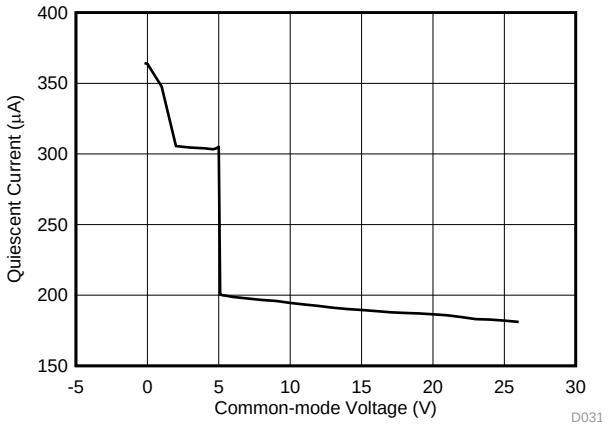



**图 26. Quiescent Current vs Common-Mode Voltage (INA180-Q1)**

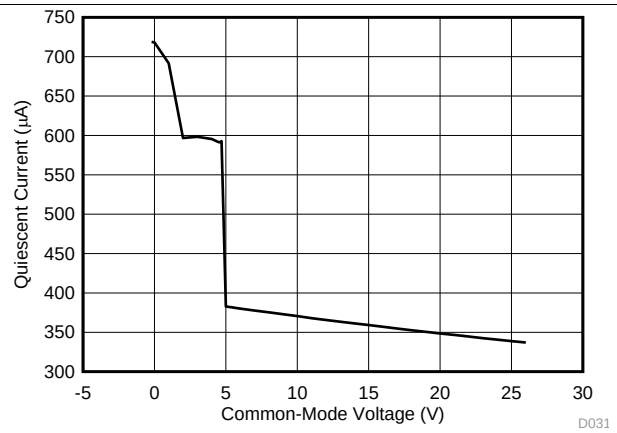



**图 27. Quiescent Current vs Common-Mode Voltage for All Amplifiers (INA2180-Q1)**

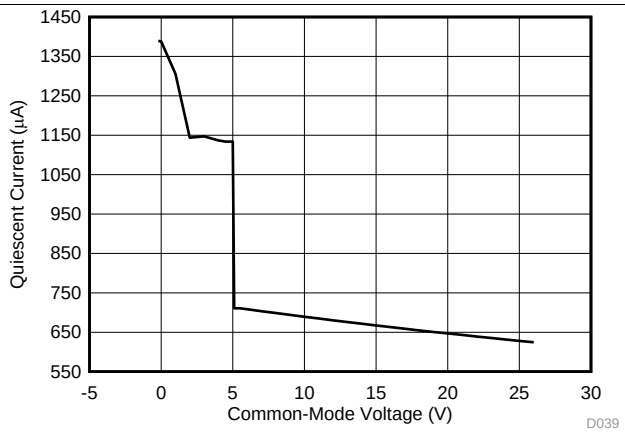



**图 28. Quiescent Current vs Common-Mode Voltage for All Amplifiers (INA4180-Q1)**

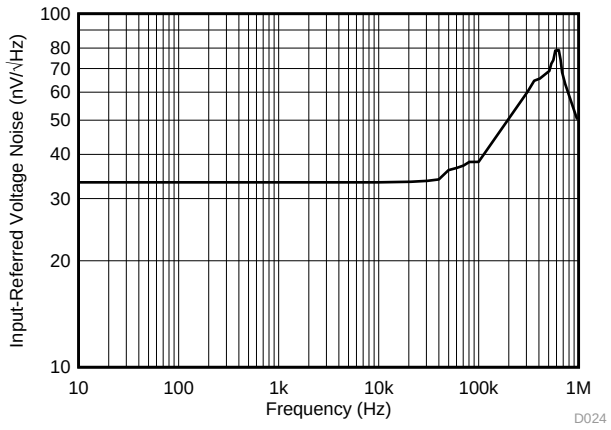



**图 29. Input-Referred Voltage Noise vs Frequency (A3 Devices)**

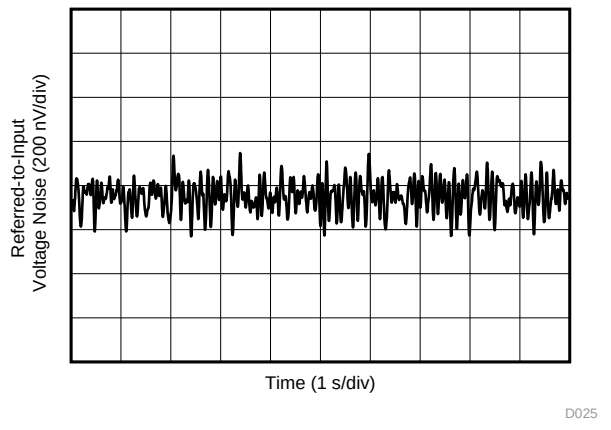
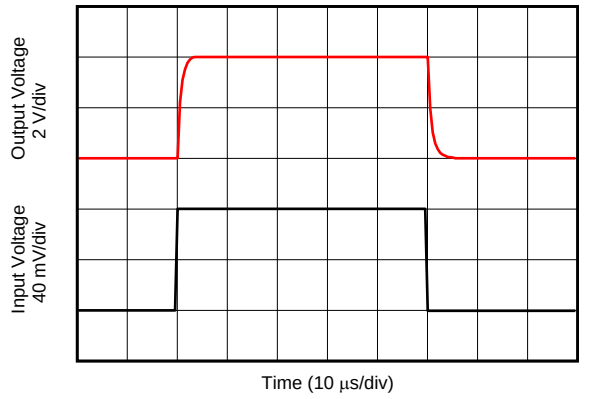



**图 30. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)**

## Typical Characteristics (接下页)

at $T_A$ = 25°C, $V_S$ = 5 V, and $V_{IN+}$ = 12 V (unless otherwise noted)




80-$mV_{PP}$ input step

**图 31. Step Response**

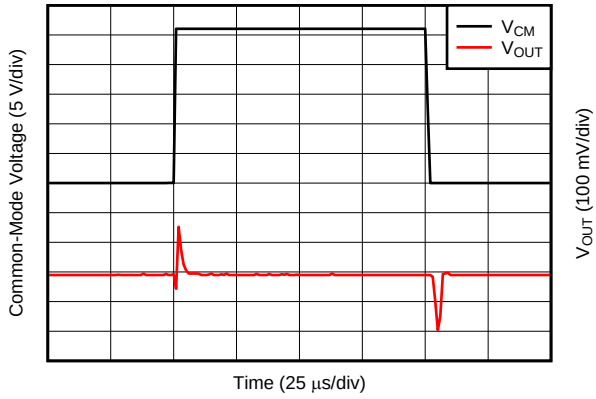



**图 32. Common-Mode Voltage Transient Response**

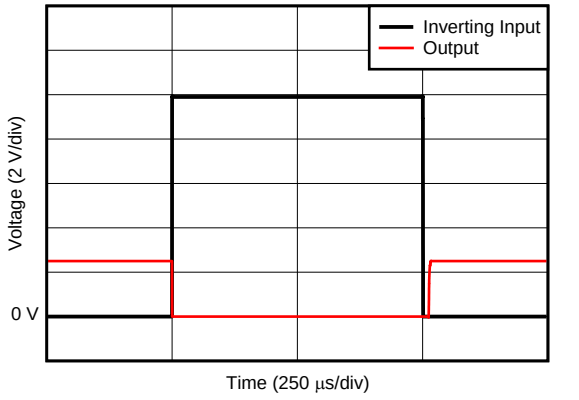



**图 33. Inverting Differential Input Overload**

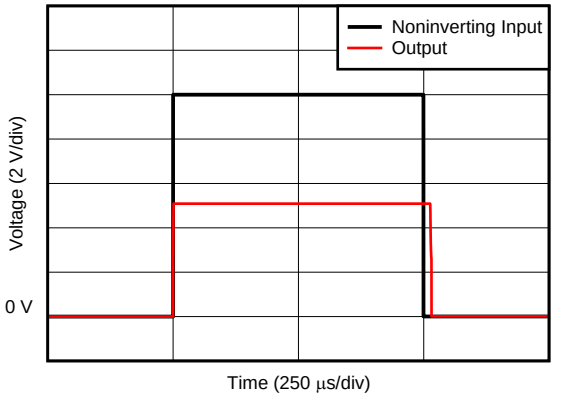



**图 34. Noninverting Differential Input Overload**

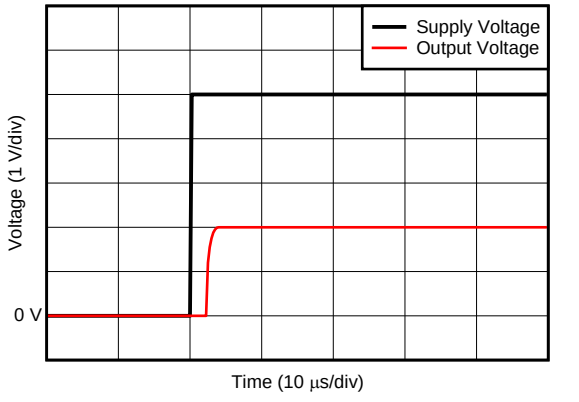



**图 35. Start-Up Response**

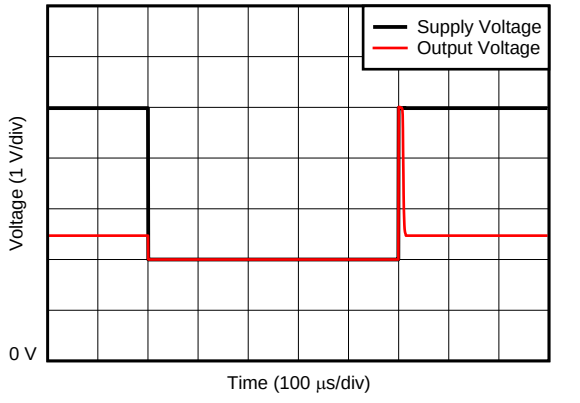



**图 36. Brownout Recovery**


版权 © 2018–2019, Texas Instruments Incorporated

## Typical Characteristics (接下页)

at $T_A$ = 25°C, $V_S$ = 5 V, and $V_{IN+}$ = 12 V (unless otherwise noted)

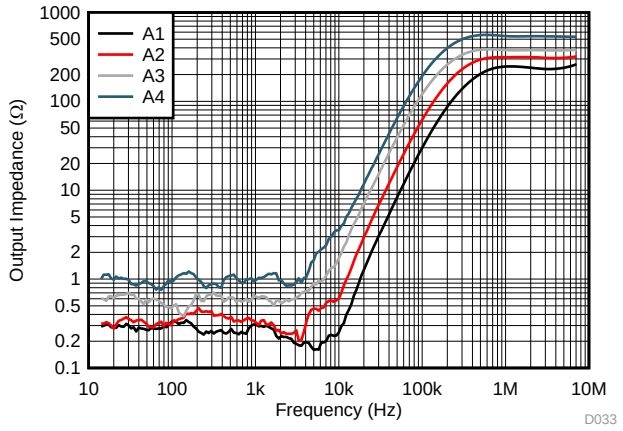



**图 37. Output Impedance vs Frequency**

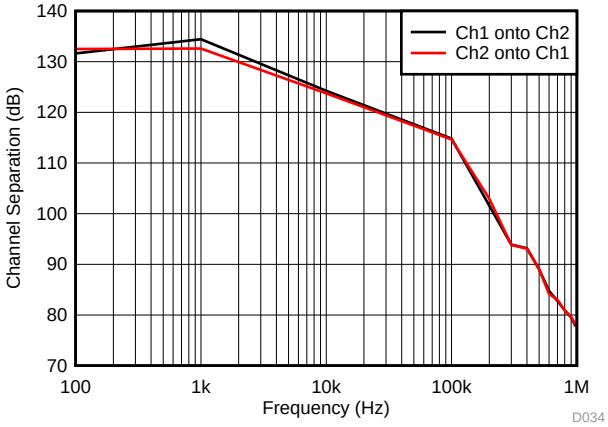



**图 38. Channel Separation vs Frequency (INA2180)**

# 8 Detailed Description

## 8.1 Overview

The INA180-Q1, INA2180-Q1, and INA4180-Q1 (INAx180-Q1) are automotive-grade, 26-V, common-mode, current-sensing amplifiers used in both low-side and high-side configurations. These specially-designed, current-sensing amplifiers accurately measures voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 26 V, and the devices can be powered from supply voltages as low as 2.7 V.

## 8.2 Functional Block Diagrams

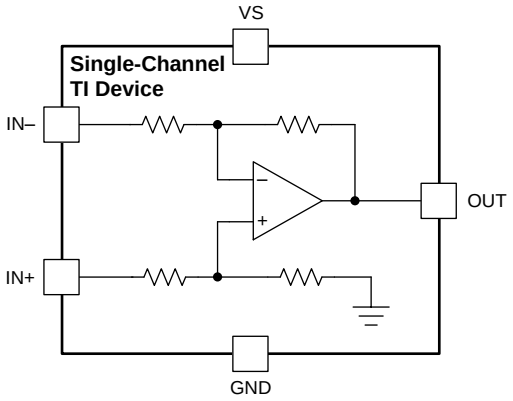



**图 39. INA180-Q1 Functional Block Diagram**

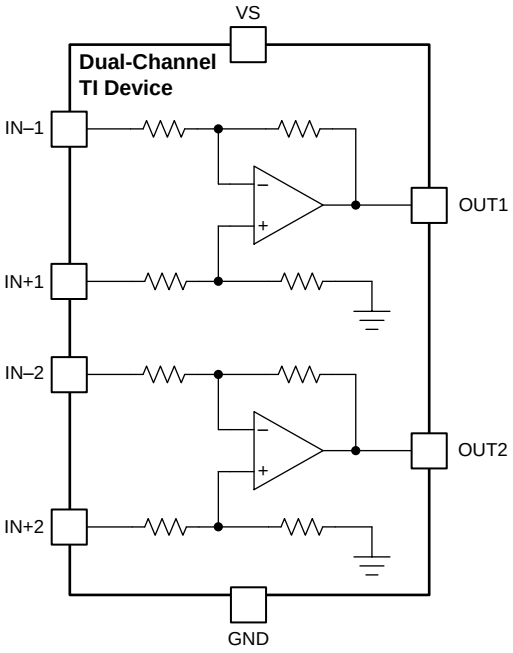



**图 40. INA2180-Q1 Functional Block Diagram**


版权 © 2018–2019, Texas Instruments Incorporated

## Functional Block Diagrams (接下页)

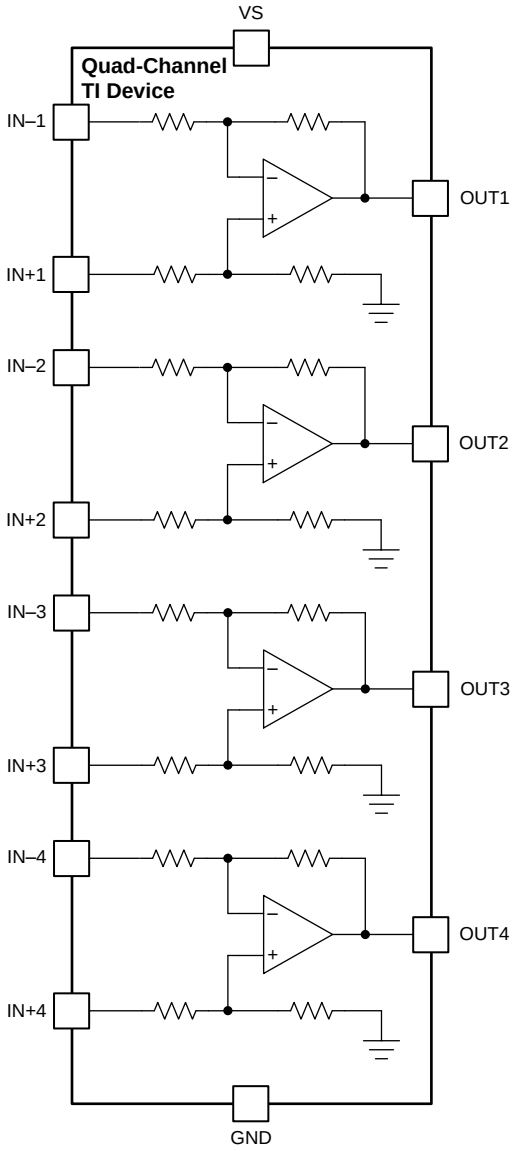



**图 41. INA4180-Q1 Functional Block Diagram**

## 8.3 Feature Description

### 8.3.1 High Bandwidth and Slew Rate

The INAx180-Q1 support small-signal bandwidths as high as 350 kHz, and large-signal slew rates of 2 V/µs. The ability to detect rapid changes in the sensed current, as well as the ability to quickly slew the output, make the INAx180-Q1 a good choice for applications that require a quick response to input current changes. One application that requires high bandwidth and slew rate is low-side motor control, where the ability to follow rapid changing current in the motor allows for more accurate control over a wider operating range. Another application that requires higher bandwidth and slew rates is system fault detection, where the INAx180-Q1 are used with an external comparator and a reference to quickly detect when the sensed current is out of range.

### 8.3.2 Wide Input Common-Mode Voltage Range

The INAx180-Q1 support input common-mode voltages from –0.2 V to +26 V. Because of the internal topology, the common-mode range is not restricted by the power-supply voltage ($V_S$) as long as $V_S$ stays within the operational range of 2.7 V to 5.5 V. The ability to operate with common-mode voltages greater or less than $V_S$ allow the INAx180-Q1 to be used in high-side, as well as low-side, current-sensing applications, as shown in 图 42.

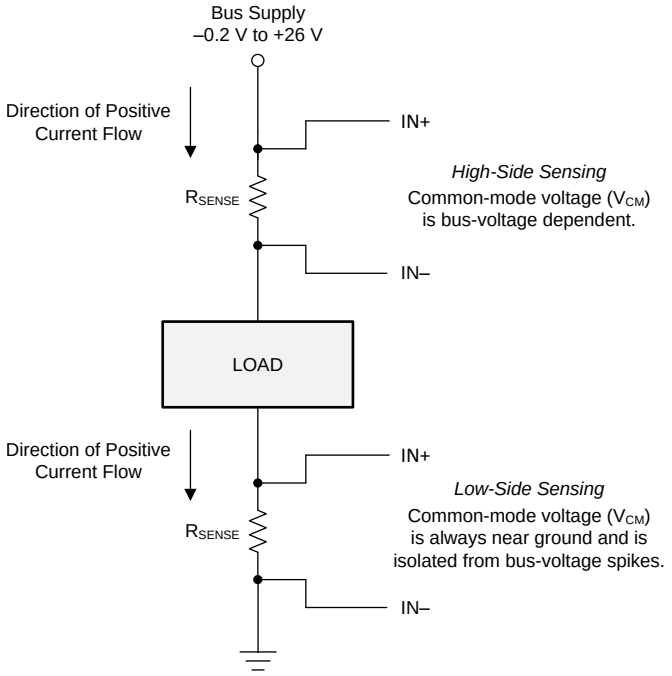



**图 42. High-Side and Low-Side Sensing Connections**

### 8.3.3 Precise Low-Side Current Sensing

When used in low-side current sensing applications the offset voltage of the INAx180-Q1 is within ±150 µV. The low offset performance of the INAx180-Q1 has several benefits. First, the low offset allows the device to be used in applications that must measure current over a wide dynamic range. In this case, the low offset improves the accuracy when the sensed currents are on the low end of the measurement range. Another advantage of low offset is the ability to sense lower voltage drop across the sense resistor accurately, thus allowing a lower-value shunt resistor. Lower-value shunt resistors reduce power loss in the current sense circuit, and help improve the power efficiency of the end application.

The gain error of the INAx180-Q1 is specified to be within 1% of the actual value. As the sensed voltage becomes much larger than the offset voltage, this voltage becomes the dominant source of error in the current sense measurement.


版权 © 2018–2019, Texas Instruments Incorporated

## Feature Description (接下页)

### 8.3.4 Rail-to-Rail Output Swing

The INAx180-Q1 allow linear current sensing operation with the output close to the supply rail and GND. The maximum specified output swing to the positive rail is 30 mV, and the maximum specified output swing to GND is only 5 mV. In order to compare the output swing of the INAx180-Q1 to an equivalent operational amplifier (op amp), the inputs are overdriven to approximate the open-loop condition specified in op amp data sheets. The current-sense amplifier is a closed-loop system; therefore, the output swing to GND can be limited by the product of the offset voltage and amplifier gain.

For devices that have positive offset voltages, the swing to GND is limited by the larger of either the offset voltage multiplied by the gain or the swing to GND specified in the *Electrical Characteristics* table.

For example, in an application where the INA180A4-Q1 (gain = 200 V/V) is used for low-side current sensing and the device has an offset of 40 µV, the product of the device offset and gain results in a value of 8 mV, greater than the specified negative swing value. Therefore, the swing to GND for this example is 8 mV. If the same device has an offset of –40 µV, then the calculated zero differential signal is –8 mV. In this case, the offset helps overdrive the swing in the negative direction, and swing performance is consistent with the value specified in the *Electrical Characteristics* table.

The offset voltage is a function of the common-mode voltage as determined by the CMRR specification; therefore, the offset voltage increases when higher common-mode voltages are present. The increase in offset voltage limits how low the output voltage can go during a zero-current condition when operating at higher common-mode voltages. 图 43 shows the typical limitation of the zero-current output voltage vs common-mode voltage for each gain option.

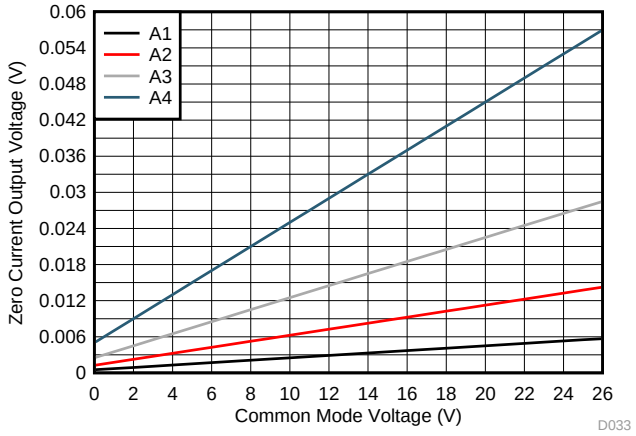



**图 43. Zero-Current Output Voltage vs Common-Mode Voltage**

## 8.4 Device Functional Modes

### 8.4.1 Normal Mode

The INAx180-Q1 is in normal operation when the following conditions are met:

- The power supply voltage ($V_S$) is between 2.7 V and 5.5 V.
- The common-mode voltage ($V_{CM}$) is within the specified range of –0.2 V to +26 V.
- The maximum differential input signal times gain is less than $V_S$ minus the output voltage swing to $V_S$.
- The minimum differential input signal times gain is greater than the swing to GND (see the *Rail-to-Rail Output Swing* section).

During normal operation, the device produces an output voltage that is the *gained-up* representation of the difference voltage from IN+ to IN–.

## Device Functional Modes (接下页)

### 8.4.2 Input Differential Overload

If the differential input voltage ($V_{IN+}$ – $V_{IN–}$) times gain exceeds the voltage swing specification, the INAx180-Q1 drive the output as close as possible to the positive supply, and does not provide accurate measurement of the differential input voltage. If this input overload occurs during normal circuit operation, then reduce the value of the shunt resistor or use a lower-gain version with the chosen sense resistor to avoid this mode of operation. If a differential overload occurs in a fault event, then the output of the INAx180-Q1 return to the expected value approximately 20 µs after the fault condition is removed.

When the INAx180-Q1 output is driven to either the supply rail or ground, increasing the differential input voltage does not damage the device as long as the absolute maximum ratings are not violated. Following these guidelines, the INAx180-Q1 output maintains polarity, and does not suffer from phase reversal.

### 8.4.3 Shutdown Mode

Although the INAx180-Q1 do not have a shutdown pin, the low power consumption of the device allows the output of a logic gate or transistor switch to power the INAx180-Q1. This gate or switch turns on and off the INAx180-Q1 power-supply quiescent current.

However, in current shunt monitoring applications, there is also a concern for how much current is drained from the shunt circuit in shutdown conditions. Evaluating this current drain involves considering the simplified schematic of the INAx180-Q1 in shutdown mode, as shown in 图 44.

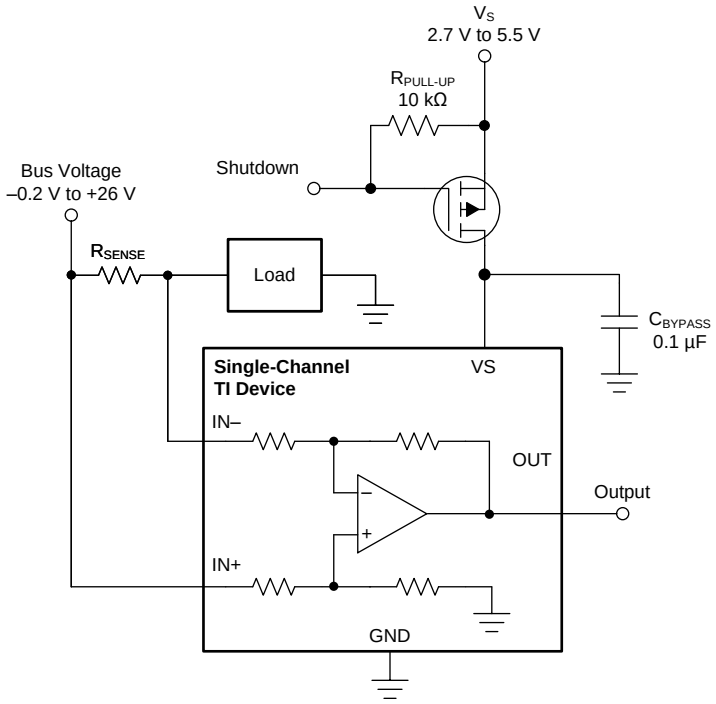



**图 44. Basic Circuit to Shut Down the INxA180-Q1**

There is typically more than 500 kΩ of impedance (from the combination of 500-kΩ feedback and input gain set resistors) from each input of the INAx180-Q1 to the OUT pin and to the GND pin. The amount of current flowing through these pins depends on the voltage at the connection.

Regarding the 500-kΩ path to the output pin, the output stage of a disabled INAx180-Q1 does constitute a good path to ground. Consequently, this current is directly proportional to a shunt common-mode voltage present across a 500-kΩ resistor.

As a final note, as long as the shunt common-mode voltage is greater than $V_S$ when the device is powered up, there is an additional and well-matched 55-µA typical current that flows in each of the inputs. If less than $V_S$, the common-mode input currents are negligible, and the only current effects are the result of the 500-kΩ resistors.


版权 © 2018–2019, Texas Instruments Incorporated

# 9 Application and Implementation

**注**

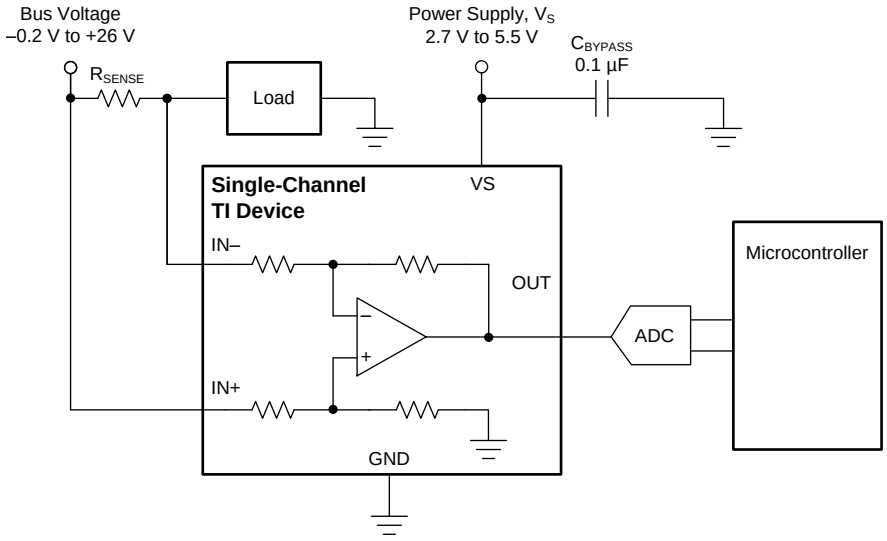
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The INAx180-Q1 amplify the voltage developed across a current-sensing resistor as current flows through the resistor to the load or ground.

### 9.1.1 Basic Connections

图 45 shows the basic connections of the INA180-Q1. Connect the input pins (IN+ and IN–) as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.




NOTE: For best measurement accuracy, connect analog-to-digital converter (ADC) reference or microcontroller ground as closely as possible to the INAx180-Q1 GND pin, and add an RC filter between the output of the INAx180-Q1 and the ADC. See *Closed-Loop Analysis of Load-Induced Amplifier Stability Issues Using $Z_{OUT}$* for more details.

**图 45. Basic Connections for the INA180**

A power-supply bypass capacitor of at least 0.1 µF is required for proper operation. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

## Application Information (接下页)

### 9.1.2 $R_{SENSE}$ and Device Gain Selection

The accuracy of the INAx180-Q1 is maximized by choosing the current-sense resistor to be as large as possible. A large sense resistor maximizes the differential input signal for a given amount of current flow and reduces the error contribution of the offset voltage. However, there are practical limits as to how large the current-sense resistor can be in a given application. The INAx180-Q1 have a typical input bias currents of 80 µA for each input when operated at a 12-V common-mode voltage input. When large current-sense resistors are used, these bias currents cause increased offset error and reduced common-mode rejection. Therefore, using current-sense resistors larger than a few ohms is generally not recommended for applications that require current-monitoring accuracy. A second common restriction on the value of the current-sense resistor is the maximum allowable power dissipation that is budgeted for the resistor. 公式 1 gives the maximum value for the current sense resistor for a given power dissipation budget:

$$R_{SENSE} < \frac{PD_{MAX}}{I_{MAX}^2} \quad (1)$$

where:

- $PD_{MAX}$ is the maximum allowable power dissipation in $R_{SENSE}$.
- $I_{MAX}$ is the maximum current that will flow through $R_{SENSE}$.

An additional limitation on the size of the current-sense resistor and device gain is due to the power-supply voltage, $V_S$, and device swing to rail limitations. In order to make sure that the current-sense signal is properly passed to the output, both positive and negative output swing limitations must be examined. 公式 2 provides the maximum values of $R_{SENSE}$ and GAIN to keep the device from hitting the positive swing limitation.

$$I_{MAX} \times R_{SENSE} \times GAIN < V_{SP} \quad (2)$$

where:

- $I_{MAX}$ is the maximum current that will flow through $R_{SENSE}$.
- GAIN is the gain of the current sense-amplifier.
- $V_{SP}$ is the positive output swing as specified in the data sheet.

To avoid positive output swing limitations when selecting the value of $R_{SENSE}$, there is always a trade-off between the value of the sense resistor and the gain of the device under consideration. If the sense resistor selected for the maximum power dissipation is too large, then it is possible to select a lower-gain device in order to avoid positive swing limitations.

The negative swing limitation places a limit on how small of a sense resistor can be used in a given application. 公式 3 provides the limit on the minimum size of the sense resistor.

$$I_{MIN} \times R_{SENSE} \times GAIN > V_{SN} \quad (3)$$

where:

- $I_{MIN}$ is the minimum current that will flow through $R_{SENSE}$.
- GAIN is the gain of the current sense amplifier.
- $V_{SN}$ is the negative output swing of the device (see Rail-to-Rail Output Swing).


版权 © 2018–2019, Texas Instruments Incorporated

## Application Information (接下页)

### 9.1.3 Signal Filtering

Provided that the INAx180-Q1 output is connected to a high impedance input, the best location to filter is at the device output using a simple RC network from OUT to GND. Filtering at the output attenuates high-frequency disturbances in the common-mode voltage, differential input signal, and INAx180-Q1 power-supply voltage. If filtering at the output is not possible, or filtering of only the differential input signal is required, it is possible to apply a filter at the input pins of the device. 图 46 provides an example of how a filter can be used on the input pins of the device.

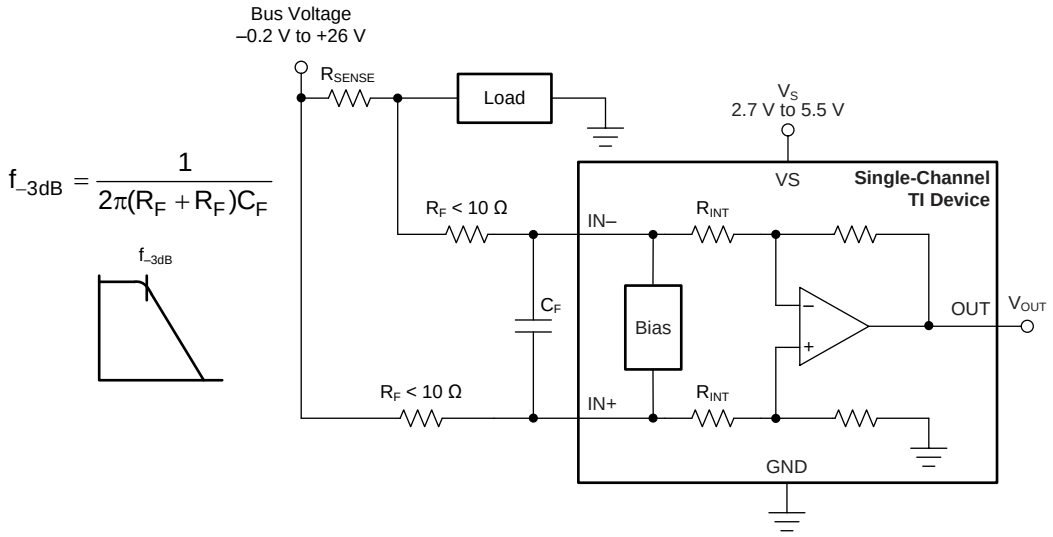



**图 46. Filter at Input Pins**

The addition of external series resistance creates an additional error in the measurement; therefore, the value of these series resistors must be kept to 10 Ω (or less, if possible) to reduce impact to accuracy. The internal bias network shown in 图 46 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed across the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistors add to the measurement can be calculated using 公式 5, where the gain error factor is calculated using 公式 4.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance ($R_F$) value as well as internal input resistor $R_{INT}$, as shown in 图 46. The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. Calculate the expected deviation from the shunt voltage to what is measured at the device input pins is given using 公式 4:

$$\text{Gain Error Factor} = \frac{1250 \times R_{INT}}{(1250 \times R_F) + (1250 \times R_{INT}) + (R_F \times R_{INT})} \quad (4)$$

where:

- $R_{INT}$ is the internal input resistor.
- $R_F$ is the external series resistance.

## Application Information (接下页)

With the adjustment factor from 公式 4, including the device internal input resistance, this factor varies with each gain version, as shown in 表 1. Each individual device gain error factor is shown in 表 2.

**表 1. Input Resistance**

| PRODUCT | GAIN | $R_{INT}$ (kΩ) |
|---|---|---|
| INAx180A1-Q1 | 20 | 25 |
| INAx180A2-Q1 | 50 | 10 |
| INAx180A3-Q1 | 100 | 5 |
| INAx180A4-Q1 | 200 | 2.5 |

**表 2. Device Gain Error Factor**

| PRODUCT | SIMPLIFIED GAIN ERROR FACTOR |
|---|---|
| INAx180A1-Q1 | $\frac{25000}{(21 \times R_F) + 25000}$ |
| INAx180A2-Q1 | $\frac{10000}{(9 \times R_F) + 10000}$ |
| INAx180A3-Q1 | $\frac{1000}{R_F + 1000}$ |
| INAx180A4-Q1 | $\frac{2500}{(3 \times R_F) + 2500}$ |

The gain error that can be expected from the addition of the external series resistors can then be calculated based on 公式 5:

$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (5)$$

For example, using an INA180A2-Q1 and the corresponding gain error equation from 表 2, a series resistance of 10 Ω results in a gain error factor of 0.991. The corresponding gain error is then calculated using 公式 5, resulting in an additional gain error of approximately 0.89% solely because of the external 10-Ω series resistors.


版权 © 2018–2019, Texas Instruments Incorporated

## 9.2 Typical Application

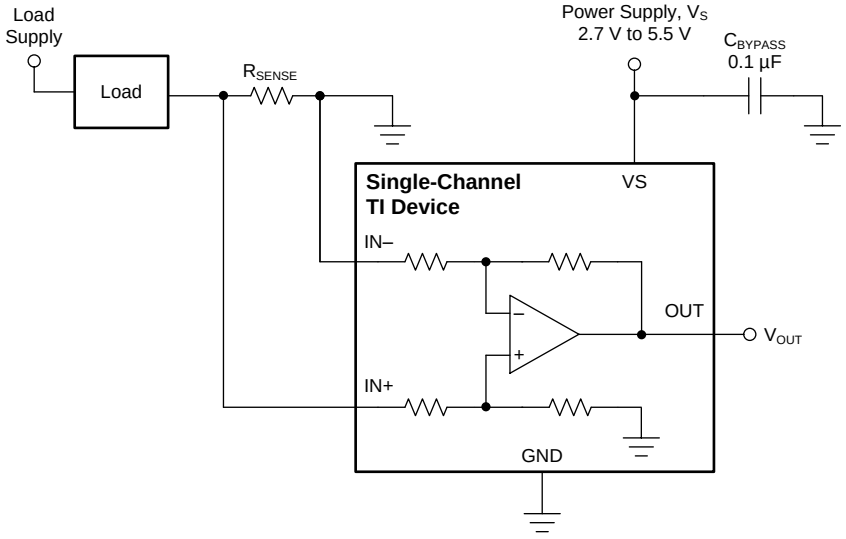



**图 47. Low-Side Sensing**

### 9.2.1 Design Requirements

The design requirements for the circuit shown in 图 47, are listed in 表 3

**表 3. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Power-supply voltage, $V_S$ | 5 V |
| Low-side current sensing | $V_{CM}$ = 0 V |
| $R_{SENSE}$ power loss | < 900 mW |
| Maximum sense current, $I_{MAX}$ | 40 A |
| Current sensing error | Less than 1.5% at maximum current, $T_J$ = 25°C |
| Small-signal bandwidth | > 80 kHz |

### 9.2.2 Detailed Design Procedure

The maximum value of the current sense resistor is calculated based on the maximum power loss requirement. By applying 公式 1, the maximum value of the current-sense resistor is calculated to be 0.563 mΩ. This is the maximum value for sense resistor $R_{SENSE}$; therefore, select $R_{SENSE}$ to be 0.5 mΩ because it is the closest standard resistor value that meets the power-loss requirement.

The next step is to select the appropriate gain and reduce $R_{SENSE}$, if needed, to keep the output signal swing within the $V_S$ range. Using 公式 2, and given that $I_{MAX}$ = 40 A and $R_{SENSE}$ = 0.5 mΩ, the maximum current-sense gain calculated to avoid the positive swing-to-rail limitations on the output is 248.5. To maximize the output signal range, the INA180A4-Q1 (gain = 200) device is selected for this application.

To calculate the accuracy at peak current, the two factors that must be determined are the gain error and the offset error. The gain error of the INAx180-Q1 is specified to be a maximum of 1%. The error due to the offset is constant, and is specified to be 125 µV (maximum) for the conditions where $V_{CM}$ = 0 V and $V_S$ = 5 V. Using 公式 6, the percentage error contribution of the offset voltage is calculated to be 0.75%, with total offset error = 150 µV, $R_{SENSE}$ = 0.5 mΩ, and $I_{SENSE}$ = 40 A.

$$\text{Total Offset Error (\%)} = \frac{\text{Total Offset Error (V)}}{I_{SENSE} \times R_{SENSE}} \times 100\% \quad (6)$$

One method of calculating the total error is to add the gain error to the percentage contribution of the offset error. However, in this case, the gain error and the offset error do not have an influence or correlation to each other. A more statistically accurate method of calculating the total error is to use the RSS sum of the errors, as shown in 公式 7:

$$\text{Total Error (\%)} = \sqrt{\text{Total Gain Error (\%)}^2 + \text{Total Offset Error (\%)}^2} \quad (7)$$

After applying 公式 7, the total current sense error at maximum current is calculated to be 1.25%, and that is less than the design example requirement of 1.5%.

The INA180A4-Q1 (gain = 200) also has a bandwidth of 105 kHz that meets the small-signal bandwidth requirement of 80 kHz. If higher bandwidth is required, lower-gain devices can be used at the expense of either reduced output voltage range or an increased value of $R_{SENSE}$.

### 9.2.3 Application Curve

图 48 shows an example output response of a unidirectional configuration. The device output swing is limited by ground; therefore, the output is biased to this zero output level. The output rises above ground for positive differential input signals, but cannot fall below ground for negative differential input signals.

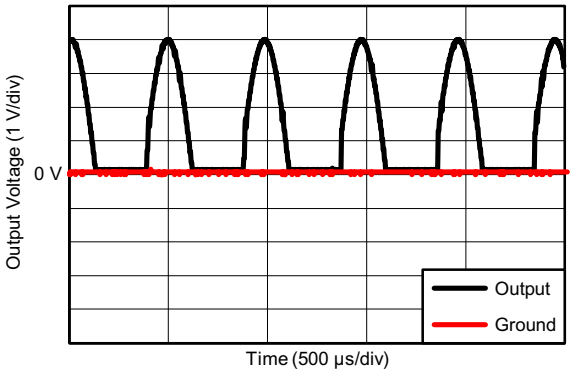



**图 48. Output Response**


版权 © 2018–2019, Texas Instruments Incorporated

# 10 Power Supply Recommendations

The input circuitry of the INAx180-Q1 accurately measures beyond the power-supply voltage, $V_S$. For example, $V_S$ can be 5 V, whereas the bus supply voltage at IN+ and IN– can be as high as 26 V. However, the output voltage range of the OUT pin is limited by the voltages on the VS pin. The INAx180-Q1 also withstand the full differential input signal range up to 26 V at the IN+ and IN– input pins, regardless of whether or not the device has power applied at the VS pin.

## 10.1 Common-Mode Transients Greater Than 26 V

With a small amount of additional circuitry, the INAx180-Q1 can be used in circuits subject to transients higher than 26 V, such as automotive applications. Use only Zener diodes or Zener-type transient absorbers (sometimes referred to as *transzorbs*)—any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as a working impedance for the Zener diode, as shown 图 49. Keep these resistors as small as possible; most often, around 10 Ω. Larger values can be used with an effect on gain that is discussed in the *Signal Filtering* section. This circuit limits only short-term transients; therefore, many applications are satisfied with a 10-Ω resistor along with conventional Zener diodes of the lowest acceptable power rating. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

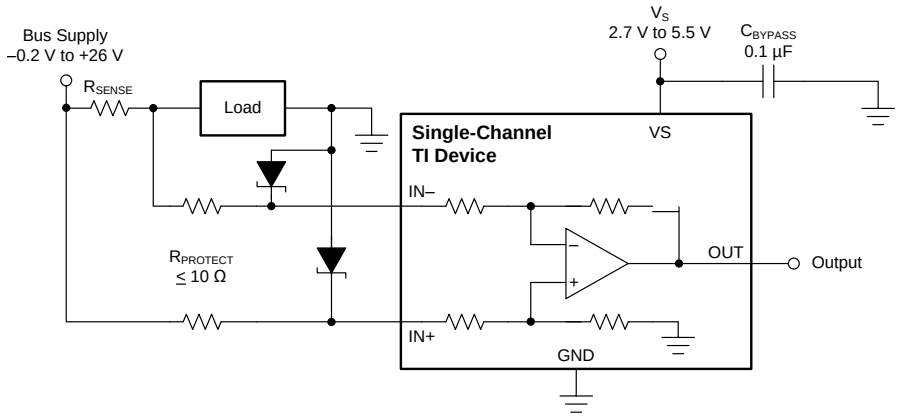



**图 49. Transient Protection Using Dual Zener Diodes**

In the event that low-power Zener diodes do not have sufficient transient absorption capability, a higher-power transzorb must be used. The most package-efficient solution involves using a single transzorb and back-to-back diodes between the device inputs, as shown in 图 50. The most space-efficient solutions are dual, series-connected diodes in a single SOT-523 or SOD-523 package. In either of the examples shown in 图 49 and 图 50, the total board area required by the INAx180-Q1 with all protective components is less than that of an SO-8 package, and only slightly greater than that of an MSOP-8 package.

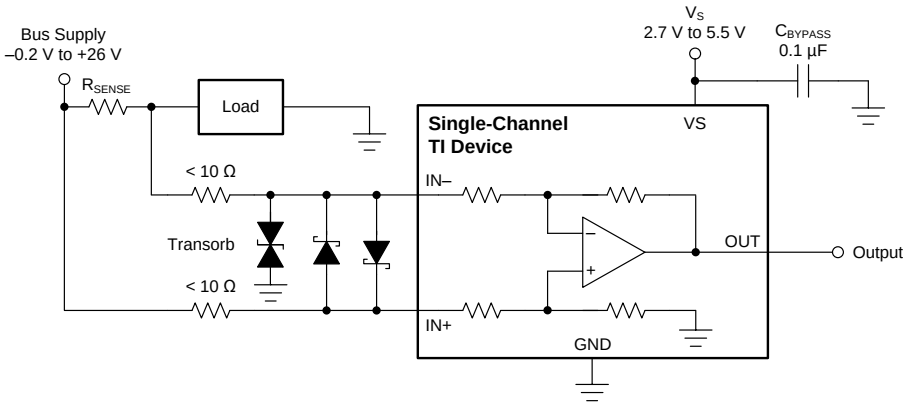



**图 50. Transient Protection Using a Single Transzorb and Input Clamps**

### Common-Mode Transients Greater Than 26 V (接下页)

For a reference design example, see *Current Shunt Monitor With Transient Robustness Reference Design.*

## 11 Layout

### 11.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close as possible to the device power supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- When routing the connections from the current sense resistor to the device, keep the trace lengths as close as possible in order to minimize any impedance mismatch.

### 11.2 Layout Examples

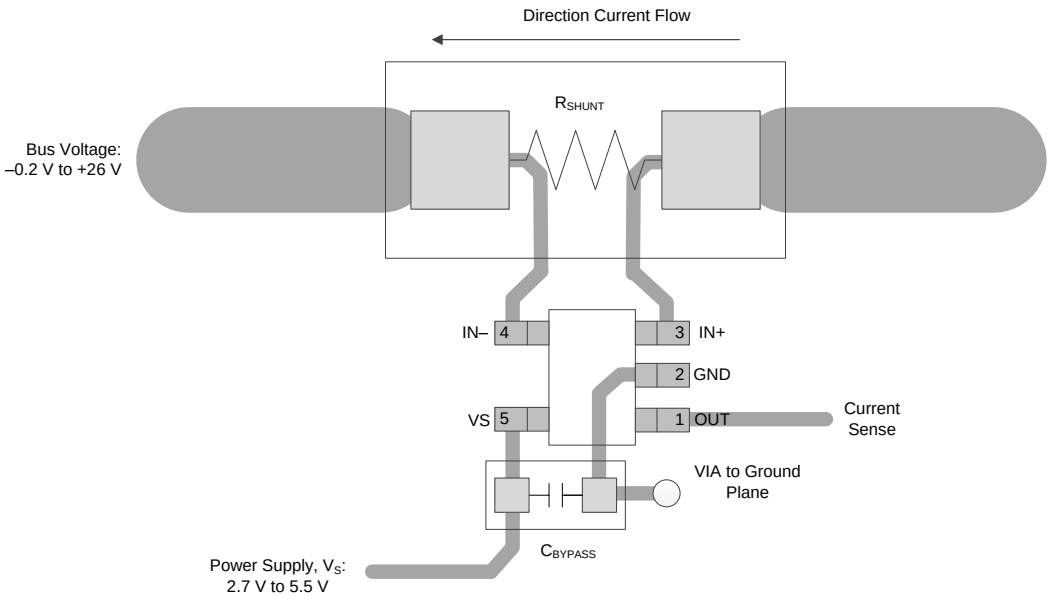



**图 51. Single-Channel Recommended Layout (Pinout A)**


版权 © 2018–2019, Texas Instruments Incorporated

## Layout Examples (接下页)

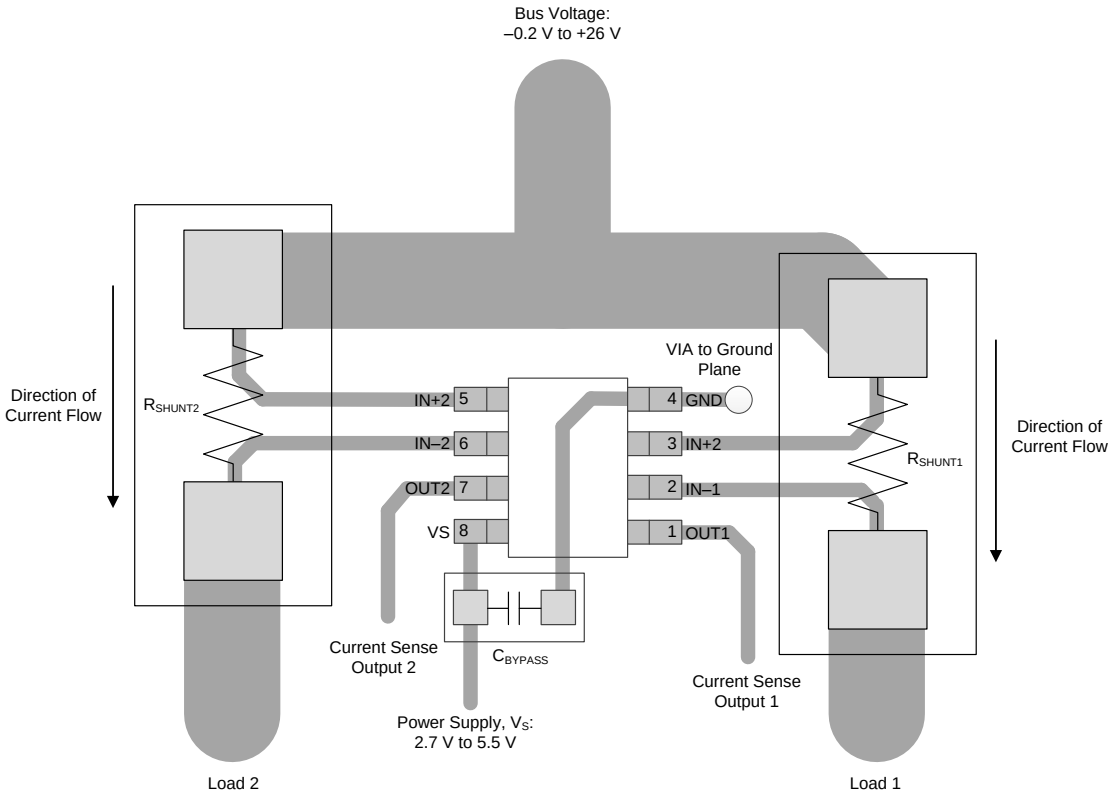



**图 52. Dual-Channel Recommended Layout**

## Layout Examples (接下页)

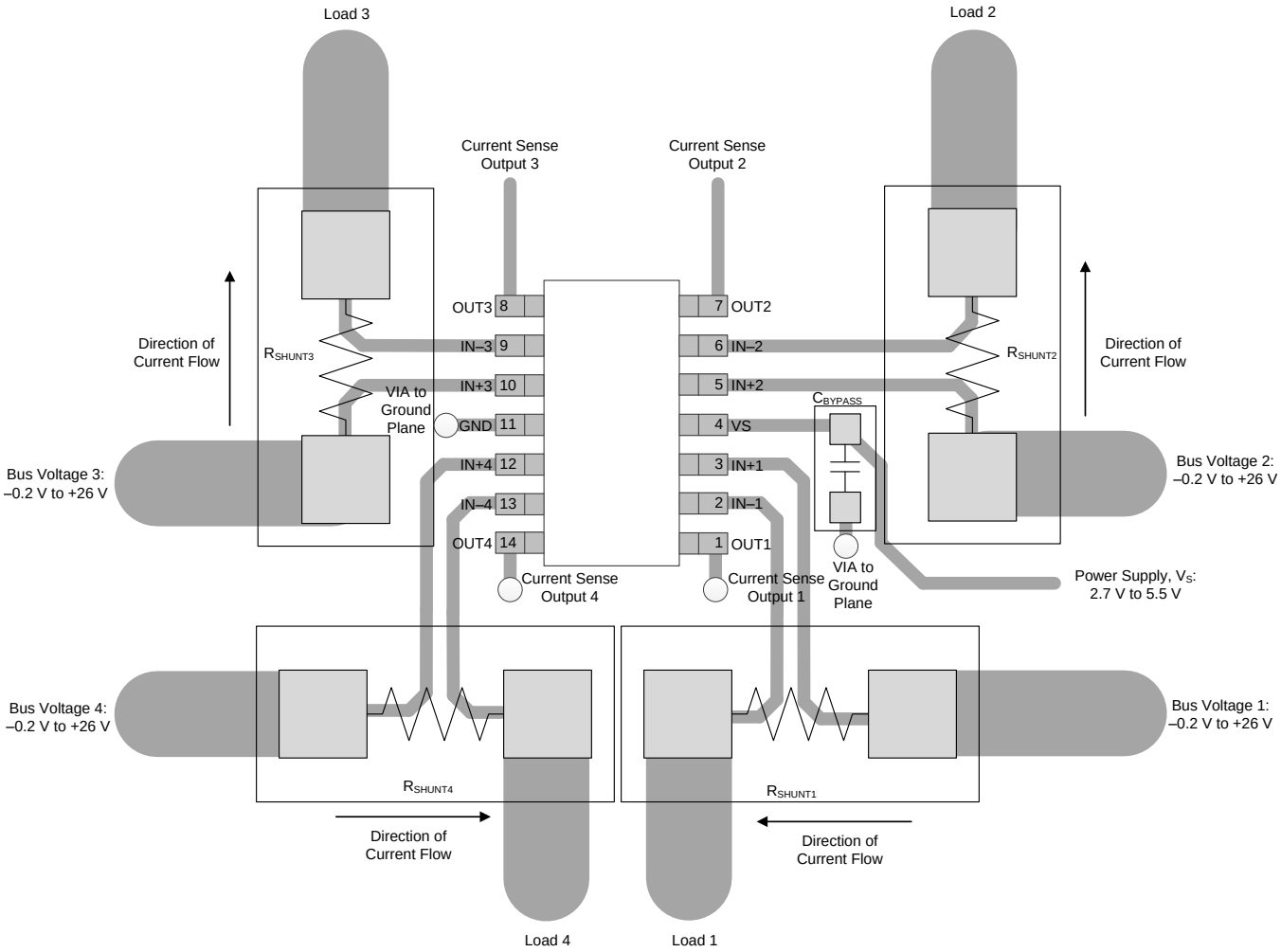



**图 53. Quad-Channel Recommended Layout**


版权 © 2018–2019, Texas Instruments Incorporated

# 12 器件和文档支持

## 12.1 文档支持

### 12.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《INA180-181EVM 用户指南》*
- 德州仪器 (TI)，*《INA2180-2181EVM 用户指南》*
- 德州仪器 (TI)，*《INA4180-4181EVM 用户指南》*

## 12.2 相关链接

表 4 列出了快速访问链接。类别包括技术文档、支持和社区资源、工具与软件，以及立即订购快速访问。

**表 4.** 相关链接

| 器件 | 产品文件夹 | 立即订购 | 技术文档 | 工具与软件 | 支持和社区 |
|---|---|---|---|---|---|
| INA180-Q1 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| INA2180-Q1 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| INA4180-Q1 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |

## 12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 12.4 社区资源

**下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。**

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

# 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

版权 © 2018–2019, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| INA180A1QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 18ID | Samples |
| INA180A2QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MN3 | Samples |
| INA180A3QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MO3 | Samples |
| INA180A4QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MP3 | Samples |
| INA180B1QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MV3 | Samples |
| INA180B2QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MW3 | Samples |
| INA180B3QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MX3 | Samples |
| INA180B4QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MZ3 | Samples |
| INA2180A1QDGKRQ1 | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 1O16 | Samples |
| INA2180A2QDGKRQ1 | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 1O26 | Samples |
| INA2180A3QDGKRQ1 | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 1O36 | Samples |
| INA2180A4QDGKRQ1 | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 1D26 | Samples |
| INA4180A1QPWRQ1 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 4180A1Q | Samples |
| INA4180A2QPWRQ1 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 4180A2Q | Samples |
| INA4180A3QPWRQ1 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 4180A3Q | Samples |
| INA4180A4QPWRQ1 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 4180A4Q | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

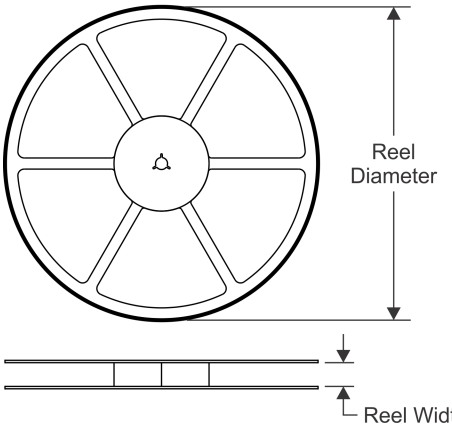
**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

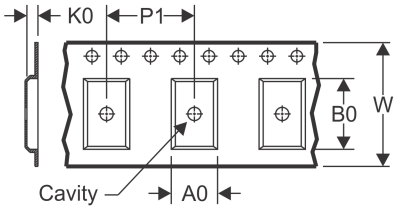
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

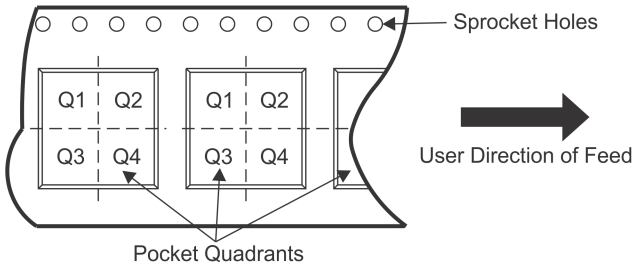



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

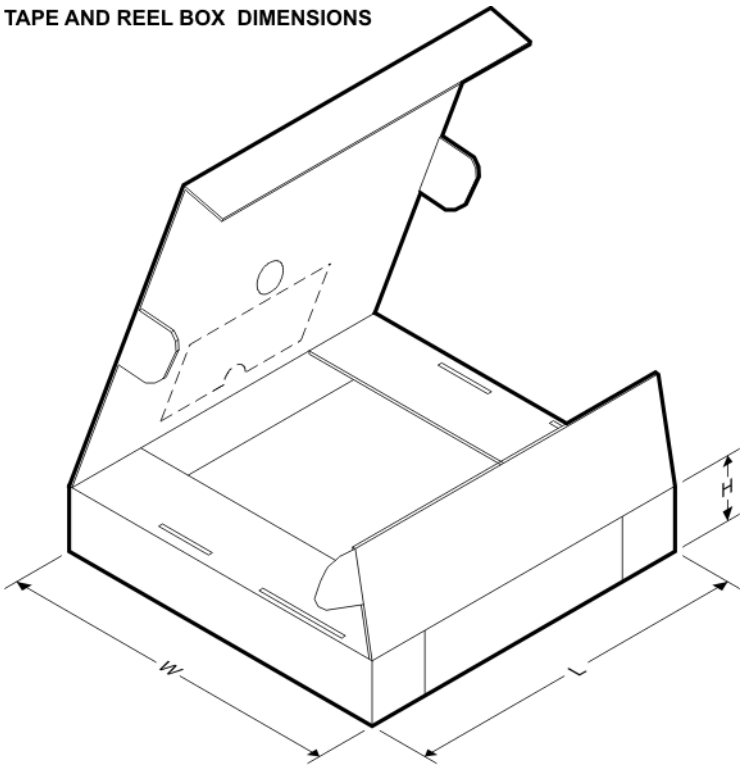
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INA180A1QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA180A2QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA180A3QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA180A4QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA180B1QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA180B2QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA180B3QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA180B4QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| INA2180A1QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA2180A2QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA2180A3QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA2180A4QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA4180A1QPWRQ1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| INA4180A2QPWRQ1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| INA4180A3QPWRQ1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| INA4180A4QPWRQ1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

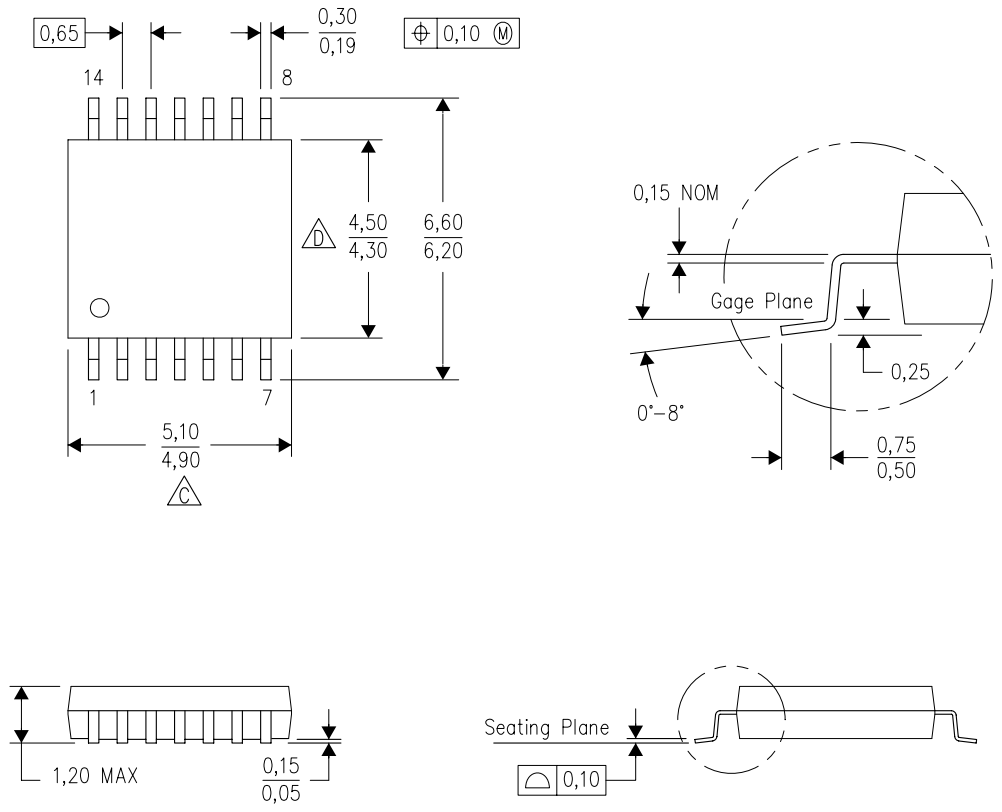
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| INA180A1QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| INA180A2QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| INA180A3QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| INA180A4QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| INA180B1QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| INA180B2QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| INA180B3QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| INA180B4QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| INA2180A1QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| INA2180A2QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| INA2180A3QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| INA2180A4QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| INA4180A1QPWRQ1 | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| INA4180A2QPWRQ1 | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| INA4180A3QPWRQ1 | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| INA4180A4QPWRQ1 | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |

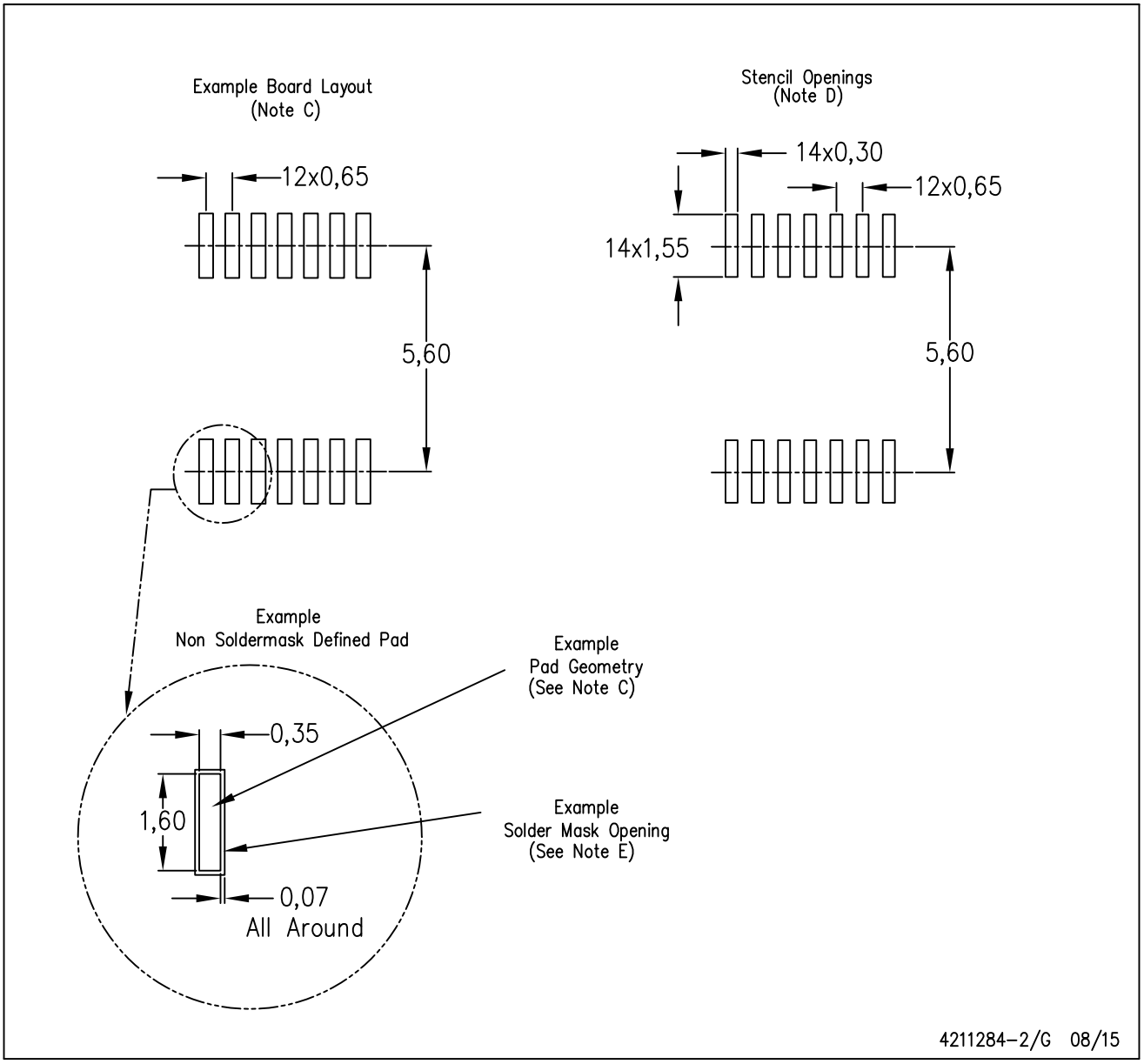
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

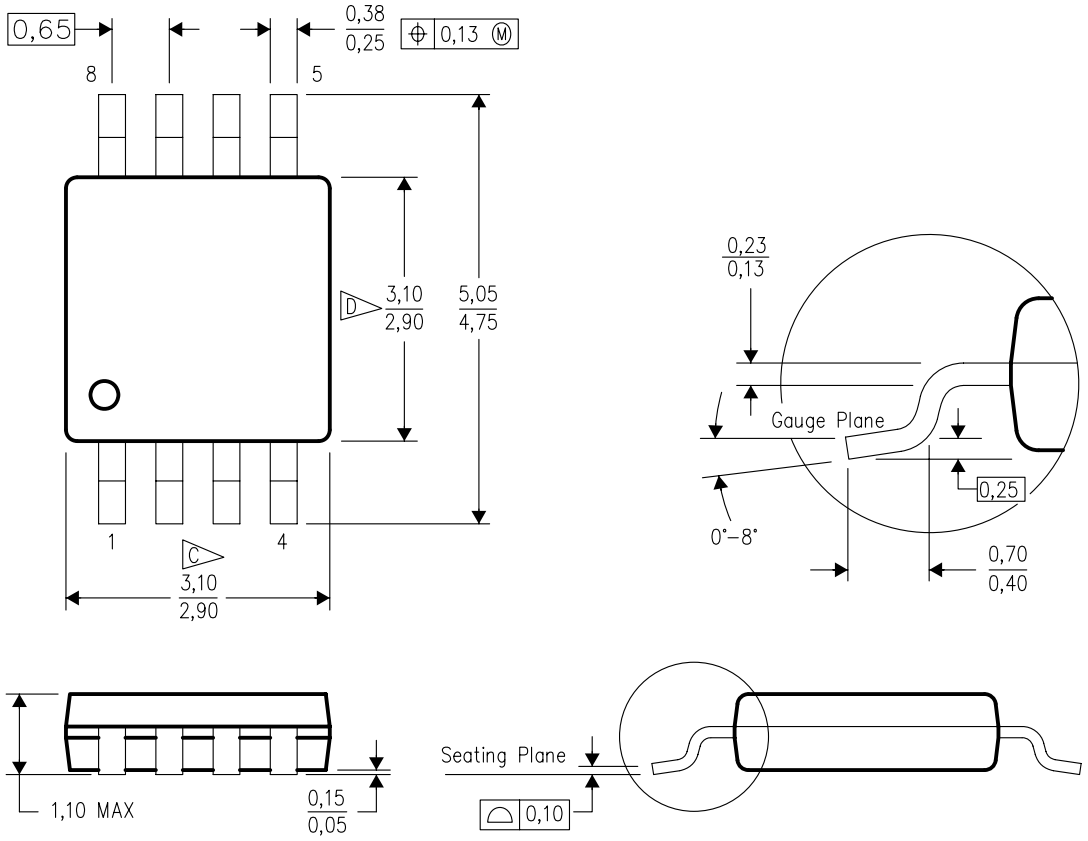
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

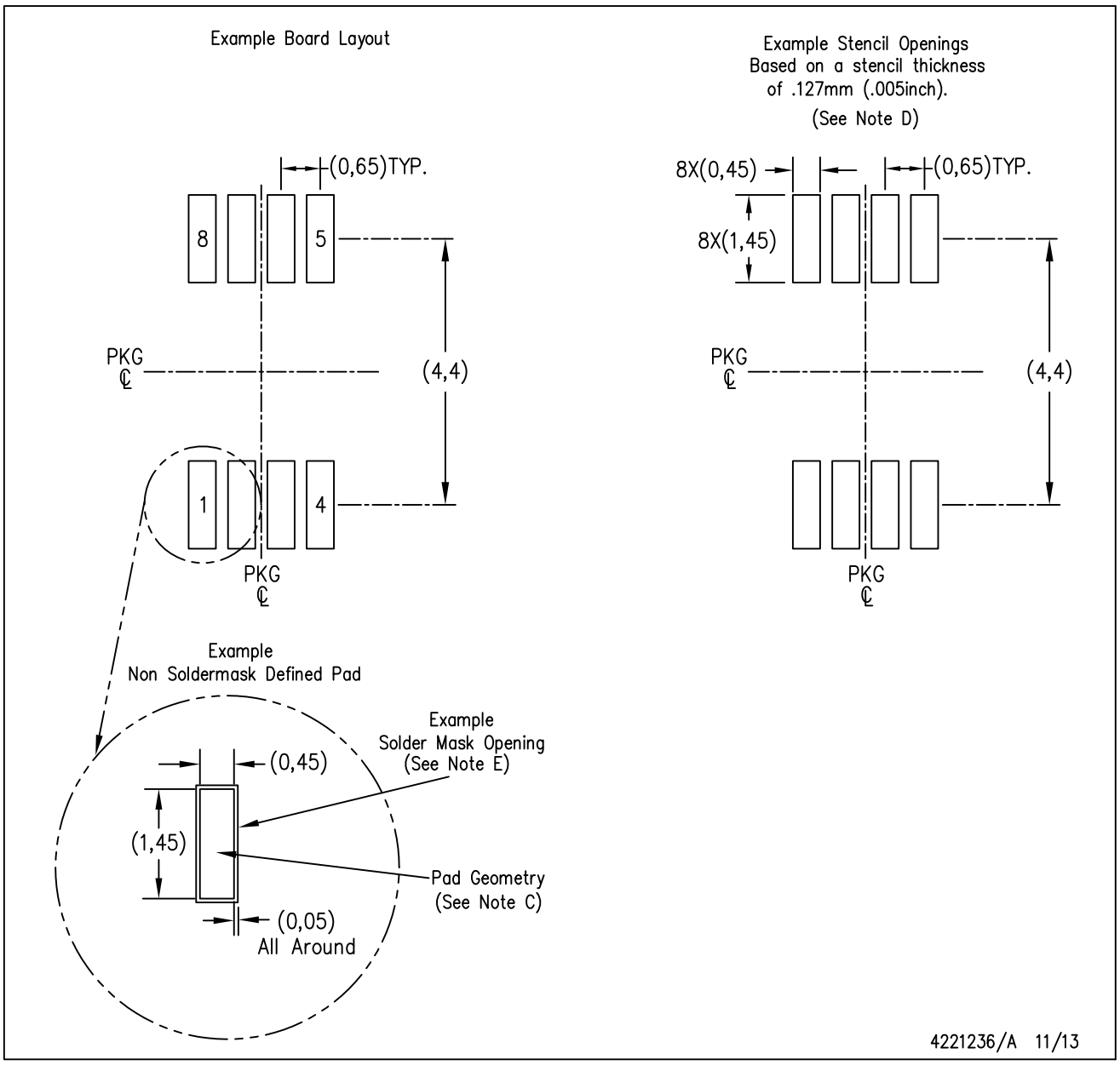
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

# DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



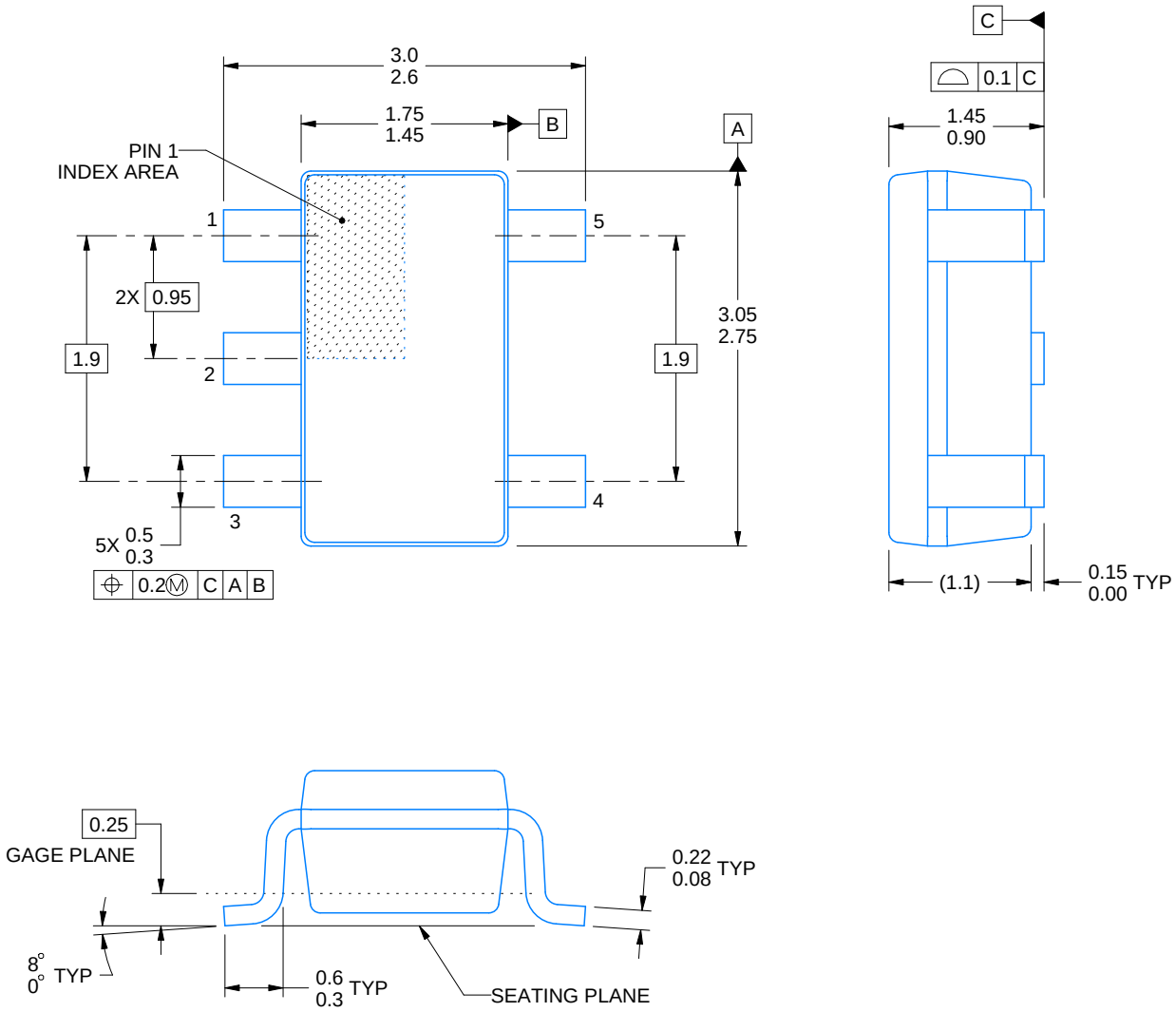

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

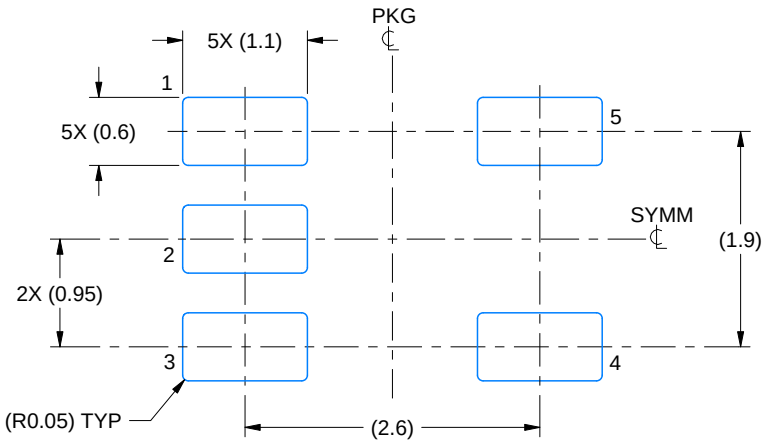
SMALL OUTLINE TRANSISTOR



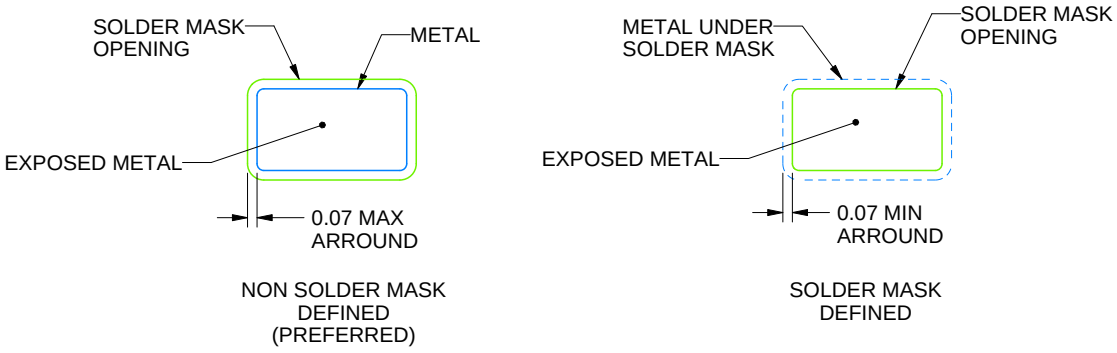

4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

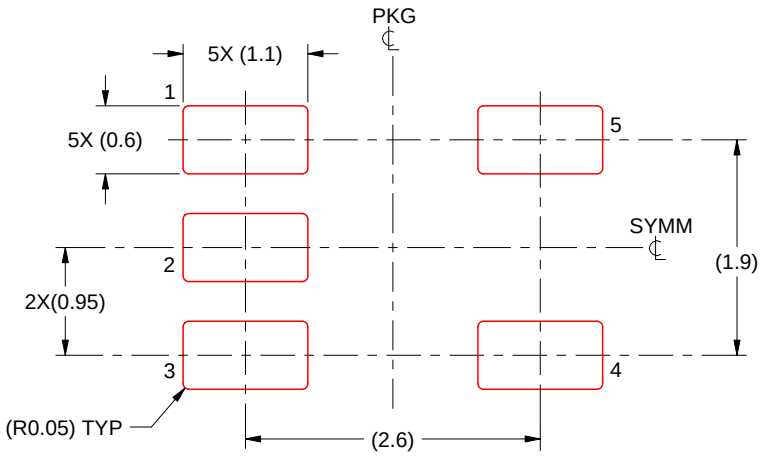



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021，德州仪器 (TI) 公司