适用于开漏和推挽应用的 LSF010x 1/2/8 通道汽车双向多电压电平转换器

1 特性

- 在无方向引脚的情况下提供双向电压转换
- 在容性负载 ≤ 30pF 时支持最高达 100MHz 的上行转换和超过 100MHz 的下行转换，
  在容性负载为 50pF 时支持最高 40MHz 的上行/下行转换
- 可实现以下电压之间的双向电压电平转换
  - 0.95V ↔ 1.8/2.5/3.3/5 V
  - 1.2V ↔ 1.8/2.5/3.3/5V
  - 1.8V ↔ 2.5/3.3/5V
  - 2.5V ↔ 3.3/5V
  - 3.3V ↔ 5V
- 低待机电流
- 支持 TTL 的 5V 耐受 I/O 端口
- 低 R_{ON} 可提供较少的信号失真
- 针对 EN 为低电平的高阻抗 I/O 引脚
- 采用直通引脚以简化 PCB 布线
- 闩锁性能超过 100mA，符合 JESD 17 规范
- -40°C 至 125°C 工作温度范围

2 应用

- GPIO、MDIO、PMBus、SMBus、SDIO、UART、I^2C 和电信基础设施中的其他接口
- 企业系统
- 通信设备
- 个人电子产品
- 工业应用

3 说明

LSF 系列器件支持双向电压转换，而且无需使用 DIR 引脚，最大限度降低了系统工作量（PMBus、I^2C、SMBus 等）。LSF 系列器件在容性负载 ≤ 30pF 时最高支持 100MHz 的升压转换和 100MHz 以上的降压转换；在容性负载为 50pF 时最高支持 40MHz 的升压/降压转换，因此可支持更多的消费类或电信接口（MDIO 或 SDIO）。

LSF 系列的 IO 端口能够耐受 5V 电压，因此与工业和电信应用中的 TTL 电平兼容。LSF 系列极具灵活性，能够为每条通道设置不同电压转换电平。

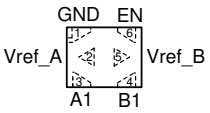
器件信息

器件型号	封装（引脚）(1)	封装尺寸（标称值）
LSF0101DRY	SON (6)	1.45mm × 1.00mm
LSF0101DTQ	X2SON (6)	1.00mm x 0.80mm
LSF0102DQE	X2SON (8)	1.40mm x 1.00mm
LSF0102YZT	DSBGA (8)	1.90mm x 1.00mm
LSF0102DCT	SM8 (8)	2.80mm x 2.95mm
LSF0102DCU	VSSOP (8)	2.30mm × 2.00mm
LSF0108RKS	VQFN (20)	4.50mm x 2.50mm
LSF0108PW	TSSOP (20)	4.40mm x 6.50mm

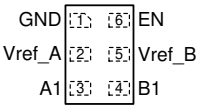
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

LSF0101

DTQ Package
6-Pin X2SON
Transparent Top View

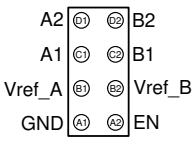


DRY Package
6-Pin SON
Transparent Top View

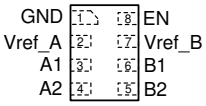


LSF0102

YZT Package
8-Pin DSBGA
Bottom View



DQE Package
8-Pin X2SON
Transparent Top View



LSF0108

RKS Package
20-Pin VQFN
Transparent Top View

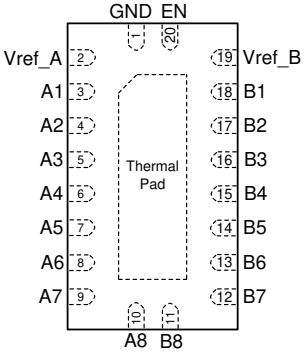


Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision J (April 2020) to Revision K (May 2021) — **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- Updated the *Bidirectional Translation* section to include inclusive terminology 13

Changes from Revision I (June 2019) to Revision J (April 2020) — **Page**

- Added section Voltage Translation for Vref_B < Vref_A + 0.8 V 16

Changes from Revision H (June 2019) to Revision I (July 2019) — **Page**

- 将产品状态从“预告信息混合”更改为“量产数据” 1
- 在“器件信息”表中删除了 DTQ 封装的预告信息注释。 1
- Deleted Advance Information note from DTQ package in the Pin Configuration and Functions section. 4
- Deleted Advance Information note for the DTQ package in the Thermal Information table. 6

Changes from Revision G (February 2016) to Revision H (June 2019) — **Page**

- 在“器件信息”表中针对 DTQ 封装添加了预告信息注释 1
- Added DTQ6 pinout drawing to *Pin Configurations and Functions* section (Advance Information) 4
- Added Advance Information note to LSF0101 Thermal Information table. 6
- General improvements to Application and Implementation section for clarity. 12

Changes from Revision F (October 2015) to Revision G (October 2015) **Page**

- 在“器件信息”中添加了所有可用封装尺寸并更改了引脚图说明。 1

Changes from Revision E (July 2015) to Revision F (October 2015) **Page**

- 将“特性”从“支持 100MHz 以上的高速转换”改为“容性负载 ≤ 30pF 时，支持最高 100MHz 的上行转换和 100MHz 以上的下行转换；容性负载为 50pF 时，支持最高 40MHz 的上行/下行转换。” 1
- Updated all propagation delay tables changed from generic to specific LSF devices. 7

Changes from Revision D (October 2014) to Revision E (July 2015) **Page**

- 删除了“特性”中的“低于最大传播延迟 1.5ns”。 1
- Updated ESD Ratings table. 5
- Increased MAX value for T_A, Operating free-air temperature, from 85°C to 125°C. 5

Changes from Revision C (May 2014) to Revision D (August 2014) **Page**

- 将双向电压电平转换从 1.0 更改为 0.95. 1
- 已更改 YZT 封装以修正视图错误。 1
- Changed YZT package to fix view error. 4
- Added Vref_A footnote. 13

Changes from Revision B (May 2014) to Revision C (May 2014) **Page**

- 已将 LSF0108 状态从预发布更改为量产。 1
- 已更新文档标题。 1
- Updated Handling Ratings table. 5

Changes from Revision A (January 2014) to Revision B (February 2014) **Page**

- 在数据表中添加了 LSF0108。 1

Changes from Revision * (December 2013) to Revision A (January 2014) **Page**

- 已更新器件型号。 1
- Updated *Electrical Characteristics* table. 6

5 Pin Configuration and Functions

Pinout drawings are not to scale.

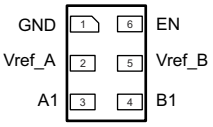


图 5-1. LSF0101 DRY Package 6-Pin SON Transparent Top View

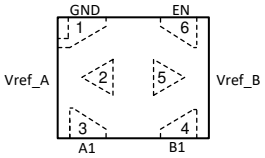


图 5-2. LSF0101 DTQ Package 6-Pin X2SON Transparent Top View

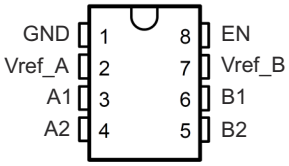


图 5-3. LSF0102 DCT or DCU Package 8-Pin SM8 or VSSOP Top View

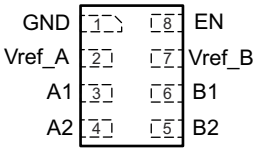


图 5-4. LSF0102 DQE Package 8-Pin X2SON Transparent Top View

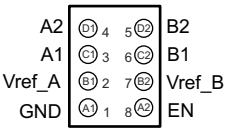


图 5-5. LSF0102 YZT Package 8-Pin DSBGA Bottom View

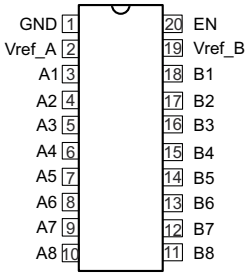


图 5-6. LSF0108 PW Package 20-Pin TSSOP Top View

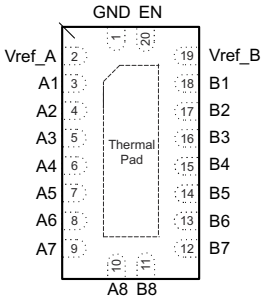


图 5-7. LSF0108 RKS Package 20-Pin VQFN Transparent Top View

Pin Functions

PIN				I/O	DESCRIPTION
NAME	DCT, DCU, DQE, YZT NO.	DRY, DTQ NO.	PW or RKS NO.		
An	3, 4	3	3 to 10	I/O	Auto-Bidirectional Data port
Bn	6, 5	4	18 to 11	I/O	
EN	8	6	20	I	Enable input; connect to Vref_B and pull-up through a high resistor (200 kΩ). See Using the Enable Pin with the LSF Family
GND	1	1	1	—	Ground
Vref_A	2	2	2	—	Reference supply voltage. For proper device biasing, see 节 9 and Understanding the Bias Circuit for the LSF Family.
Vref_B	7	5	19	—	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage(2)		–0.5	7	V
$V_{I/O}$	Input/output voltage(2)		–0.5	7	V
	Continuous channel current			128	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
T_J	Junction Temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	5	V
$V_{ref\_A/B/EN}$	Reference voltage	0	5	V
I_{PASS}	Pass transistor current		64	mA
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information: LSF0101, LSF0108

THERMAL METRIC[1]		LSF0101		LSF0108		UNIT
		DTQ (X2SON)	DRY (SON)	RKS (VQFN)	PW (TSSOP)	
		6 PINS	6 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	294.4	407.0	49.3	106.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	188.9	285.2	45.9	41.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	216.8	271.6	20.6	57.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26.5	113.5	2.5	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	216.0	271.0	20.6	47.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	3.4	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: LSF0102

THERMAL METRIC[1]		LSF0102				UNIT
		DCU (US8)	DCT (SM8)	DQE (X2SON)	YZT (DSBGA)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.1	189.6	246.5	125.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.1	119.6	149.1	1.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	88.8	102.1	100.0	62.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.3	44.5	17.1	3.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	88.4	101.0	99.8	62.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
V_{IK}	I_I = – 18 mA,	V_{EN} = 0				– 1.2	V
I_{IH}	V_I = 5 V	V_{EN} = 0				5.0	µA
I_{CC}	$V_{ref\_B} = V_{EN}$ = 5.5 V, V_{ref_A} = 4.5 V or 1 V, I_O = 0, $V_I = V_{CC}$ or GND				1		µA
$C_{I(ref\_A/B/EN)}$	V_I = 3 V or 0				11		pF
$C_{io(off)}$	V_O = 3 V or 0,	V_{EN} = 0			4.0	6.0	pF
$C_{io(on)}$	V_O = 3 V or 0,	V_{EN} = 3 V			10.5	12.5	pF
r_{on} [2]	V_I = 0,	I_O = 64 mA	V_{ref_A} = 3.3 V; $V_{ref\_B} = V_{EN}$ = 5 V		8.0		Ω
			V_{ref_A} = 1.8 V; $V_{ref\_B} = V_{EN}$ = 5 V		9.0		
			V_{ref_A} = 1.0 V; $V_{ref\_B} = V_{EN}$ = 5 V		10		
	V_I = 0,	I_O = 32 mA	V_{ref_A} = 1.8 V; $V_{ref\_B} = V_{EN}$ = 5 V		10		Ω
			V_{ref_A} = 2.5 V; $V_{ref\_B} = V_{EN}$ = 5 V		15		
	V_I = 1.8 V,	I_O = 15 mA	V_{ref_A} = 3.3 V; $V_{ref\_B} = V_{EN}$ = 5 V		9.0		Ω
	V_I = 1.0 V,	I_O = 10 mA	V_{ref_A} = 1.8 V; $V_{ref\_B} = V_{EN}$ = 3.3 V		18		Ω
	V_I = 0 V,	I_O = 10 mA	V_{ref_A} = 1.0 V; $V_{ref\_B} = V_{EN}$ = 3.3 V		20		Ω
	V_I = 0 V,	I_O = 10 mA	V_{ref_A} = 1.0 V; $V_{ref\_B} = V_{EN}$ = 1.8 V		30		Ω

(1) All typical values are at T_A = 25°C.
(2) Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) pins.

6.7 LSF0101/02 AC Performance (Translating Down) Switching Characteristics , V_{GATE} = 3.3 V

over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 3.3 V, V_{IL} = 0, and V_M = 1.15 V (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	1.1		0.7		0.3		ns
t_{PHL}			1.2		0.8		0.4		

6.8 LSF0108 AC Performance (Translating Down) Switching Characteristics, V_{GATE} = 3.3 V

over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 3.3 V, V_{IL} = 0, and V_M = 1.15 V (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	1.9		1.4		0.75		ns
t_{PHL}			2		1.5		0.85		

6.9 LSF0101/02 AC Performance (Translating Down) Switching Characteristics, V_{GATE} = 2.5 V

over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 2.5 V, V_{IL} = 0, and V_M = 0.75 V (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	1.2		0.8		0.35		ns
t_{PHL}			1.3		1		0.5		

6.10 LSF0108 AC Performance (Translating Down) Switching Characteristics, V_{GATE} = 2.5 V

over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 2.5 V, V_{IL} = 0, and V_M = 0.75 V (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	2		1.45		0.8		ns
t_{PHL}			2.1		1.55		0.9		

6.11 LSF0101/02 AC Performance (Translating Up) Switching Characteristics, V_{GATE} = 3.3 V

over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 2.3 V, V_{IL} = 0, V_T = 3.3 V, V_M = 1.15 V and R_L = 300 (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	1		0.8		0.4		ns
t_{PHL}			1		0.9		0.4		

6.12 LSF0108 AC Performance (Translating Up) Switching Characteristics, V_{GATE} = 3.3 V

over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 2.3 V, V_{IL} = 0, V_T = 3.3 V, V_M = 1.15 V and R_L = 300 (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	2.1		1.55		0.9		ns
t_{PHL}			2.2		1.65		1		

6.13 LSF0101/02 AC Performance (Translating Up) Switching Characteristics, V_{GATE} = 2.5 V

over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 1.5 V, V_{IL} = 0, V_T = 2.5 V, V_M = 0.75 V and R_L = 300 (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	1.1		0.9		0.45		ns
t_{PHL}			1.3		1.1		0.6		

6.14 LSF0108 AC Performance (Translating Up) Switching Characteristics, V_{GATE} = 2.5 V

over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 1.5 V, V_{IL} = 0, V_T = 2.5 V, V_M = 0.75 V and R_L = 300 (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A or B	B or A	1.8		1.35		0.8		ns
t_{PHL}			1.9		1.45		0.9		

6.15 Typical Characteristics

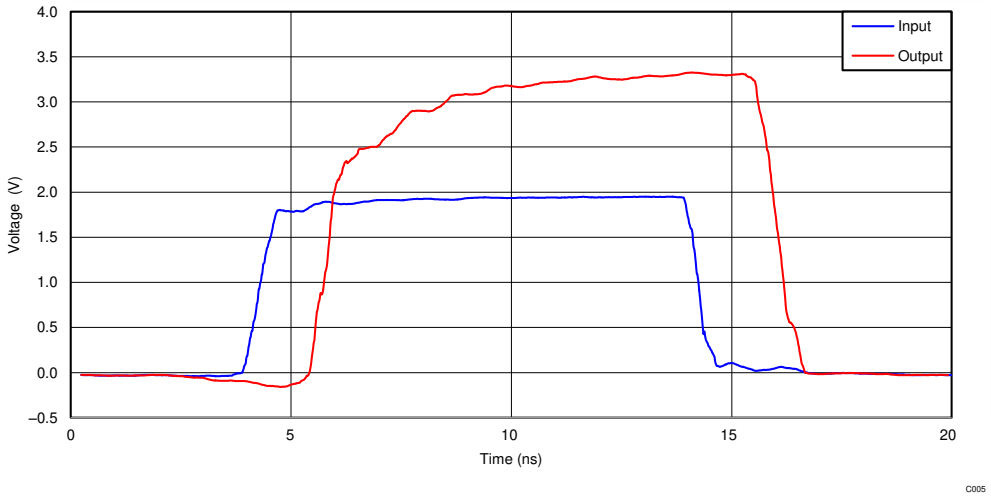
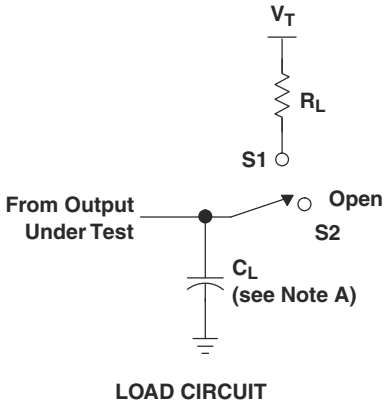


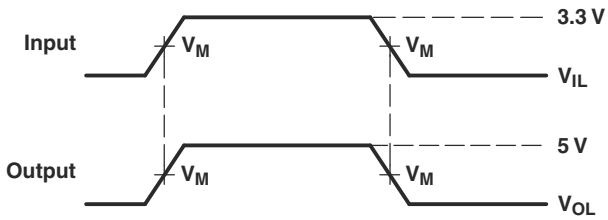
图 6-1. Signal Integrity (1.8 to 3.3 V Up Translation at 50 MHz)

7 Parameter Measurement Information

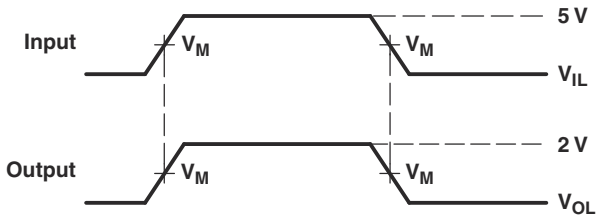


LOAD CIRCUIT

USAGE	SWITCH
Translating up	S1
Translating down	S2



TRANSLATING UP



TRANSLATING DOWN

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

图 7-1. Load Circuit for Outputs

8 Detailed Description

8.1 Overview

The LSF family can be used in level-translation applications for interfacing devices or systems operating with one another, that operate at different interface voltages. The LSF family is ideal for use in applications where an open-drain driver is connected to the data I/Os. With appropriate pull-up resistors and layout, LSF can achieve 100 MHz. The LSF family can also be used in applications where a push-pull driver is connected to the data I/Os. For an overview of device setup and operation, see *The Logic Minute* training series on *Understanding the LSF Family of Bidirectional, Multi-Voltage Level Translators*.

8.2 Functional Block Diagrams

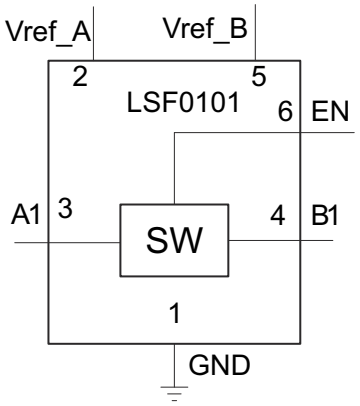


图 8-1. LSF0101 Functional Block Diagram

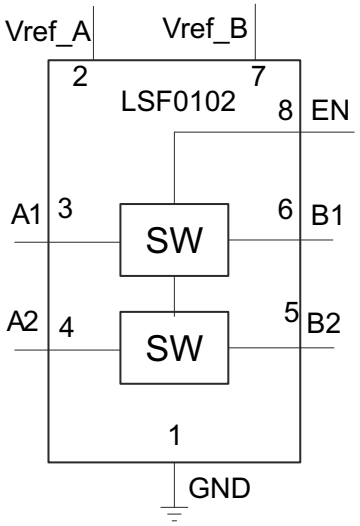


图 8-2. LSF0102 Functional Block Diagram

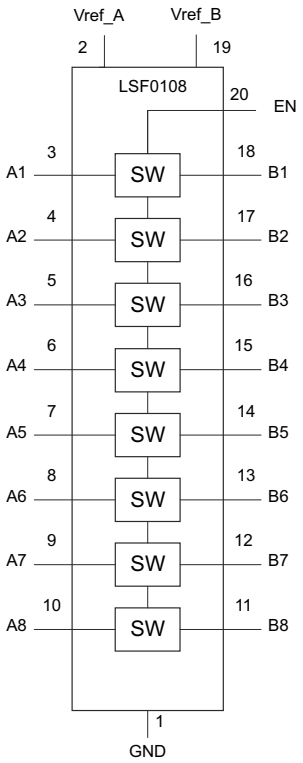


图 8-3. LSF0108 Functional Block Diagram

8.3 Feature Description

8.3.1 Auto Bidirectional Voltage Translation

All devices in the LSF family are auto bidirectional voltage level translators that are operational from 0.95 to 4.5 V on the Vref_A supply and from 1.8 to 5.5 V on the Vref_B supply. This allows bidirectional voltage translation between 0.95 V and 5.5 V without the need for a direction pin in open-drain or push-pull applications. LSF family supports level translation applications with transmission speeds greater than 100 Mbps for open-drain systems using a 30-pF capacitance and 250-Ω pullup resistor. For additional details on the recommended setup and operation of the LSF family of devices, see the *Understanding the LSF Family of Bidirectional, Multi-Voltage Level Translators* training series.

8.3.2 Output Enable

To enable the I/O pins, the EN input should be tied directly to Vref_B during operation. To ensure the high impedance state during power-up, power-down, or during operation, the EN pin must be LOW. The EN pin should always be tied directly to the Vref_B pin and is recommended to be disabled by an open-drain driver without a pullup resistor. For additional details on how to use the enable pin, see the *Using the Enable Pin with the LSF Family* video.

表 8-1. Enable Pin Function Table

INPUT EN(1) PIN	Data Port State
Tied directly to Vref_B	An = Bn
L	Hi-Z

(1) EN is controlled by V_{ref_B} logic levels.

8.4 Device Functional Modes

For each channel (n), when either the An or Bn port is LOW, the switch provides a low impedance path between the An and Bn ports; the corresponding Bn or An port will be pulled LOW. The low R_{ON} of the switch allows connections to be made with minimal propagation delay and signal distortion.

When the signal is being driven from Bn to An and the Bn port is driven HIGH, the switch will be OFF, clamping the voltage on the An port to the voltage set by Vref_A. When the signal is being driven from A to B and the An port is HIGH, the switch will be OFF and the Bn port will then driven to a voltage higher than Vref_A by the pullup resistor that is connected to the pull-up supply voltage ($V_{pu\#}$). This functionality allows seamless translation between higher and lower voltages selected by the user, without the need for directional control.

Refer to 表 8-1 for a summary of device operation. For additional details on the functional operation of the LSF family of devices, see the *Down Translation with the LSF Family* and *Up Translation with the LSF Family* videos.

表 8-2. Device Functionality

Signal Direction(1)	Input State	Switch State	Functionality
B to A (Down Translation)	B = LOW	ON (Low Impedance)	A-side voltage is pulled low through the switch to the B-side voltage
	B = HIGH	OFF (High Impedance)	A-side voltage is clamped at Vref_A (2)
A to B (Up Translation)	A = LOW	ON (Low Impedance)	B-side voltage is pulled low through the switch to the A-side voltage
	A = HIGH	OFF (High Impedance)	B-side voltage is clamped at Vref_A and then pulled up to the Vpu# supply voltage

(1) The downstream channel should not be actively driven through a low impedance driver, or else there may be bus contention.
(2) The A-side can have a pullup to Vref_A for additional current drive capability or may also be pulled above Vref_A with a pullup resistor. Specifications in the 节 6.3 should always be followed.

9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The LSF devices are able to perform voltage translation for open-drain or push-pull interfaces. 表 9-1 provides common interfaces and the corresponding device recommendation from the LSF family which supports the corresponding bit count.

表 9-1. Voltage Translator for Common Interfaces

Part Name	Channel Number	Interface
LSF0101	1	GPIO
LSF0102	2	GPIO, MDIO, SMBus, PMBus, I^2C
LSF0108	8	GPIO, MDIO, SDIO, SVID, UART, SMBus, PMBus, I^2C, SPI

9.2 Typical Applications

9.2.1 Open-Drain Interface (I^2C, PMBus, SMBus, GPIO)

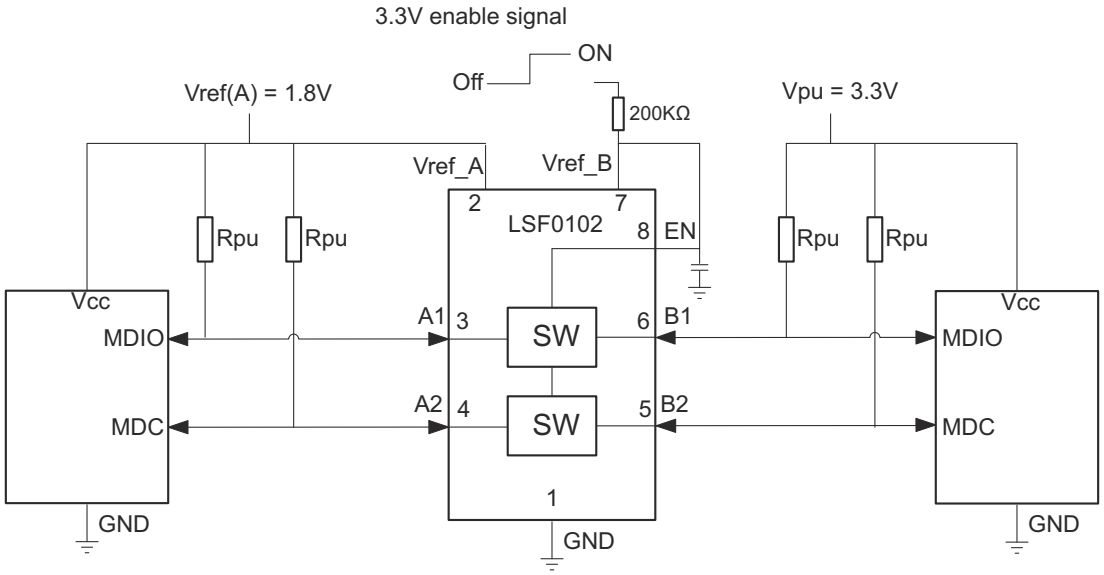


图 9-1. Typical Application Circuit for Open-Drain Translation (MDIO shown as an example)

9.2.1.1 Design Requirements

9.2.1.1.1 Enable, Disable, and Reference Voltage Guidelines

The LSF family has an EN input that is used to disable the device by setting EN LOW, placing all I/Os in the high-impedance state. Since the LSF family of devices are switch-type voltage translators, the power consumption is very low. TI recommends always enabling the LSF family for bidirectional applications (I^2C, SMBus, PMBus, or MDIO).

表 9-2. Application Operating Condition

PARAMETER		MIN	TYP	MAX	UNIT
Vref_A(1)	reference voltage (A)	0.95		4.5	V
Vref_B	reference voltage (B)	Vref_A + 0.8		5.5	V
$V_{I(EN)}$	input voltage on EN pin	Vref_A + 0.8		5.5	V
Vpu	pull-up supply voltage	0		Vref_B	V

(1) Vref_A is required to be the lowest voltage level across all inputs and outputs.

The 200 kΩ, pull-up resistor is required to allow Vref_B to regulate the EN input and properly bias the device for translation. For additional details on device biasing, see the *Understanding the Bias Circuit for the LSF Family* video. A filter capacitor on Vref_B is recommended. Also Vref_B and $V_{I(EN)}$ are recommended to be 1.0 V higher than Vref_A for best signal integrity.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Bidirectional Translation

For the bidirectional translation configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to Vref_B and both pins must be pulled up to the HIGH side Vpu through a pull-up resistor (typically 200 kΩ). This allows Vref_B to regulate the EN input and bias the channels for proper translation. A filter capacitor on Vref_B is recommended for a stable supply at the device. The controller output driver can be push-pull or open-drain (pull-up resistors may be required) and the peripheral device output can be push-pull or open-drain (pull-up resistors are required to pull the Bn outputs to Vpu).

If either output is push-pull, data must be unidirectional or the outputs must be tri-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW bus contention in either direction. If both outputs are open-drain, no direction control is needed.

When Vref_B is connected through a 200-kΩ resistor to a 3.3-V Vpu power supply and Vref_A is set 1.8 V, as shown in 图 9-1, the A1 and A2 channels have a maximum output voltage equal to Vref_A, and the B1 and B2 channels have has a maximum output voltage equal to Vpu.

9.2.1.2.2 Pull-up Resistor Sizing

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This ensures a voltage drop of 260 mV to 350 mV to have a valid LOW signal on the downstream channel. If the current through the pass transistor is higher than 15 mA, the voltage drop is also higher in the ON state. To set the current through each pass transistor at 15 mA, calculate the pull-up resistor value using the following equation:

$$Rpu = (Vpu - 0.35\ V) / 0.015\ A \quad (1)$$

表 9-3 summarizes resistor values, reference voltages, and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the voltage drop across the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the LSF family device at 0.175 V, although the 15 mA applies only to current flowing through the LSF family device.

表 9-3. Pull-up Resistor Values

V_{DPU} (1) (2)	15 mA		10 mA		3 mA	
	NOMINAL (Ω)	+10%(3) (Ω)	NOMINAL (Ω)	+10%(3) (Ω)	NOMINAL (Ω)	+10%(3) (Ω)
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) Calculated for V_{OL} = 0.35 V
(2) Assumes output driver V_{OL} = 0.175 V at stated current
(3) +10% to compensate for V_{DD} range and resistor tolerance

9.2.1.3 Application Curve

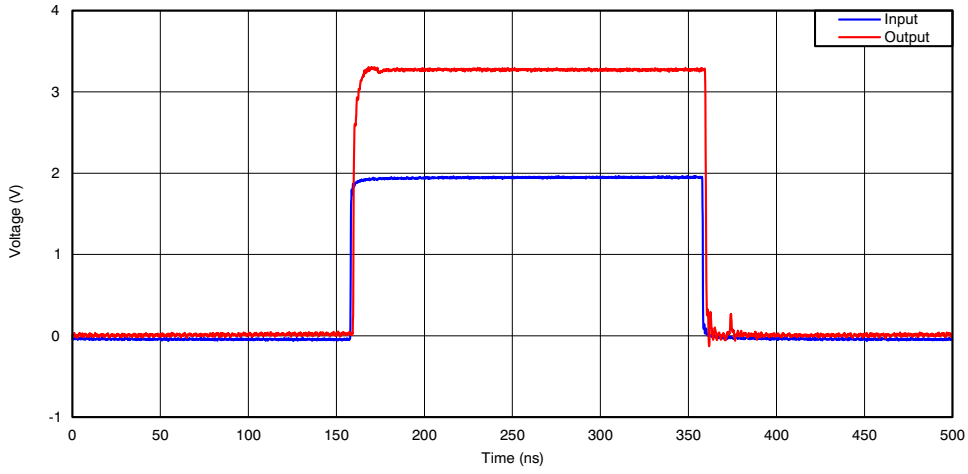


图 9-2. Open Drain Translation (1.8 V to 3.3 V at 2.5 MHz)

9.2.2 Mixed-Mode Voltage Translation

The supply voltage ($V_{pu\#}$) for each channel can be individually set with a pull-up resistor. An example of this mixed-mode multi-voltage translation is shown in 图 9-3. For additional details on multi-voltage translation, see the *Multi-voltage Translation with the LSF Family* video.

With the Vref_B pulled up to 5V and Vref_A connected to 1.8V, all channels will be clamped to 1.8V at which point a pullup can be used to define the high level voltage for a given channel.

- **Push-Pull Down Translation (5V to 1.8V):** Channel 1 is an example of this setup. When B1 is 5V, A1 is clamped to 1.8V, and when B1 is LOW, A1 is driven LOW through the switch.
- **Push-Pull Up Translation (1.8V to 5V)**: Channel 2 is an example of this setup. When A2 is 1.8V, the switch is high impedance and the B2 channel is pulled up to 5V. When A2 is LOW, B2 is driven LOW through the switch.
- **Push-Pull Down Translation (3.3V to 1.8V):** Channels 3 and 4 are examples of this setup. When either B3 or B4 are driven to 3.3V, A3 or A4 are clamped to 1.8V, and when either B3 or B4 are LOW, A3 or A4 are driven LOW through the switch.
- **Open-Drain Bidirectional Translation (3.3V ↔ 1.8V):** Channels 5 through 8 are examples of this setup. These channels are for bidirectional operation for I^2C and MDIO to translate between 1.8V and 3.3V with open-drain drivers.

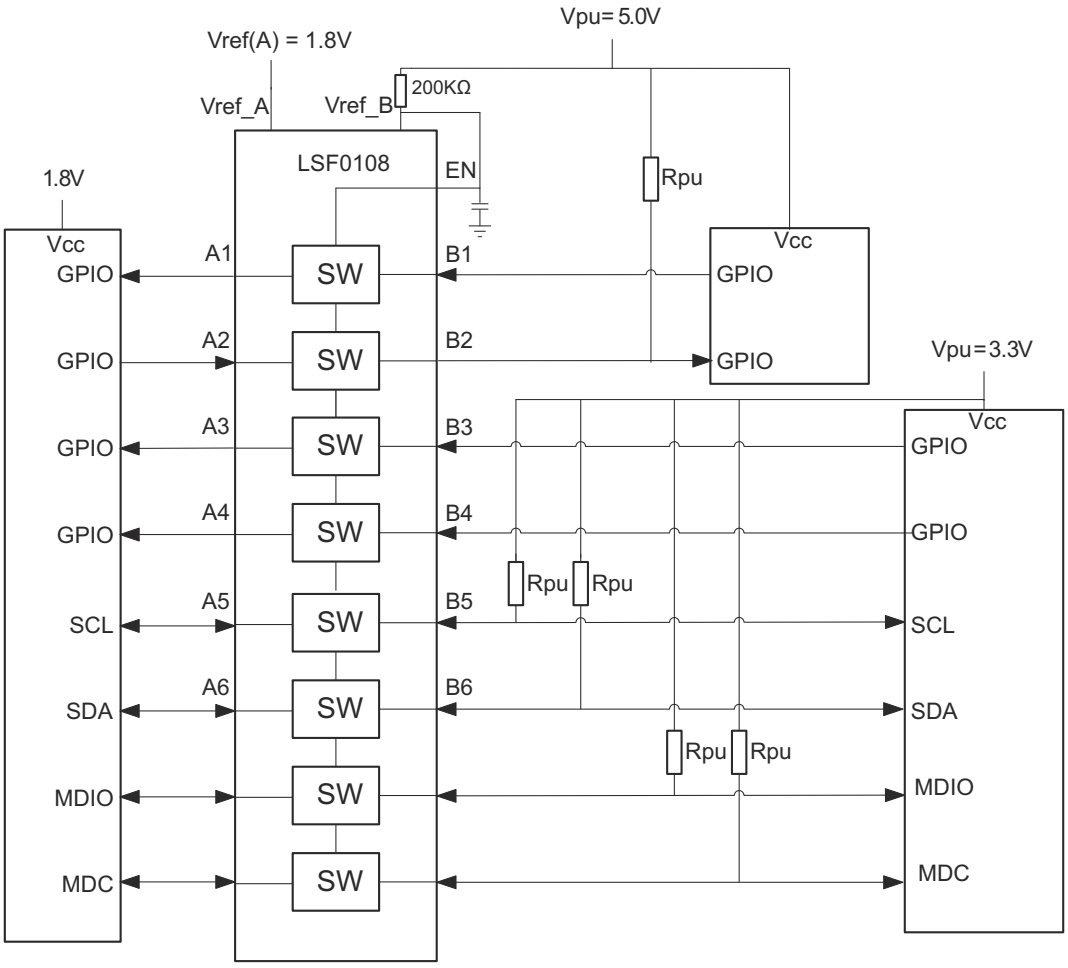


图 9-3. Multi-Voltage Translation with the LSF0108

9.2.3 Voltage Translation for Vref_B < Vref_A + 0.8 V

As described in 表 9-2, it is generally recommended that Vref_B > Vref_A + 0.8 V; however, the device can still be operated in the condition where Vref_B < Vref_A + 0.8 V as long as additional considerations are made for the design.

Typical Operation (Vref_B > Vref_A + 0.8 V): In this scenario, pullup resistors are not required on the A-side for proper down-translation as is shown for channels 1 and 2 of 图 9-3. The typical operating mode of the device ensures that when down translating from B to A, the A-side I/O ports will clamp at Vref_A to provide proper voltage translation. For further explanation of device operation, see the *Down Translation with the LSF Family* video.

Requirements for Vref_B < Vref_A + 0.8 V Operation: In this scenario, there is not a large enough voltage difference between Vref_A and Vref_B to ensure that the A side I/O ports will be clamped at Vref_A, but rather at a voltage approximately equal to Vref_B - 0.8V. For example, if Vref_B = 1.8V and Vref_A = 1.2V, the A-side I/Os will clamp to a voltage around 1.0V. Therefore, to operate in such a condition, the following additional design considerations must be met:

- Vref_B must be greater than Vref_A during operation (Vref_B > Vref_A)
- Pullup resistors should be populated on A-side I/O ports to ensure the line will be fully pulled up to the desired voltage

An example of this setup is shown in 图 9-4, where 1.2V ↔ 1.8V translation is achieved with the LSF0102. This type of setup also applies for other voltage nodes such as 1.8V ↔ 2.5V, 1.05V ↔ 1.5V, and others as long as the 节 6.3 table is followed.

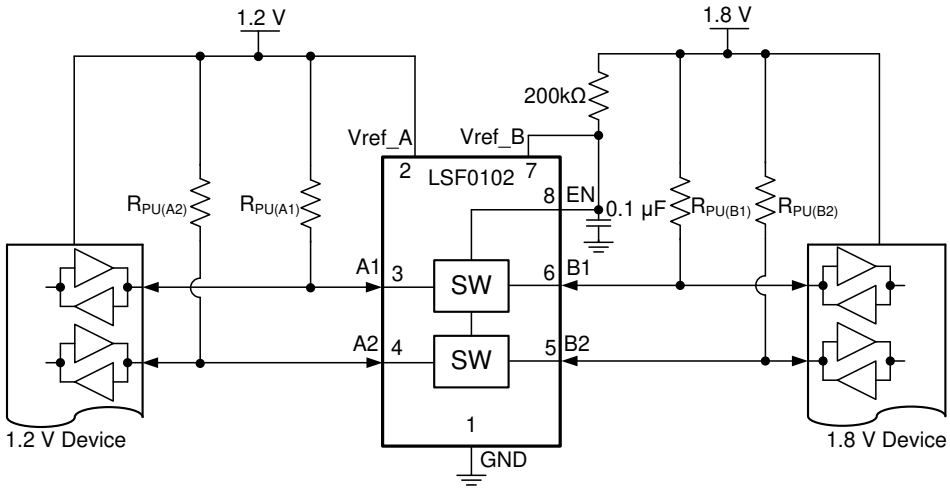


图 9-4. 1.2 to 1.8V Level Translation with LSF0102

10 Power Supply Recommendations

There are no power sequence requirements for the LSF family. For recommended operating voltages for all supply and input pins, see 表 10-1.

表 10-1. Recommended Operating Voltages

PARAMETER		MIN	TYP	MAX	UNIT
Vref_A(1)	reference voltage (A)	0.95		4.5	V
Vref_B	reference voltage (B)	Vref_A + 0.8		5.5	V
$V_{I(EN)}$	input voltage on EN pin	Vref_A + 0.8		5.5	V
Vpu	pull-up supply voltage	0		Vref_B	V

11 Layout

11.1 Layout Guidelines

Because the LSF family is a switch-type level translator, the signal integrity is highly related with a pull-up resistor and PCB capacitance condition.

- Short signal trace as possible to reduce capacitance and minimize stub from pull-up resistor.
- Place LSF close to high voltage side.
- Select the appropriate pull-up resistor that applies to translation levels and driving capability of transmitter.

11.2 Layout Example

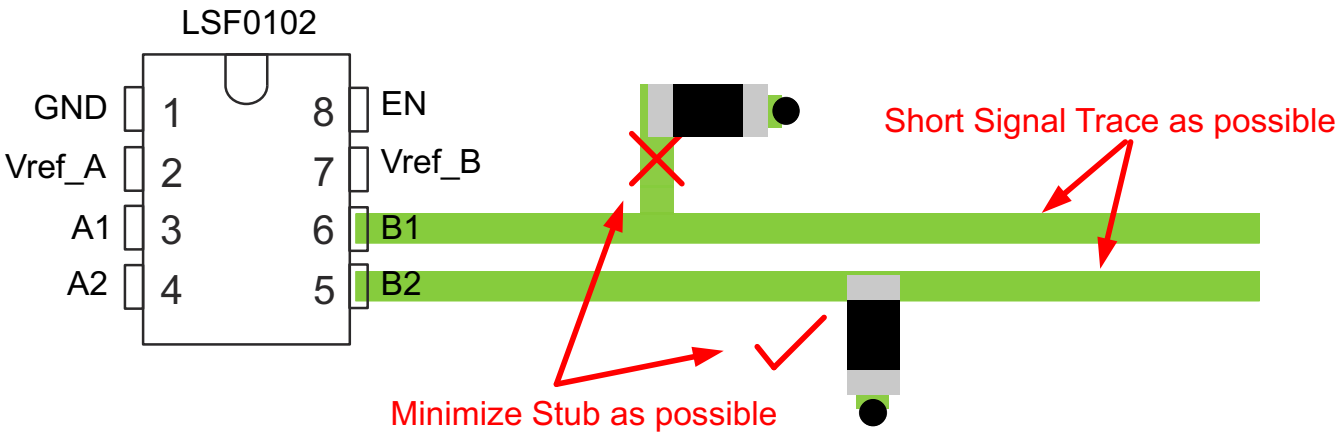


图 11-1. Short Trace Layout

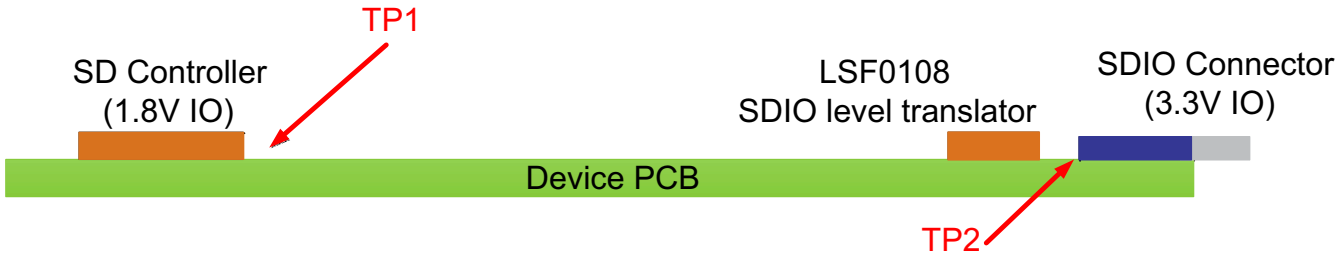


图 11-2. Device Placement

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LSF0101	Click here	Click here	Click here	Click here	Click here
LSF0102	Click here	Click here	Click here	Click here	Click here
LSF0108	Click here	Click here	Click here	Click here	Click here

1. LSF Translator Family Evaluation Module
2. The Logic Minute Video Training Series on Understanding the LSF Family of Devices
   - *Introduction - Voltage Level Translation with the LSF Family*
   - *Understanding the Bias Circuit for the LSF Family*
   - *Using the Enable Pin with the LSF Family*
   - *Translation Basics with the LSF Family*
   - *Down Translation with the LSF Family*
   - *Up Translation with the LSF Family*
   - *Multi-Voltage Translation with the LSF Family*
   - *Single Supply Translation with the LSF Family*
3. *Voltage Level Translation with the LSF Family* Application Note
4. *Biasing Requirements for TXS, TXB, and LSF Auto-Bidirectional Translators* Application Note

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LSF0101DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD	Samples
LSF0101DTQR	ACTIVE	X2SON	DTQ	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	FC	Samples
LSF0102DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NG2 (S, Y)	Samples
LSF0102DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(G2, NG2J, NG2P, NG2S) NY	Samples
LSF0102DQER	ACTIVE	X2SON	DQE	8	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RV	Samples
LSF0102YZTR	ACTIVE	DSBGA	YZT	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	RV	Samples
LSF0108PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LSF0108	Samples
LSF0108RKSR	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LSF0108	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LSF0102, LSF0108 :

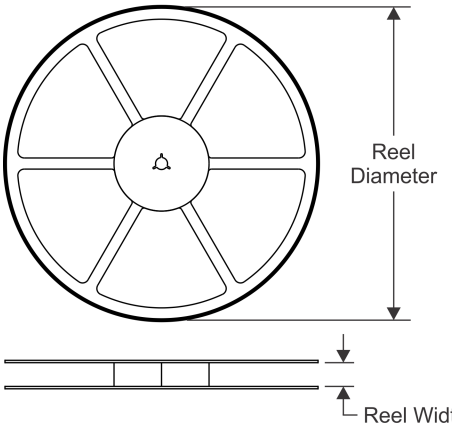
- Automotive : LSF0102-Q1, LSF0108-Q1

NOTE: Qualified Version Definitions:

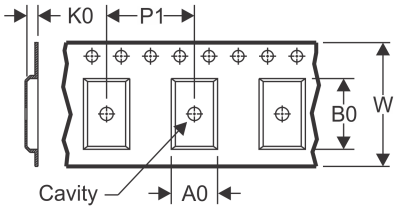
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

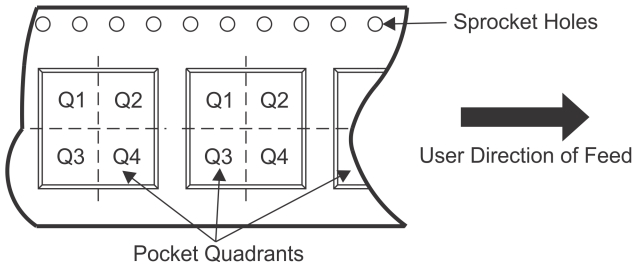


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

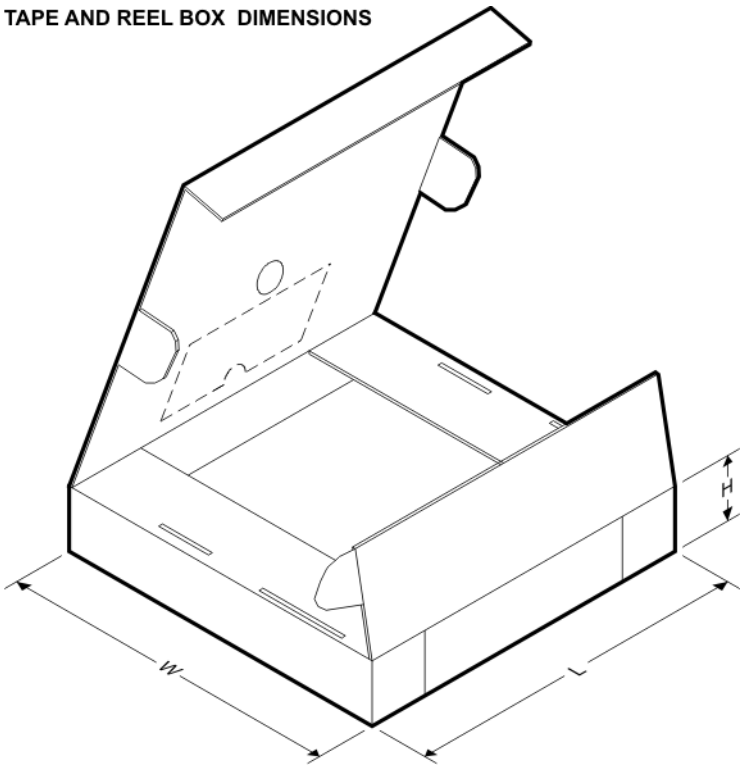
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LSF0101DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
LSF0101DTQR	X2SON	DTQ	6	3000	180.0	9.5	0.94	1.13	0.5	2.0	8.0	Q2
LSF0102DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
LSF0102DCTR	SM8	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
LSF0102DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
LSF0102DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
LSF0102DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
LSF0102DQER	X2SON	DQE	8	5000	180.0	9.5	1.15	1.6	0.5	4.0	8.0	Q1
LSF0102YZTR	DSBGA	YZT	8	3000	180.0	8.4	1.02	2.02	0.75	4.0	8.0	Q1
LSF0108PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LSF0108RKSR	VQFN	RKS	20	3000	177.8	12.4	2.73	4.85	1.03	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LSF0101DRYR	SON	DRY	6	5000	184.0	184.0	19.0
LSF0101DTQR	X2SON	DTQ	6	3000	189.0	185.0	36.0
LSF0102DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
LSF0102DCTR	SM8	DCT	8	3000	183.0	183.0	20.0
LSF0102DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
LSF0102DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
LSF0102DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
LSF0102DQER	X2SON	DQE	8	5000	184.0	184.0	19.0
LSF0102YZTR	DSBGA	YZT	8	3000	182.0	182.0	20.0
LSF0108PWR	TSSOP	PW	20	2000	364.0	364.0	27.0
LSF0108RKSR	VQFN	RKS	20	3000	202.0	201.0	28.0

GENERIC PACKAGE VIEW

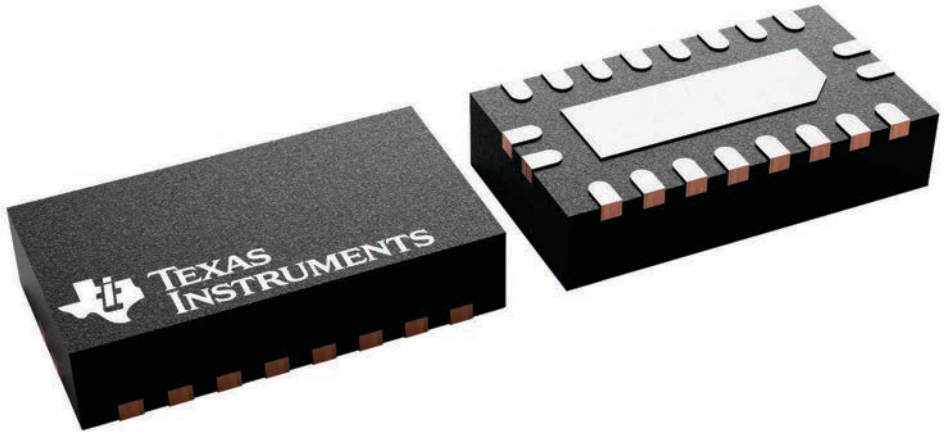
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

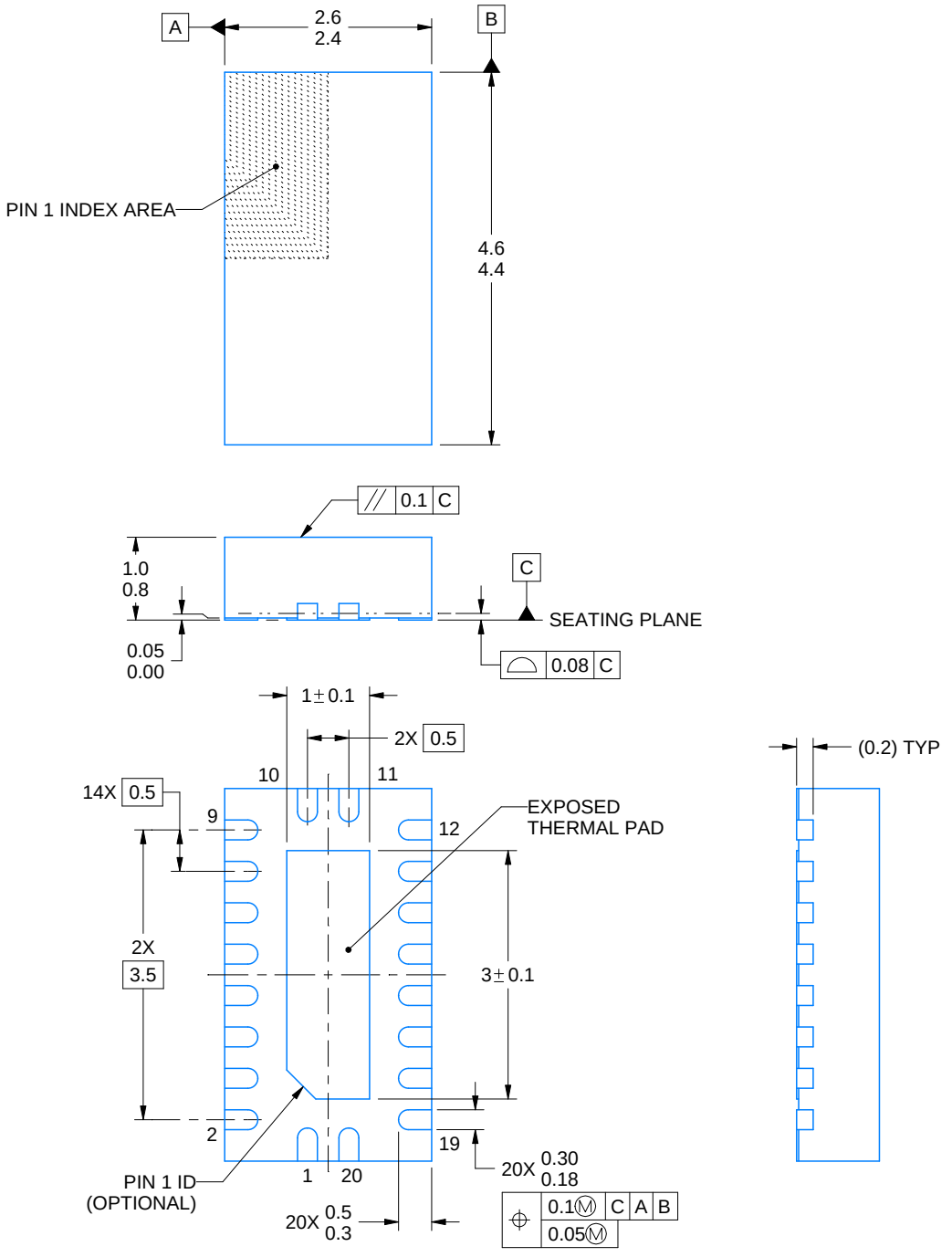


PACKAGE OUTLINE

RKS0020A

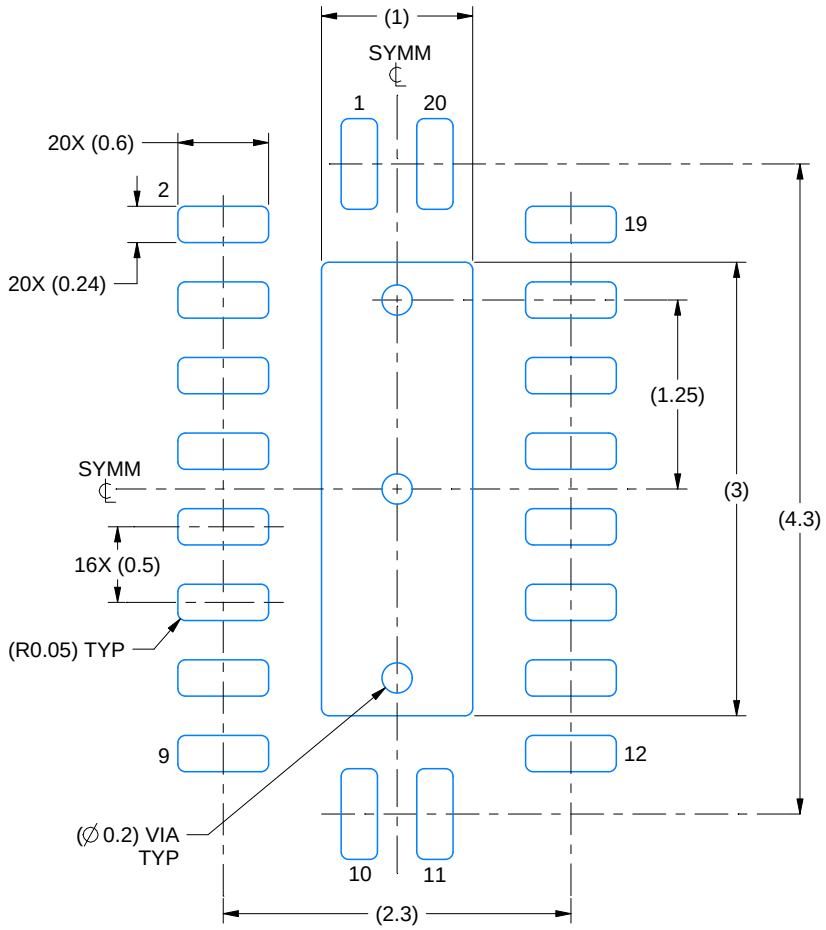
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

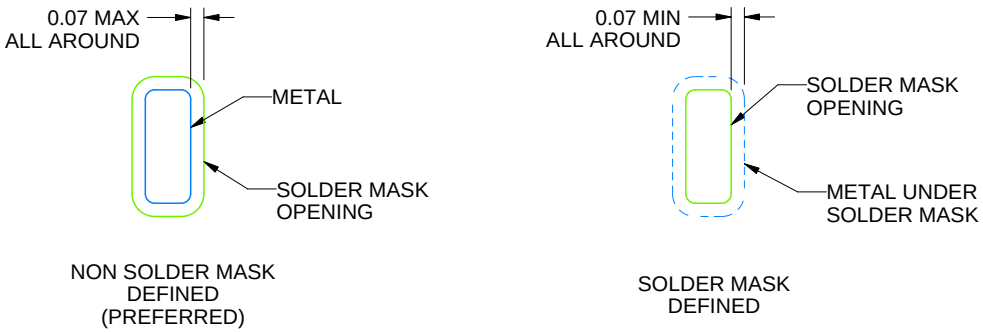


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

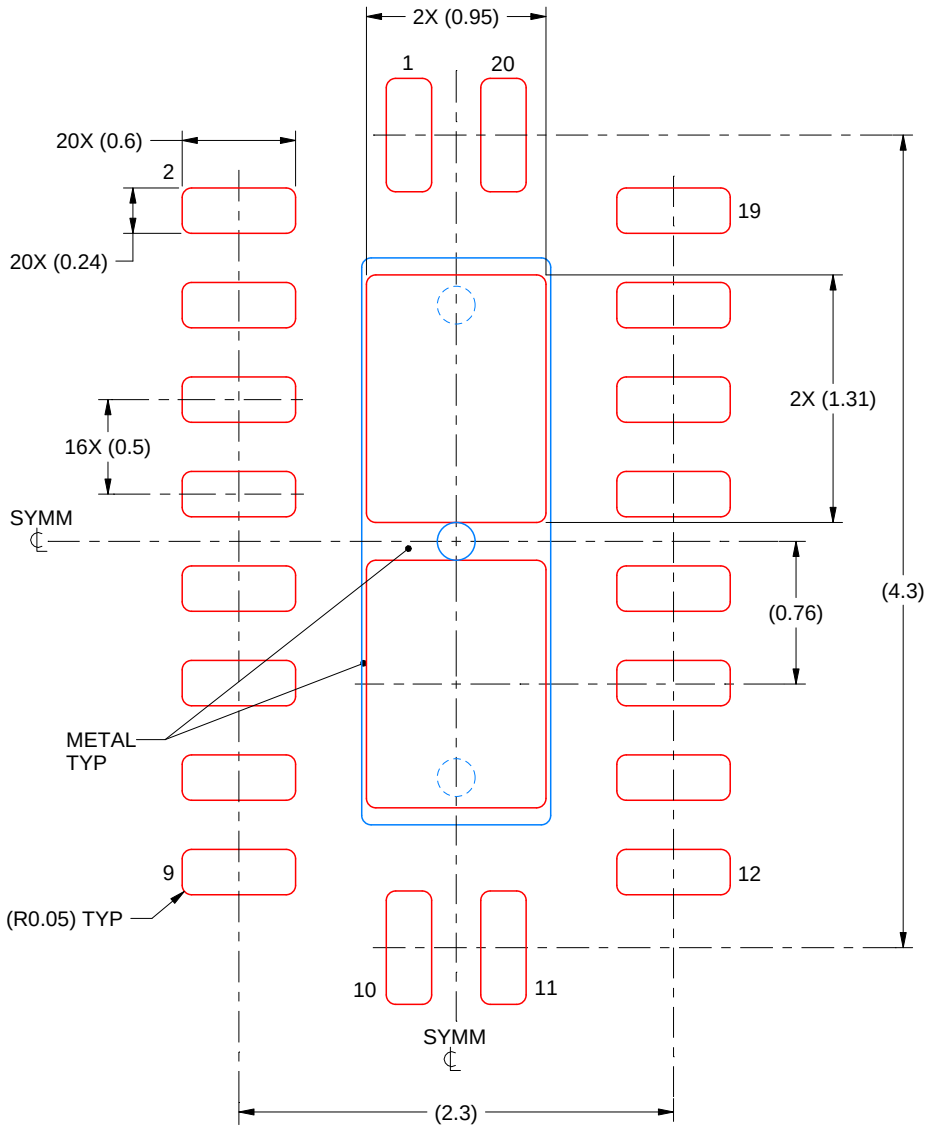


SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

NOTES: (continued)

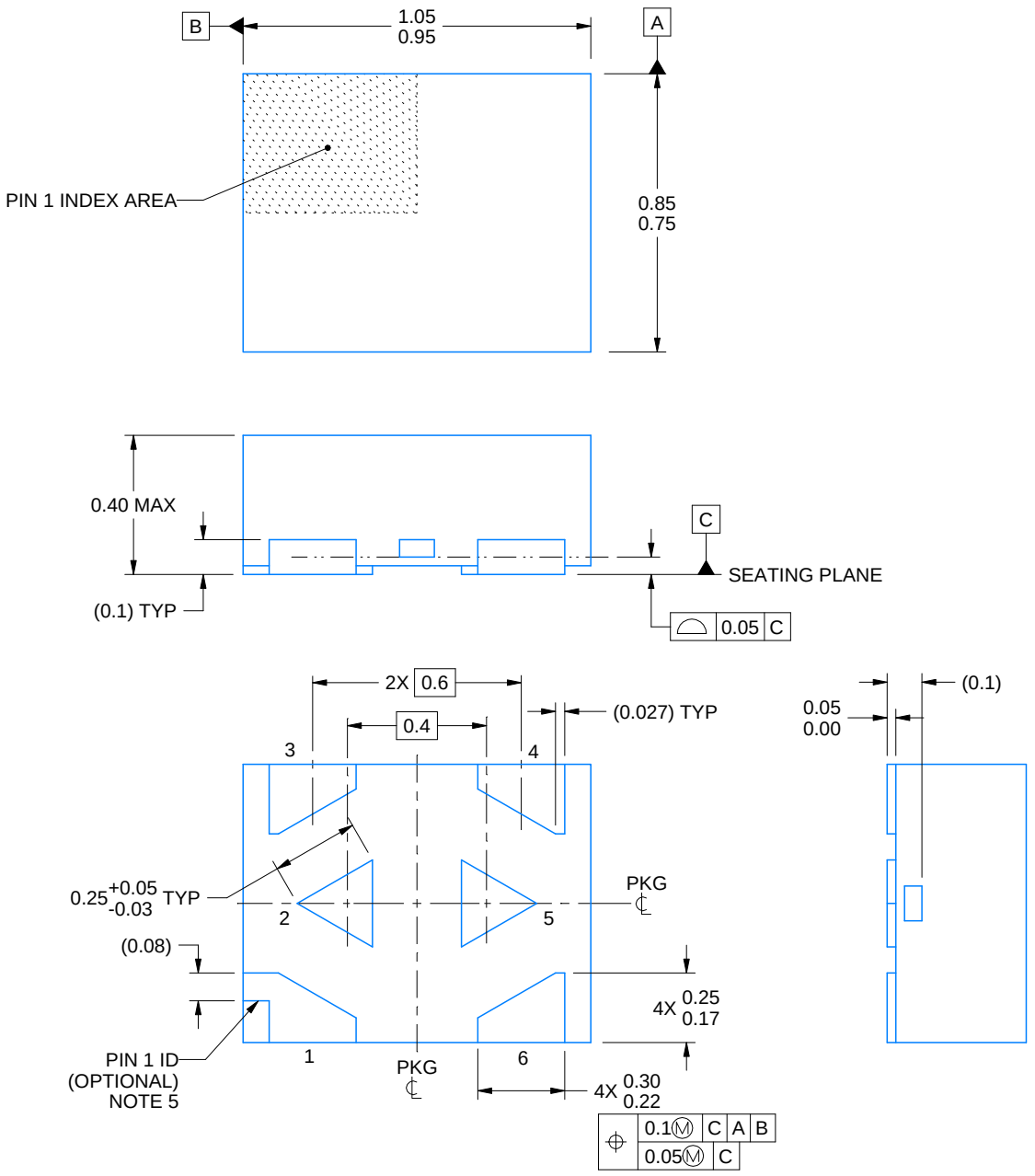
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DTQ0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

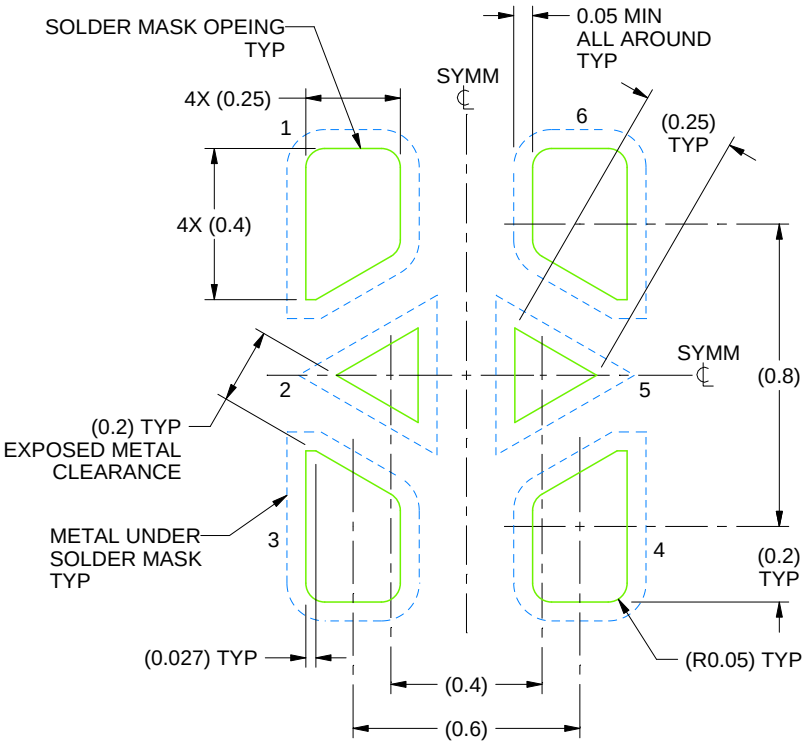
PLASTIC SMALL OUTLINE - NO LEAD



4224056/A 11/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

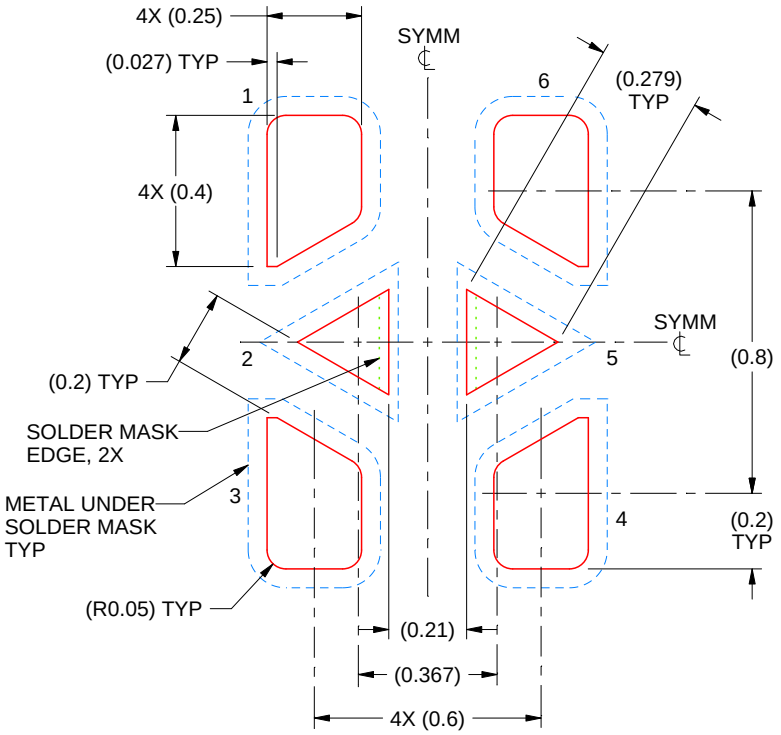


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4224056/A 11/2017

NOTES: (continued)

6. This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.07 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:50X

4224056/A 11/2017

NOTES: (continued)

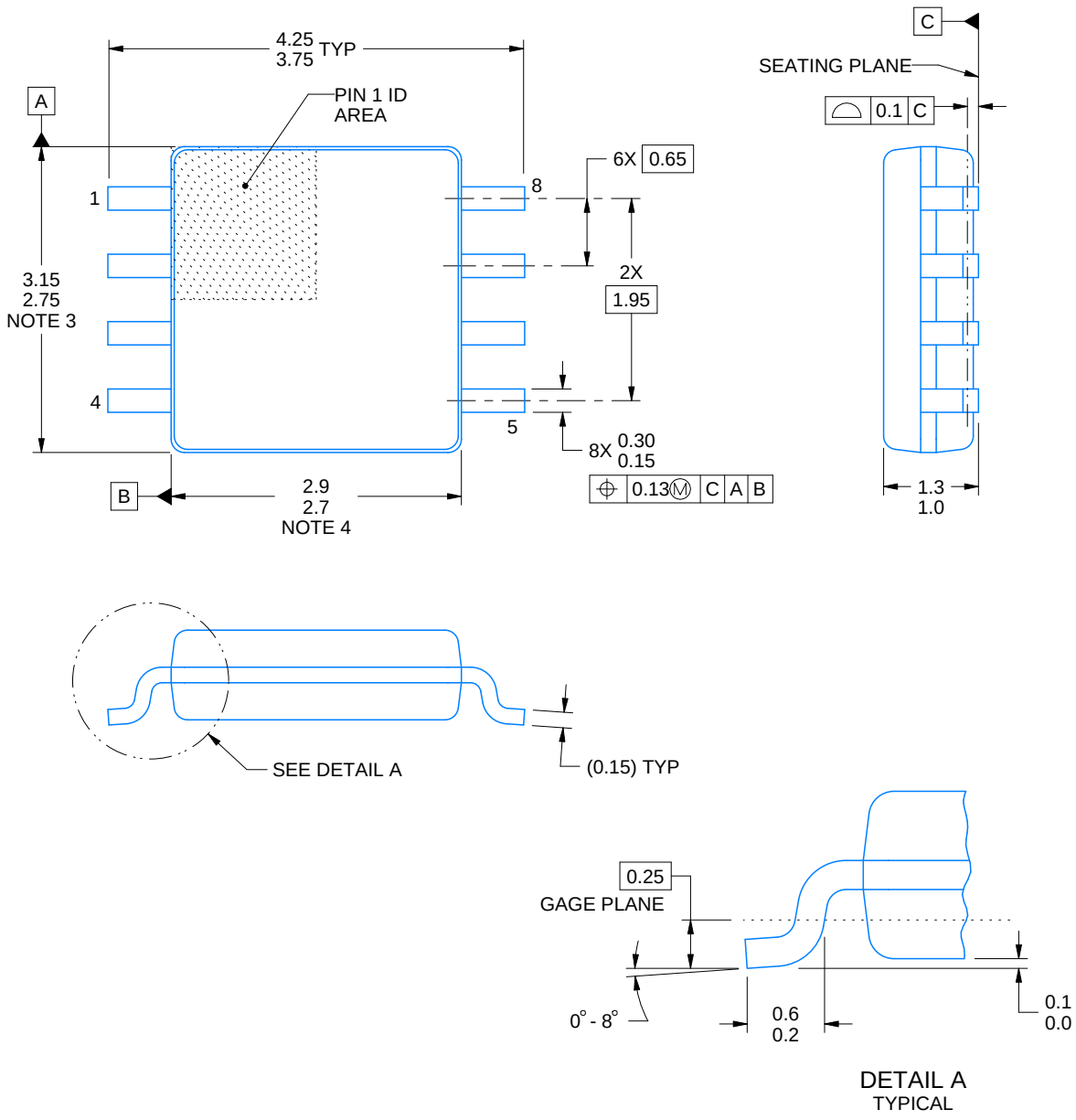
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DCT0008A

SSOP - 1.3 mm max height

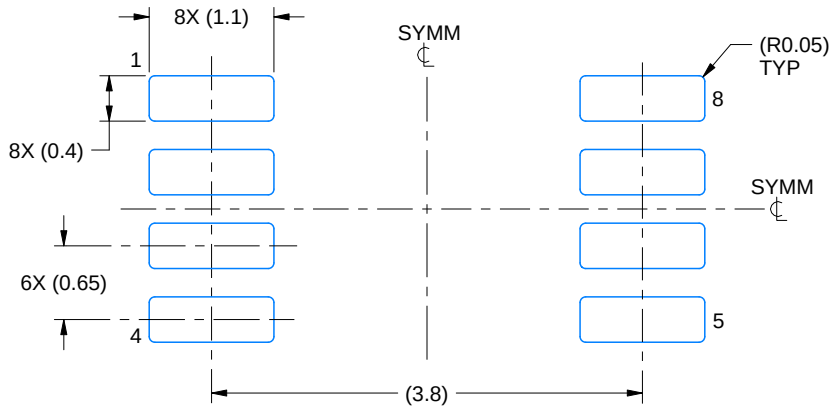
SMALL OUTLINE PACKAGE



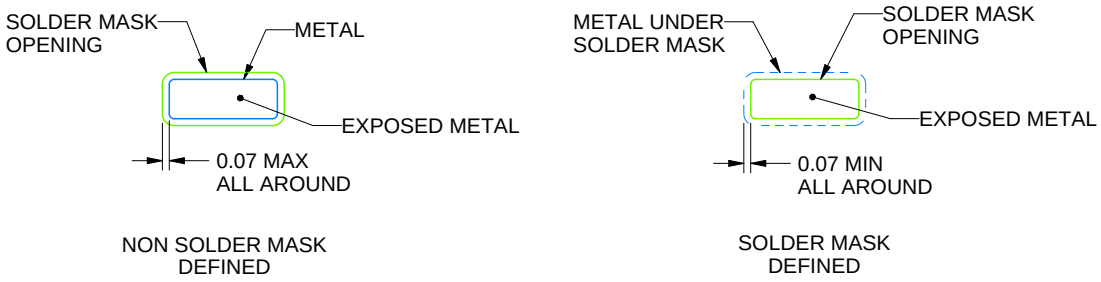
4220784/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

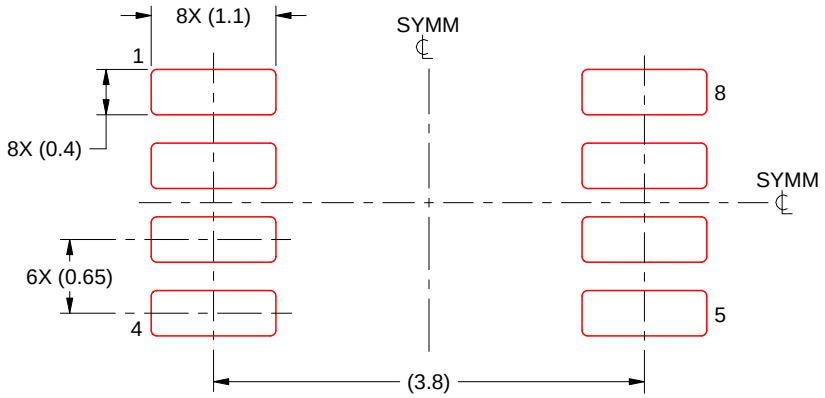


SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

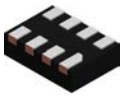
4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

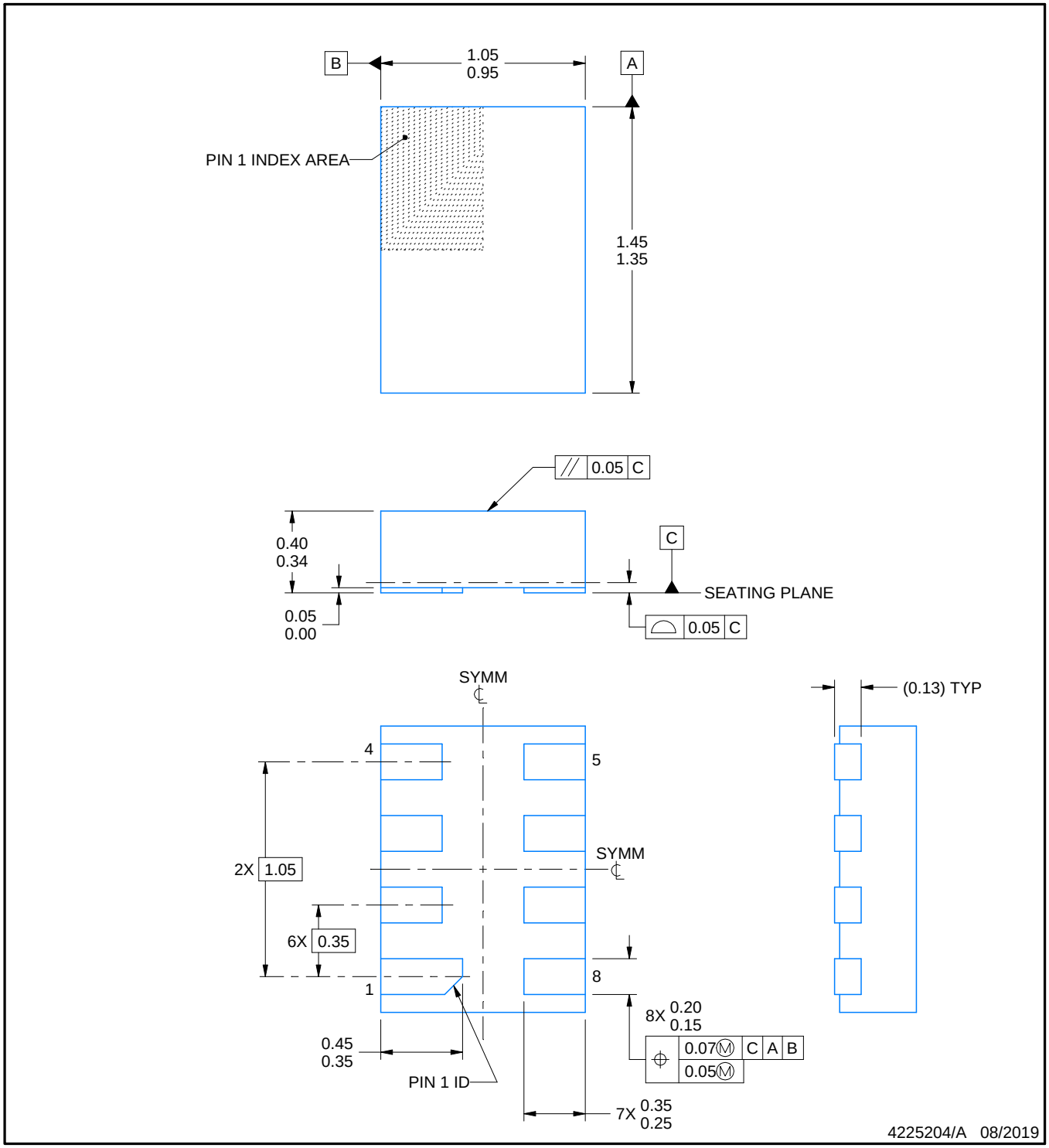
PACKAGE OUTLINE

DQE0008A



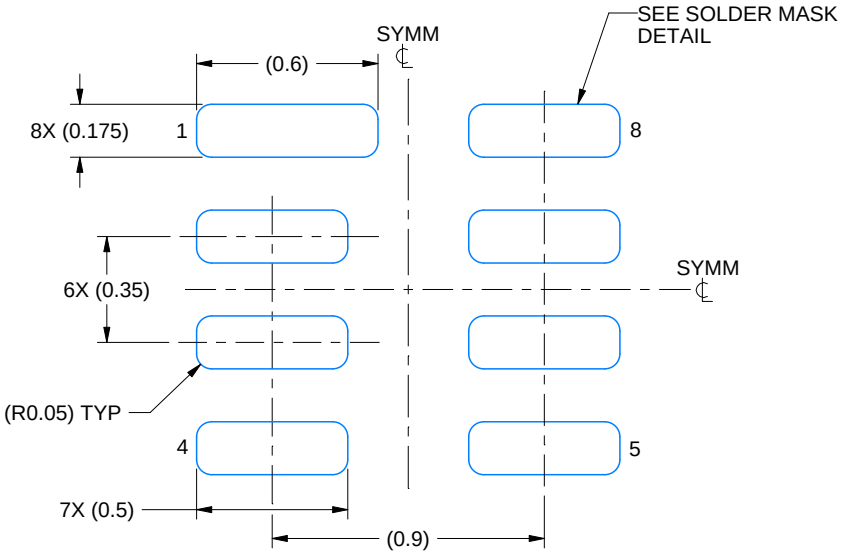
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

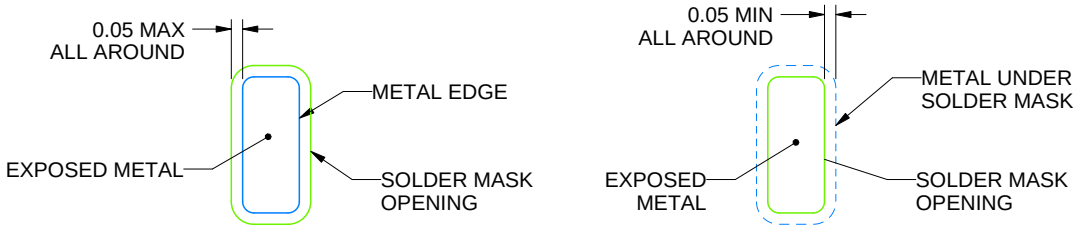


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-287 variation X2EAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X

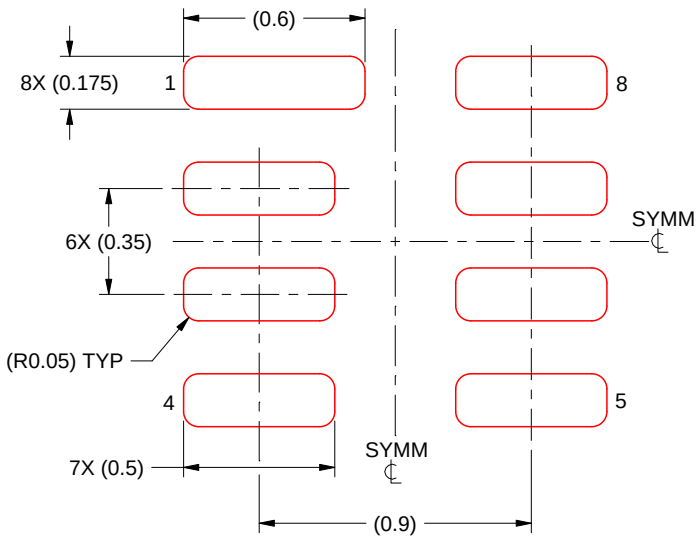


SOLDER MASK DETAILS

4225204/A 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



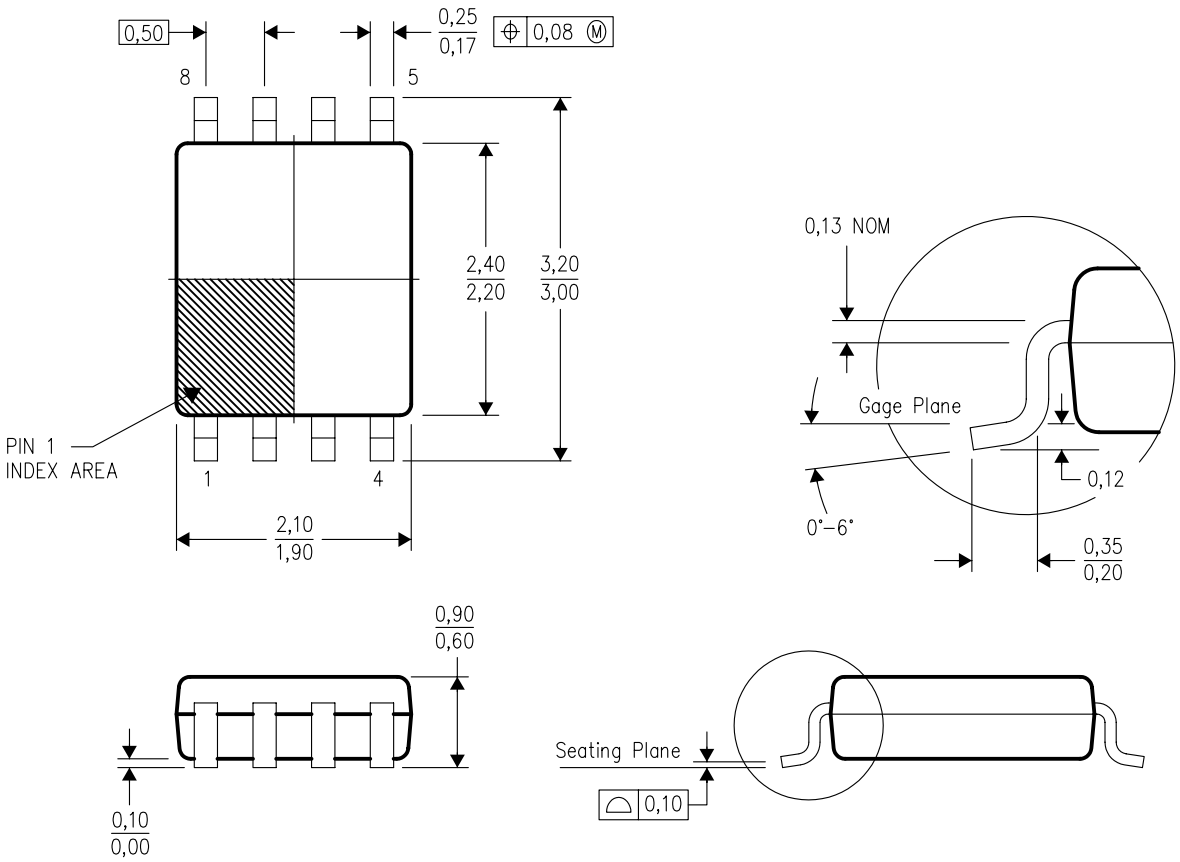
SOLDER PASTE EXAMPLE
BASED ON 0.075 MM THICK STENCIL
SCALE: 40X

4225204/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

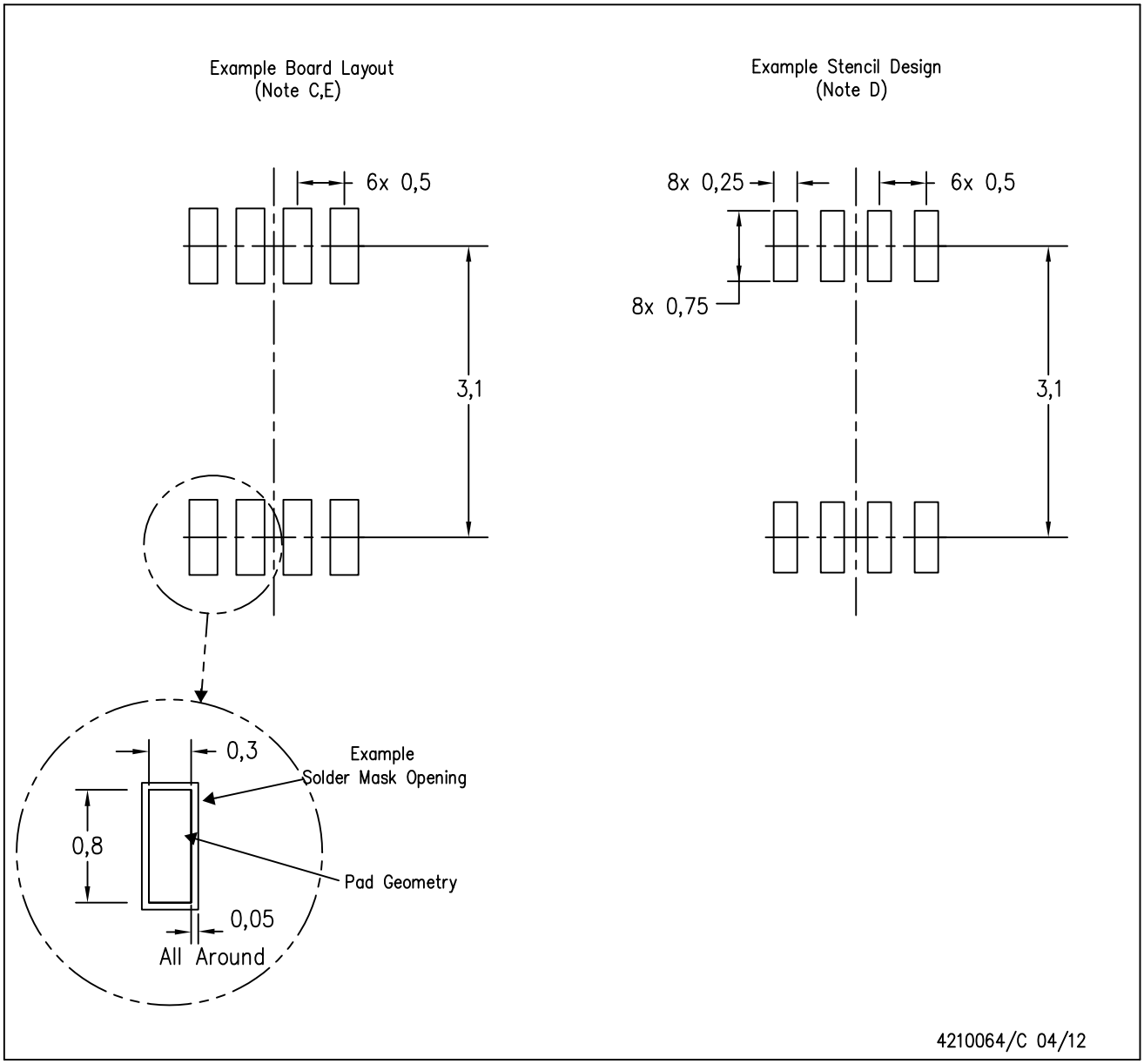
DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4200503/F 07/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



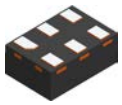
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

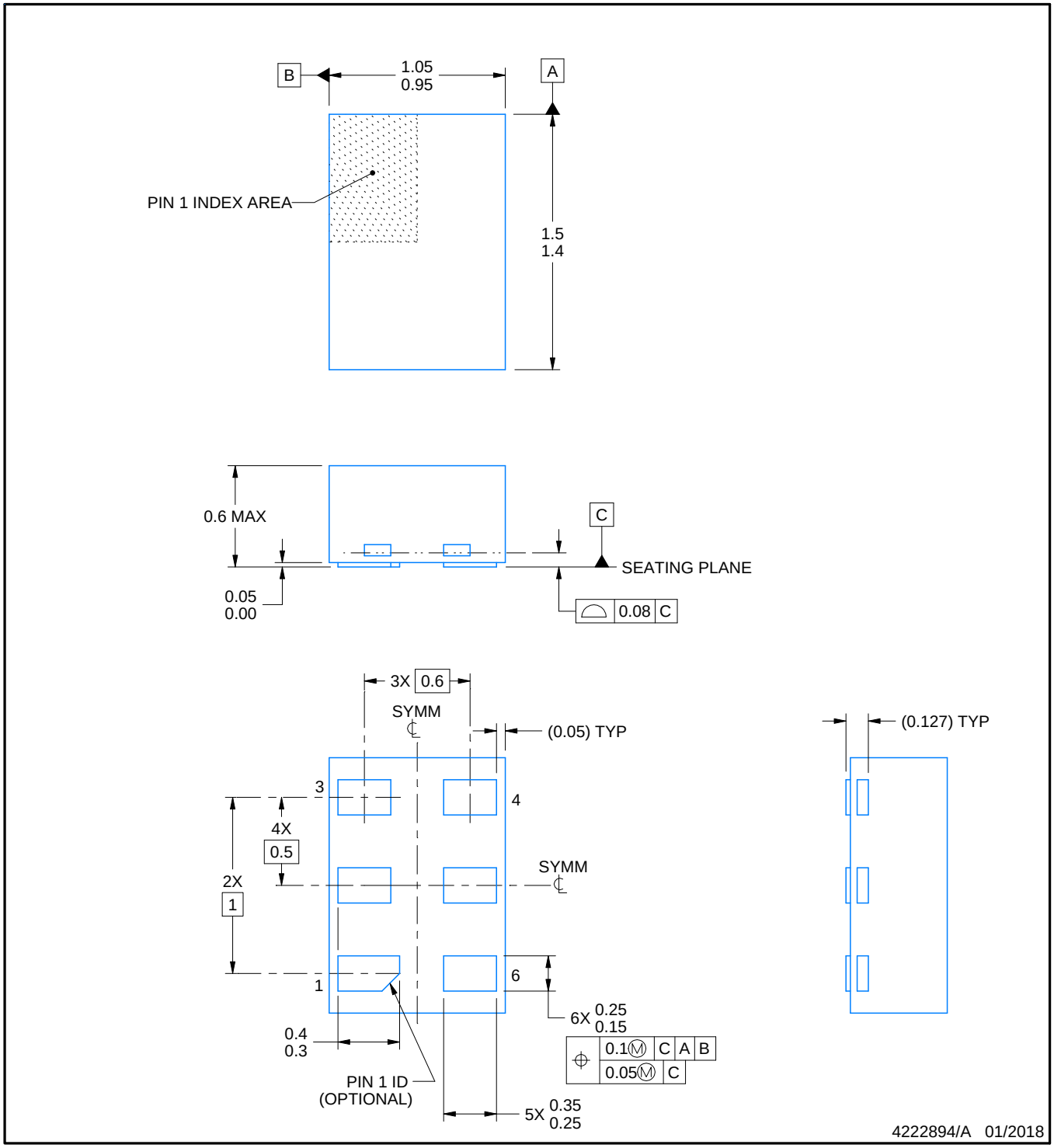
DRY0006A



PACKAGE OUTLINE

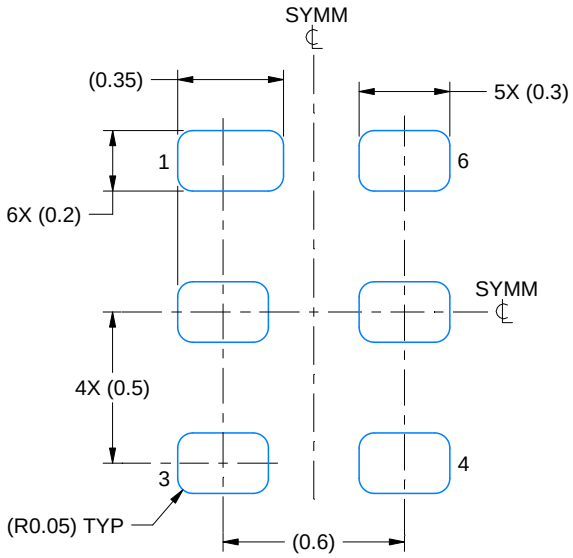
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

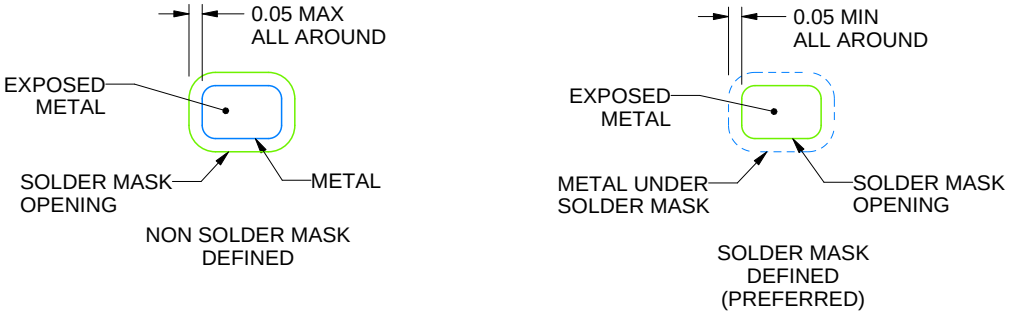


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

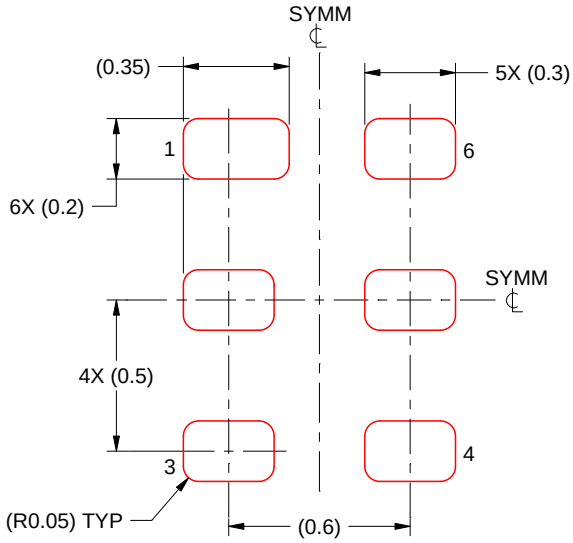
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

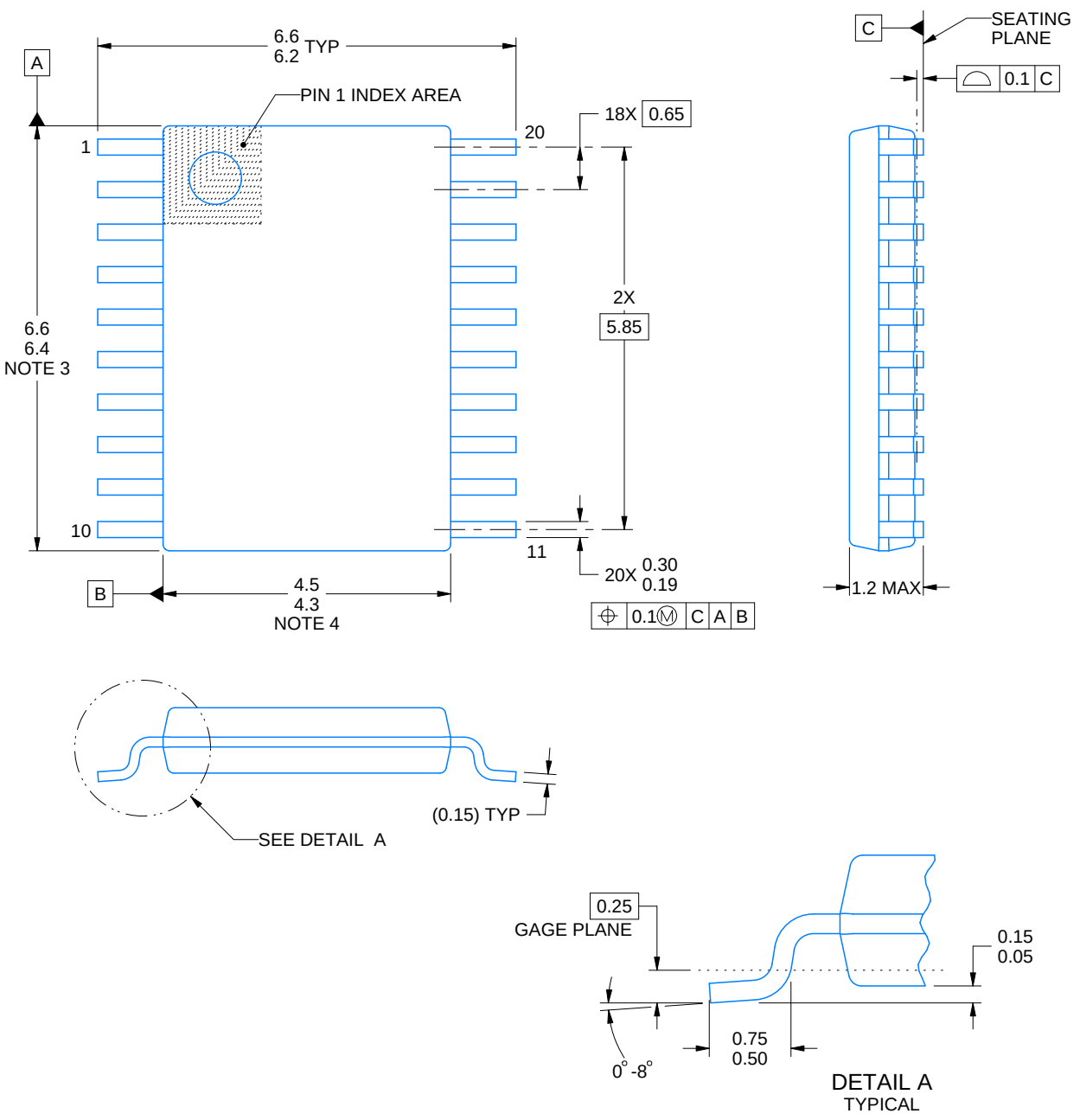
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0020A

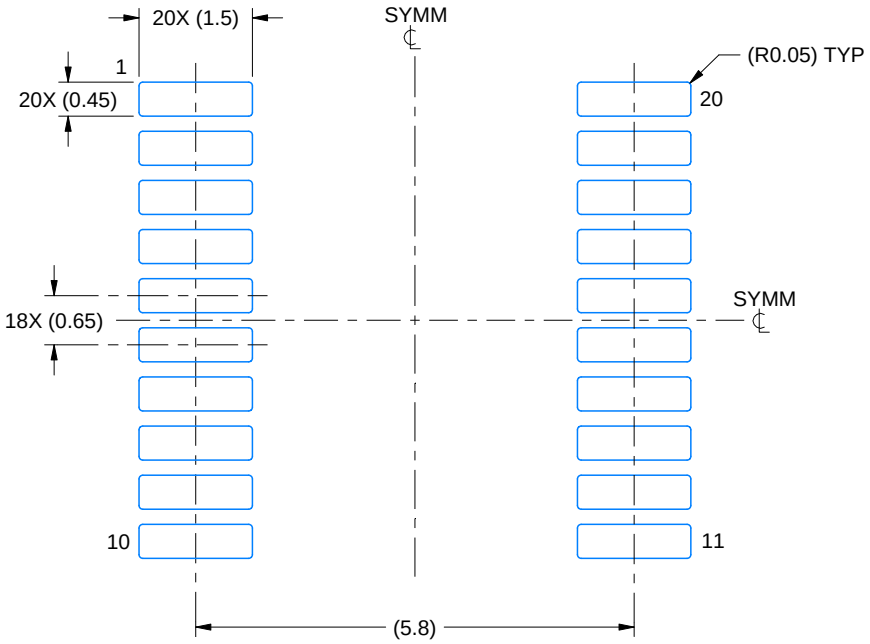
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



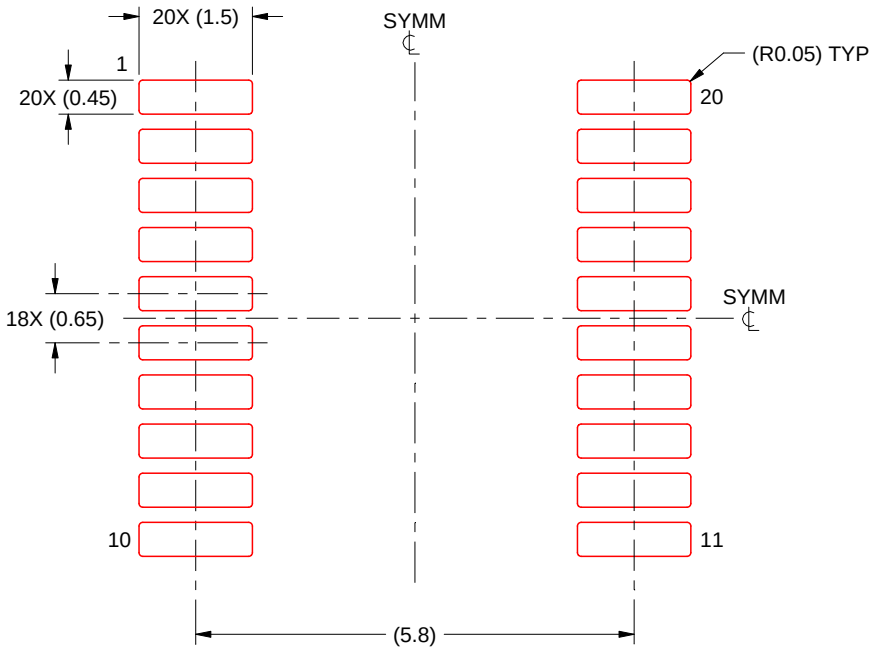
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



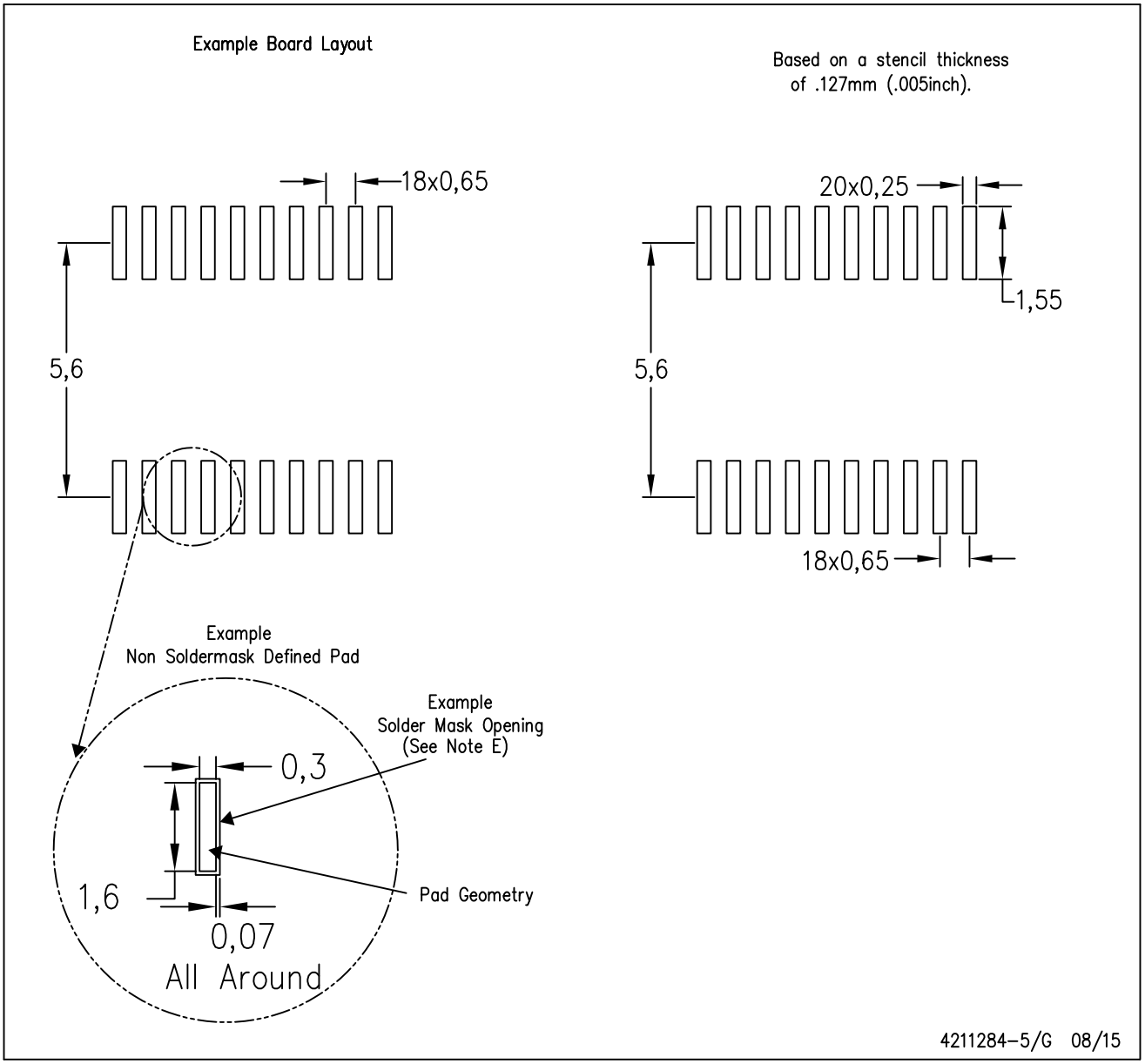
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

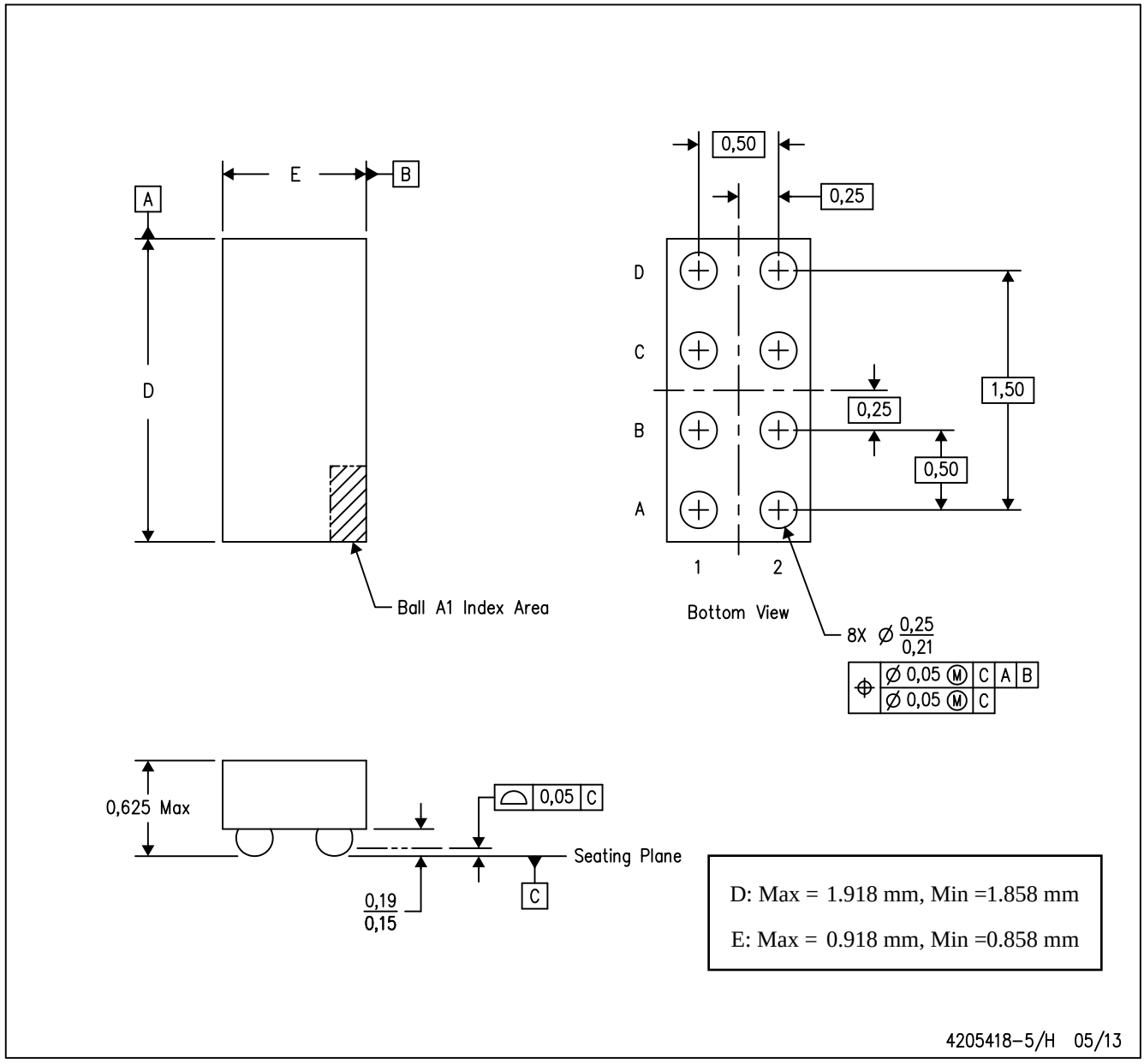
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZT (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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