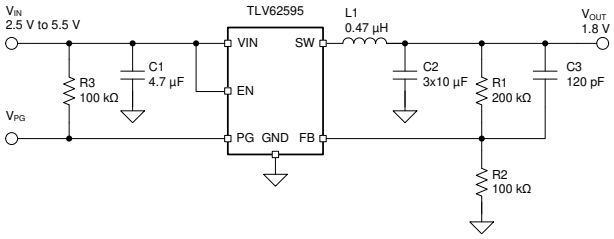
采用 1.5mm × 1.5mm QFN 封装、具有 1% 输出精度的 TLV62595 2.5V 至 5.5V 输入、4A 降压转换器

1 特性

- 效率高达 97%
- 低 $R_{DS(ON)}$ 电源开关：26mΩ/25mΩ
- 输入电压范围为 2.5V 至 5.5V
- 可调输出电压范围为 0.6V 至 4V
- 反馈电压精度为 1%（整个温度范围）
- DCS-Control 拓扑
- 可实现轻负载效率的省电模式
- 100% 占空比，可实现超低压降
- 工作静态电流为 10μA
- 典型开关频率为 2.2MHz
- 短路保护 (HICCUP)
- 有源输出放电
- 电源正常状态输出
- 热关断保护
- 使用 TLV62595 并借助 WEBENCH® Power Designer 创建定制设计方案

2 应用

- 固态硬盘
- 便携式电子产品
- IP 网络摄像头
- 工业 PC
- 多功能打印机



典型应用原理图

3 说明

TLV62595 是一款高频同步降压转换器，经优化具有解决方案尺寸紧凑和高效率两大优点。该器件集成了可提供高达 4A 输出电流的开关。在中等负载至重负载情况下，该转换器将以 2.2MHz 典型开关频率在脉宽调制 (PWM) 模式下运行。在轻负载情况下，该器件自动进入节能模式 (PSM)，从而在整个负载电流范围内保持高效率，且静态电流低至 10μA。

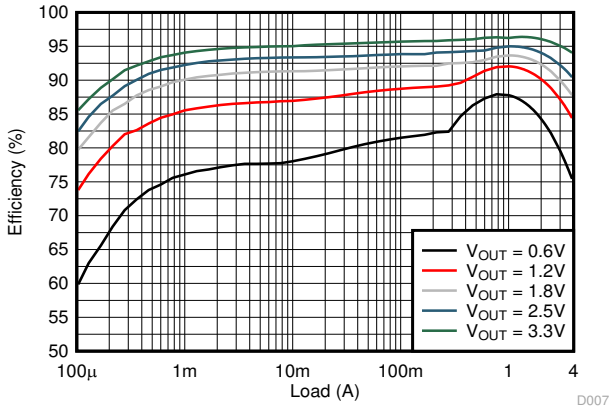
该器件基于 DCS-Control 拓扑，可提供快速瞬态响应。内部基准在 -40°C 至 125°C 的结温范围内，以 1% 的高反馈电压精度将输出电压调低至 0.6V。整个解决方案需要一个小型 470nH 电感器、一个 4.7μF 输入电容器以及三个 10μF 或一个 47μF 输出电容器。

该器件采用 6 引脚 1.5mm x 1.5mm QFN 封装，可提供高功率密度解决方案。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TLV62595	6 引脚 VSON-HR	1.5mm x 1.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



V_{IN} = 5V 时的效率

Table of Contents

4 Revision History

DATE	REVISION	NOTES
December 2020	*	Initial release

5 Pin Configuration and Functions

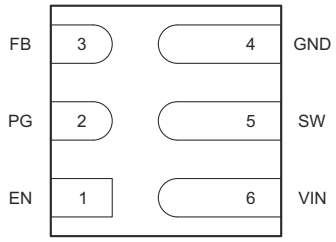


图 5-1. 6-Pin VSON-HR DMQ Package (Bottom View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Device enable pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. Do not leave floating.
PG	2	O	Power-good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave it floating.
FB	3	I	Feedback pin. For the fixed output voltage versions, this pin must be connected to the output.
GND	4		Ground pin
SW	5	PWR	Switch pin of the power stage
VIN	6	PWR	Input voltage pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN, FB, EN, PG	– 0.3	6	V
Pin voltage(2)	SW (DC)	– 0.3	V_{IN} + 0.3	V
Pin voltage(2)	SW (DC, in current limit)	– 1	V_{IN} + 0.3	
Pin voltage(2)	SW (AC, less than 10ns)(3)	– 2.5	10	V
Temperature	Operating Junction, T_J	– 40	150	°C
Temperature	Storage, T_{STG}	– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal
(3) While switching

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.5		5.5	V
V_{OUT}	Output voltage range	0.6		4.0	V
I_{OUT}	Output curent range	0		4	A
V_{PG}	Pull-up resistor voltage			5.5	V
I_{SINK_PG}	Sink current at PG pin			1	mA
T_J	Operating junction temperature	– 40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV62595 DMQ (JEDEC) 6 PINS	TLV62595EVM-794 DMQ (EVM) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	129.5	71.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	103.9	n/a	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.1	n/a	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.8	3.9	°C/W
Y_{JB}	Junction-to-board characterization parameter	33.1	38.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_J = 25 °C and V_{IN} = 5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = High, no load, device not switching		10		µA
I_{SD}	Shutdown current	EN = Low, T_J = -40℃ to 85℃		0.05		µA
V_{UVLO}	Undervoltage lock out threshold	V_{IN} falling	2.1	2.2	2.3	V
	Undervoltage lock out hysteresis	V_{IN} rising		160		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE EN						
V_{IH}	High-level threshold voltage	V_{IN} = 2.5 V to 5.5 V	1.0			V
V_{IL}	Low-level threshold voltage	V_{IN} = 2.5 V to 5.5 V			0.4	V
SOFT START, POWER GOOD						
t_{SS}	Soft start time	Time from EN high to 95% of V_{OUT} nominal		1.75		ms
V_{PG}	Power good lower threshold	V_{PG} rising, V_{FB} referenced to V_{FB} nominal		96		%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal		92		%
	Power good upper threshold	V_{PG} rising, V_{FB} referenced to V_{FB} nominal		105		%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal		110		%
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V		0.01		µA
$t_{PG,DLY}$	Power good deglitch delay	PG rising edge		100		µs
		PG falling edge		20		
OUTPUT						
V_{FB}	Feedback regulation voltage	PWM mode, 2.5 V ⩽ V_{IN} ⩽ 5.5 V, T_J = -40°C to 125°C	594	600	606	mV
$I_{FB,LKG}$	Feedback input leakage current for adjustable output voltage	V_{FB} = 0.6 V		0.01		µA
I_{DIS}	Output discharge current	V_{SW} = 0.4V; EN = LOW		400		mA
	Load regulation	I_{OUT} = 0.5 A to 3 A, V_{OUT} = 1.8 V		0.1		%/A
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance			26		mΩ
	Low-side FET on-resistance			25		mΩ
I_{LIM}	High-side FET switch current limit, DC		4.8	5.6		A
f_{SW}	PWM switching frequency	I_{OUT} = 1 A, V_{OUT} = 1.8 V		2.2		MHz

6.6 Typical Characteristics

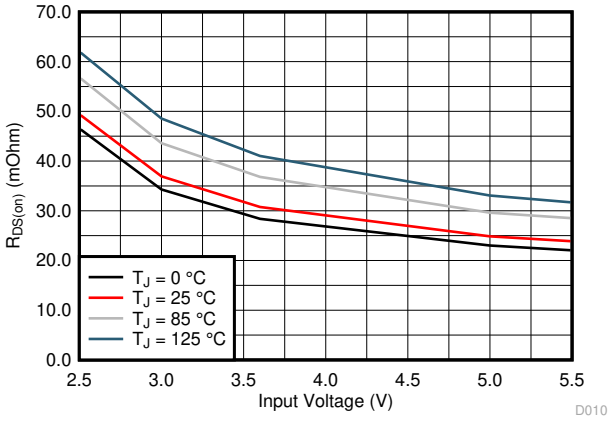


图 6-1. High-Side FET On-Resistance

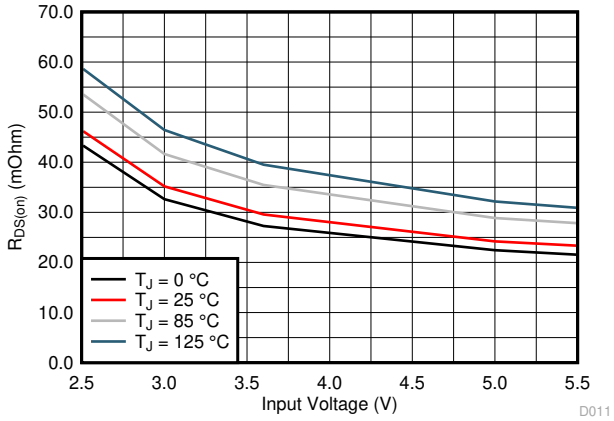


图 6-2. Low-Side FET On-Resistance

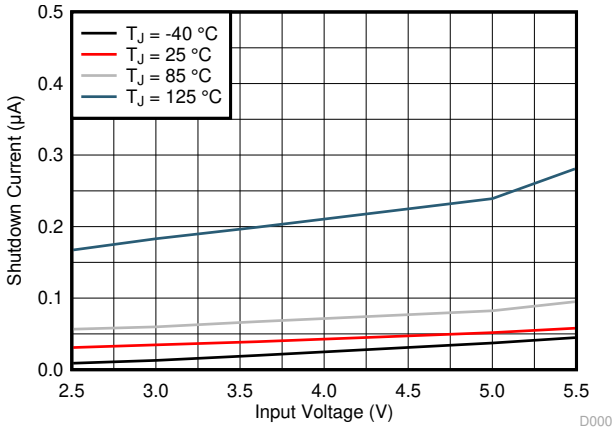


图 6-3. Shutdown Current

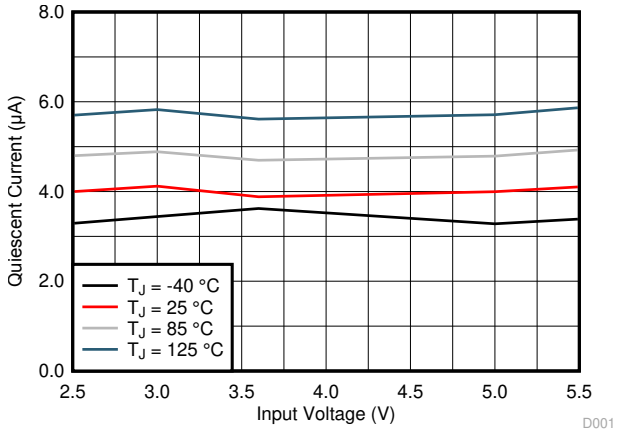


图 6-4. Quiescent Current

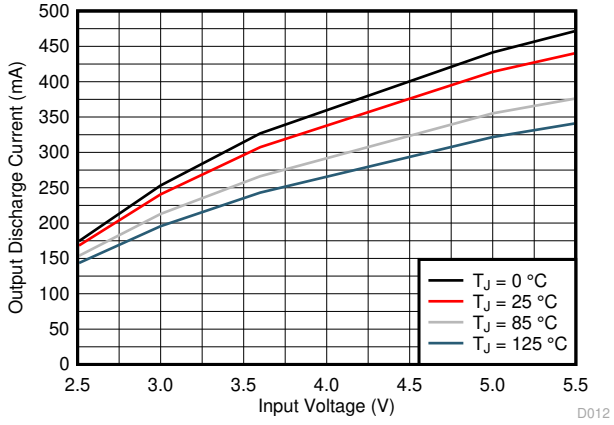


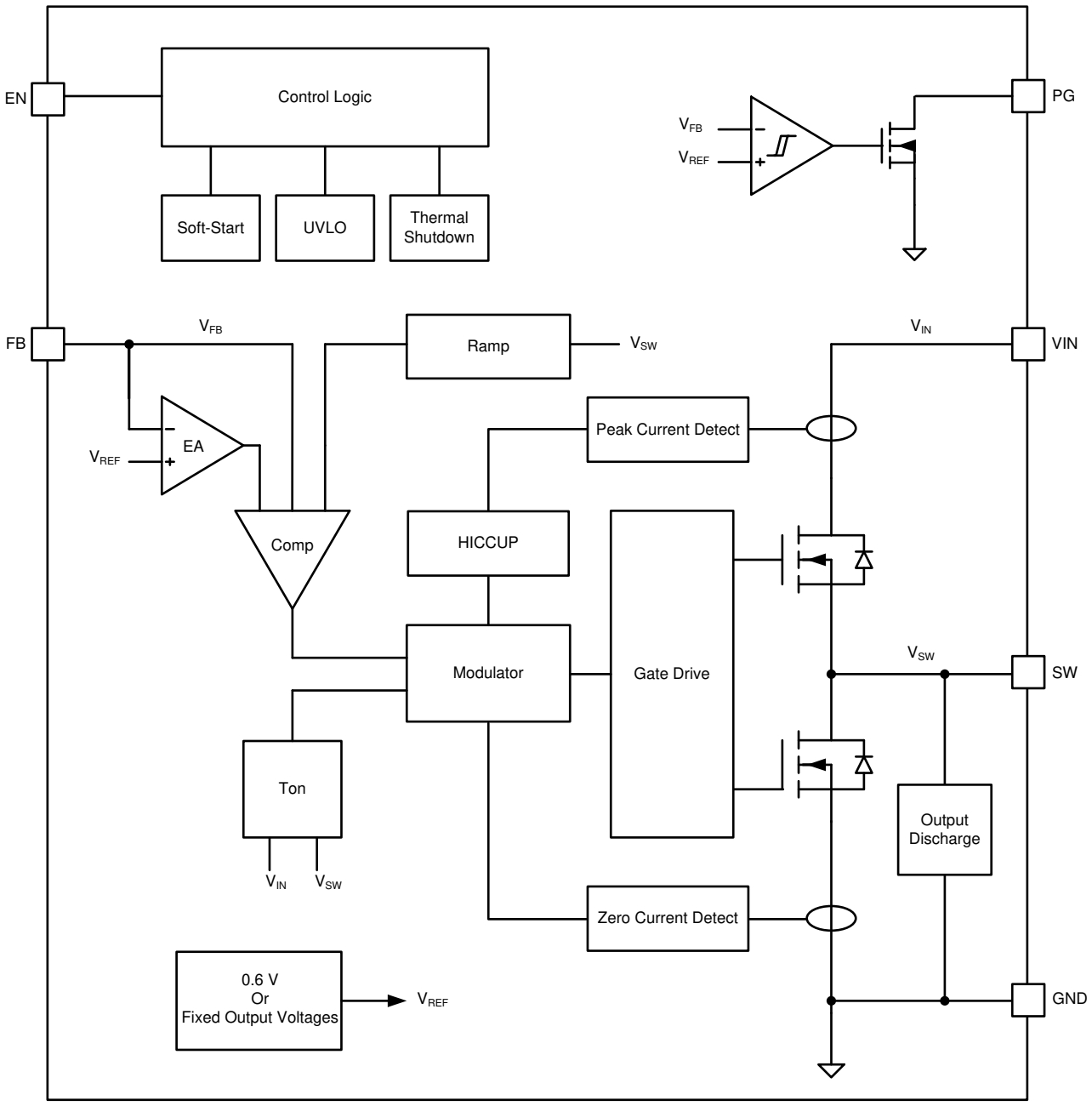
图 6-5. Output Discharge Current

7 Detailed Description

7.1 Overview

The TLV62595 are synchronous step-down converters based on the DCS-Control topology with an adaptive constant on-time control and a stabilized switching frequency. It operates in PWM (pulse width modulation) mode for medium to heavy loads and in PSM (power save mode) at light load conditions, keeping the output voltage ripple small. The nominal switching frequency is about 2.2 MHz with a small and controlled variation over the input voltage range. As the load current decreases, the converter enters PSM, reducing the switching frequency to keep efficiency high over the entire load current range. Since combining both PWM and PSM within a single building block, the transition between modes is seamless and without effect on the output voltage. The devices offer both excellent dc voltage and fast load transient regulation, combined with a very low output voltage ripple.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Pulse Width Modulation (PWM) Operation

At load currents larger than half the inductor ripple current, the device operates in pulse width modulation in continuous conduction mode (CCM). The PWM operation is based on an adaptive constant on-time control with stabilized switching frequency. To achieve a stable switching frequency in a steady state condition, the on-time is calculated as:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 450ns \tag{1}$$

7.3.2 Power Save Mode (PSM) Operation

To maintain high efficiency at light loads, the device enters power save mode (PSM) at the boundary to discontinuous conduction mode (DCM). This happens when the output current becomes smaller than half of the ripple current of the inductor. The device operates now with a fixed on-time and the switching frequency further decreases proportionally to the load current. It can be calculated as:

$$f_{PSM} = \frac{2 \cdot I_{OUT}}{T_{ON}^2 \cdot \frac{V_{IN}}{V_{OUT}} \left[\frac{V_{IN} - V_{OUT}}{L} \right]} \tag{2}$$

In PSM, the output voltage rises slightly above the nominal target, which can be minimized using larger output capacitance. At duty cycles larger than 90%, the device may not enter PSM. The device maintains output regulation in PWM mode.

7.3.3 Minimum Duty Cycle and 100% Mode Operation

There is no limitation for small duty cycles, since even at very low duty cycles, the switching frequency is reduced as needed to always ensure a proper regulation.

If the output voltage level comes close to the input voltage, the device enters 100% mode. While the high-side switch is constantly turned on, the low-side switch is switched off. The difference between VIN and VOUT is determined by the voltage drop across the high-side FET and the dc resistance of the inductor. The minimum VIN that is needed to maintain a specific VOUT value is estimated as:

$$V_{IN,MIN} = V_{OUT} + I_{OUT,MAX} \times (R_{DS(on)} + R_L) \tag{3}$$

where

- $V_{IN,MIN}$ = Minimum input voltage to maintain an output voltage
- $I_{OUT,MAX}$ = Maximum output current
- $R_{DS(on)}$ = High-side FET ON-resistance
- R_L = Inductor ohmic resistance (DCR)

7.3.4 Soft Start

About 250 μs after EN goes high, the internal soft-start circuitry controls the output voltage during start-up. This avoids excessive inrush current and ensures a controlled output voltage ramp. It also prevents unwanted voltage drops from high-impedance power sources or batteries. The TLV62595 can start into a pre-biased output.

7.3.5 Switch Current Limit and HICCUP Short-Circuit Protection

The switch current limit prevents the device from drawing excessive current in case of externally-caused overcurrent or short circuit condition. Due to an internal propagation delay (typically 60 ns), the actual ac peak current can exceed the static current limit during that time.

If the current limit threshold is reached, the device delivers its maximum output current. Detecting this condition for 32 switching cycles (about 13 µs), the device turns off the high-side MOSFET for about 100 µs which allows the inductor current to decrease through the low-side MOSFET's body diode and then restart again with a soft start cycle. As long as the overload condition is present, the device hiccups that way, limiting the output power.

7.3.6 Undervoltage Lockout

The undervoltage lockout (UVLO) function prevents misoperation of the device, if the input voltage drops below the UVLO threshold. It is set to about 2.2 V with a hysteresis of typically 160 mV.

7.3.7 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 150°C (typ.), the device goes in thermal shutdown with a hysteresis of typically 20°C. Once the TJ has decreased enough, the device resumes normal operation.

7.4 Device Functional Modes

7.4.1 Enable, Disable and Output Discharge

The device starts operation, when Enable (EN) is set High. The input threshold levels are typically 0.9 V for rising and 0.7 V for falling signals. Do not leave EN floating. Shutdown is forced if EN is pulled low with a shutdown current of typically 50 nA. During shutdown, the internal power MOSFETs as well as the entire control circuitry, are turned off and the output voltage is actively discharged through the SW pin by a current sink. Therefore VIN must remain present for the discharge to function.

7.4.2 Power Good

The TLV62595 has a built-in power good (PG) function. The PG pin goes high impedance, when the output voltage has reached its nominal value. Otherwise, including when disabled, in UVLO or in thermal shutdown, PG is low (see 表 7-1). The PG function is formed with a window comparator, which has an upper and lower voltage threshold. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pullup resistor connecting to any voltage rail less than 5.5 V.

The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used. The PG rising edge has a 100-µs blanking time and the PG falling edge has a deglitch delay of 20 µs.

表 7-1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, $V_{FB} \geqslant 0.576$ V	√	
	EN = High, $V_{FB} \leqslant 0.552$ V		√
	EN = High, $V_{FB} \leqslant 0.63$ V	√	
	EN = High, $V_{FB} \geqslant 0.66$ V		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$0.7\text{ V} < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} < 0.7$ V	√	

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

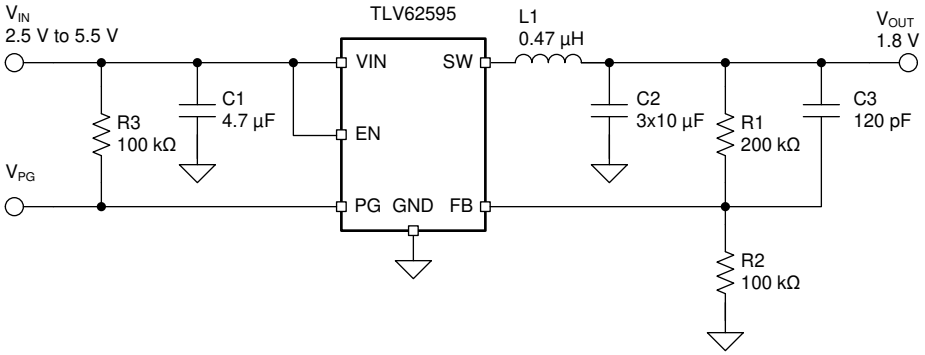


图 8-1. Typical Application of TLV62595

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage, TLV62595	2.5 V to 5.5 V
Output voltage	1.8 V
Output ripple voltage	<20 mV
Maximum output current, TLV62595	4 A

表 8-2 lists the components used for the example.

表 8-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	4.7 µF, Ceramic capacitor, 6.3 V, X7R, size 0603, JMK107BB7475MA	Taiyo Yuden
C2	3 x 10 µF, Ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106MA73D	Murata
C3	120 pF, Ceramic capacitor, 50 V, size 0402	Std
L1	0.47 µH, Power Inductor, XFL4015-471MEB	Coilcraft
R1	Depending on the output voltage, 1%, size 0402	Std
R2	100 kΩ, Chip resistor, 1/16 W, 1%, size 0402	Std
R3	100 kΩ, Chip resistor, 1/16 W, 1%, size 0402	Std

1. See the *Third-Party Products Disclaimer*.

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TLV62595 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to 方程式 4:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R2 \times \left(\frac{V_{OUT}}{0.6V} - 1 \right) \quad (4)$$

R2 must not be higher than 100 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. 方程式 5 shows how to compute the value of the feedforward capacitor for a given R2 value. For the recommended 100 k value for R2, a 120-pF feedforward capacitor is used.

$$C3 = \frac{12\mu}{R2} \quad (5)$$

For the fixed output voltage versions, connect the FB pin to the output. R1, R2, and C3 are not needed. The fixed output voltage devices have an internal feedforward capacitor.

8.2.2.3 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify this process, 表 8-3 outlines possible inductor and capacitor value combinations for most applications. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

表 8-3. Matrix of Output Capacitor and Inductor Combinations, TLV62595

NOMINAL L [µH](2)	NOMINAL C_{OUT} [µF](3)			
	10	2 x 10 or 22	47	100
0.33				
0.47	+	+(1)	+	
1.0				

(1) This LC combination is the standard value and recommended for most applications.
(2) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –35%.

表 8-4. Matrix of Output Capacitor and Inductor Combinations, TLV62595

NOMINAL L [µH](2)	NOMINAL C_{OUT} [µF](3)			
	22	3 x 10	47	100
0.33				
0.47		+(1)	+	+
1.0				

8.2.2.4 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 方程式 6 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (6)$$

where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor. 表 8-5 lists recommended inductors.

表 8-5. List of Recommended Inductors

INDUCTANCE [µH]	CURRENT RATING [A]	DIMENSIONS [L x W x H mm]	MAX. DC RESISTANCE [mΩ]	MFR PART NUMBER(1)
0.47	4.8	2.0 x 1.6 x 1.0	32	HTEN20161T-R47MDR, Cyntec
	4.6	2.0 x 1.2 x 1.0	25	HTEH20121T-R47MSR, Cyntec
	4.8	2.0 x 1.6 x 1.0	32	DFE201610E - R47M, MuRata
	4.8	2.0 x 1.6 x 1.0	32	DFE201210S - R47M, MuRata
	5.1	2.0 x 1.6 x 1.0	34	TFM201610ALM-R47MTAA, TDK
	5.2	2.0 x 1.6 x 1.0	25	TFM201610ALC-R47MTAA, TDK
	6.6	4.0 x 4.0 x 1.6	8.36	XFL4015-471ME, Coilcraft
	8.0	3.5 x 3.2 x 2.0	10.85	XEL3520-471ME, Coilcraft
	6.8	4.5 x 4 x 1.8	11.2	WE-LHMI-744373240047, Würth

(1) See *Third-party Products Disclaimer*.

8.2.2.5 Capacitor Selection

The input capacitor is the low-impedance energy source for the converters which helps to provide stable operation. A low-ESR multilayer ceramic capacitor is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins. For most applications, a minimum effective input capacitance of 3 µF should be present, though a larger value reduces input current ripple.

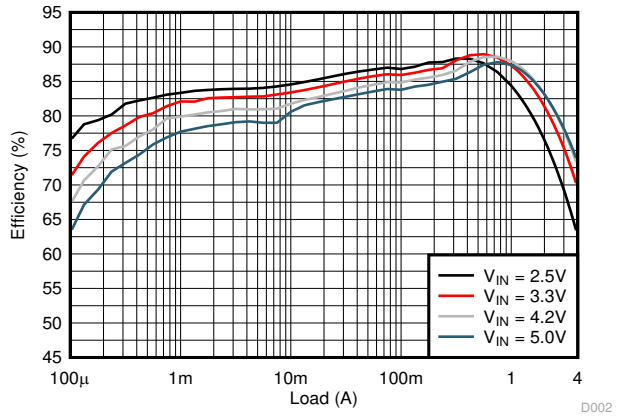
The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends

using X7R or X5R dielectrics. Considering the DC-bias derating the capacitance, the minimum effective output capacitance is 20 µF for TLV62595.

A feedforward capacitor is required for the adjustable version, as described in 节 8.2.2.2. This capacitor is not required for the fixed output voltage versions.

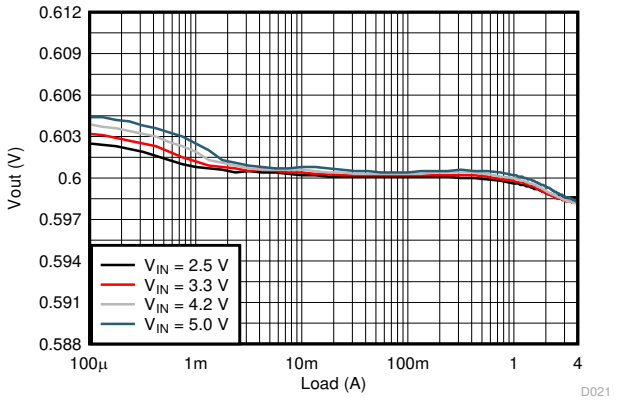
8.2.3 Application Curves

V_{IN} = 5.0 V, V_{OUT} = 1.8 V, T_A = 25°C, BOM = 表 8-2, unless otherwise noted.



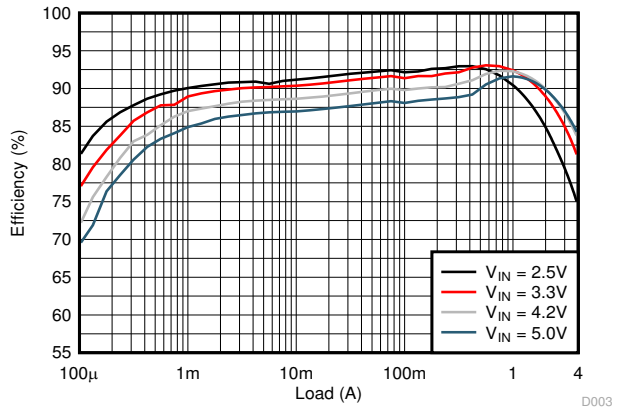
V_{OUT} = 0.6 V

图 8-2. Efficiency



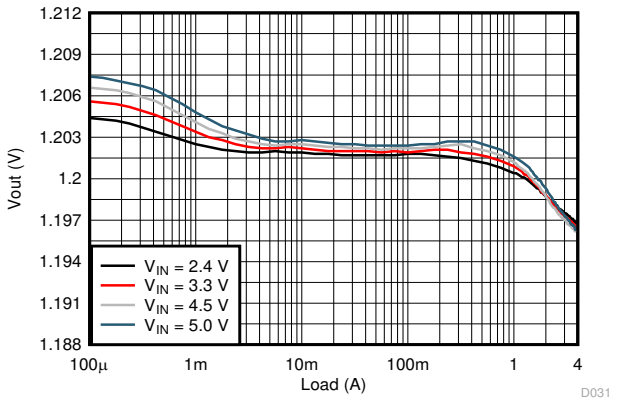
V_{OUT} = 0.6 V

图 8-3. Load Regulation



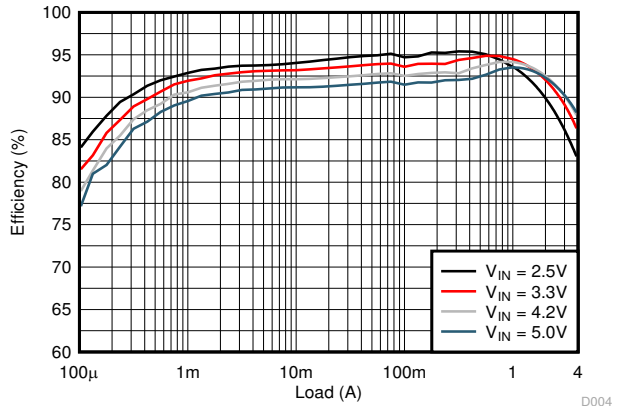
V_{OUT} = 1.2 V

图 8-4. Efficiency



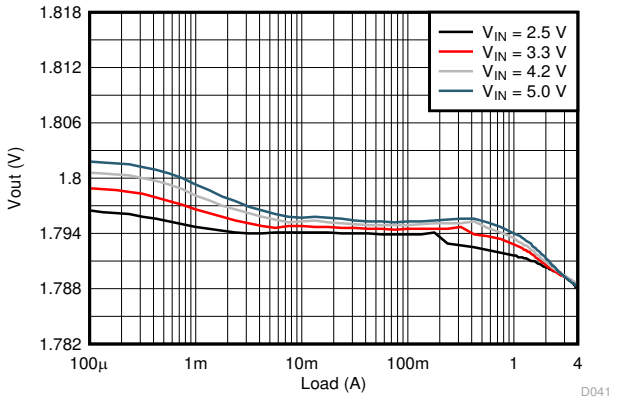
V_{OUT} = 1.2 V

图 8-5. Load Regulation



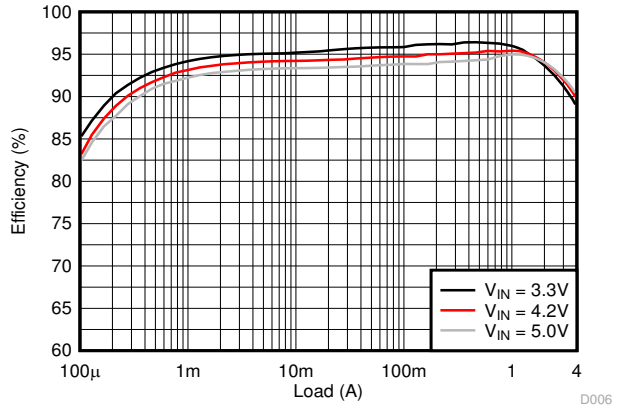
V_{OUT} = 1.8 V

图 8-6. Efficiency



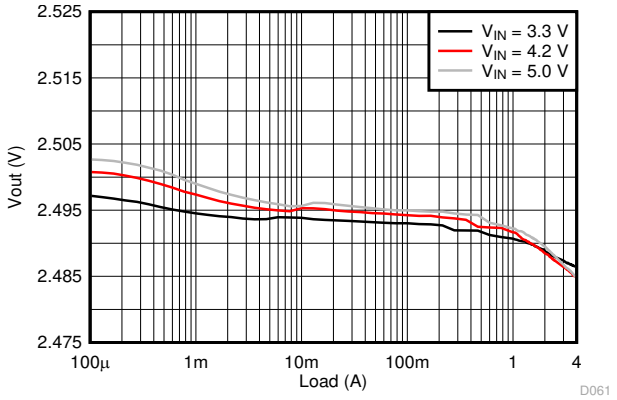
V_{OUT} = 1.8 V

图 8-7. Load Regulation



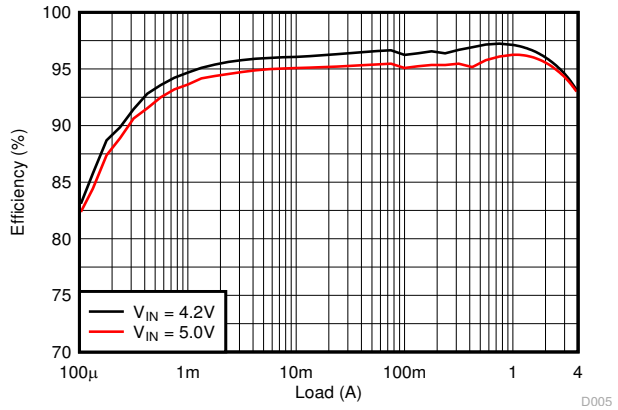
V_{OUT} = 2.5 V

图 8-8. Efficiency



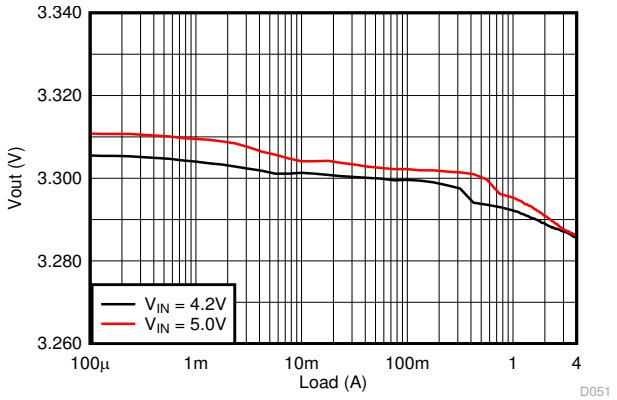
V_{OUT} = 2.5 V

图 8-9. Load Regulation



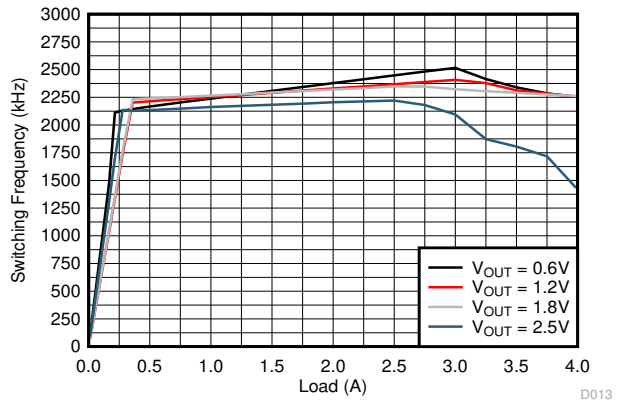
V_{OUT} = 3.3 V

图 8-10. Efficiency



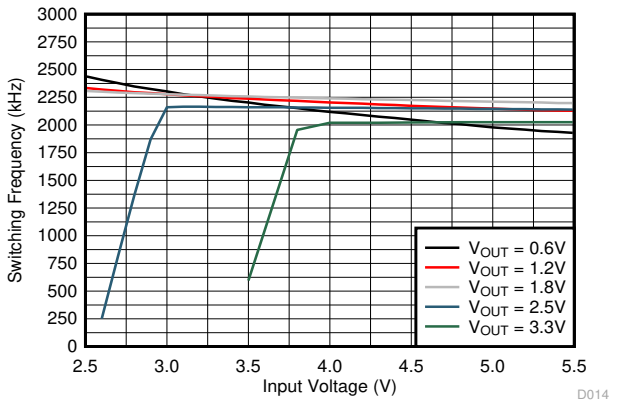
V_{OUT} = 3.3 V

图 8-11. Load Regulation



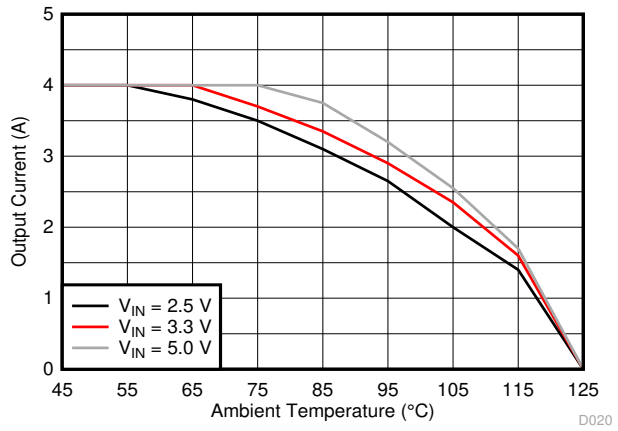
V_{IN} = 3.3 V

图 8-12. Switching Frequency



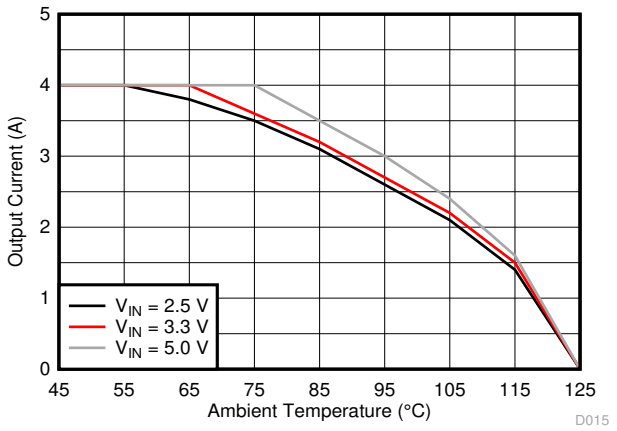
I_{OUT} = 1.0 A

图 8-13. Switching Frequency



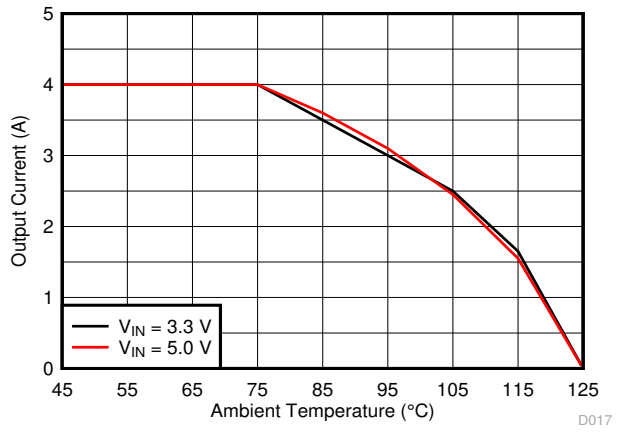
V_{OUT} = 1.2 V θ_{JA}= 71.4 °C/W

图 8-14. Thermal Derating



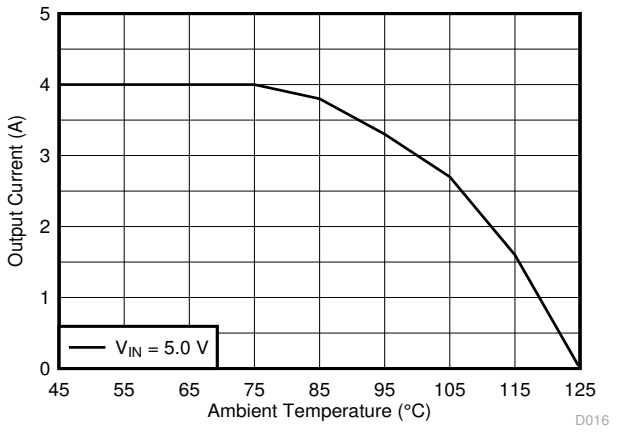
V_{OUT} = 1.8 V θ_{JA}= 71.4 °C/W

图 8-15. Thermal Derating



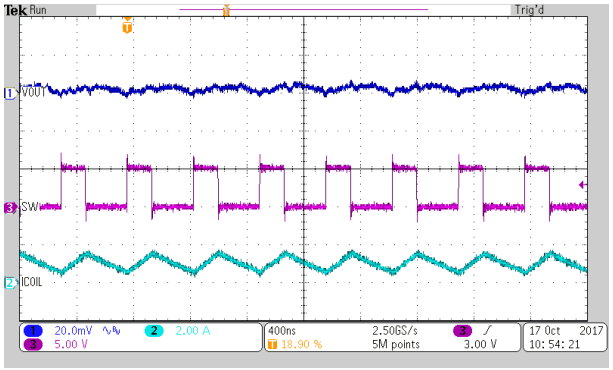
V_{OUT} = 2.5 V θ_{JA}= 71.4 °C/W

图 8-16. Thermal Derating



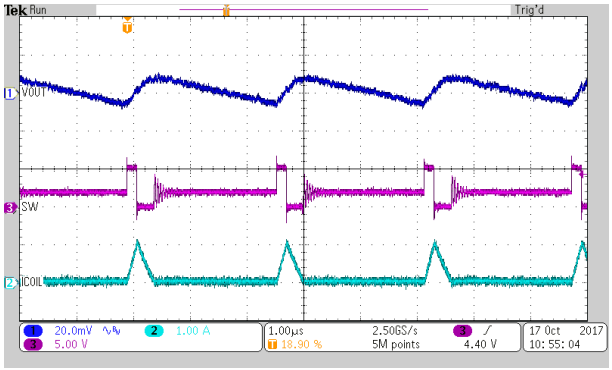
V_{OUT} = 3.3 V θ_{JA}= 71.4 °C/W

图 8-17. Thermal Derating



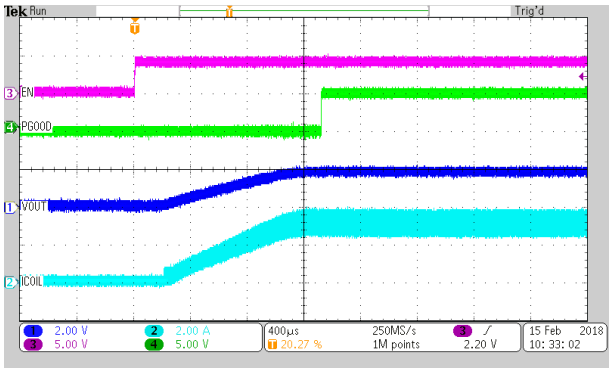
I_{OUT} = 1.0 A

图 8-18. PWM Operation



I_{OUT} = 0.1 A

图 8-19. PSM Operation



Load = 0.6 Ω

图 8-20. Start-up with Load

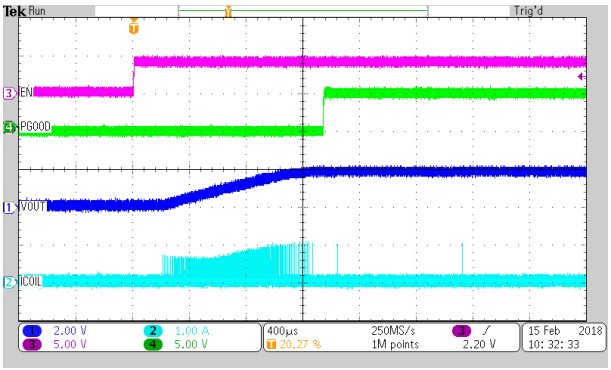
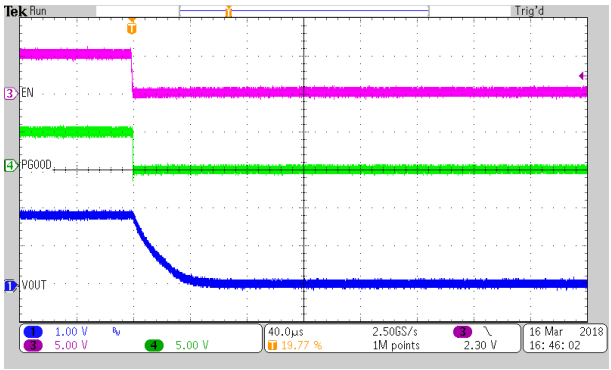


图 8-21. Startup with No Load



Load = 1.8 Ω

图 8-22. Disable, Active Output Discharge

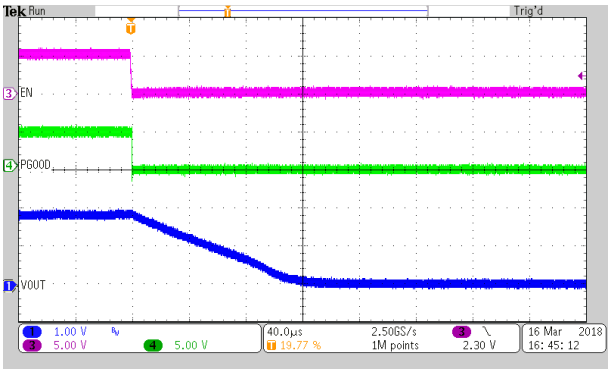
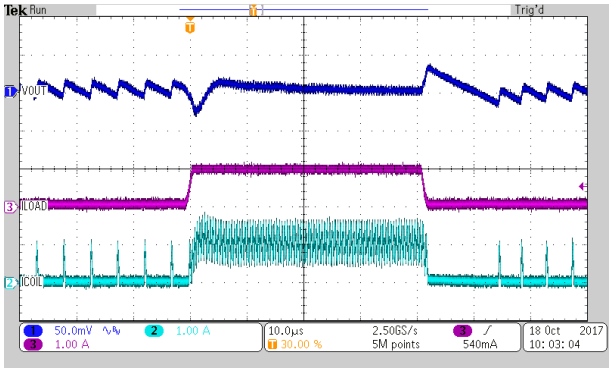
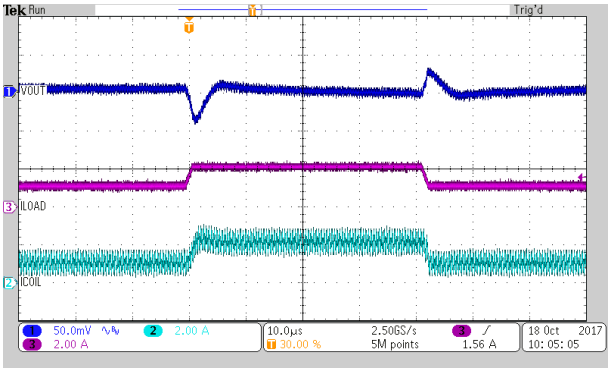


图 8-23. Disable, Active Output Discharge at No Load



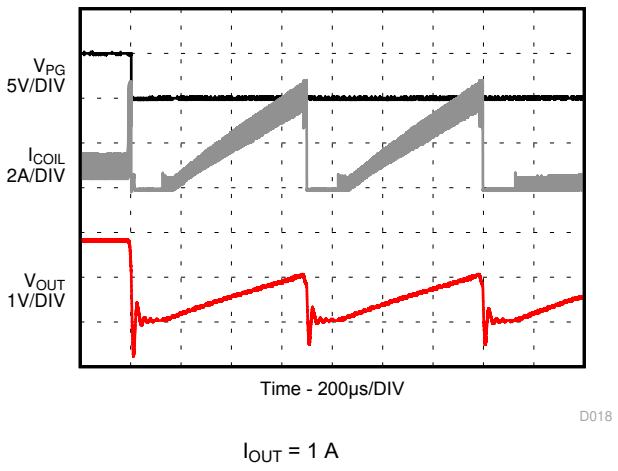
I_{OUT} = 0.05 A to 1A

图 8-24. Load Transient



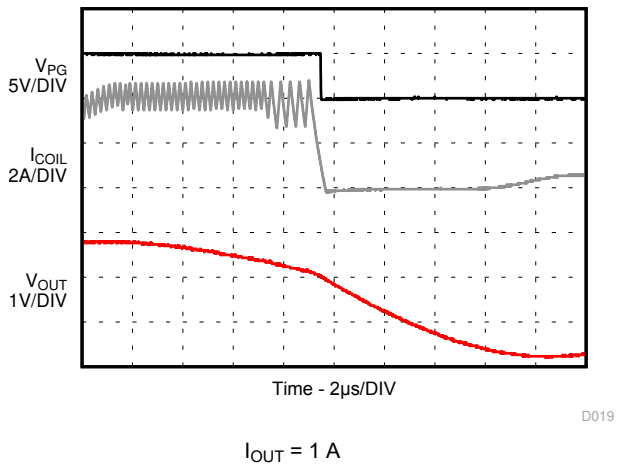
I_{OUT} = 1 A to 2 A

图 8-25. Load Transient



I_{OUT} = 1 A

图 8-26. HICCUP Short Circuit Protection



I_{OUT} = 1 A

图 8-27. HICCUP Short Circuit Protection (Zoom In)

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.4 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application.

10 Layout

10.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the device. See 图 10-1 for the recommended PCB layout.

- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the GND pin to avoid a ground potential shift.
- The sense traces connected to FB is a signal trace. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes. The connection of the output voltage trace for the FB resistors should be made at the output capacitor.
- Refer to 图 10-1 for an example of component placement, routing and thermal design.

10.2 Layout Example

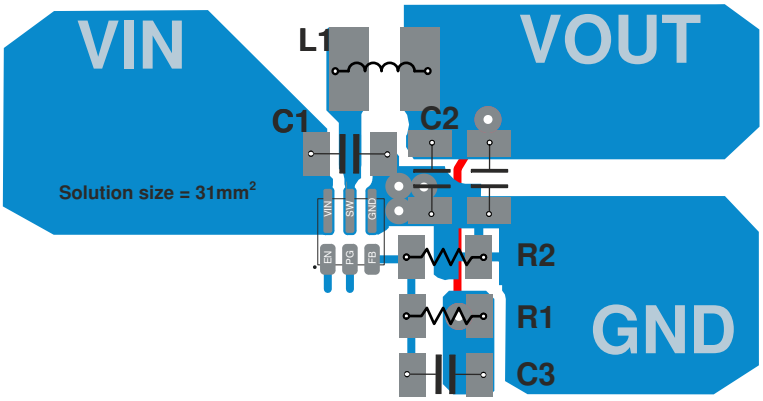


图 10-1. PCB Layout Recommendation

10.2.1 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

节 6.4 provides the thermal metric of the device on the EVM after considering the PCB design of real applications. The big copper planes connecting to the pads of the IC on the PCB improve the thermal performance of the device. For more details on how to use the thermal parameters, see the *Thermal Characteristics Application Notes*, SZZA017 and SPRA953.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TLV62595 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Characteristics Application Note*, SZZA017
- Texas Instruments, *Thermal Characteristics Application Note*, SPRA953

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62595DMQR	ACTIVE	VSON-HR	DMQ	6	3000	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 125	IM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

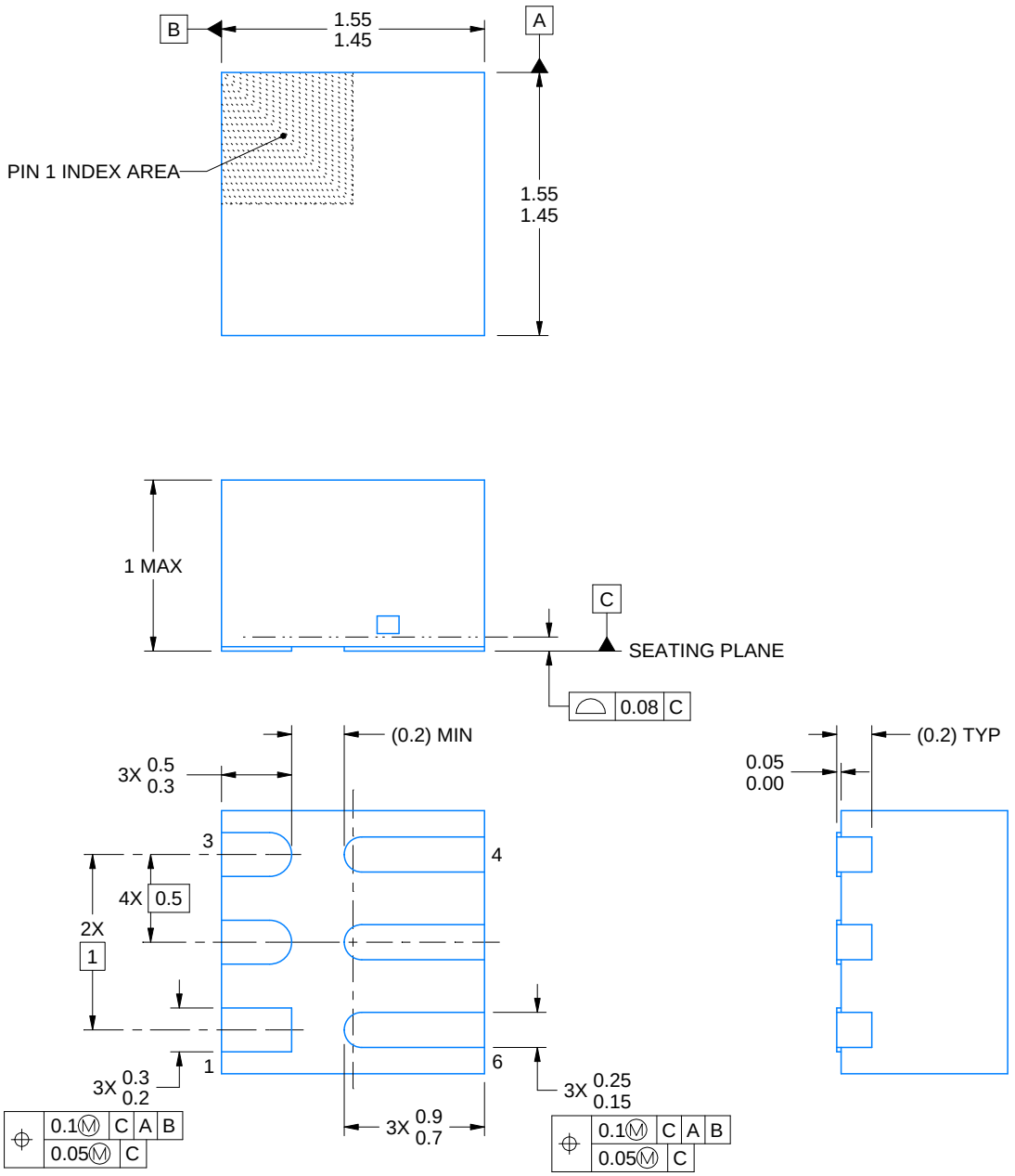
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

DMQ0006A

PACKAGE OUTLINE

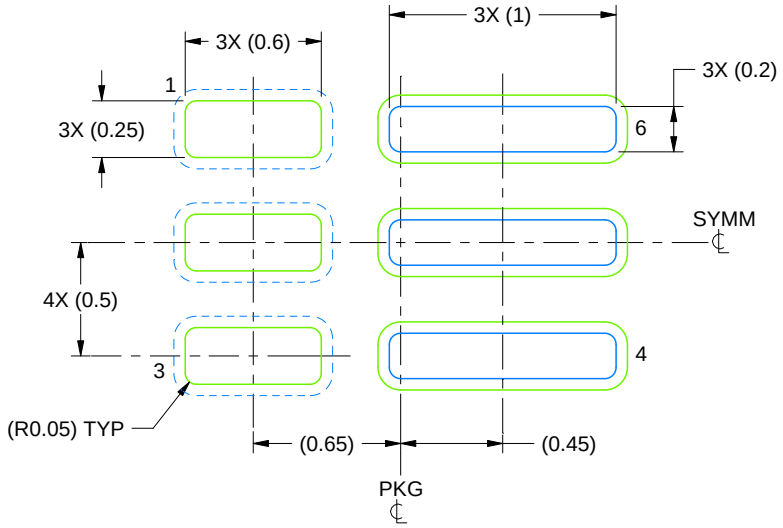
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

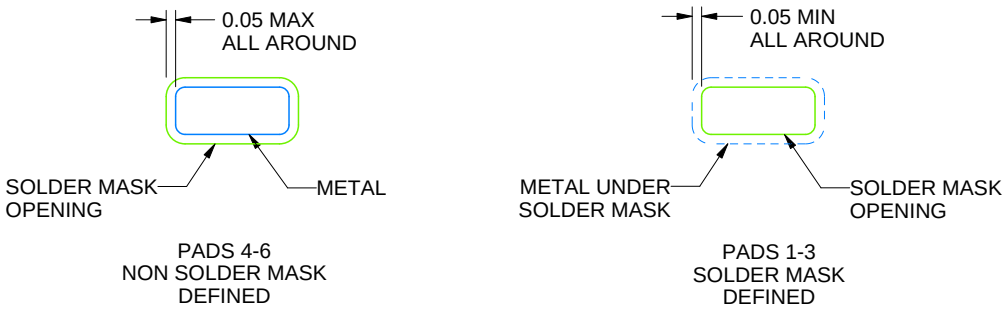


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

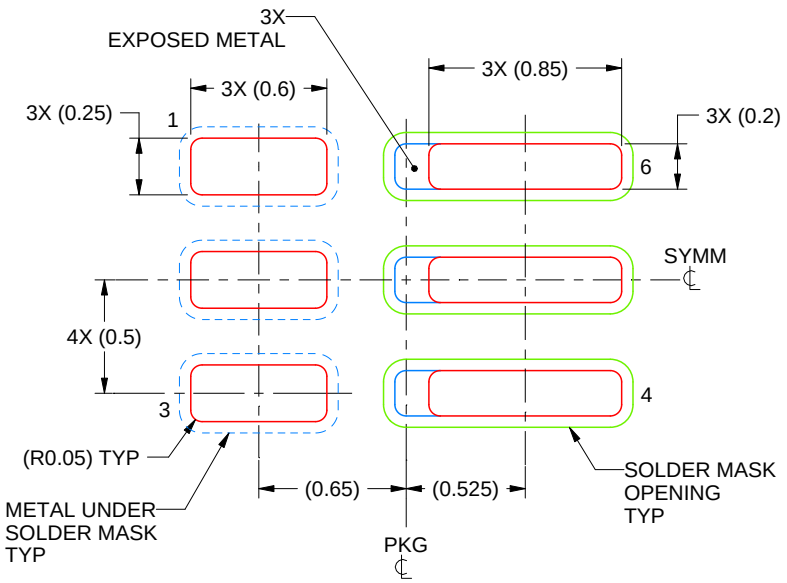


SOLDER MASK DETAILS

4222645/C 10/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PADS 4, 5 & 6:
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222645/C 10/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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