TCAN33x 具备 CAN FD（灵活数据速率）的 3.3V CAN 收发器

1 特性

- 3.3V 单电源运行
- 数据速率高达 5Mbps（TCAN33xG 器件）
- 符合 ISO 11898-2 标准
- SOIC-8 和 SOT-23 封装选项
- 工作模式：
  - 正常模式（所有器件）
  - 具有唤醒功能的低功耗待机模式 (TCAN334)
  - 静音模式（TCAN330、TCAN337）
  - 关断模式（TCAN330、TCAN334）
- ±12V 的宽共模工作电压范围
- ±14V 的总线引脚故障保护
- 总环路延迟 < 135ns
- 宽工作环境温度范围：–40°C 至 125°C
- 优化了未上电时的性能：
  - 总线和逻辑引脚为高阻抗（运行总线或应用上无负载）
  - 上电/断电无干扰运行
- 出色的 EMC 性能
- 保护 功能：
  - 总线终端的 ESD 保护
    - HBM ESD 保护超过 ±25kV
    - IEC61000-4-2 ESD 接触放电保护超过 ±12kV
  - 驱动器显性超时 (TXD DTO)
  - 接收器显性超时 (RXD DTO)
  - 故障输出引脚（仅 TCAN337）
  - V_{CC} 欠压保护
  - 热关断保护
  - 总线引脚限流

2 应用

- 具有灵活数据速率网络的 CAN 中的 5Mbps 运行（TCAN33xG 器件）
- 高负载 CAN 网络中的 1Mbps 运行
- 工业自动化、控制、传感器和驱动系统
- 楼宇、安全和温度控制自动化
- 电信基站状态和控制
- CANopen、DeviceNet、NMEA2000、ARINC825、ISO11783、CANaerospace 等 CAN 总线标准

3 说明

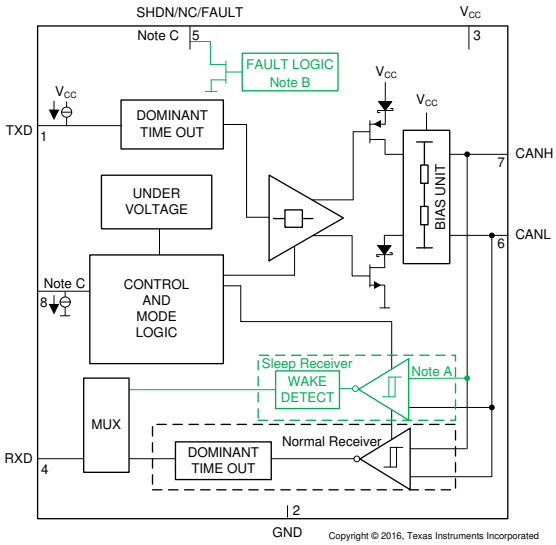
TCAN33x 系列器件兼容 ISO 11898 高速 CAN（控制器局域网）物理层标准。TCAN330、TCAN332、TCAN334 和 TCAN337 的数据传输速率均高达 1Mbps。TCAN330G、TCAN332G、TCAN334G 和 TCAN337G 器件的 ISO 11898-2 更新版本发布正在审理中（包括 CAN FD 和定义环路延迟对称的附加时序参数）。这些器件具有许多保护 特性， 包括驱动器和接收器显性超时 (DTO)，用以确保 CAN 网络的稳定性。该系列器件还集成有 12kV IEC-61000-4-2 ESD 接触放电保护，无需使用附加组件即可确保系统级的稳定性。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TCAN330/G TCAN332/G TCAN334/G TCAN337/G	SOIC (8)	4.90mm × 3.91mm
	SOT-23 (8)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

方框图



A: Sleep Receiver and Wake Detect are device dependent options and are only available in TCAN334.
B: Fault Logic are only available in TCAN337.
C: Pin 5 and 8 functions are device dependent. Refer to Device Comparison Table.

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

Changes from Revision D (April 2016) to Revision E — **Page**

- Changed the Pin Configuration image appearance ... 4
- Changed the titles of Figure 21 and Figure 22 ... 14

Changes from Revision C (April 2016) to Revision D — **Page**

- 将*应用* 列表中的 ARNIC825 更改成了 ARINC825 ... 1

Changes from Revision B (April 2016) to Revision C — **Page**

- Removed the Preview Note from TCAN337 and TCAN337G in the *Device Options* table ... 3

Changes from Revision A (January 2016) to Revision B — **Page**

- Removed the Preview Note from all device except for TCAN337 and TCAN337G in the *Device Comparison* table ... 3
- Changed FAULT Pin I_{CL} MIN value From: 5 mA To: 4 mA in the *Electrical Characteristics* ... 7

Changes from Original (December 2015) to Revision A — **Page**

- 将*特性* 中的“总环路延迟 < 150ns”更改成了“总环路延迟 < 135ns” ... 1
- Changed $V_{IT(SLEEP)}$ To: $V_{IT(STB)}$ and added Test conditions in the *Electrical Characteristics* ... 7
- Added –12 V < V_{CM} < 12 V to t_{WK_FILTER} in the Test Conditions of *Switching Characteristics* ... 8

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5 说明 （续）

该系列收发器采用 3.3V 单电源供电，因此可以直接连接 3.3V CAN 控制器/微控制器 (MCU)。此外，这些器件完全兼容同一总线上的其他 5V CAN 收发器。

由于显性共模和隐性共模相匹配，这些器件具有卓越的 EMC 性能。这些器件具有超低功耗的关断模式和待机模式，对于电池供电型应用而言极具 吸引力中的数字输入 D 类音频放大器。

该系列器件提供便于插接的标准 8 引脚 SOIC 封装以及面向空间受限类应用的小型 SOT-23 封装提供了出色的功能性与安全性。

6 Device Options

DEVICE	PIN 5	PIN 8	DERATE	DESCRIPTION
TCAN330	SHDN	S	1 Mbps	Shutdown and silent modes
TCAN332	NC	NC	1 Mbps	Normal mode only
TCAN334	SHDN	STB	1 Mbps	Shutdown and standby with wake
TCAN337	FAULT	S	1 Mbps	Fault output and silent mode
TCAN330G	SHDN	S	5 Mbps	Shutdown and silent modes
TCAN332G	NC	NC	5 Mbps	Normal mode only
TCAN334G	SHDN	STB	5 Mbps	Shutdown and standby with wake
TCAN337G	FAULT	S	5 Mbps	Fault output and silent mode

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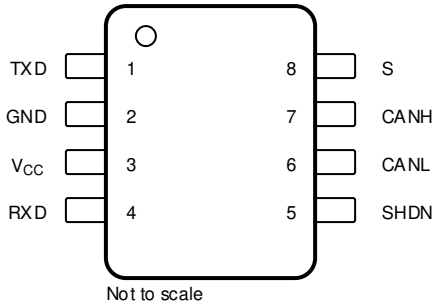
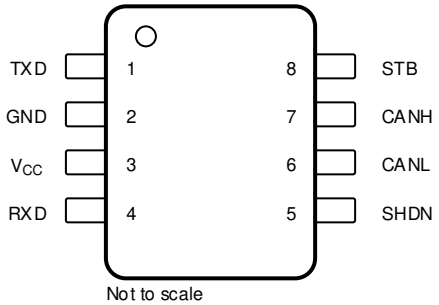
7 Pin Configuration and Functions

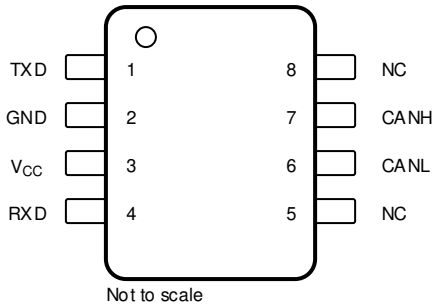
TCAN330 D, DCN Packages
8-Pin SOIC, SOT-23
Top View



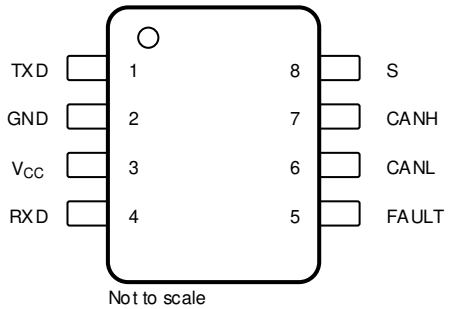
TCAN334 D, DCN Packages
8-Pin SOIC, SOT-23
Top View



TCAN332 D, DCN Packages
8-Pin SOIC, SOT-23
Top View



TCAN337 D, DCN Packages
8-Pin SOIC, SOT-23
Top View



Pin Functions

PIN					I/O	DESCRIPTION
NAME	TCAN330	TCAN332	TCAN334	TCAN337		
TXD	1	1	1	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states), integrated pull up
GND	2	2	2	2	GND	Ground connection
V_{CC}	3	3	3	3	Supply	3.3-V supply voltage
RXD	4	4	4	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states), tri-state
SHDN	5	—	5	—	I	Drive high for shutdown mode. Internal pull-down.
NC	—	5	—	—	NC	No Connect – Not internally connected
FAULT	—	—	—	5	O	Open drain fault output pin.
CANL	6	6	6	6	I/O	Low level CAN bus line
CANH	7	7	7	7	I/O	High level CAN bus line
S	8	—	—	8	I	Drive high for silent mode, integrated pull down
NC	—	8	—	—	NC	No Connect – Not internally connected
STB	—	—	8	—	I	Drive high for low power standby mode, integrated pull down

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)(2)]

	MIN	MAX	UNIT
Supply Voltage range, V_{CC}	–0.3	5	V
Voltage at any bus terminal (CANH or CANL), $V_{(BUS)}$	–14	14	V
Logic input terminal voltage range $V_{(Logic_Input)}$	–0.3	5	V
Logic output terminal voltage range, $V_{(Logic_Output)}$	–0.3	5	V
Logic output current, $I_{O(LOGIC)}$		8	mA
Operating junction temperature range, T_J	–40	150	°C
Storage temperature, T_{stg}		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	All pins except CANH and CANL	±4000	V
			Pins CANH and CANL	±25000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	All pins	±1500	
		IEC 61400-4-2 Contact Discharge	CANH and CANL terminals to GND	±12000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3		3.6	V
$I_{OH(LOGIC)}$	Logic terminal HIGH level output current	–2			mA
$I_{OL(LOGIC)}$	Logic terminal LOW level output current			2	
T_A	Operational free-air temperature	–40		125	°C

8.4 Thermal Information

THERMAL METRIC[(1)]			TCAN33x D (SOIC) 8 PINS	TCAN33x DCN (SOT-23) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance		114.4	154.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		58.7	76.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		55.2	49.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter		11.7	11.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter		54.6	49.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	N/A	°C/W
P_D	Average power dissipation	V_{CC} = 3.3 V, T_J = 27°C, R_L = 60 Ω, SHDN, S and STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, $C_{L(RXD)}$ = 15 pF	65	65	mW
T_{SD}	Thermal shutdown temperature		175	175	°C
T_{HYS}	Thermal shutdown hysteresis		5	5	°C

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.5 Electrical Characteristics

over operating free-air temperature range, T_J = –40°C to 150°C. All typical values are at 25°C and supply voltages of V_{CC} = 3.3 V, R_L = 60 Ω, (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply							
I_{CC}	Supply current Normal Mode	Dominant	See Figure 18. TXD = 0 V, R_L = 60 Ω, C_L = open, S, STB and SHDN = 0 V. Typical Bus Load.			55	mA
			See Figure 18. TXD = 0 V, R_L = 50 Ω, C_L = open, S, STB and SHDN = 0 V. High Bus Load.			60	
		Dominant with bus fault	See Figure 18. TXD = 0 V, S, STB and SHDN = 0 V, CANH = -12 V, R_L = open, C_L = open			180	
		Recessive	See Figure 18. TXD = V_{CC}, R_L = 50 Ω, C_L = open, S, STB and SHDN = 0 V			3.5	
	Supply Current: Silent Mode		See Figure 18. TXD = V_{CC}, R_L = 50 Ω, C_L = open, S = V_{CC}			2.5	
	Supply Current: Standby Mode		T_A < 85°C, STB at V_{CC}, RXD floating, TXD at V_{CC}			15	µA
			STB at V_{CC}, RXD floating, TXD at V_{CC}			20	
	Supply Current: Shutdown Mode		T_A < 85°C, SHDN at V_{CC}, RXD floating, TXD at V_{CC}			1	
			SHDN = V_{CC}, RXD floating, TXD at V_{CC}			2.5	
$UV_{(VCC)}$	Rising under voltage detection on V_{CC} for protected mode				2.2	2.6	V
	Falling under voltage detection on V_{CC} for protected mode			1.65	2	2.5	
$V_{HYS(UVVCC)}$	Hysteresis voltage on $UV_{(VCC)}$				200		mV
Driver							
$V_{O(D)}$	Bus output voltage (dominant)	CANH	See Figure 31 and Figure 19, TXD = 0 V, S, STB and SHDN = 0 V, R_L = 60 Ω, C_L = open	2.45		V_{CC}	V
		CANL		0.5		1.25	
$V_{O(R)}$	Bus output voltage (recessive)		See Figure 31 and Figure 19, TXD = V_{CC}, STB, SHDN = 0 V, S = 0 V or V_{CC} (1), R_L = open (no load)		1.85		V
$V_{OD(D)}$	Differential output voltage (dominant)		See Figure 31 and Figure 19, TXD = 0 V, S, STB and SHDN = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open	1.6		3	V
			See Figure 31 and Figure 19, TXD = 0 V, S, STB and SHDN = 0 V, 45 Ω ≤ R_L < 50 Ω, C_L = open	1.5		3	
$V_{OD(R)}$	Differential output voltage (recessive)		See Figure 31 and Figure 19, TXD = V_{CC}, S, STB and SHDN = 0 V, R_L = 60 Ω, C_L = open	–120		12	mV
			T_A < 85°C, See Figure 31 and Figure 19, TXD = V_{CC}, S, STB and SHDN = 0 V, R_L = open (no load), C_L = open	–50		50	
			See Figure 31 and Figure 19, TXD = V_{CC}, S, STB and SHDN = 0 V, R_L = open (no load), C_L = open	–50		100	
$V_{(SYM)}$	Output symmetry (dominant and recessive) ($CANH_{REC}$ + $CANL_{REC}$ – $CANH_{DOM}$ – $CANL_{DOM}$)		See Figure 31 and Figure 19, S, STB and SHDN = 0 V, R_L = 60 Ω, C_L = open	–400		400	mV
$I_{OS(DOM)}$	Short-circuit steady-state output current, Dominant		See Figure 26, $V_{(CANH)}$ = –12 V, CANL = open, TXD = 0 V	–200			mA
			See Figure 26, $V_{(CANL)}$ = 12 V, CANH = open, TXD = 0 V			200	
$I_{OS(REC)}$	Short-circuit steady-state output current, Recessive		See Figure 26, –12 V ≤ V_{BUS} ≤ 12 V, V_{BUS} = CANH = CANL, TXD = V_{CC}	–5		5	mA

(1) The bus output voltage (recessive) will be the same if the device is in normal mode with S terminal LOW or if the device is in silent mode with the S terminal is HIGH.

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Electrical Characteristics (continued)

over operating free-air temperature range, T_J = –40°C to 150°C. All typical values are at 25°C and supply voltages of V_{CC} = 3.3 V, R_L = 60 Ω, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver						
V_{IT}	Input threshold voltage, normal modes and selective wake modes	See Figure 20 and Table 7	500		900	mV
V_{HYS}	Hysteresis voltage for input threshold, normal modes and selective wake modes	See Figure 20 and Table 7		120		mV
V_{CM}	Common Mode Range: normal and silent modes	See Figure 20 and Table 7	–12		12	V
$V_{IT(STB)}$	Input Threshold, standby mode	–2 V < V_{CM} < 7 V See Figure 20 and Table 7	400		1150	mV
		–12 V < V_{CM} < 12 V See Figure 20 and Table 7	400		1350	mV
$I_{IOFF(LKG)}$	Power-off (unpowered) bus input leakage current	T_A < 85°C, CANH = CANL = 3.3 V, V_{CC} to GND via 0-Ω and 47-kΩ resistor			6	µA
		CANH = CANL = 3.3 V, V_{CC} to GND via 0-Ω and 47-kΩ resistor			12	µA
C_I	Input capacitance to ground (CANH or CANL)				20	pF
C_{ID}	Differential input capacitance				10	pF
R_{ID}	Differential input resistance	TXD = V_{CC}, Normal Mode	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)	TXD = V_{CC}, Normal mode	15		40	kΩ
$R_{IN(M)}$	Input resistance matching: [1 – ($R_{IN(CANH)}$) / $R_{IN(CANL)}$)] × 100 %	$V_{(CANH)}$ = $V_{(CANL)}$	–3%		3%	
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	HIGH level input voltage		2			V
V_{IL}	LOW level input voltage				0.8	V
I_{IH}	HIGH level input leakage current	TXD = V_{CC} = 3.6 V	–2.5	0	3	µA
I_{IL}	LOW level input leakage current	TXD = 0 V, V_{CC} = 3.6 V	–4	0	0	µA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 3.6 V, V_{CC} = 0 V	–2	0	2.5	µA
$I_{(CAP)}$	Input Capacitance			2.5		pF
RXD Terminal (CAN Receive Data Output)						
V_{OH}	HIGH level output voltage	See Figure 20, I_O = –2 mA	0.8 x V_{CC}			V
V_{OL}	LOW level output voltage	See Figure 20, I_O = 2 mA		0.2	0.4	V
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 3.6 V, V_{CC} = 0 V	–1	0	1	µA
STB/S/SHDN Terminals						
V_{IH}	HIGH level input voltage		2			V
V_{IL}	LOW level input voltage				0.8	V
I_{IH}	HIGH level input leakage current	STB, S, SHDN = V_{CC} = 3.6 V	–3	0	10	µA
I_{IL}	LOW level input leakage current	STB, S, SHDN = 0 V, V_{CC} = 3.6 V	–4	0	1	µA
$I_{LKG(OFF)}$	Unpowered leakage current	STB, S, SHDN = 3.6 V, V_{CC} = 0 V	–3	0	5	µA
FAULT Pin (Fault Output), TCAN337 only						
I_{CH}	Output current high level	FAULT = V_{CC}, See Figure 28	–10			µA
I_{CL}	Output current low level	FAULT = 0.4 V, See Figure 28	4	12		mA

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8.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant and dominant to recessive	See Figure 23, S, STB and SHDN = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		100	135	ns
$t_{PROP(LOOP)}$	Total Loop delay in highly loaded network	See Figure 23, S, STB and SHDN = 0 V, R_L = 120 Ω, C_L = 200 pF, $C_{L(RXD)}$ = 15 pF		120	180	ns
$t_{BUS_SYM_2}$	2 Mbps transmitted recessive bit width	See Figure 24, S or STB = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, t_{BIT} = 500 ns TCAN330G, TCAN332G, TCAN334G and TCAN337G only	435		530	ns
$t_{REC_SYM_2}$	2 Mbps received recessive bit width		400		550	ns
Δt_{SYM_2}	2 Mbps receiver timing symmetry ($t_{REC_SYM_2}$ - $t_{BUS_SYM_2}$)		–65		40	ns
$t_{BUS_SYM_5}$	5 Mbps transmitted recessive bit width	See Figure 24, S or STB = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, t_{BIT} = 200 ns TCAN330G, TCAN332G, TCAN334G and TCAN337G only	155		210	ns
$t_{REC_SYM_5}$	5 Mbps received recessive bit width		120		220	ns
Δt_{SYM_5}	5 Mbps receiver timing symmetry ($t_{REC_SYM_5}$ - $t_{BUS_SYM_5}$)		–45		15	ns
t_{MODE}	Mode change time	See Figure 21 and Figure 22. R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		5	10	µs
$t_{UV_RE\text{-}ENABLE}$	Re-enable time after UV event	Time for device to return to normal operation from $UV_{(VCC)}$ under voltage event			1000	µs
t_{WK_FILTER}	Bus time to meet Filtered Bus Requirements for Wake Up Request	See Figure 33, Standby mode. –12 V < V_{CM} < 12 V	0.5		4	µs
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, HIGH TXD to Driver Recessive	See Figure 19, S, STB and SHDN = 0 V. R_L = 60 Ω, C_L = 100 pF,		25		ns
t_{pLD}	Propagation delay time, LOW TXD to Driver Dominant			20		
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHR} - t_{pLD} \rvert$)			5		
t_r	Differential output signal rise time			17		
t_f	Differential output signal fall time			9		
t_{TXD_DTO}	Driver dominant time out (1)	See Figure 25, R_L = 60 Ω, C_L = 100 pF	1.2	2.6	3.8	ms
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to high RXD output	See Figure 20, $C_{L(RXD)}$ = 15 pF CANL = 1.5 V, CANH = 3.5 V		62		ns
t_{pDL}	Propagation delay time, bus dominant input to RXD low output			56		
t_r	Output signal rise time (RXD)			7		
t_f	Output signal fall time (RXD)			6		
t_{RXD_DTO}	Receiver dominant time out (2)	See Figure 27, $C_{L(RXD)}$ = 15 pF	1.6	3	5	ms

(1) The TXD dominant time out (t_{TXD_DTO}) disables the driver of the transceiver once the TXD has been dominant longer than t_{TXD_DT}O, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11/ t_{TXD_DTO} = 11 bits / 1.2 ms = 9.2 kbps.

(2) The RXD timeout (t_{RXD_DTO}) disables the RXD output in the case that the bus has been dominant longer than t_{RXD_DTO}, which releases RXD pin to the recessive state (high), thus preventing a dominant bus failure from permanently keeping the RXD pin low. The RXD pin will automatically resume normal operation once the bus has been returned to a recessive state. While this protects the protocol controller from a permanent dominant state, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on RXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{RXD_DTO} minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11 / t_{RXD_DTO} = 11 bits / 1.6 ms = 6.9 kbps.

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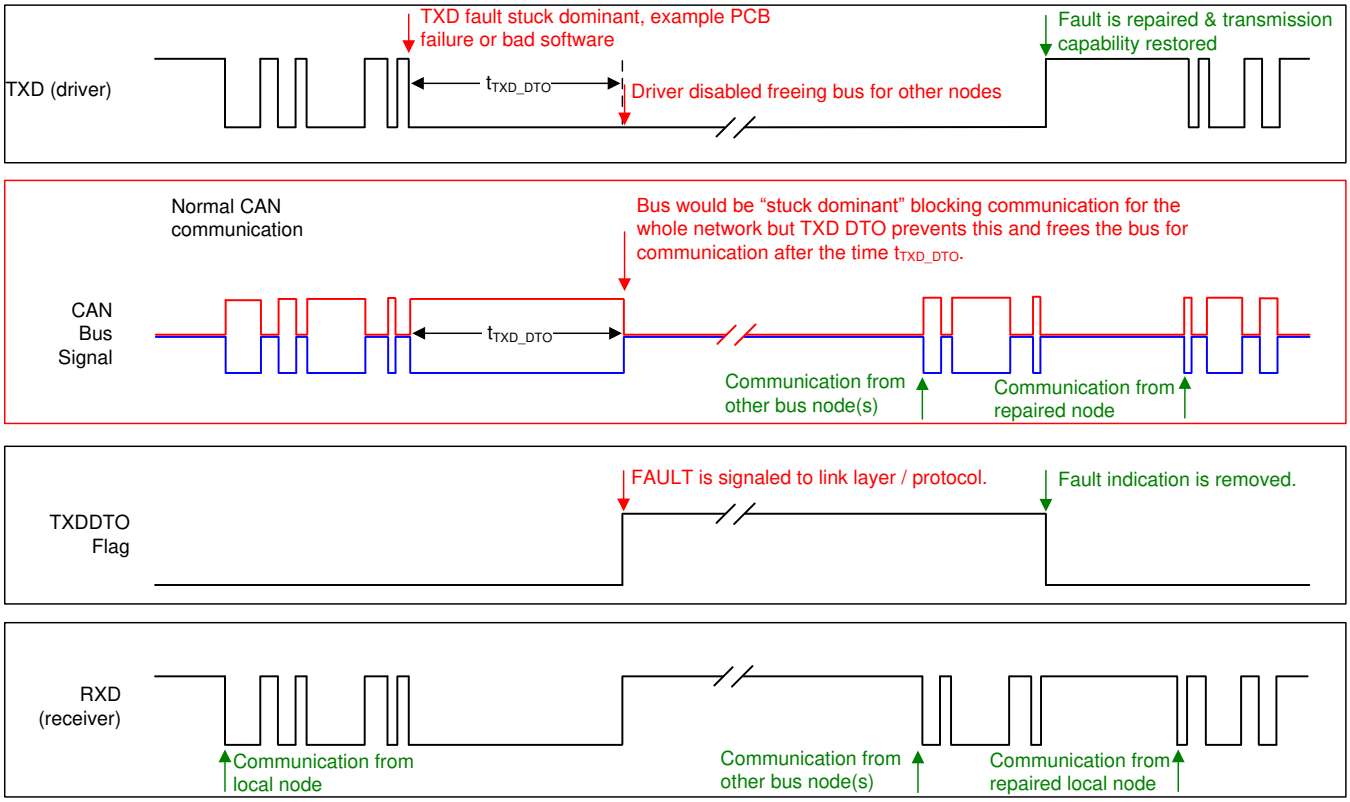


Figure 1. Example Timing Diagram for TXD DTO and FAULT Pin

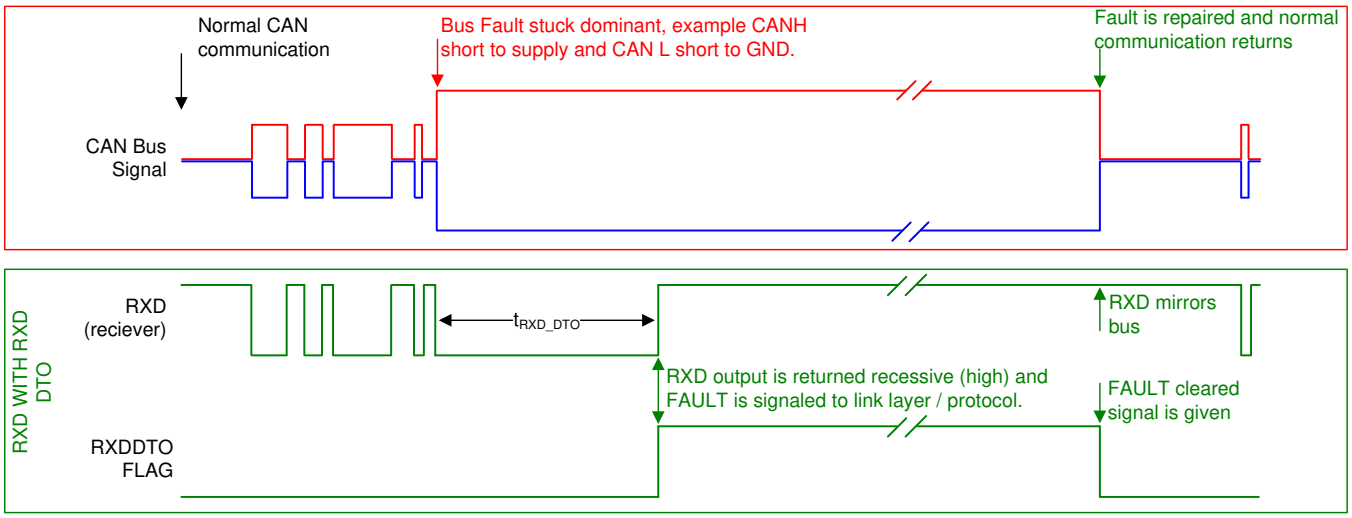
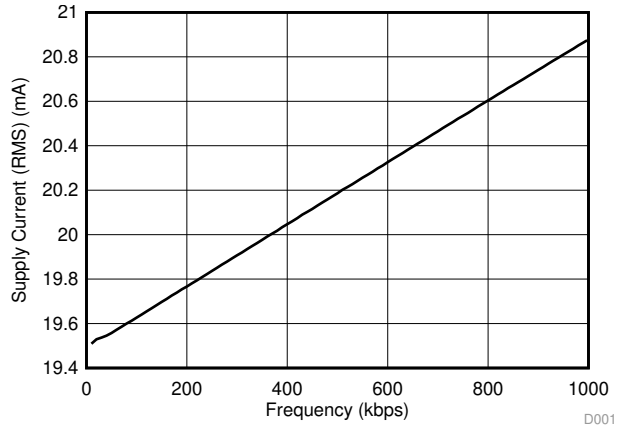


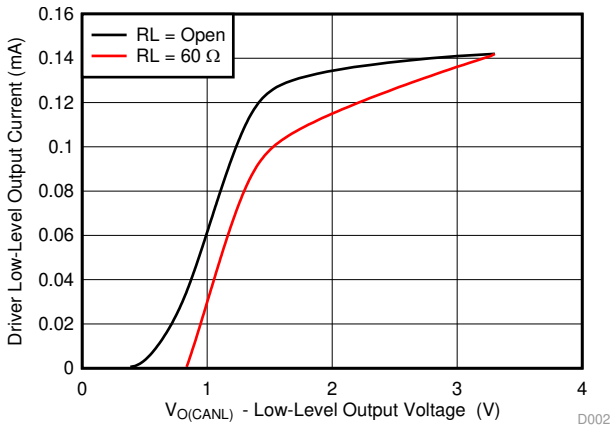
Figure 2. Example Timing Diagram for RXD DTO and FAULT Pin

8.7 Typical Characteristics



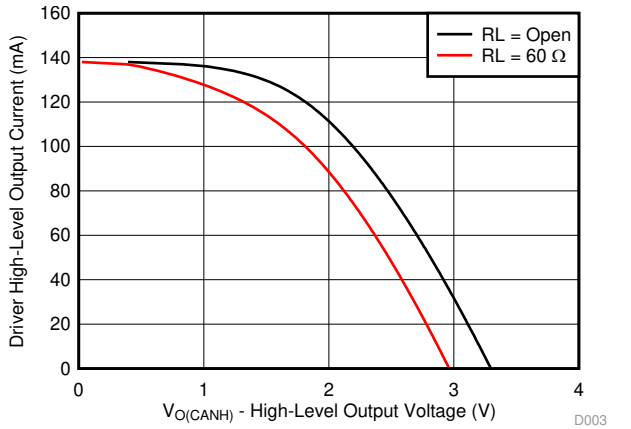
V_{CC} = 3.3 V Normal Mode Temp = 25°C
60 Ω Load

Figure 3. Supply Current (RSM) vs Frequency



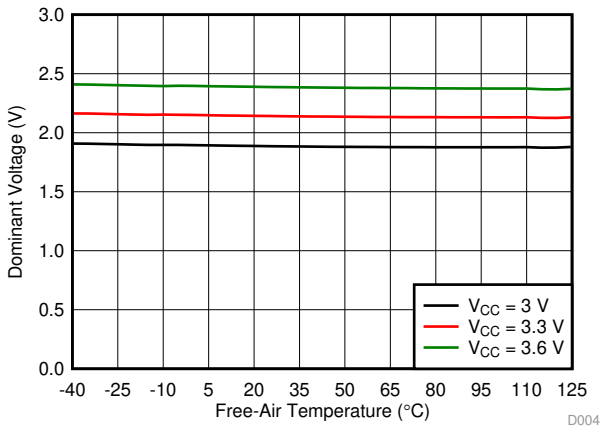
V_O = 0.5 to 3.3 V Normal Mode Temp = 25°C
V_{CC} = 3.3 V

Figure 4. Driver Low-Level Output Current vs Low-level Output Voltage



V_O = 0.5 to 3.3 V Normal Mode Temp = 25°C
V_{CC} = 3.3 V

Figure 5. Driver High-Level Output Current vs High-level Output Voltage



V_O = 0.5 to 3.3 V Normal Mode Temp = 25°C
V_{CC} = 3.3 V 60 Ω Load

Figure 6. Dominant Voltage (V_{OD}) vs Free-Air Temperature

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8.8 Typical Characteristics, TCAN330 Receiver

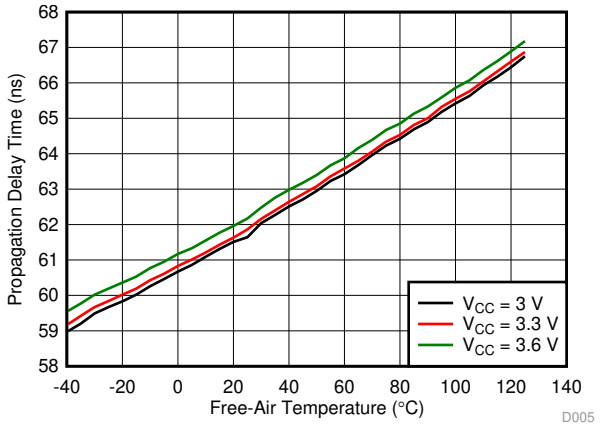

Figure 7. Receiver Bus Recessive Input to High RXD Output Propagation Delay Time vs Free-Air Temperature

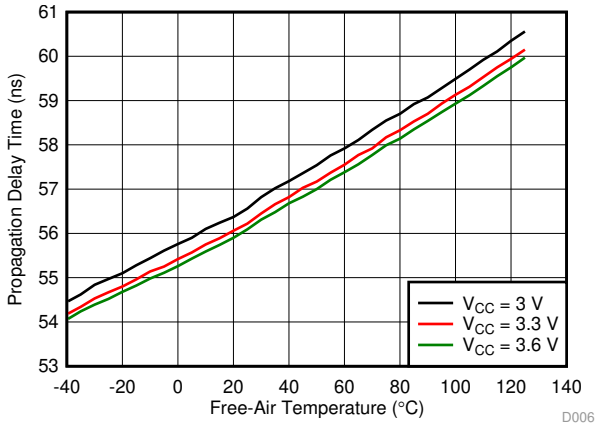

Figure 8. Receiver Bus Dominant Input to Low RXD Output Propagation Delay Time vs Free-Air Temperature

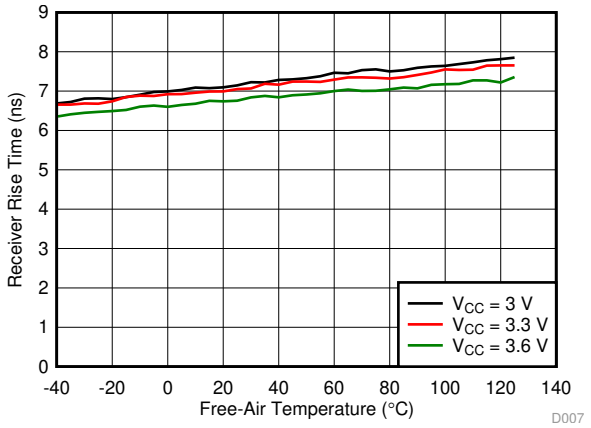

Figure 9. Receiver Rise Time vs Free-Air Temperature

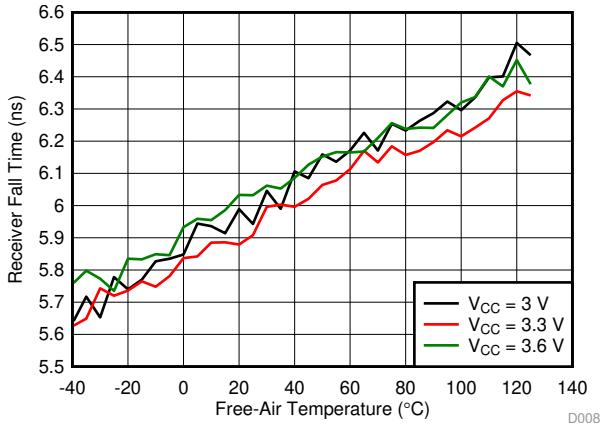

Figure 10. Receiver Fall Time vs Free-Air Temperature

8.9 Typical Characteristics, TCAN330 Driver

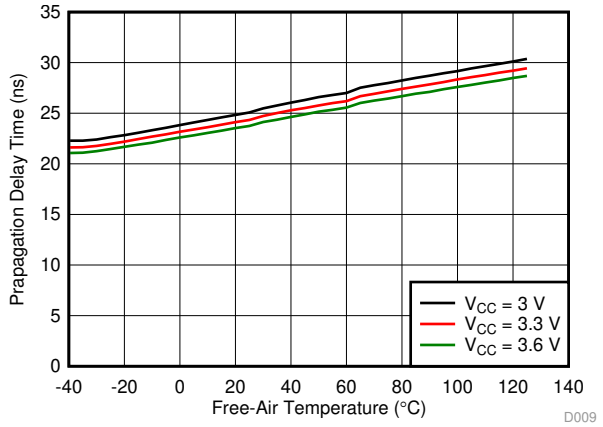

Figure 11. Driver High TXD Input to Driver Recessive Output Propagation Delay Time vs Free-Air Temperature

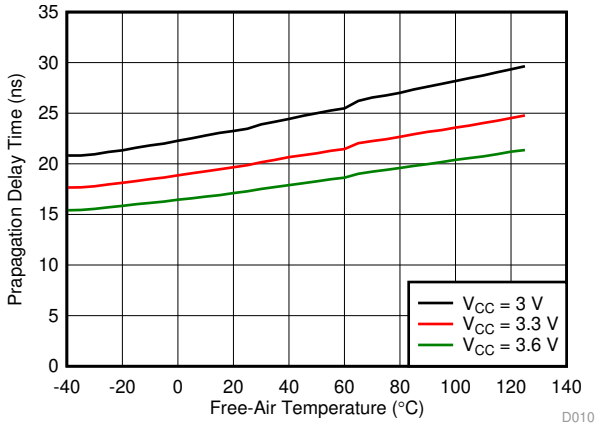

Figure 12. Driver Low TXD Input to Driver Dominant Output Propagation Delay Time vs Free-Air Temperature

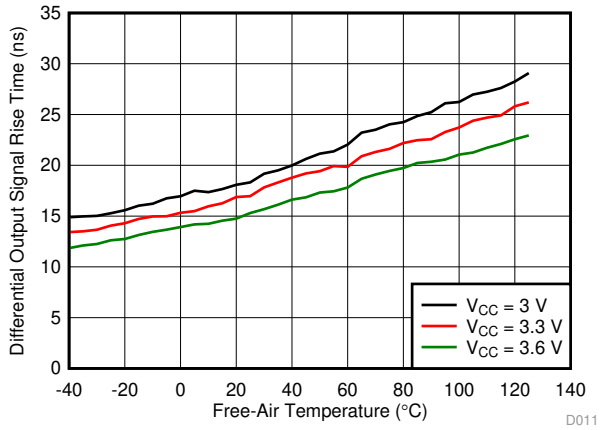

Figure 13. Differential Output Signal Rise Time vs Free-Air Temperature

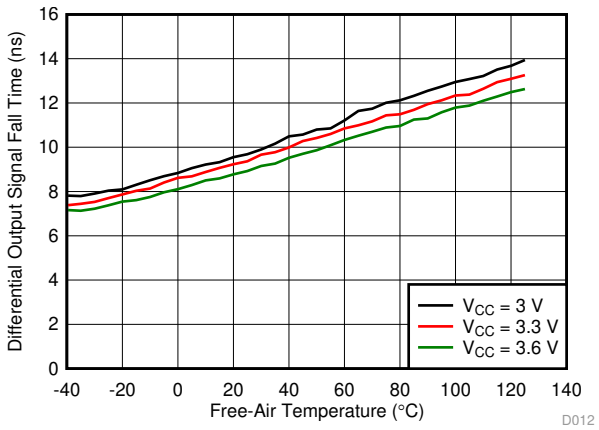

Figure 14. Differential Output Signal Fall Time vs Free-Air Temperature

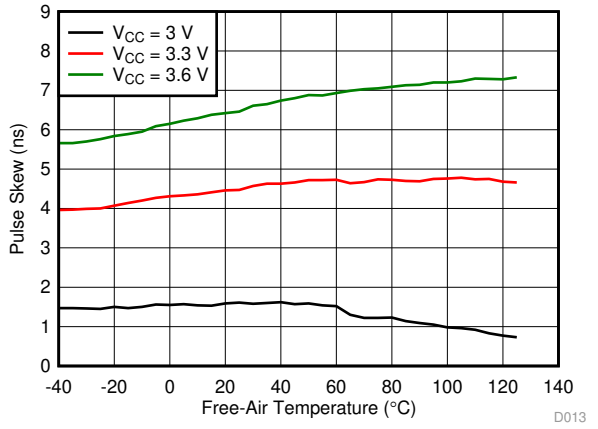

Figure 15. Pulse Skew ($|t_{pHR} - t_{pLD}|$) vs Free-Air Temperature

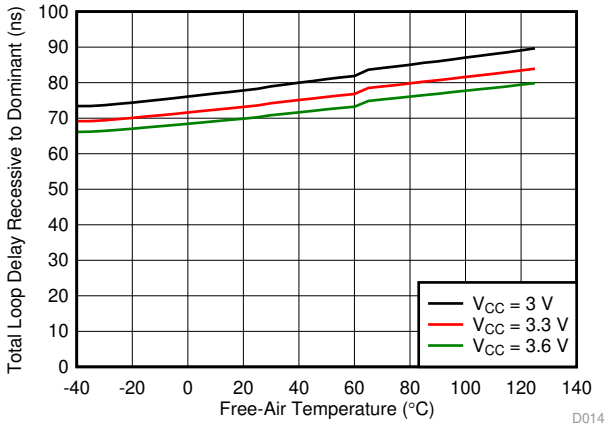

Figure 16. Total Loop Delay Recessive to Dominant $t_{PROP(LOOP1)}$ vs Free-Air Temperature

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Typical Characteristics, TCAN330 Driver (continued)

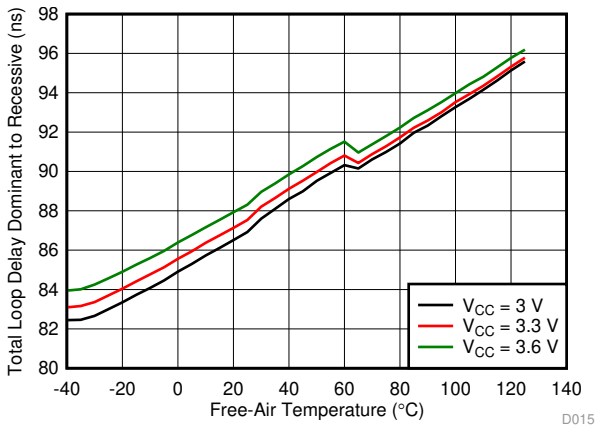

Figure 17. Total Loop Delay Dominant to Recessive $t_{PROP(LOOP2)}$ vs Free-Air Temperature

9 Parameter Measurement Information

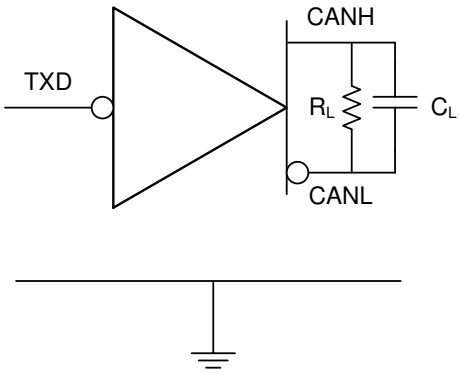

Figure 18. Supply Test Circuit

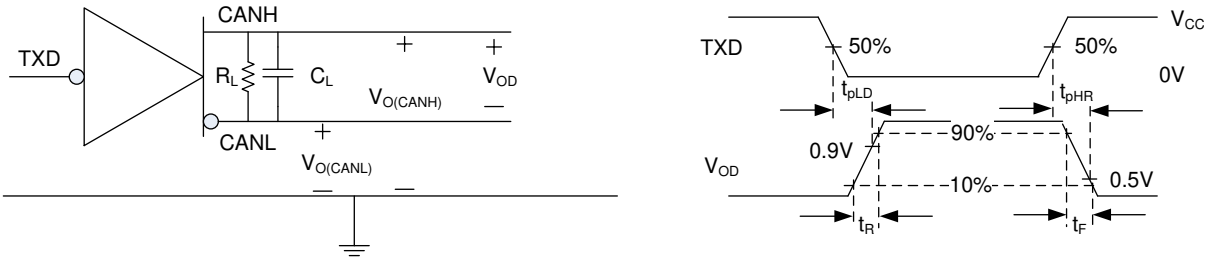

Figure 19. Driver Test Circuit and Measurement

Parameter Measurement Information (continued)

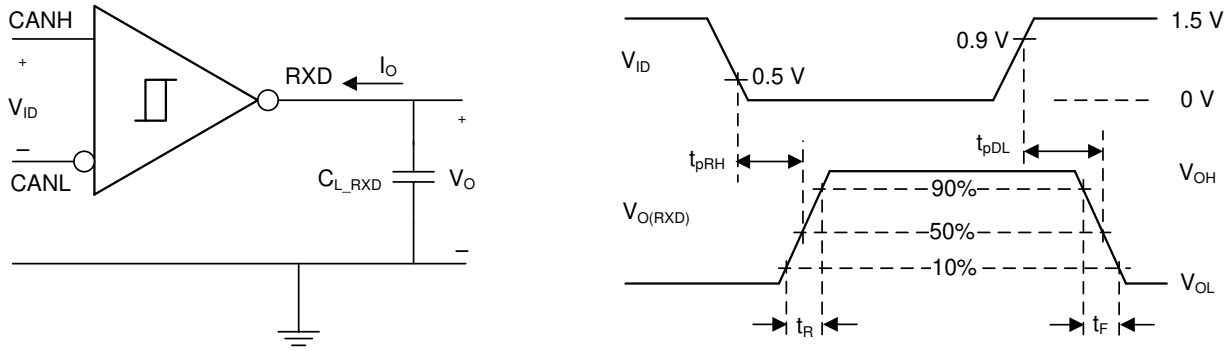

Figure 20. Receiver Test Circuit and Measurement

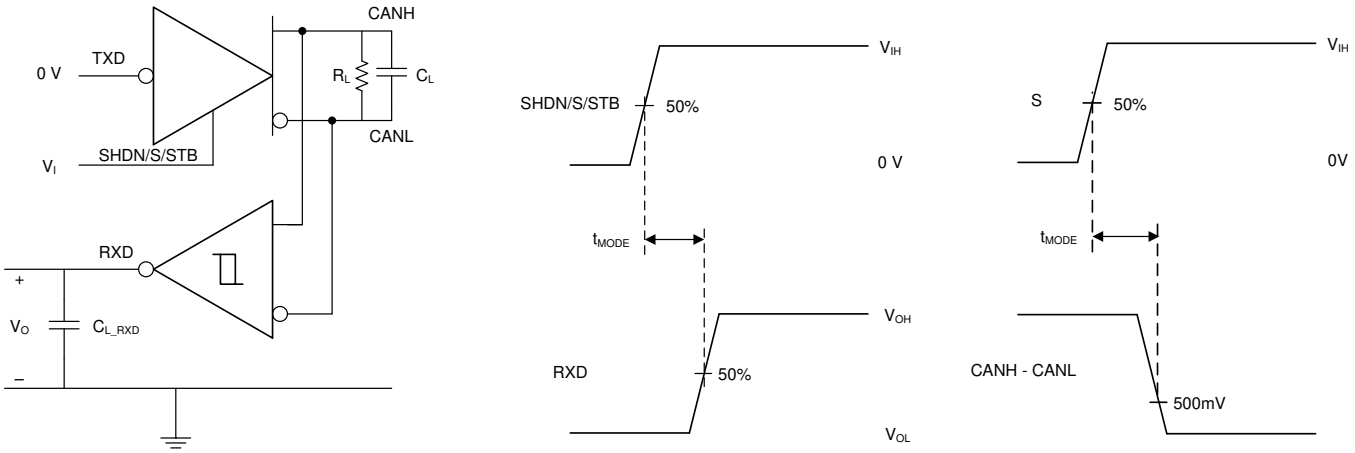

Figure 21. t_{MODE} Test Circuit and Measurement, from Normal to Shutdown, Standby or Silent Mode

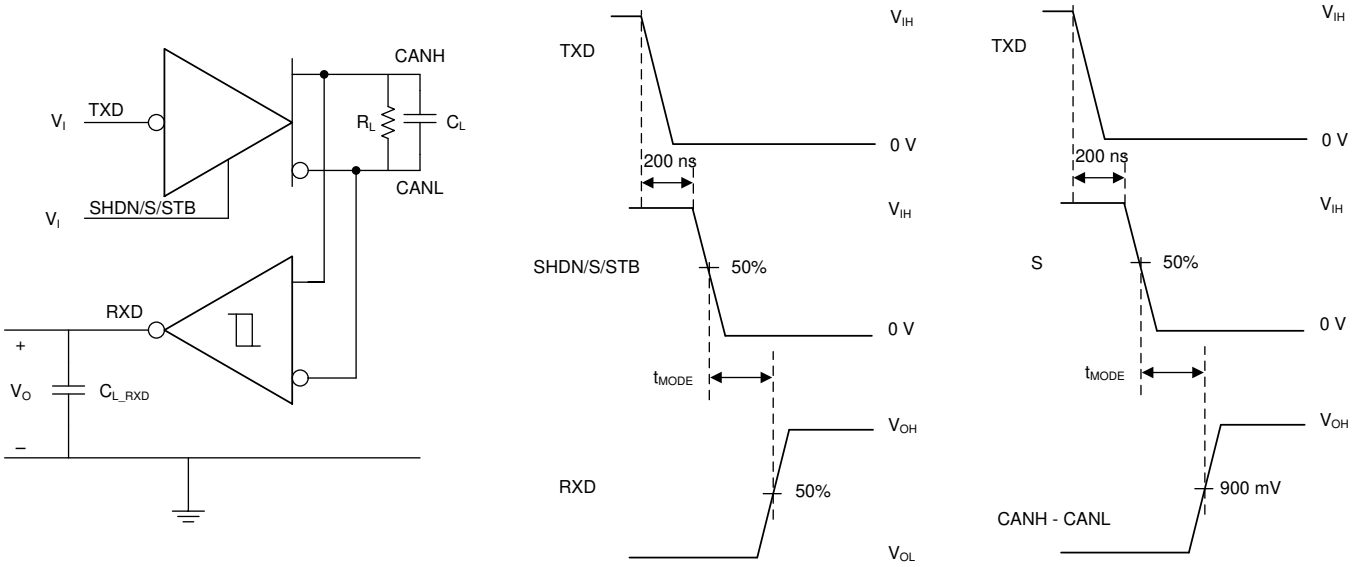

Figure 22. t_{MODE} Test Circuit and Measurement, from Shutdown, Standby or Silent to Normal Mode

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Parameter Measurement Information (continued)

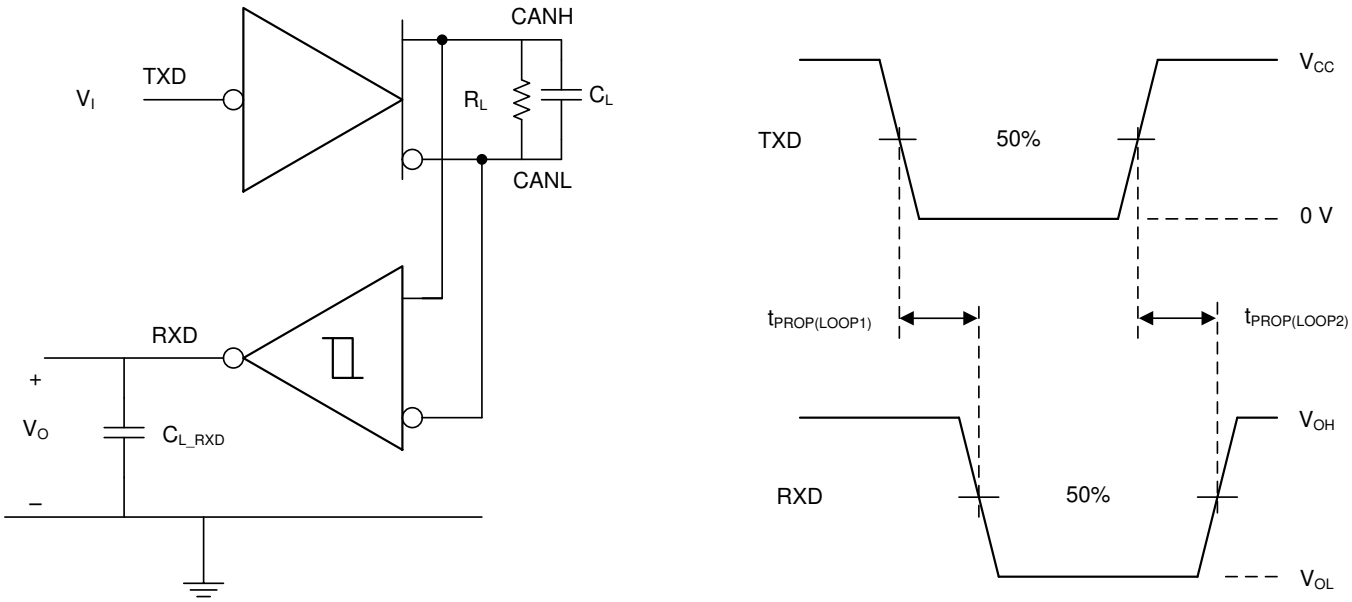

Figure 23. $t_{PROP(LOOP)}$ Test Circuit and Measurement

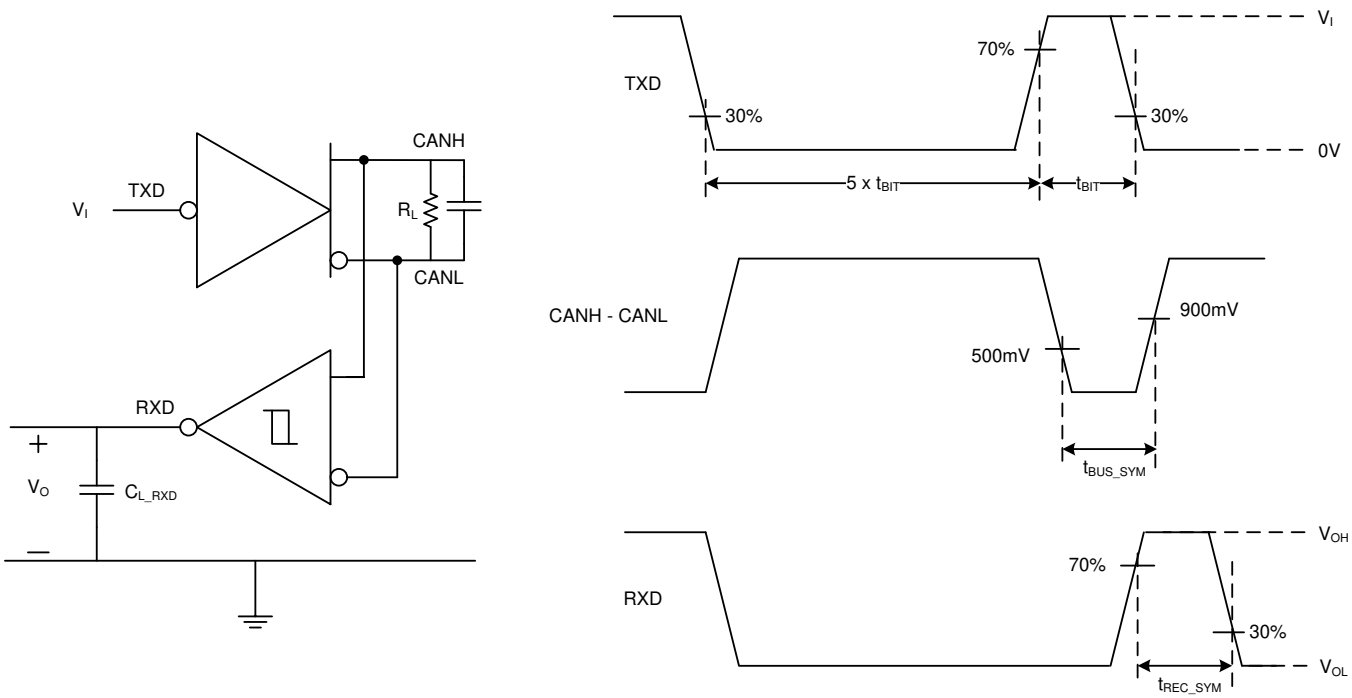

Figure 24. Loop Delay Symmetry Test Circuit and Measurement

Parameter Measurement Information (continued)

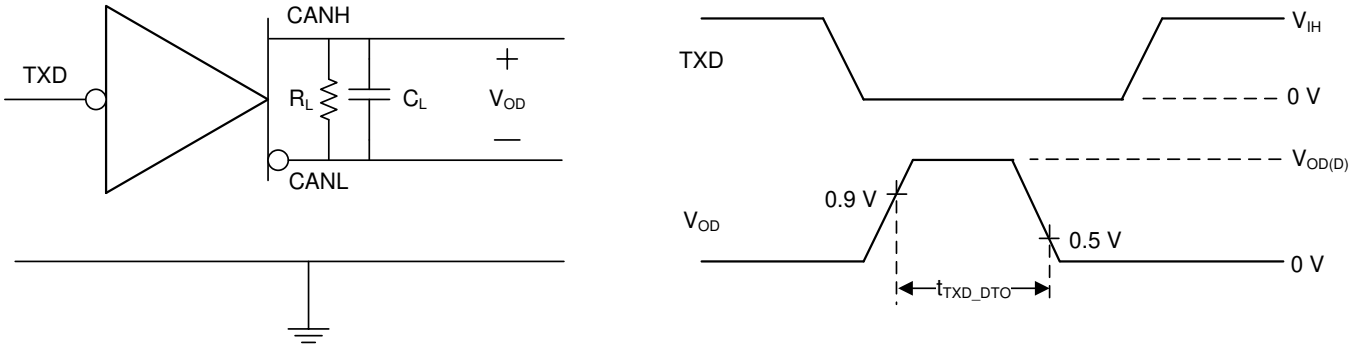

Figure 25. TXD Dominant Time Out Test Circuit and Measurement

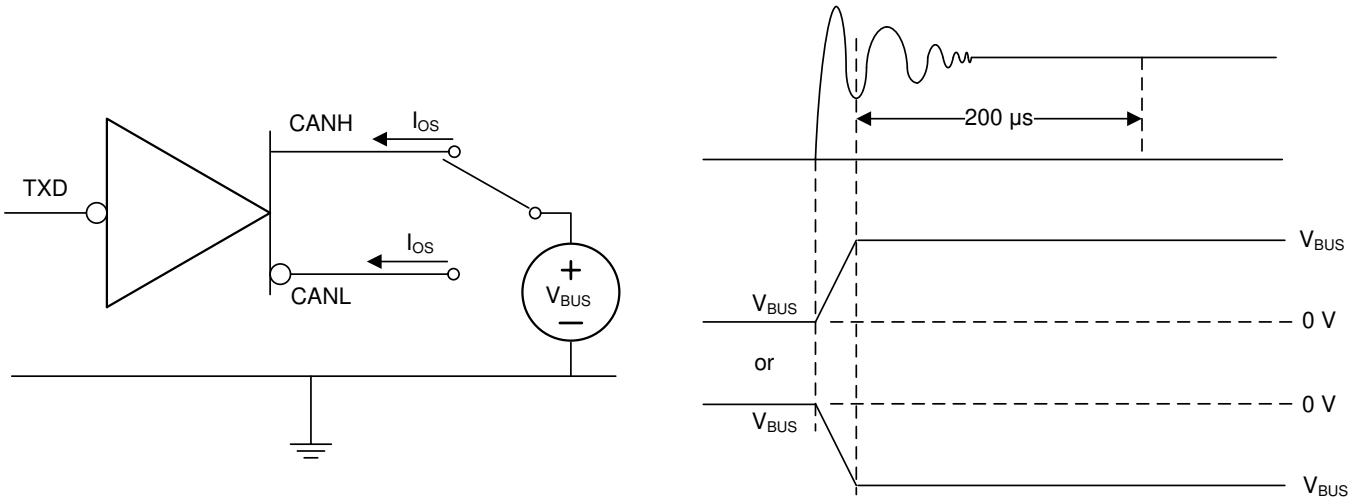

Figure 26. Driver Short-Circuit Current Test and Measurement

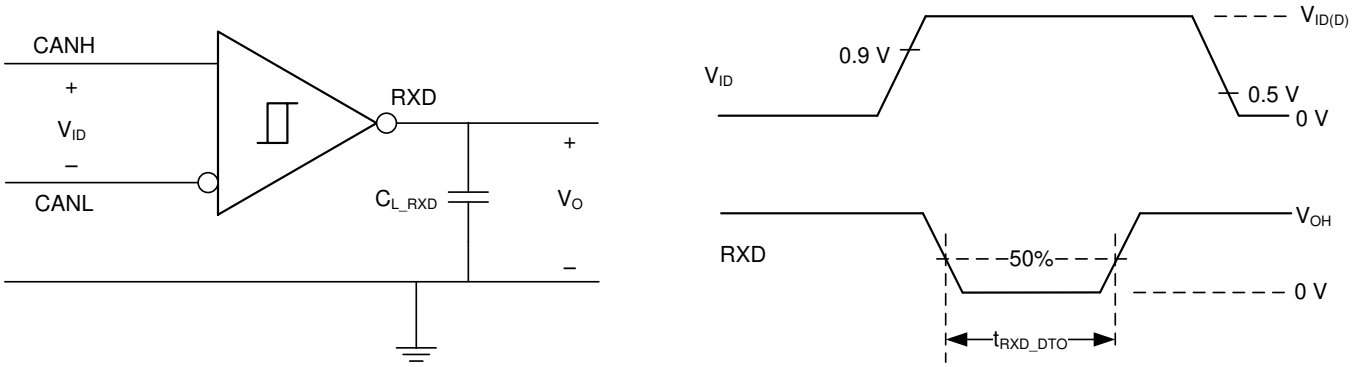

Figure 27. RXD Dominant Timeout Test Circuit and Measurement

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Parameter Measurement Information (continued)

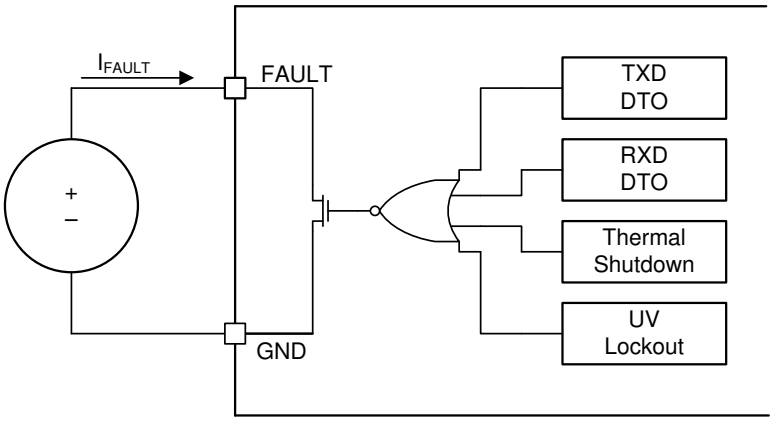


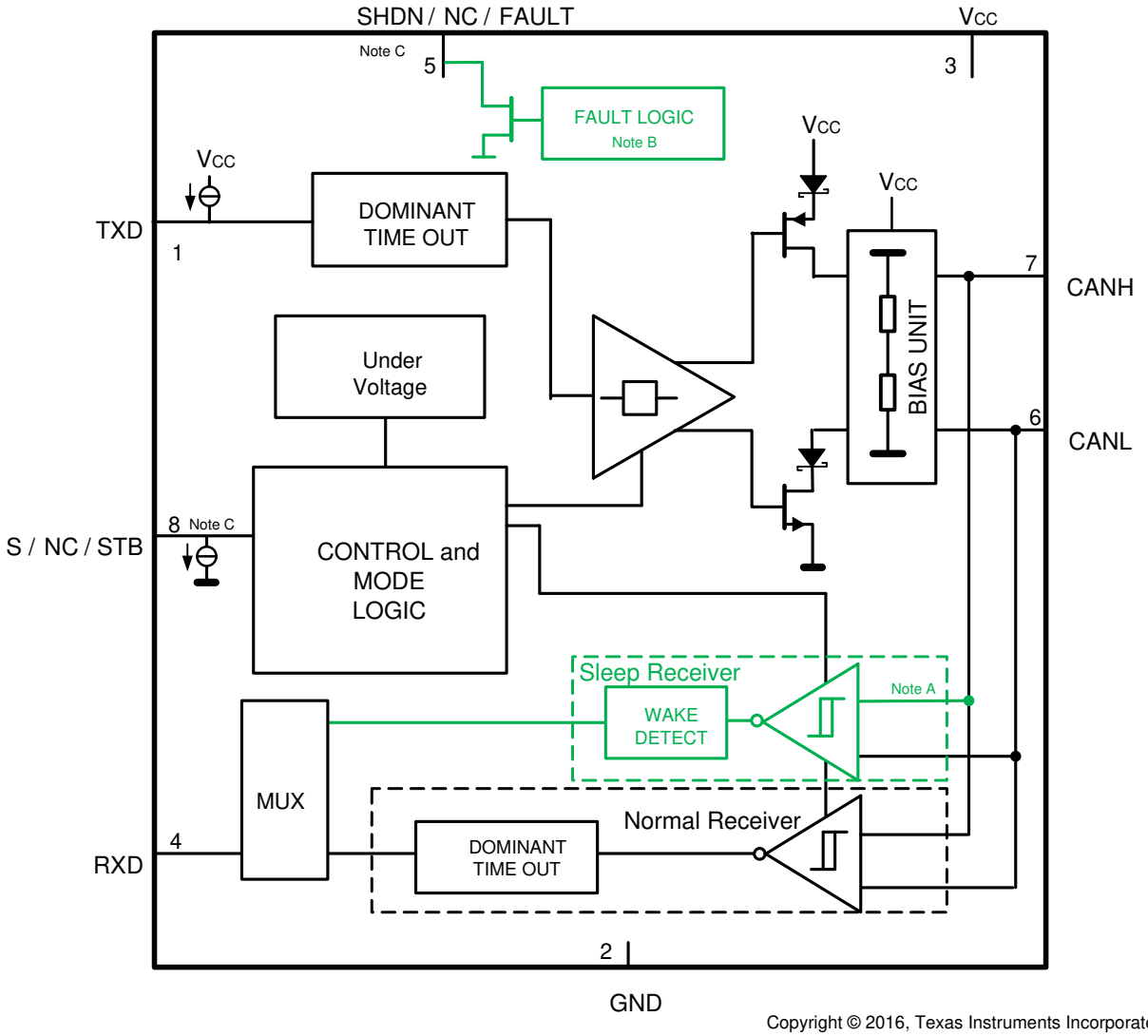
Figure 28. FAULT Test and Measurement

10 Detailed Description

10.1 Overview

This family of CAN transceivers is compatible with the ISO11898-2 High-Speed CAN (controller area network) physical layer standard. They are designed to interface between the differential bus lines in CAN and the CAN protocol controller.

10.2 Functional Block Diagram



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A. Sleep Receiver and Wake Detect are device dependent options and are only available in TCAND334.

B. Fault Logic is only available in TCAND337.

C. Pin 5 and 8 functions are device dependent. Refer to *Device Options*.

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10.3 Feature Description

10.3.1 TXD Dominant Timeout (TXD DTO)

During normal mode (the only mode where the CAN driver is active), the TXD DTO circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The DTO circuit timer starts on a falling edge on TXD. The DTO circuit disables the CAN bus driver if no rising edge is seen before the timeout period expires. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on TXD pin, thus clearing the TXD DTO condition. The receiver and RXD pin still reflect the CAN bus, and the bus pins are biased to recessive level during a TXD dominant timeout.

10.3.2 RXD Dominant Timeout (RXD DTO)

All devices have a RXD DTO circuit that prevents a bus stuck dominant fault from permanently driving the RXD output dominant (low) when the bus is held dominant longer than the timeout period t_{RXD_DTO}. The RXD DTO timer starts on a falling edge on RXD (bus going dominant). If no rising edge (bus returning recessive) is seen before the timeout constant of the circuit expires (t_{RXD_DTO}), the RXD pin returns high (recessive). The RXD output is re-activated to mirror the bus receiver output when a recessive signal is seen on the bus, clearing the RXD dominant timeout. The CAN bus pins are biased to the recessive level during a RXD DTO.

10.3.3 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shutdown threshold, the device turns off the CAN driver circuits thus blocking the TXD-to-bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below the thermal shutdown temperature of the device. If the fault condition that caused the thermal shutdown is still present, the temperature may rise again and the device will enter thermal shut down again. Prolonged operation with thermal shutdown conditions may affect device reliability. The thermal shutdown circuit includes hysteresis to avoid oscillation of the driver output.

During thermal shutdown the CAN bus drivers are turned off, thus no transmission is possible from TXD to the bus. The CAN bus pins are biased to recessive level during a thermal shutdown and the receiver to RXD path remains operational.

10.3.4 Undervoltage Lockout and Unpowered Device

The V_{CC} supply terminal has under voltage detection which will place the device in protected mode if the supply drops below the UVLO threshold. This protects the bus during an under voltage event on V_{CC} by placing the bus into a high impedance biased to ground state and the RXD terminal into a tri-stated (high impedance) state. During undervoltage the device does not pass any signals from the bus. If the device is in normal mode and V_{CC} supply is lost the device will transition to a protected mode.

The device is designed to be an "ideal passive" or “no load” to the CAN bus if the device is unpowered. The bus terminals (CANH, CANL) have low leakage currents when the device is unpowered, so the device does not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational. Logic pins also have low leakage currents when the device is unpowered, so the device does not load other circuits which may remain powered.

Table 1. Undervoltage Protection 3.3-V Single Supply Devices

V_{CC}	DEVICE STATE	BUS	RXD
GOOD	Operational	Per Operating Mode	Per Operating Mode
BAD	Protected	Common mode bias to GND	High Impedance
UNPOWERED	Unpowered	High Impedance (no load)	High Impedance

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10.3.5 Fault Pin (TCAN337)

If one or more of the faults (TXD-Dominant Timeout, RXD dominant Timeout, Thermal Shutdown or Undervoltage Lockout) occurs, the FAULT pin (open-drain) turns off, resulting in a high level when externally pulled up to V_{CC} supply.

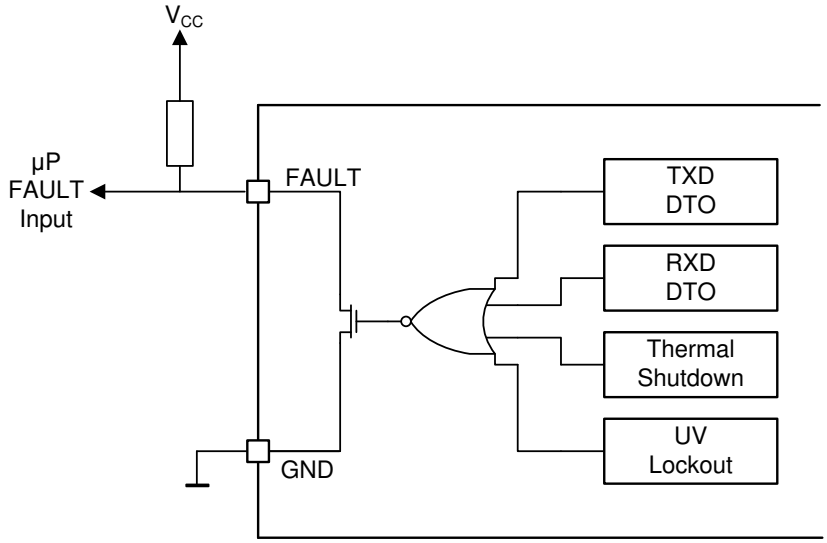

Figure 29. FAULT Pin Function Diagram and Application

10.3.6 Floating Pins

The device has internal pull ups and pull downs on critical terminals to place the device into known states if the pin floats. See Table 1 for details on pin bias conditions.

Table 2. Pin Bias

PIN	PULL UP or PULL DOWN	COMMENT
TXD	Pull up	Weakly biases TXD toward recessive to prevent bus blockage or TXD DTO triggering.
STB	Pull down	Weakly biases STB terminal towards normal mode.
S	Pull down	Weakly biases S terminal towards normal mode.
SHDN	Pull down	Weakly biases SHDN terminal towards normal mode.

The internal bias should not be relied on by design, especially in noisy environments, but should be considered a fall back protection. Special care needs to be taken when the device is used with MCUs using open drain outputs. TXD is weakly internally pulled up. The TXD pull up strength and CAN bit timing require special consideration when this device is used with an open drain TXD output on the microprocessor's CAN controller. An adequate external pull up resistor must be used to ensure that the TXD output of the microprocessor maintains adequate bit timing input to the CAN transceiver.

10.3.7 CAN Bus Short Circuit Current Limiting

The device has several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting (dominant and recessive). The device has TXD dominant time out which prevents permanently having the higher short circuit current of dominant state in case of a system fault. During CAN communication the bus switches between dominant and recessive states, thus the short circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in the termination resistors and common mode choke ratings the average short circuit current should be used. The percentage dominant is limited by the TXD dominant time out and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and interframe space. These ensure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

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The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated with the following formula:

$$I_{OS(AVG)} = \%Transmit \times [(\%REC_Bits \times I_{OS(SS)_REC}) + (\%DOM_Bits \times I_{OS(SS)_DOM})] + [\%Receive \times I_{OS(SS)_REC}] \quad (1)$$

Where:

- $I_{OS(AVG)}$ is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)_DOM}$ is the dominant steady state short circuit current

The short circuit current and possible fault cases of the network should be taken into consideration when sizing the power ratings of the termination resistance and other network components.

10.3.8 ESD Protection

The bus pins of the TCAN33x family possess on-chip ESD protection against ±25-kV human body model (HBM) and ±12-kV IEC61000-4-2 contact discharge. The IEC-ESD test is far more severe than the HBM-ESD test. The 50% higher charge capacitance, C_S, and 78% lower discharge resistance, R_D of the IEC model produce significantly higher discharge currents than the HBM-model.

As stated in the IEC 61000-4-2 standard, contact discharge is the preferred test method; although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results.

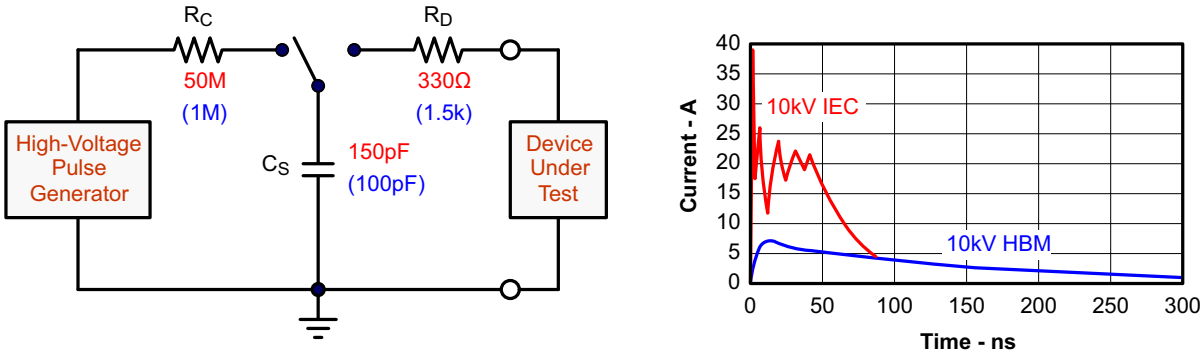

Figure 30. HBM and IEC-ESD Models and Currents in Comparison (HBM Values in Parenthesis)

10.3.9 Digital Inputs and Outputs

All the devices in this family are single 3.3-V nominal supply devices. The digital logic input and output levels for these devices have TTL threshold levels.

10.4 Device Functional Modes

10.4.1 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 31 and Figure 32.

Recessive bus state is when the high resistive internal input resistors of each node's receiver bias the bus to a common mode of about 1.85 V across the bus termination resistors. Recessive is equivalent to logic high and is typically a differential voltage on the bus of about 0 V. Recessive state is also the idle state.

Dominant bus state is when the bus is driven differentially by one or more drivers. Current is induced to flow through the termination resistors and generate a differential voltage on the bus. Dominant is equivalent to logic low and is a differential voltage on the bus greater than the minimum threshold for a CAN dominant. A dominant state overwrites the recessive state.

During arbitration, multiple CAN nodes may transmit a dominant bit at the same time. In this case the differential voltage of the bus will be greater than the differential voltage of a single driver.

The host microprocessor of the CAN node will use the TXD terminal to drive the bus and will receive data from the bus on the RXD pin.

Transceivers with low power Standby Mode have a third bus state where the bus terminals are weakly biased to ground via the high resistance internal resistors of the receiver. See Figure 31 and Figure 32.

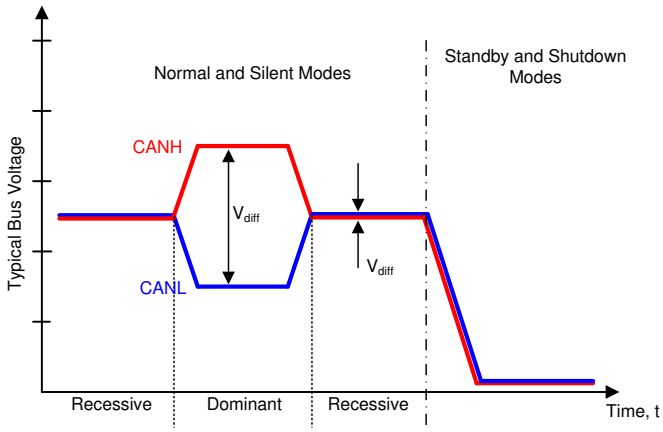

Figure 31. Bus States (Physical Bit Representation)

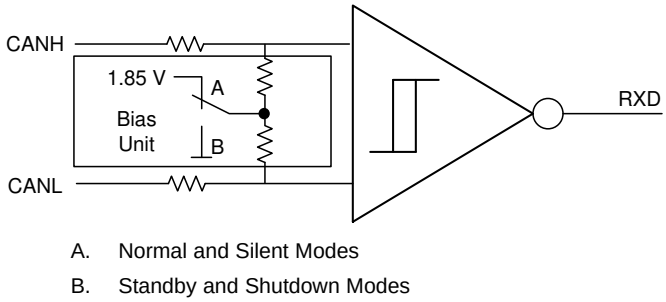

Figure 32. Simplified Recessive Common Mode Bias Unit and Receiver

The devices have four main operating modes:

1. Normal mode (all devices)
2. Silent mode (TCAN330, TCAN337)
3. Standby mode with wake (TCAN334)
4. Shutdown mode (TCAN330, TCAN334)

Table 3. CAN Transceivers with Silent Mode

S	Device MODE	DRIVER	RECEIVER	RXD PIN
HIGH	Reduced Power Silent (Listen) Mode	Disabled (OFF)(1)	Enabled (ON)	Mirrors Bus State(2)
LOW/NC	Normal Mode	Enabled (ON)	Enabled (ON)	

(1) See Figure 31 for bus state.
(2) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

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Table 4. CAN Transceivers with Standby Mode with Wake

STB	Device MODE	DRIVER	RECEIVER	RXD Terminal
HIGH	Ultra Low Current Standby Mode	Disabled (OFF)(1)	Low Power Receiver and Bus Monitor Enabled (ON)	High (Recessive) until WUP, then filtered mirrors of Bus State (2)
LOW/NC	Normal Mode	Enabled (ON)	Enabled (ON)	Mirrors Bus State (3)

(1) See Figure 31 for bus state.
(2) Standby Mode RXD behavior: See Figure 33.
(3) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

Table 5. CAN Transceivers with Shutdown Mode

SHDN	Device MODE	DRIVER	RECEIVER	RXD Terminal
HIGH	Lowest Current	Disabled (OFF)(1)	Disabled (OFF)	High (Recessive)
LOW/NC	Normal Mode	Enabled (ON)	Enabled (ON)	Mirrors Bus State (2)

(1) See Figure 31 for bus state.
(2) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

10.4.2 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

10.4.3 Silent Mode

This is the silent or receive only mode of the device. The CAN driver is disabled but the receiver is fully operational. CAN communication is unidirectional and only flows from the CAN bus through the receive path of the transceiver to the CAN protocol controller via the RXD output pin. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

10.4.4 Standby Mode with Wake

This is the low power mode of the device. The CAN driver and main receiver are turned off and bi-directional CAN communication is not possible. The low power receiver and bus monitor are enabled to allow for RXD Wake Requests via the CAN bus. A wake up request will be output to RXD (driven low) as shown in Figure 33. The local CAN protocol microprocessor should monitor RXD for transitions (high to low) and reactivate the device to normal mode based on the RXD Wake Request. The CAN bus pins are weakly pulled to GND during this mode, see Figure 32.

10.4.5 Bus Wake via RXD Request (BWRR) in Standby Mode

The TCAN334 with low power standby mode, offers a wake up from the CAN bus mechanism called bus wake via RXD Request (BWRR) to indicate to a host microprocessor that the bus is active and it should wake up and return to normal CAN communication.

This device uses the multiple filtered dominant wake-up pattern (WUP) from ISO11898-5 to qualify bus traffic into a request to wake the host microprocessor. The bus wake request is signaled to the microprocessor by a falling edge and low corresponding to a “filtered” bus dominant on the RXD terminal (BWRR).

The wake up pattern (WUP) consists of a filtered dominant bus, then a filtered recessive bus time followed by a second filtered bus time. Once the WUP is detected the device will start issuing wake up requests (BWRR) on the RXD terminal every time a filtered dominant time is received from the bus. The first filtered dominant initiates the WUP and the bus monitor waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received, the bus monitor waits on a filtered dominant and again; other bus traffic does not reset the bus monitor. Immediately upon receiving of the second filtered dominant, the bus monitor recognizes the WUP and transitions to BWRR mode. In this mode, RXD is driven low for all dominant bits lasting for longer than t_{WK_FILTER}. The RXD output during BWRR matches the classical 8-pin CAN devices, such as the TCANA1040A-Q1 device, that used the single filtered dominant on the bus as the wake up request mechanism from ISO11898-5.

For a dominant or recessive to be considered *filtered*, the bus must be in that state for more than t_{WK_FILTER} time. Due to variability in the t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK_FILTER(MIN)}$ are never detected as part of a WUP and thus no BWRR is generated. Bus state times between $t_{WK_FILTER(MIN)}$ and $t_{WK_FILTER(MAX)}$ may be detected as part of a WUP and a BWRR may be generated. Bus state times more than $t_{WK_FILTER(MAX)}$ are always detected as part of a WUP and thus a BWRR is always generated.

See Figure 33 for the timing diagram of the WUP. The pattern, t_{WK_FILTER} time used for the WUP and BWRR prevent noise and bus stuck dominant faults from causing false wake requests. If the device is switched to normal mode, or an under voltage event occurs on V_{CC} the BWRR will be lost.

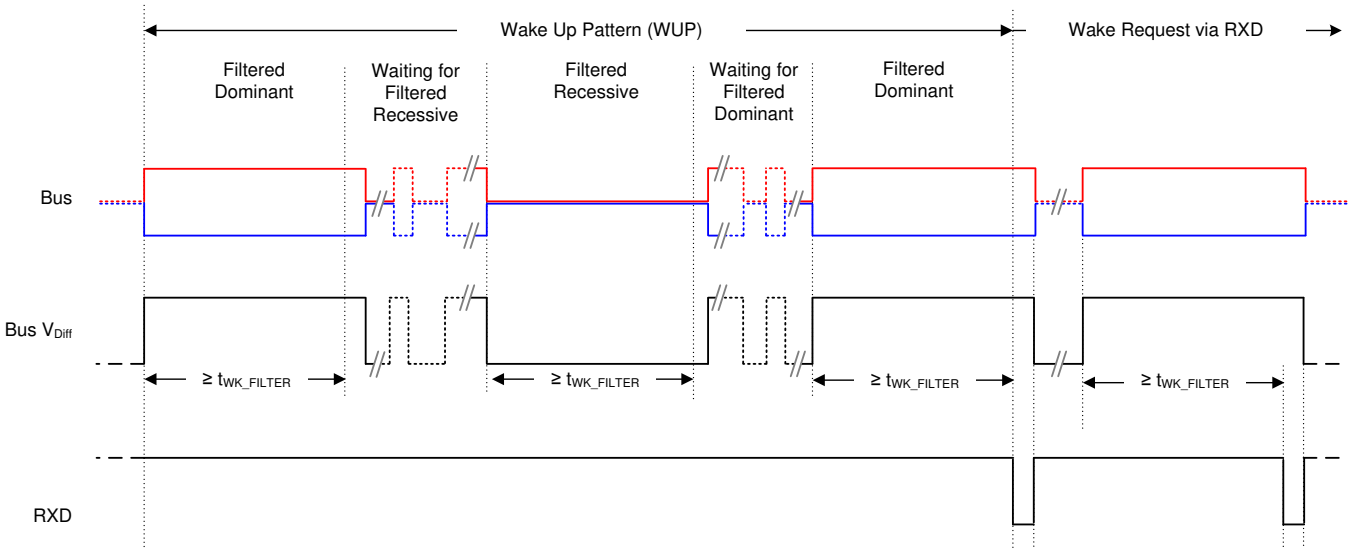

Figure 33. Wake Up Pattern (WUP) and Bus Wake via RXD Request (BWRR)

10.4.6 Shutdown Mode

This is the lowest power mode of all of the devices. The CAN driver and receiver are turned off and bi-directional CAN communication is not possible. It is not possible to receive a remote wake request via the CAN bus in this mode. The CAN bus pins are pulled to GND during this mode as shown in Figure 31.

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10.4.7 Driver and Receiver Function Tables

Table 6. Driver Function Table

DEVICE MODE	TXD[1] INPUT	BUS OUTPUTS[2]		DRIVEN BUS STATE [3]
		CANH	CANL	
Normal	L	H	L	Dominant
	H or Open	Z	Z	Biased Recessive
Silent	X	Z	Z	Biased Recessive
Standby	X	Z	Z	Weak Pull to GND
Shutdown	X	Z	Z	Weak Pull to GND

(1) H = high level, L = low level, X = irrelevant.
(2) H = high level, L = low level, Z = high Z receiver bias.
(3) For Bus state and bias see Figure 31 and Figure 32.

Table 7. Receiver Function Table Normal and Standby Modes

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{(ID)} = V_{(CANH)} - V_{(CANL)}$	BUS STATE	RXD PIN[1]
Normal or Silent	$V_{(ID)} \geq 0.9$ V	Dominant	L
	$0.5 V < V_{(ID)} < 0.9$ V	?	?
	$V_{(ID)} \leq 0.5$ V	Recessive	H
Standby	$V_{(ID)} \geq 1.15$ V	Dominant	See Figure 33
	$0.4 V < V_{(ID)} < 1.15$ V	?	
	$V_{(ID)} \leq 0.4$ V	Recessive	
Shutdown	Any	Recessive	H
Any	Open ($V_{(ID)} \approx 0$ V)	Open	H

(1) I = high level, L = low level, ? = indeterminate.

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

11.1.1 Bus Loading, Length and Number of Nodes

The ISO 11898 standard specifies a data rate up to 1 Mbps, maximum CAN bus cable length of 40 m, maximum drop line (stub) length of 0.3 m and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898 standard. They have made system level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, CAN Kingdom, DeviceNet and NMEA200.

A high number of nodes requires a transceiver with high input impedance and wide common mode range such as the TCAN33x CAN family. ISO 11898-2 specifies the driver differential output with a 60-Ω load (two 120- Ω termination resistors in parallel) and the differential output must be greater than 1.5 V. The TCAN33x devices are specified to meet the 1.5-V requirement with a 50-Ω load across a common mode range of –12 V to 12 V through a 330-Ω coupling network. This network represents the bus loading of 120 TCAN33x transceivers based on their minimum differential input resistance of 40 kΩ.

For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity, thus a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, number of nodes and data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898 CAN standard.

11.2 Typical Application

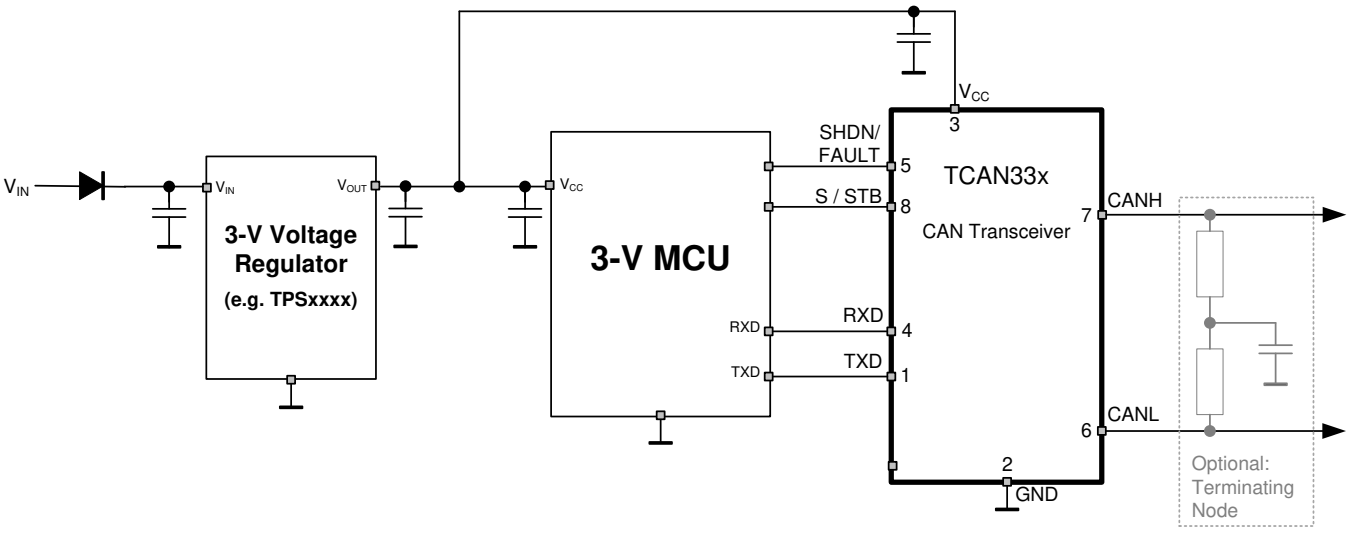

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Figure 34. Typical 3.3-V Application

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Typical Application (continued)

11.2.1 Design Requirements

11.2.1.1 CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted-pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

11.2.2 Detailed Design Procedure

Termination is typically a 120-Ω resistor at each end of the bus. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used (see Figure 8). Split termination uses two 60-Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltages at the start and end of message transmissions.

Care should be taken in the power ratings of the termination resistors used. Typically the worst case condition would be if the system power supply was shorted across the termination resistance to ground. In most cases the current flow through the resistor in this condition would be much higher than the transceiver's current limit.

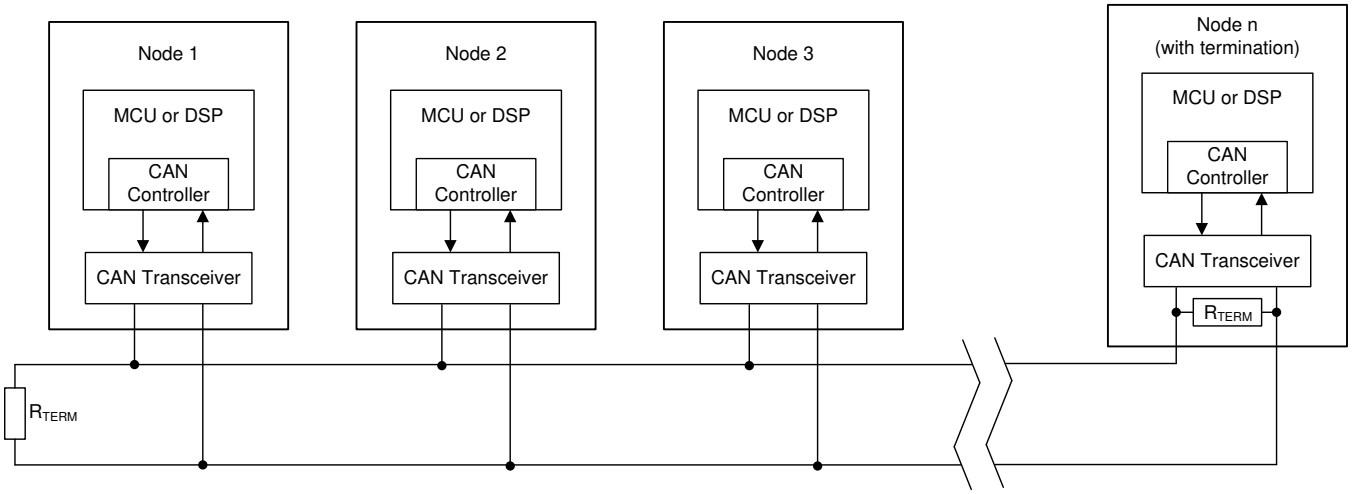


Figure 35. Typical CAN Bus

Typical Application (continued)

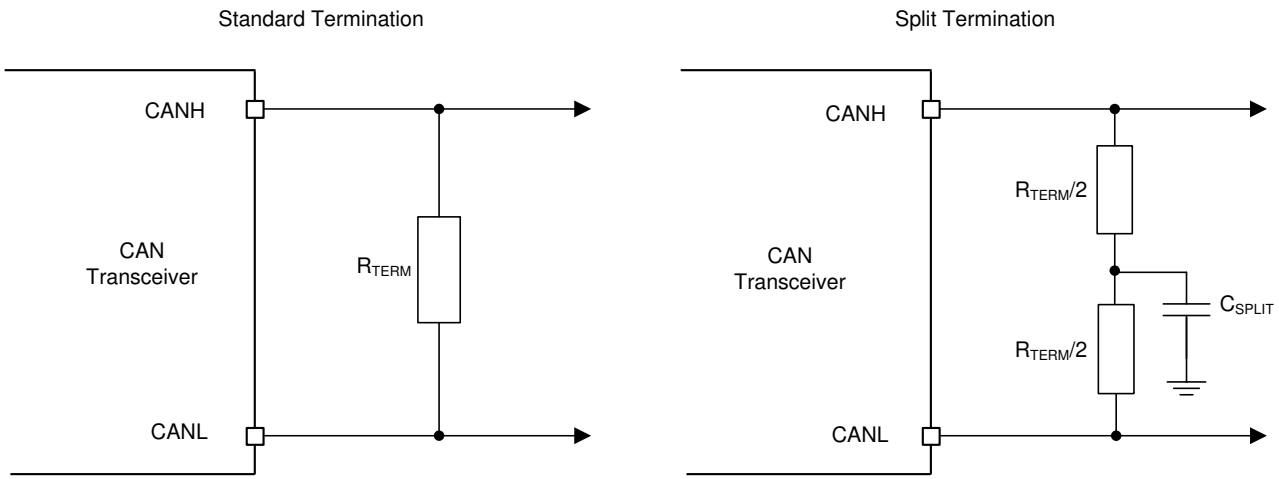
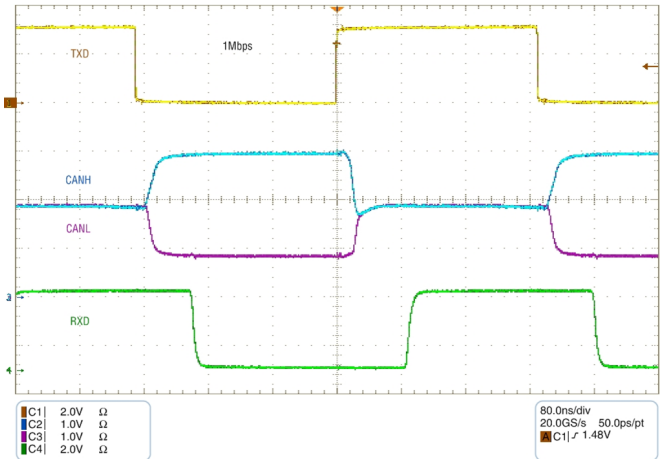


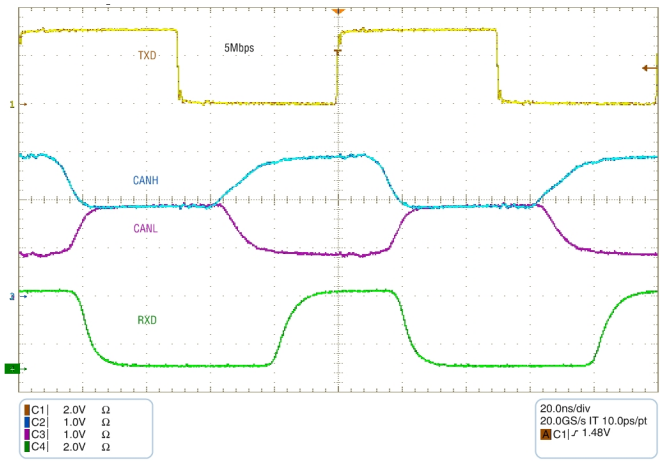
Figure 36. CAN Bus Termination Concepts

11.2.3 Application Curves



1 Mbps Temp = 25°C V_{CC} = 3.3 V
60 Ω Load

Figure 37. TXD, CANH/L and RXD Waveforms



5 Mbps Temp = 25°C V_{CC} = 3.3 V
60 Ω Load

Figure 38. TXD, CANH/L and RXD Waveforms

11.3 System Examples

11.3.1 ISO11898 Compliance of TCAN33x Family of 3.3-V CAN Transceivers Introduction

Many users value the low power consumption of operating their CAN transceivers from a 3.3-V supply. However, some are concerned about the interoperability with 5 V supplied transceivers on the same bus. This report analyzes this situation to address those concerns.

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System Examples (continued)

11.3.2 Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single ended logic level output signal.

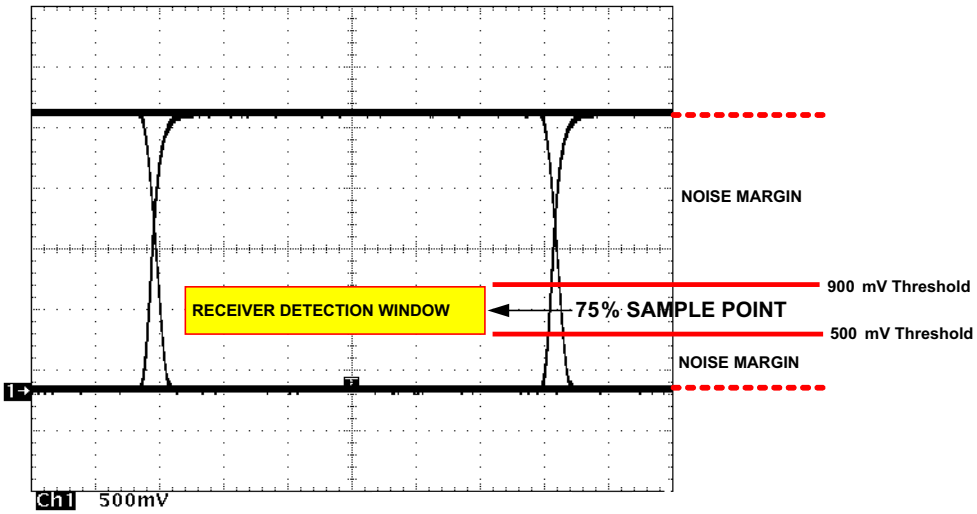

Figure 39. Typical Differential Output Waveform

The CAN driver creates the differential voltage between CANH and CANL in the dominant state. The dominant differential output of the TCAN33x is greater than 1.5 V and less than 3 V across a 60-Ω load as defined by the ISO11898 standard. These are the same limiting values for 5 V supplied CAN transceivers. The bus termination resistors drive the recessive bus state and not the CAN driver.

A CAN receiver is required to output a recessive state when less than 500 mV of differential voltage exists on the bus, and a dominant state when more than 900 mV of differential voltage exists on the bus. The CAN receiver must do this with common-mode input voltages from –2 V to 7 V. The TCAN33x family receivers meet these same input specifications as 5 V supplied receivers.

11.3.3 Common-Mode Signal and EMC Performance

A common-mode signal is an average voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. Since the bias voltage of the recessive state of the device is dependent on V_{CC}, any noise present or variation of V_{CC} has an effect on this bias voltage seen by the bus. The TCAN33x family has the recessive bias voltage set higher than 0.5 x V_{CC} to match common mode in recessive mode to dominant mode. This results in superior EMC performance.

12 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the V_{CC} supply pins as possible. The TPS76333 is a linear voltage regulator suitable for the 3.3 V supply.

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13 Layout

13.1 Layout Guidelines

TCAN33x family of devices incorporates integrated IEC 61000-4-2 ESD protection. Should the system requires additional protection against ESD, EFT or surge, additional external protection and filtering circuitry may be needed.

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. Below is a list of layout recommendations when designing a CAN transceiver into an application.

- Transient Protection on CANH and CANL: Transient Voltage Suppression (TVS) and capacitors (D1, C5 and C7 shown in Figure 40) can be used for additional system level protection. These devices must be placed as close to the connector as possible. This prevents the transient energy and noise from penetrating into other nets on the board.
- Bus Termination on CANH and CANL: Figure 40 shows split termination where the termination is split into two resistors, R5 and R6, with the center or split tap of the termination connected to ground through capacitor C6. Split termination provides common mode filtering for the bus. When termination is placed on the board instead of directly on the bus, care must be taken to ensure the terminating node is not removed from the bus, as this causes signal integrity issues if the bus is not properly terminated on both ends.
- Decoupling Capacitors on V_{CC}: Bypass and bulk capacitors must be placed as close as possible to the supply pins of transceiver (examples are C2 and C3).
- Ground and power connections: Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.
- Digital inputs and outputs: To limit current of digital lines, serial resistors may be used. Examples are R1, R2, R3 and R4.
- Filtering noise on digital inputs and outputs: To filter noise on the digital I/O lines, a capacitor may be used close to the input side of the I/O as shown by C1, C8 and C4.
- Fault Output Pin (TCAN337 only): Because the FAULT output pin is an open drain output, an external pullup resistor is required to pull the pin voltage high for normal operation (R7).
- TXD input pin: If an open-drain host processor is used to drive the TXD pin of the device, an external pullup resistor between 1 kΩ and 10 kΩ must be used to help drive the recessive input state of the device (weak internal pullup resistor).

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13.2 Layout Example

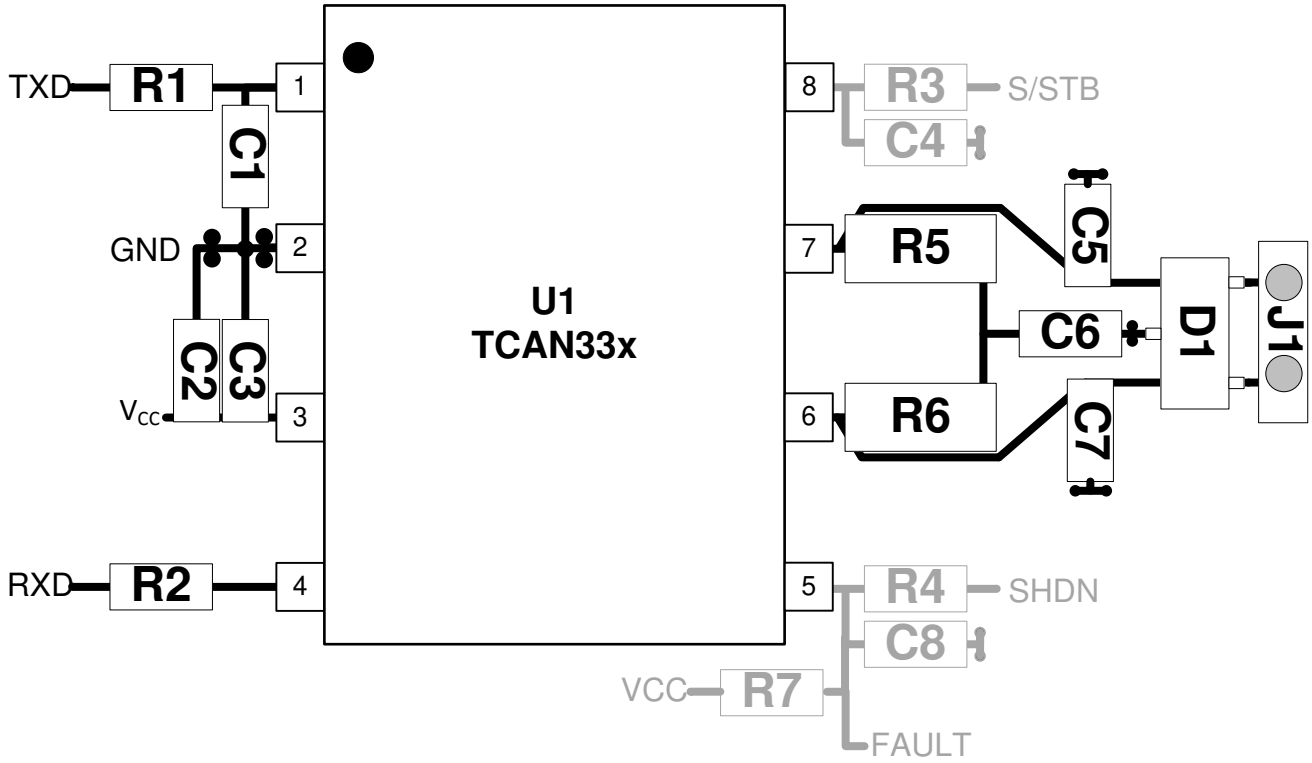

Figure 40. Layout Example

14 器件和文档支持

14.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **8.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
TCAN330	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TCAN332	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TCAN334	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TCAN337	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TCAN330G	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TCAN332G	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TCAN334G	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TCAN337G	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

14.2 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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14.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

14.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN330D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC330	Samples
TCAN330DCNR	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	330	Samples
TCAN330DCNT	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	330	Samples
TCAN330DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC330	Samples
TCAN330GD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC330	Samples
TCAN330GDCNR	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	330	Samples
TCAN330GDCNT	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	330	Samples
TCAN330GDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC330	Samples
TCAN332D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC332	Samples
TCAN332DCNR	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	332	Samples
TCAN332DCNT	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	332	Samples
TCAN332DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC332	Samples
TCAN332GD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC332	Samples
TCAN332GDCNR	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	332	Samples
TCAN332GDCNT	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	332	Samples
TCAN332GDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC332	Samples
TCAN334D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC334	Samples
TCAN334DCNR	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	334	Samples
TCAN334DCNT	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	334	Samples
TCAN334DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC334	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN334GD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC334	Samples
TCAN334GDCNR	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	334	Samples
TCAN334GDCNT	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	334	Samples
TCAN334GDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC334	Samples
TCAN337D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC337	Samples
TCAN337DCNR	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	337	Samples
TCAN337DCNT	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	337	Samples
TCAN337DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC337	Samples
TCAN337GD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC337	Samples
TCAN337GDCNR	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	337	Samples
TCAN337GDCNT	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	337	Samples
TCAN337GDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC337	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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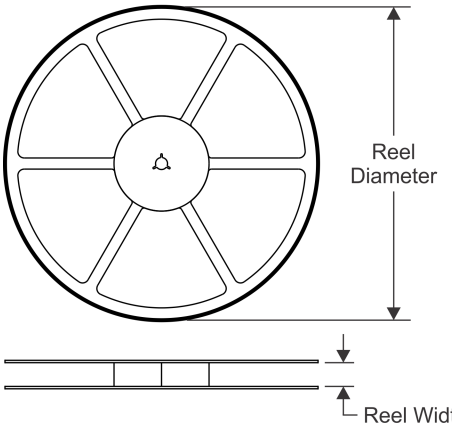
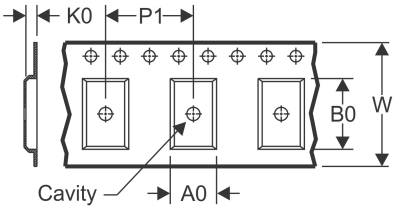
TAPE AND REEL INFORMATION

REEL DIMENSIONS

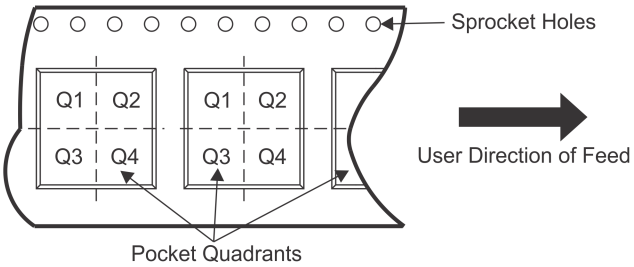


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

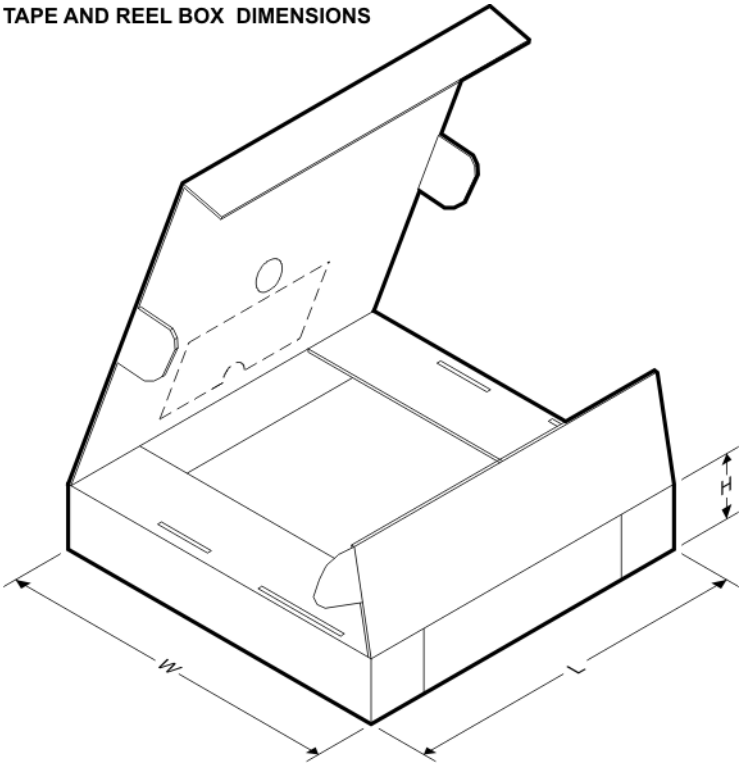


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN330DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN330DCNT	SOT-23	DCN	8	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN330DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN330GDCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN330GDCNT	SOT-23	DCN	8	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN330GDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN332DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN332DCNT	SOT-23	DCN	8	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN332DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN332GDCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN332GDCNT	SOT-23	DCN	8	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN332GDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN334DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN334DCNT	SOT-23	DCN	8	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN334DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN334GDCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN334GDCNT	SOT-23	DCN	8	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN334GDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN337DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN337DCNT	SOT-23	DCN	8	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN337DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN337GDCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN337GDCNT	SOT-23	DCN	8	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TCAN337GDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

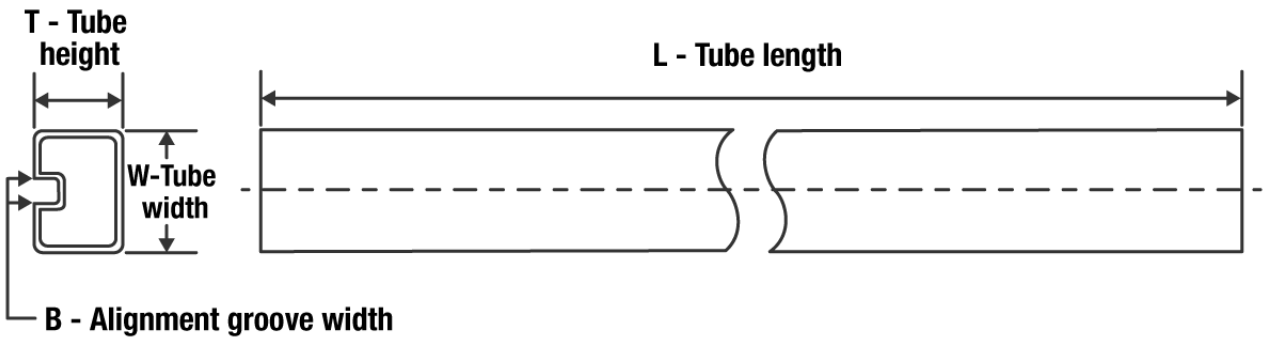


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN330DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TCAN330DCNT	SOT-23	DCN	8	250	202.0	201.0	28.0
TCAN330DR	SOIC	D	8	2500	340.5	336.1	25.0
TCAN330GDCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TCAN330GDCNT	SOT-23	DCN	8	250	202.0	201.0	28.0
TCAN330GDR	SOIC	D	8	2500	340.5	336.1	25.0
TCAN332DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TCAN332DCNT	SOT-23	DCN	8	250	202.0	201.0	28.0
TCAN332DR	SOIC	D	8	2500	340.5	336.1	25.0
TCAN332GDCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TCAN332GDCNT	SOT-23	DCN	8	250	202.0	201.0	28.0

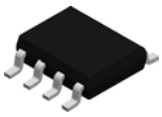
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN332GDR	SOIC	D	8	2500	340.5	336.1	25.0
TCAN334DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TCAN334DCNT	SOT-23	DCN	8	250	202.0	201.0	28.0
TCAN334DR	SOIC	D	8	2500	340.5	336.1	25.0
TCAN334GDCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TCAN334GDCNT	SOT-23	DCN	8	250	202.0	201.0	28.0
TCAN334GDR	SOIC	D	8	2500	340.5	336.1	25.0
TCAN337DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TCAN337DCNT	SOT-23	DCN	8	250	202.0	201.0	28.0
TCAN337DR	SOIC	D	8	2500	340.5	336.1	25.0
TCAN337GDCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TCAN337GDCNT	SOT-23	DCN	8	250	202.0	201.0	28.0
TCAN337GDR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TCAN330D	D	SOIC	8	75	507	8	3940	4.32
TCAN330GD	D	SOIC	8	75	507	8	3940	4.32
TCAN332D	D	SOIC	8	75	507	8	3940	4.32
TCAN332GD	D	SOIC	8	75	507	8	3940	4.32
TCAN334D	D	SOIC	8	75	507	8	3940	4.32
TCAN334GD	D	SOIC	8	75	507	8	3940	4.32
TCAN337D	D	SOIC	8	75	507	8	3940	4.32
TCAN337GD	D	SOIC	8	75	507	8	3940	4.32

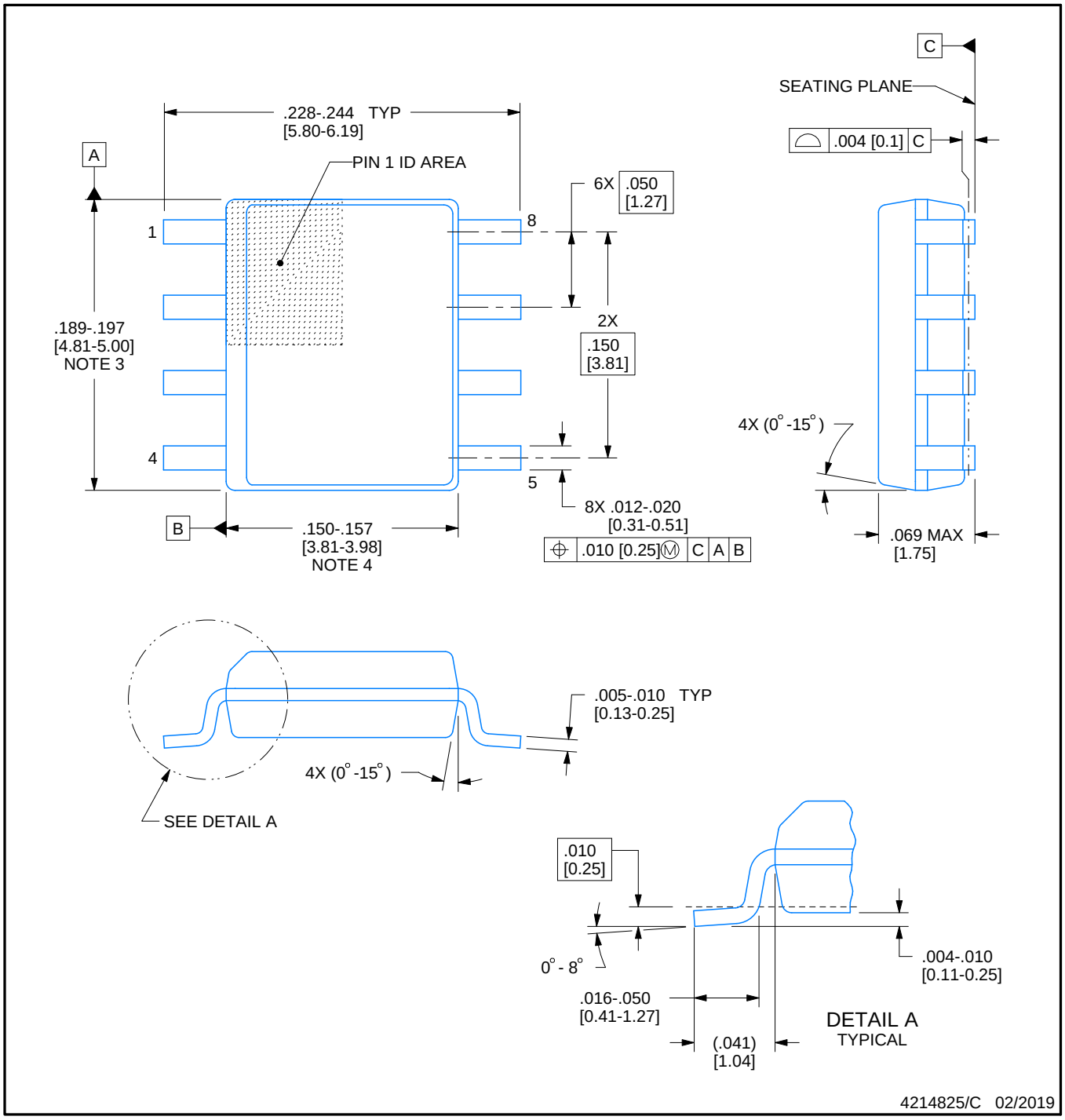


PACKAGE OUTLINE

D0008A

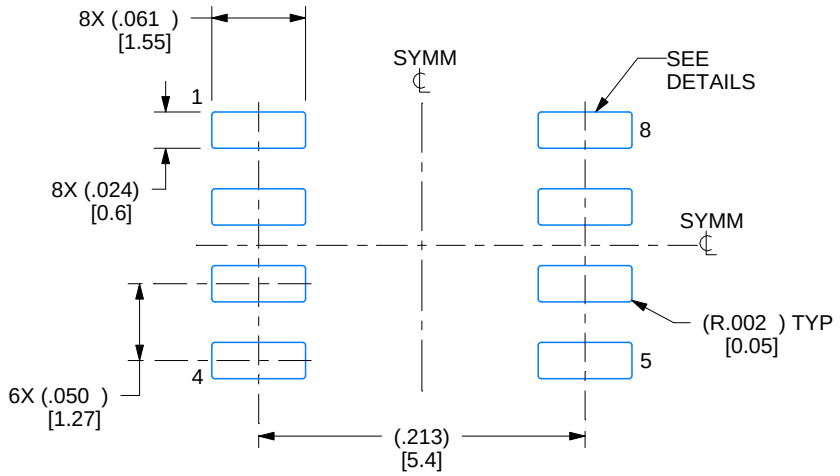
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

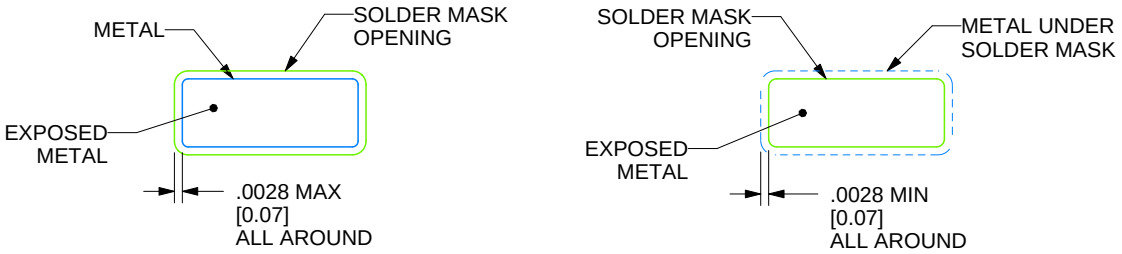


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

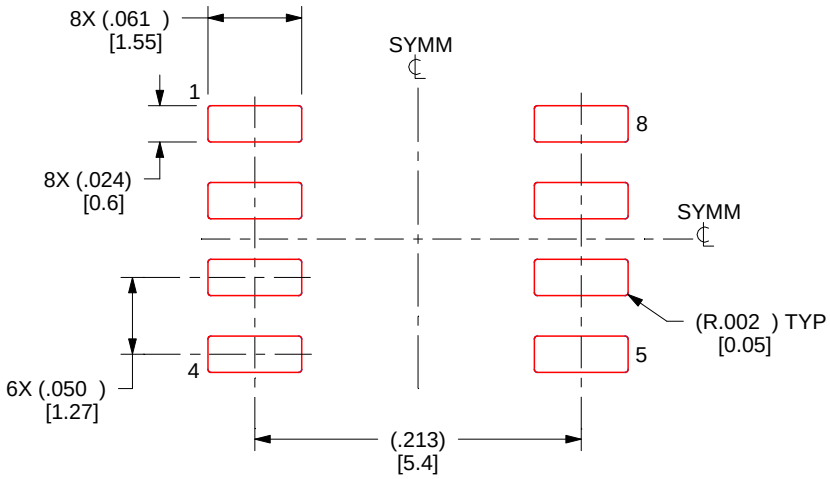


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



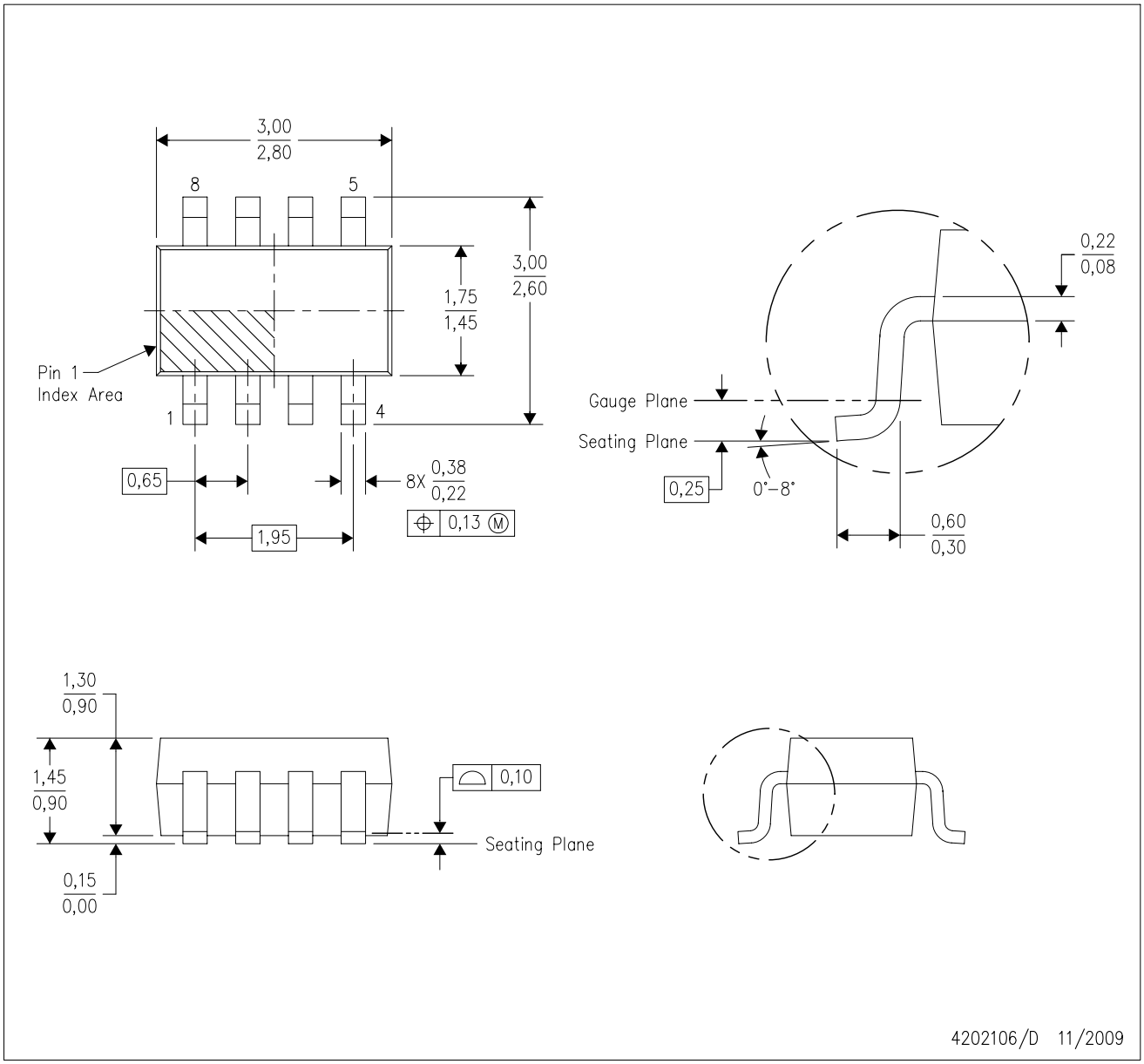
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

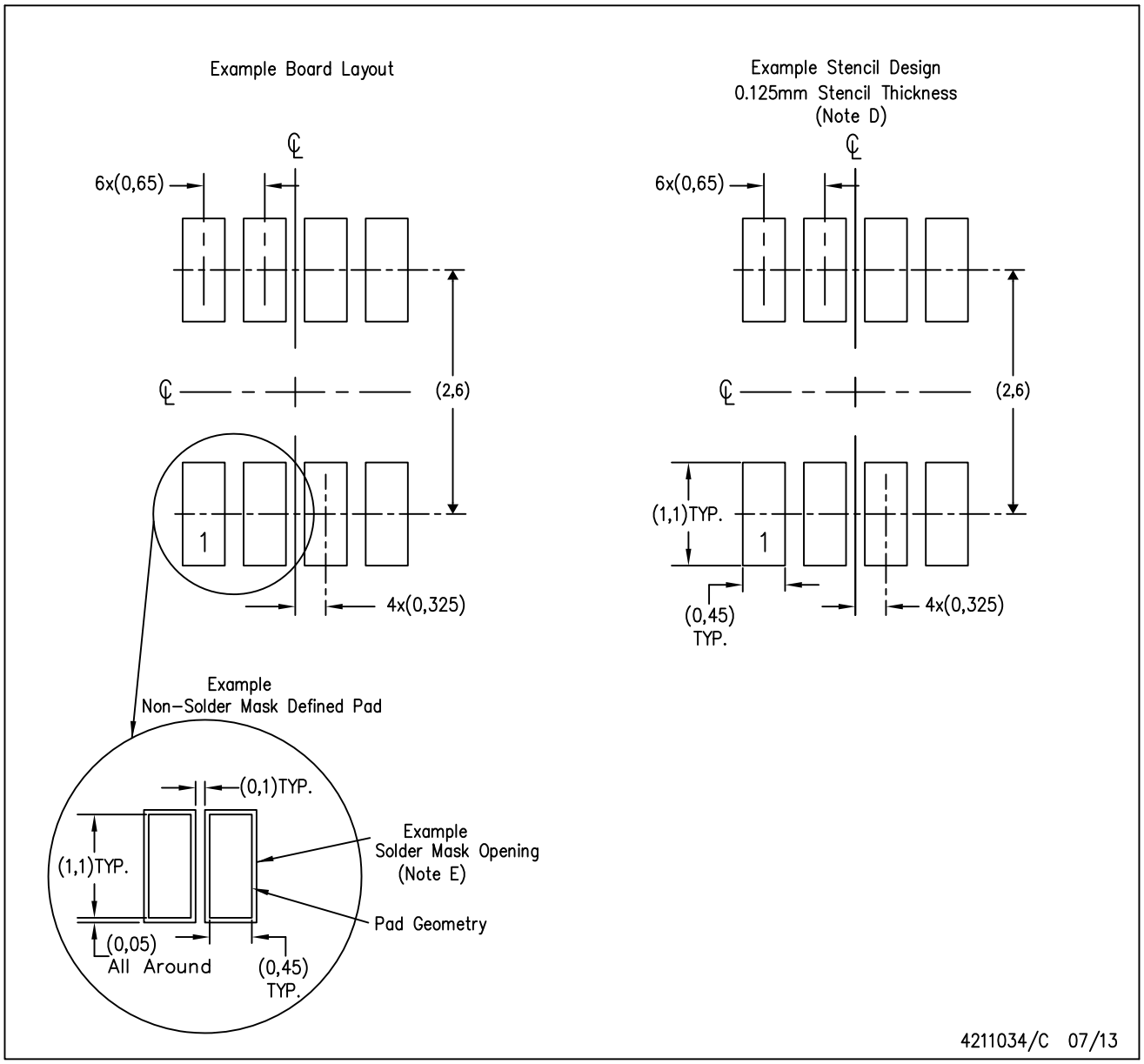
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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