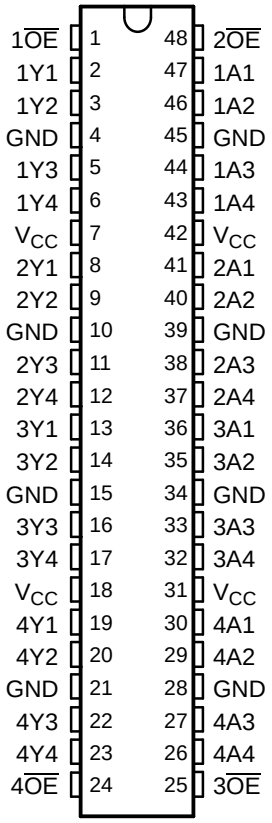
SN74ALVCH16244
16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES014K – JULY 1995 – REVISED OCTOBER 2005

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **Operates From 1.65 V to 3.6 V**
- **Max t_{pd} of 3 ns at 3.3 V**
- **±24-mA Output Drive at 3.3 V**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16244 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	FBGA – GRD	Tape and reel	SN74ALVCH16244GRDR	VH244
	FBGA – ZRD (Pb-free)		SN74ALVCH16244ZRDR	
	SSOP – DL	Tube	SN74ALVCH16244DL	ALVCH16244
		Tape and reel	SN74ALVCH16244DLR	
	TSSOP – DGG	Tape and reel	SN74ALVCH16244DGGR	ALVCH16244
			74ALVCH16244DGGRE4	
	TVSOP – DGV	Tape and reel	SN74ALVCH16244DGVR	VH244
			74ALVCH16244DGVRE4	
	VFBGA – GQL	Tape and reel	SN74ALVCH16244KR	VH244
	VFBGA – ZQL (Pb-free)		74ALVCH16244ZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

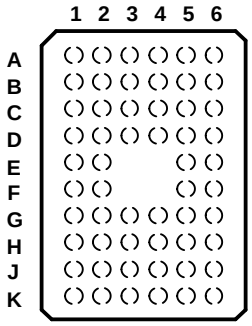
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1995–2005, Texas Instruments Incorporated

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

GQL OR ZQL PACKAGE
(TOP VIEW)

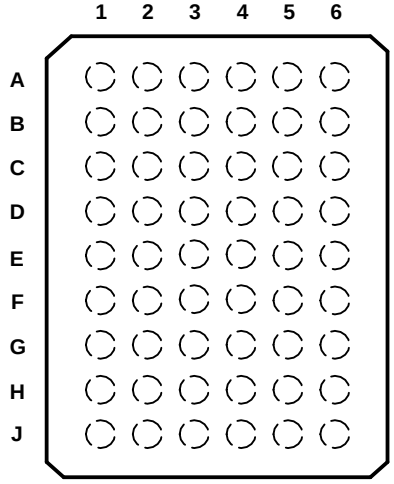


TERMINAL ASSIGNMENTS(1)
(56-Ball GQL/ZQL Package)

	1	2	3	4	5	6
A	1$\overline{OE}$	NC	NC	NC	NC	2$\overline{OE}$
B	1Y2	1Y1	GND	GND	1A1	1A2
C	1Y4	1Y3	V_{CC}	V_{CC}	1A3	1A4
D	2Y2	2Y1	GND	GND	2A1	2A2
E	2Y4	2Y3			2A3	2A4
F	3Y1	3Y2			3A2	3A1
G	3Y3	3Y4	GND	GND	3A4	3A3
H	4Y1	4Y2	V_{CC}	V_{CC}	4A2	4A1
J	4Y3	4Y4	GND	GND	4A4	4A3
K	4$\overline{OE}$	NC	NC	NC	NC	3$\overline{OE}$

(1) NC – No internal connection

GRD OR ZRD PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS(1)
(54-Ball GRD/ZRD Package)

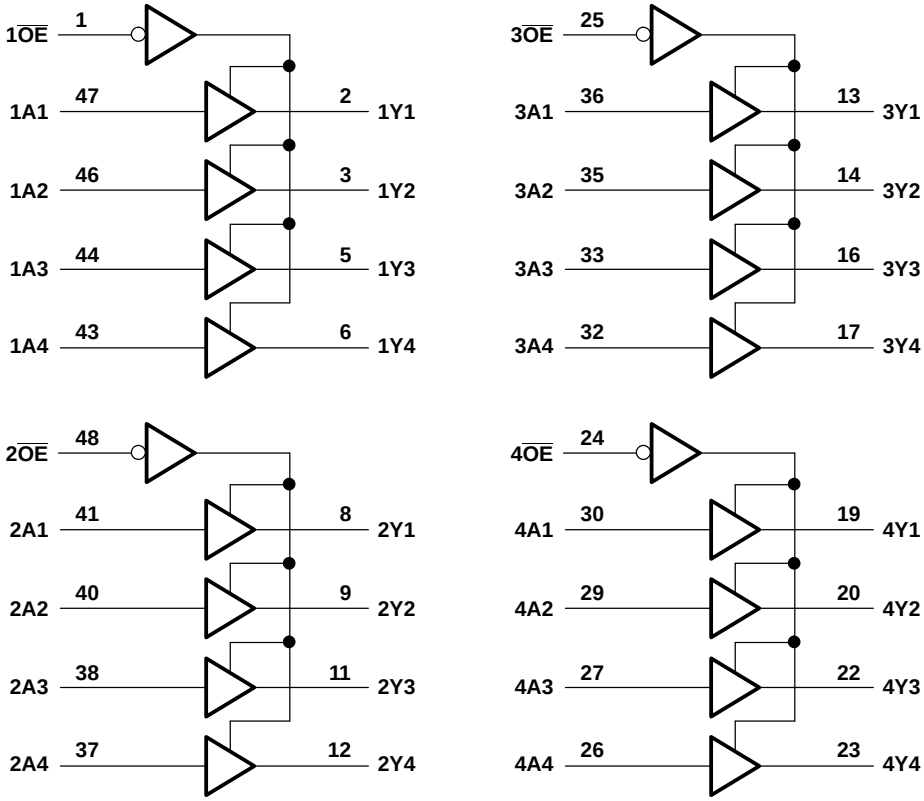
	1	2	3	4	5	6
A	1Y1	NC	1$\overline{OE}$	2$\overline{OE}$	NC	1A1
B	1Y3	1Y2	NC	NC	1A2	1A3
C	2Y1	1Y4	V_{CC}	V_{CC}	1A4	2A1
D	2Y3	2Y2	GND	GND	2A2	2A3
E	3Y1	2Y4	GND	GND	2A4	3A1
F	3Y3	3Y2	GND	GND	3A2	3A3
G	4Y1	3Y4	V_{CC}	V_{CC}	3A4	4A1
H	4Y3	4Y2	NC	NC	4A2	4A3
J	4Y4	NC	4$\overline{OE}$	3$\overline{OE}$	NC	4A4

(1) NC – No internal connection

FUNCTION TABLE
(EACH 4-BIT BUFFER)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DGV, and DL packages.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)		–0.5	4.6	V
V_O	Output voltage range(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		-50	mA
I_{OK}	Output clamp current	V_O < 0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(4)	DGG package		70	°C/W
		DGV package		58	
		DL package		63	
		GQL/ZQL package		42	
		GRD/ZRD package		36	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–12	
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		12	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		1.65 V to 3.6 V	V_{CC} – 0.2			V
		I_{OH} = –4 mA		1.65 V	1.2			
		I_{OH} = –6 mA		2.3 V	2			
		I_{OH} = –12 mA		2.3 V	1.7			
				2.7 V	2.2			
				3 V	2.4			
		I_{OH} = –24 mA		3 V	2			
V_{OL}		I_{OL} = 100 µA		1.65 V to 3.6 V			0.2	V
		I_{OL} = 4 mA		1.65 V			0.45	
		I_{OL} = 6 mA		2.3 V			0.4	
		I_{OL} = 12 mA		2.3 V			0.7	
				2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.58 V		1.65 V	25			µA
		V_I = 1.07 V		1.65 V	–25			
		V_I = 0.7 V		2.3 V	45			
		V_I = 1.7 V		2.3 V	–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V		3 V	–75			
		V_I = 0 to 3.6 V(2)		3.6 V			±500	
I_{OZ}		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		3		pF
	Data inputs					6		
C_o	Outputs	V_O = V_{CC} or GND		3.3 V		7		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	(1)	1	3.7		3.6	1	3	ns
t_{en}	$\overline{OE}$	Y	(1)	1	5.7		5.4	1	4.4	ns
t_{dis}	$\overline{OE}$	Y	(1)	1	5.2		4.6	1	4.1	ns

(1) This information was not available at the time of publication.

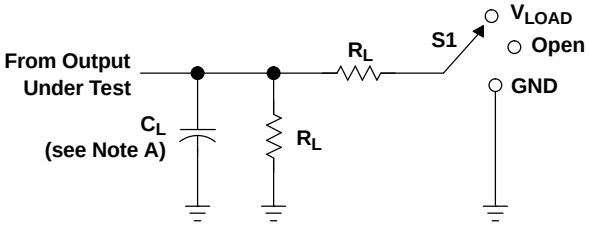
Operating Characteristics

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	(1)	16	19	pF
		Outputs disabled		(1)	4	5	

(1) This information was not available at the time of publication.

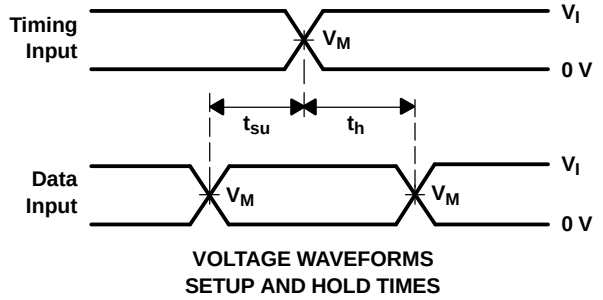
PARAMETER MEASUREMENT INFORMATION



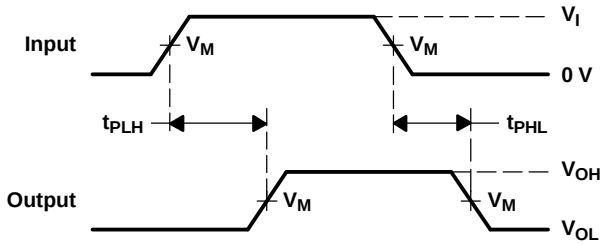
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

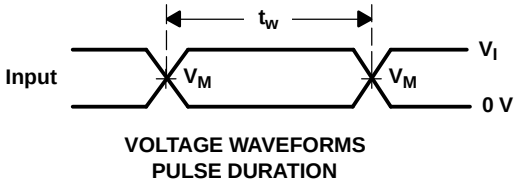
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



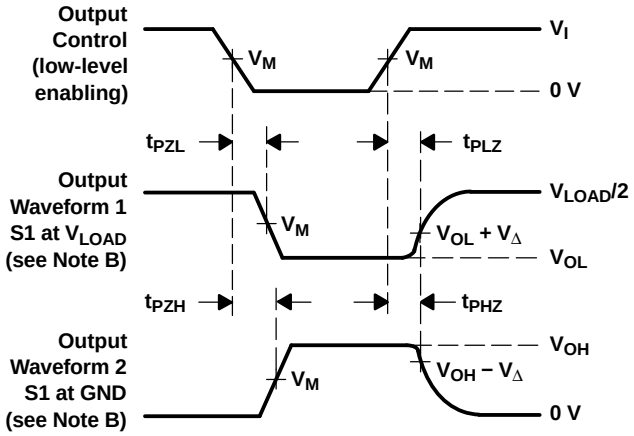
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ALVCH16244DGGRE4	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16244	Samples
74ALVCH16244DLG4	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16244	Samples
SN74ALVCH16244DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16244	Samples
SN74ALVCH16244DGVR	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VH244	Samples
SN74ALVCH16244DL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16244	Samples
SN74ALVCH16244DLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16244	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

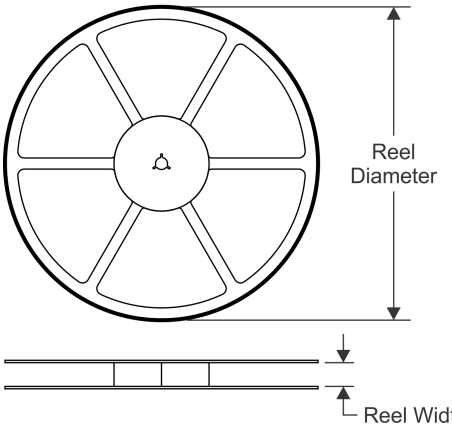
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

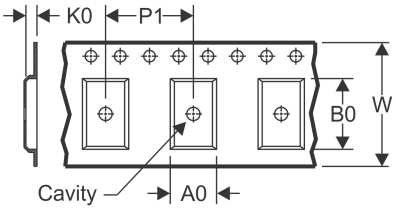
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

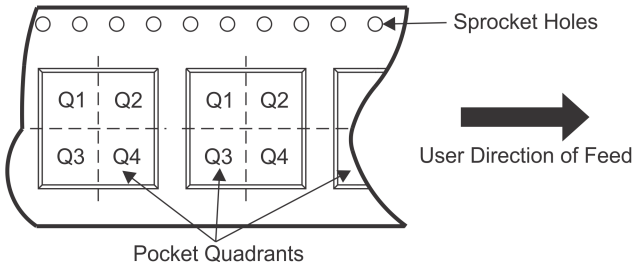


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

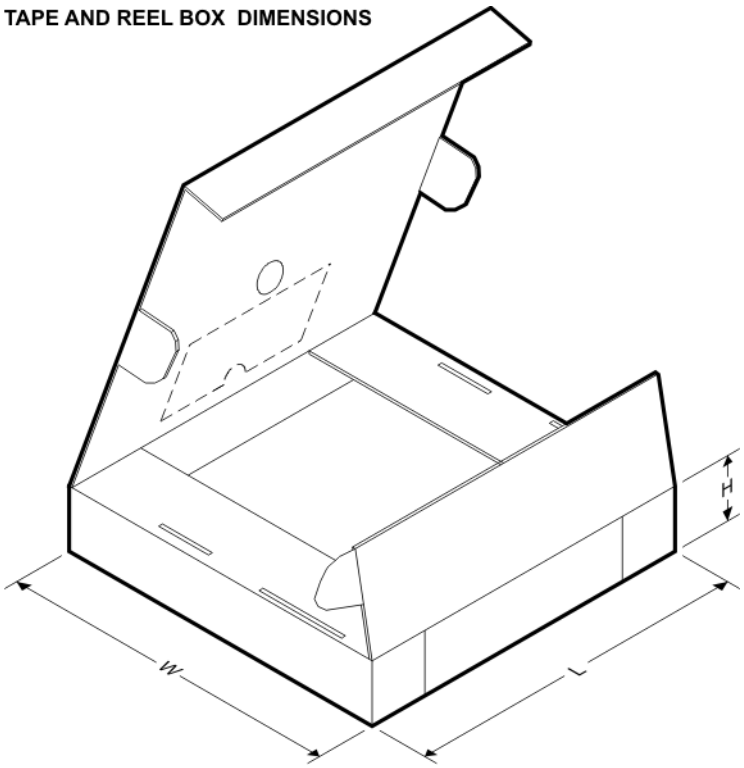
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16244DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ALVCH16244DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74ALVCH16244DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

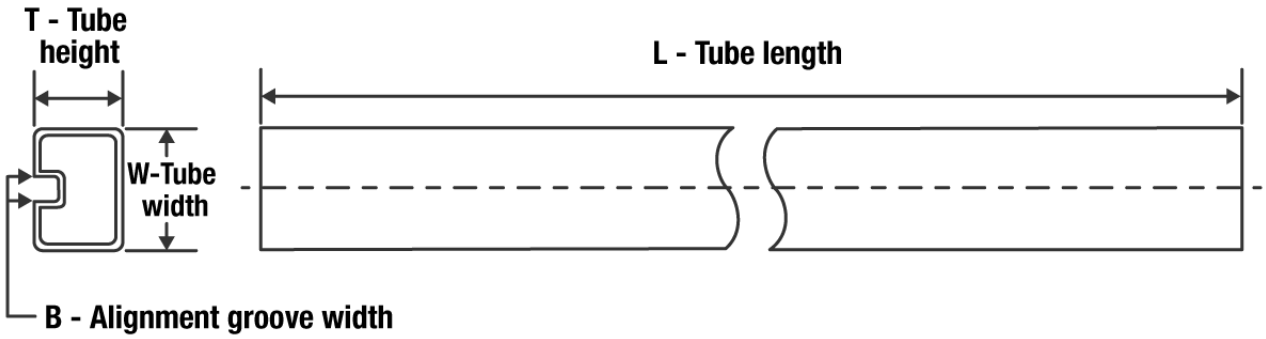
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16244DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ALVCH16244DGVR	TVSOP	DGV	48	2000	853.0	449.0	35.0
SN74ALVCH16244DLR	SSOP	DL	48	1000	367.0	367.0	55.0

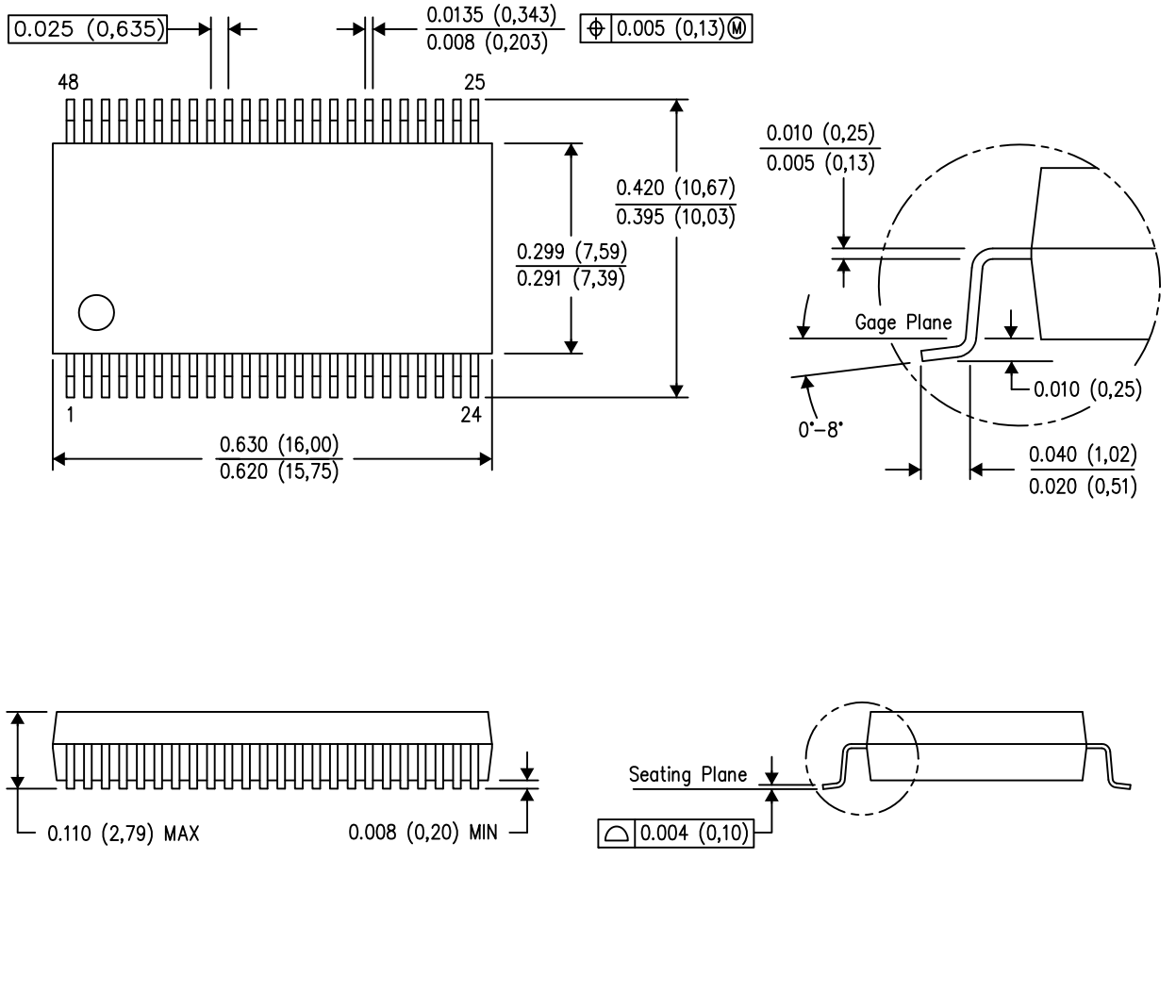
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
74ALVCH16244DLG4	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74ALVCH16244DL	DL	SSOP	48	25	473.7	14.24	5110	7.87

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE

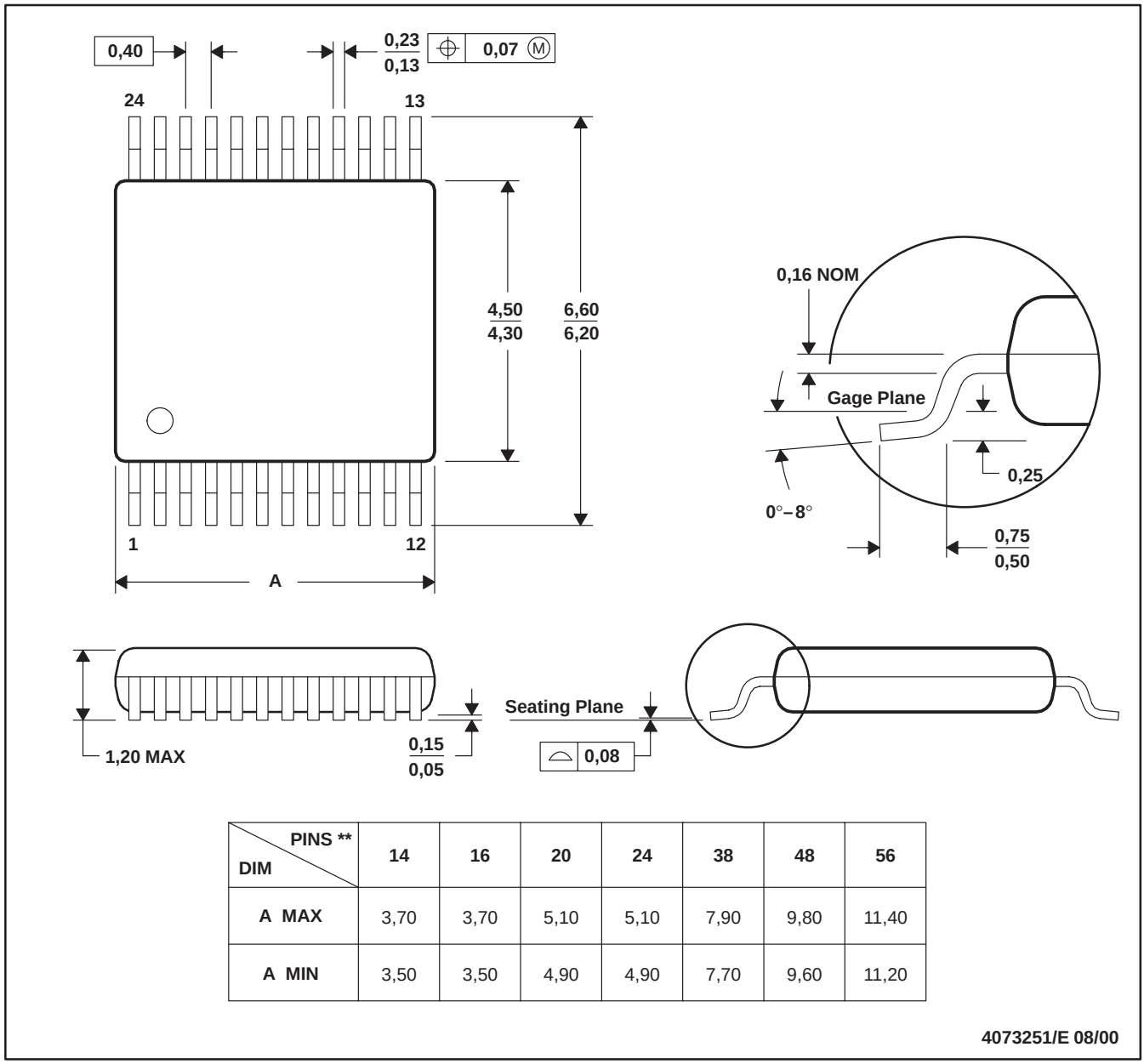


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

PowerPAD is a trademark of Texas Instruments.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

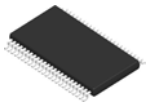
24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

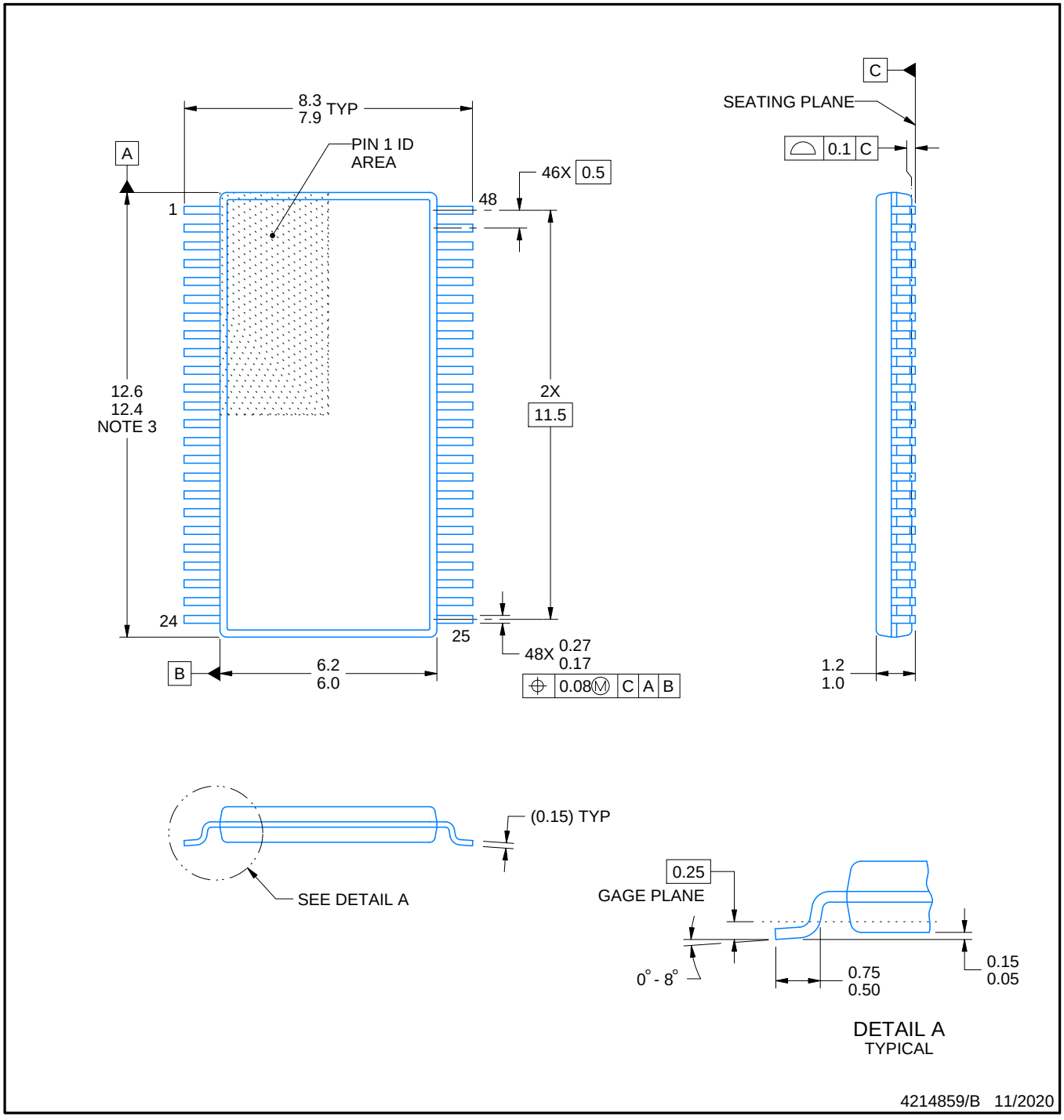


PACKAGE OUTLINE

DGG0048A

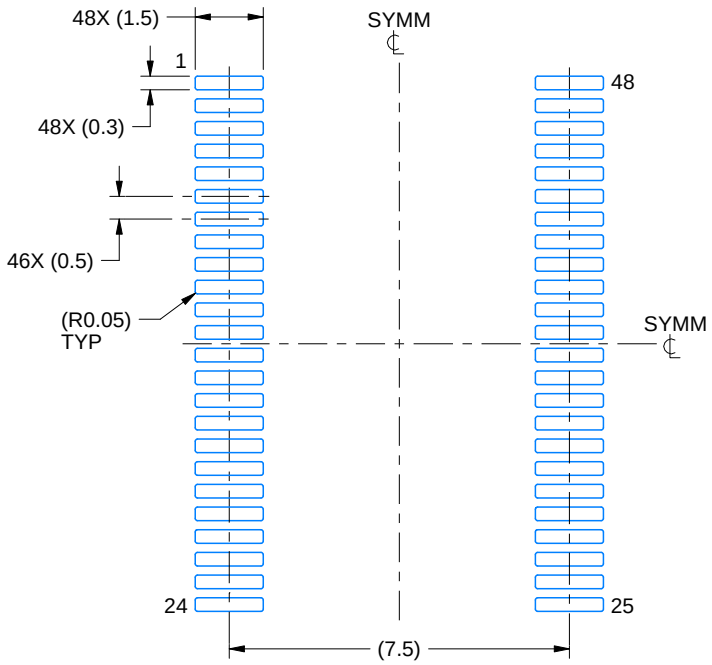
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

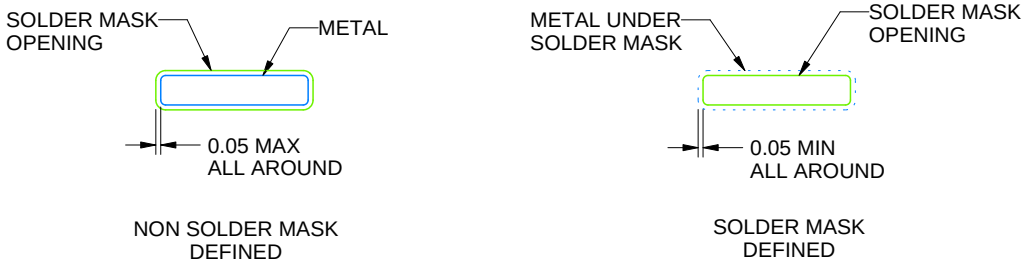


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

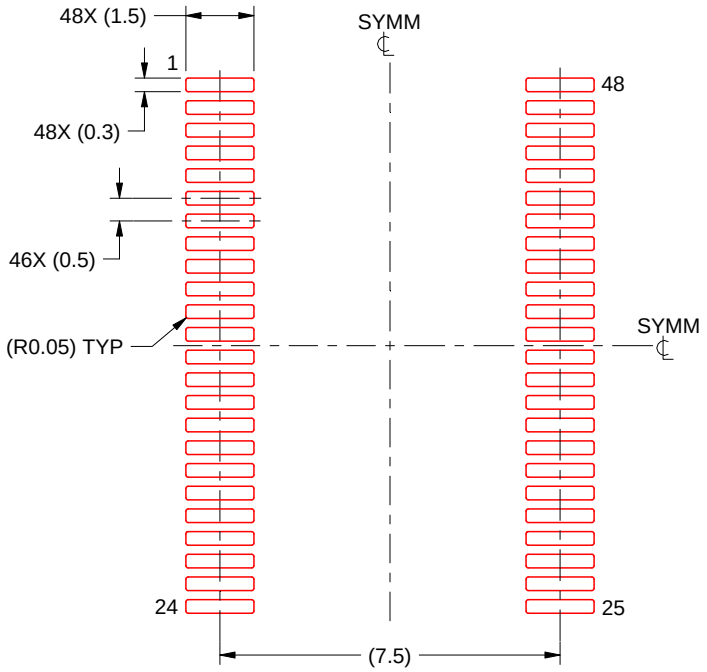


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

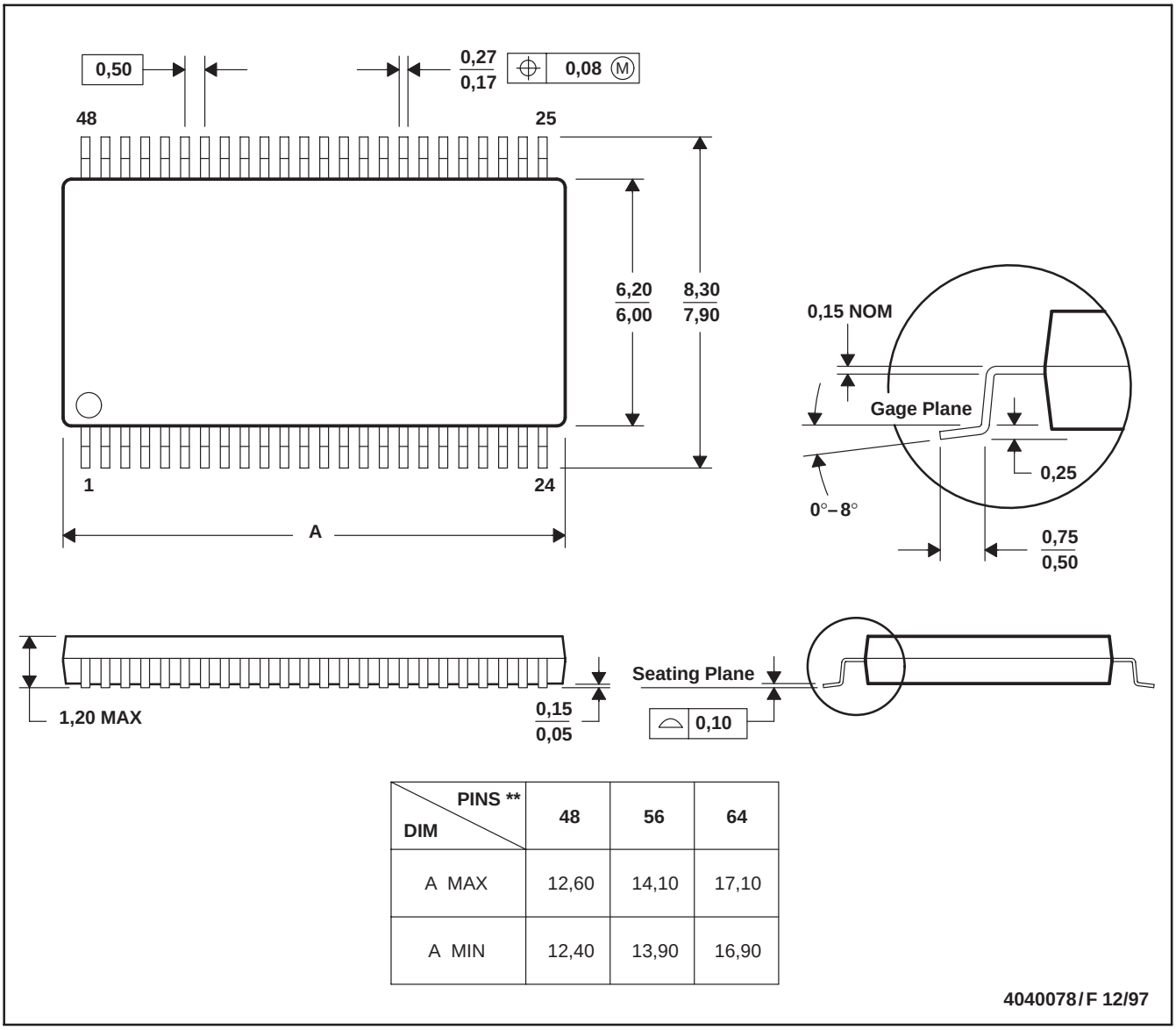
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated