DUAL OUTPUT BOOST WLED DRIVER USING SINGLE INDUCTOR

FEATURES

- **2.5V to 6V Input Voltage Range**
- **0.7A Integrated Switch**
- **Built-in Power Diode**
- **1.2MHz Fixed PWM Frequency**
- **Individually Programmable Output Current**
- **Input-to-Output Isolation**
- **Built-in Soft Start**
- **27V Overvoltage Protection**
- **3% at 15mA Matching between Two Current Strings, Improvement from TPS61150/1**
- **Up to 83% Efficiency**
- **Up to 30kHz PWM Dimming Frequency**
- **Availiable in a 10 Pin, 3 × 3 mm QFN Package**

APPLICATIONS

- **Up to 14 WLED Driver for Media Form Factor Display**
- **Sub and Main Display Backlight in Clam Shell Phones**
- **Display and Keypad Backlight in Portable Equipment**

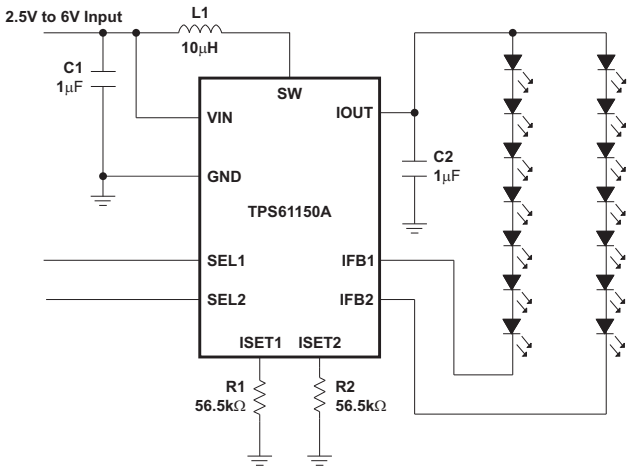
DESCRIPTION

The TPS61150A is a high frequency boost converter with two regulated current outputs for driving WLEDs. Each current output can be individually programmed through external resistors. There is dedicated selection pin for each output, so the two outputs can be turned on separately or simultaneously. The output current can be reduced by a pulse width modulation (PWM) signal on the select pins or an analog voltage on the ISET pin. The boost regulator runs at 1.2MHz fixed switching frequency to reduce output ripple and avoid audible noises associated with PFM control.

The two current outputs are ideal for driving WLED backlight for the sub and main displays in clam shell phones. The two outputs can also be used for driving display and keypad backlights. When used together, the two outputs can drive up to 14 WLED for one large display.

In addition to the small inductor, small capacitor and 3mm x 3mm QFN package, the built-in MOSFET and diode eliminate the need for any external power devices. Overall, the IC provides an extremely compact solution with high efficiency and plenty of flexibility.

TYPICAL APPLICATION



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

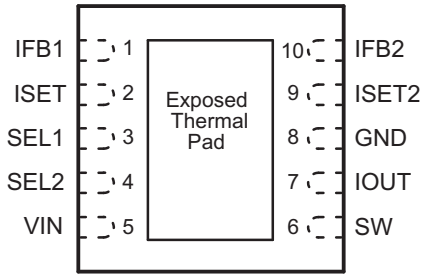
ORDERING INFORMATION(1)

T_A	PACKAGE	OVP (Typ.)	PACKAGE MARKING
–40 to 85°C	TPS61150ADRCR	28V	BTK
–40 to 85°C	TPS61150ADRCT	28V	BTK

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

DEVICE INFORMATION

QFN PACKAGE
(TOP VIEW)



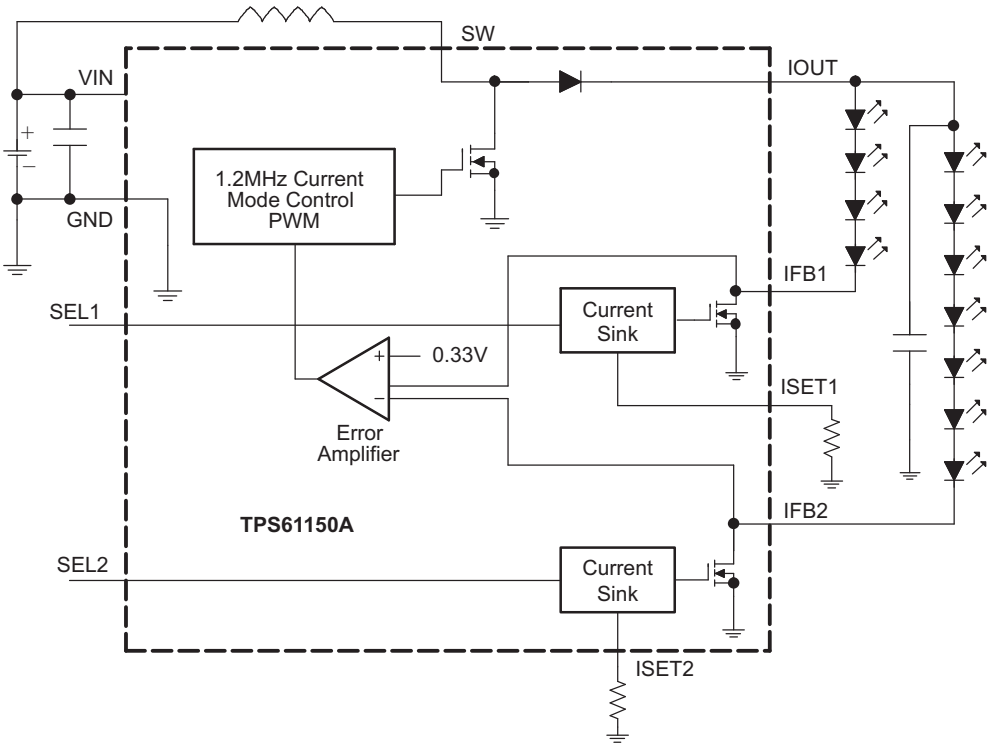
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VIN	5	I	Input pin. VIN provides the current to the boost power stage, and also powers the IC circuit. When VIN is below the undervoltage lockout threshold, the IC turns off and disables outputs; thereby disconnecting the WLEDs from the input.
GND	8	O	Ground. Connect the input and output capacitors as close as possible to this pin.
SW	6	I	Switching node of the IC.
IOUT	7	O	Constant current supply output. IOUT is directly connected to the boost converter output.
IFB1, IFB2	10	I	Return path for the IOUT regulation. The current regulator is connected to this pin, and it can be disabled to open the current path.
ISET1, ISET2	2 9	I	Output current programming. The resistor connected to the pin programs the corresponding output current.
SEL1, SEL2	3 4	I	Mode selection. See Table 1 for details.
Thermal Pad			The thermal pad should be soldered to the analog ground. If possible, use the thermal pad to connect to ground plane for ideal power dissipation.

Table 1. TPS61150A Mode Selection

SEL1	SEL2	IFB1	IFB2
H	L	Enable	Disable
L	H	Disable	Enable
H	H	Enable	Enable
L	L	IC Shutdown	

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

	VALUE	UNIT
Supply voltages on pin VIN(2)	–0.3 to 7	V
Voltages on pins SEL1/2, ISET1/2(2)	–0.3 to 7	V
Voltage on pin IOUT, SW, IFB1 and IFB2(2)	30	V
Continuous power dissipation	See Dissipation Rating Table	
Operating junction temperature range	–40 to 150	°C
Storage temperature range	–65 to 150	°C
Lead Temperature (soldering, 10 sec)	260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	$T_A \leq 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
QFN (1)	270°C/W	370mW	204mW	148mW
QFN(2)(2	48.7°C/W	2.05W	1.13W	821mW

(1) Soldered PowerPAD on a standard 2-layer PCB without vias for thermal pad.
(2) Soldered PowerPAD on a standard 4-layer PCB with vias for thermal pad .

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	2.5		6.0	V
V_O	Output voltage range	VIN		27	V
L	Inductor(1)		10		µH
C_I	Input capacitor(1)	1			µF
C_O	Output capacitor(1)	1			µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) See *Application Section* for further information.

ELECTRICAL CHARACTERISTICS

VIN = 3.6V, SELx = VIN, Rset = 80kΩ, $V_{(IOUT)}$ = 15V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range		2.5		6.0	V
I_Q	Operating quiescent current into VIN	Device PWM switching no load			2	mA
I_{SD}	Shutdown current	SELx = GND, T_A = 25°C		1.7	1.9	µA
		SELx = GND		2.7	3	
V_{UVLO}	Under-voltage lockout threshold	VIN falling		1.65	1.8	V
V_{hys}	Under-voltage lockout hysterisis			70		mV
ENABLE AND SOFT START						
$V_{(selh)}$	SEL logic high voltage	V_I = 2.5V to 6V	1.2			V
$V_{(sell)}$	SEL logic low voltage	V_I = 2.5V to 6V			0.4	V
$R_{(en)}$	SEL pull down resistor		300	700		kΩ
$t_{(off)}$	SEL pulse width to disable	SELx high to low	40			ms
$I_{(ss)}$	IFB soft start current steps			16		
$t_{(ss)}$	Soft start time step	Measured as clock divider		64		
$t_{(ss_en)}$	Soft start enable time	Time between falling and rising of two adjacent SELx pulses	40			ms
CURRENT FEEDBACK						
$V_{(ISET)}$	ISET pin voltage		1.204	1.229	1.254	V
K_{ISET}	Current multipler, I_{fb1}/I_{set1} , I_{fb2}/I_{set2}	ISET current = 16.7µA	883	920	957	
		ISET current = 1.2µA	736	920	1104	
K_M	Current matching, $(2\times\lvert I_{fb1}-I_{fb2}\rvert)/(I_{fb1}+I_{fb2})$	ISET current = 16.7µA	0%		3%	
		ISET current = 1.2µA	0%		20%	
$V_{(IFB)}$	IFB regulation voltage		300	330	360	mV
$V_{hys(IFB_L)}$	IFB low threshold hysteresis			60		mV
$t_{I(sink)}$	Current sink settle time measured from SELx rising edge(1)				6	µs
I_{lkg}	IFB pin leakage current	IFB voltage = 25V			1	µA
POWER SWITCH AND DIODE						
$R_{DS(ON)}$	N-channel MOSFET on-resistance	V_{IN} = V_{GS} = 3.6V		0.6	0.9	Ω
$I_{lkg(N_NFET)}$	N-channel leakage current	V_{DS} = 25V			1	µA
$V_{(F)}$	Power diode forward voltage	Diode current = 0.7A		0.83	1.0	V
OC AND OVP						
I_L	N-Channel MOSFET current limit	Dual output, IOUT= 15V, Duty cycle = 76%	0.75	1.0	1.25	A
		Single output , IOUT= 15V, Duty cycle = 76%	0.40	0.55	0.7	
$I_{(IFB_MAX)}$	Current sink max output current	IFB current = 330mV	34			mA
V_{ovp}	Overvoltage threshold		27	28	29	V
V_{ovp_hys}	Overvoltage hysteresis			550		mV
PWM AND PFM CONTROL						
F_S	Oscillator frequency		1.0	1.2	1.5	MHz
D_{max}	Maximum duty cycle	Feedback voltage = 1.0V	89%	93%		
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
T_{hys}	Thermal shutdown threshold hysteresis			15		°C

(1) This specification determines the minimum on time required for PWM dimming for desirable linearity. The maximum PWM dimming frequency can be calculated from the minimum duty cycle required in the application.

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURES
Overcurrent Limit	VIN = 3.0V, 3.6V, and 4.2V, single and dual output	1,2
WLED efficiency	VIN = 3.3V, 3.6V and 4.2V, 3 WLED, WLED voltage = 11V	3
WLED efficiency	VIN = 3.3V, 3.6V and 4.2V, 4 WLED, WLED voltage = 15V	4
WLED efficiency	VIN = 3.3V, 3.6V and 4.2V, 5 WLED, WLED voltage = 19V	5
WLED efficiency	VIN = 3.3V, 3.6V and 4.2V, 6 WLED, WLED voltage = 23V	6
Both on efficiency	VIN = 3.3V, 3.6V and 4.2V, 4 WLED on each output	7
K value over current	VIN = 3.6V, I_{WLED} = 1mA to 25mA	8
PWM dimming linearity	Frequency = 20kHz and 30kHz	9
Single output PWM dimming waveform		10
Multiplexed PWM dimming waveform		11
Start up waveform		12

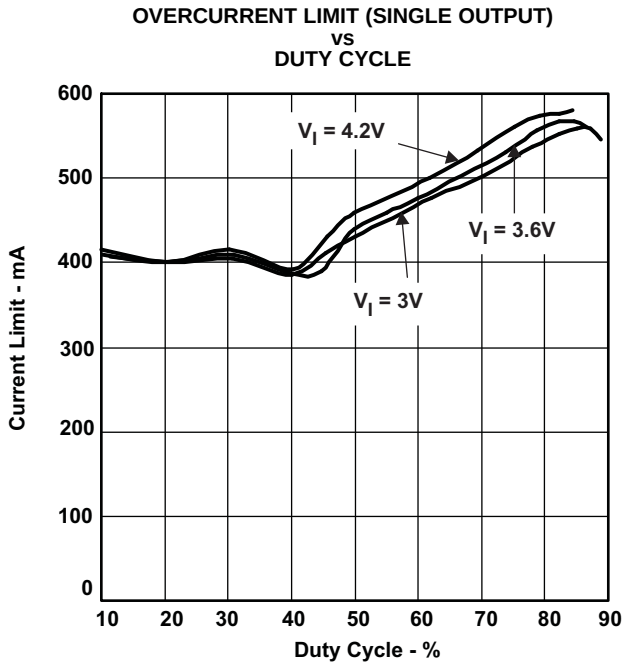


Figure 1.

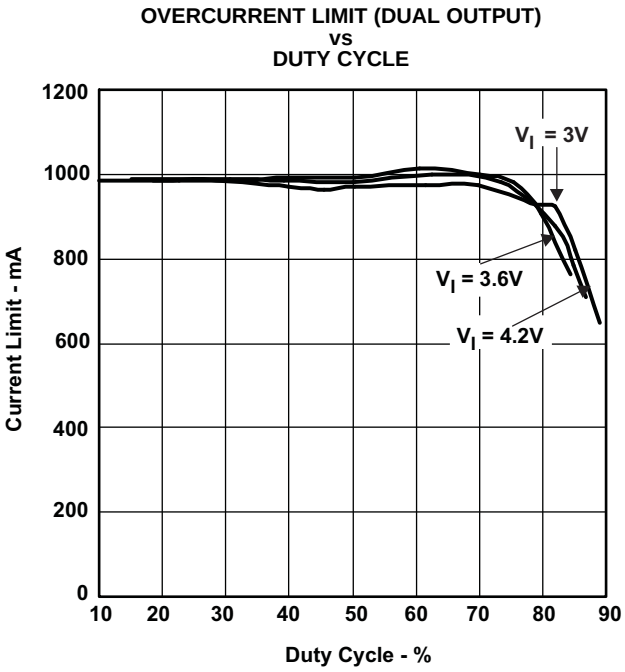


Figure 2.

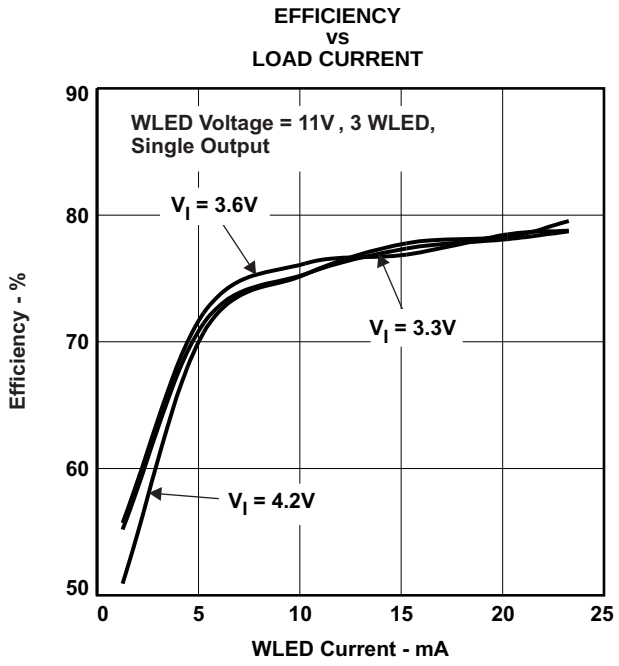


Figure 3.

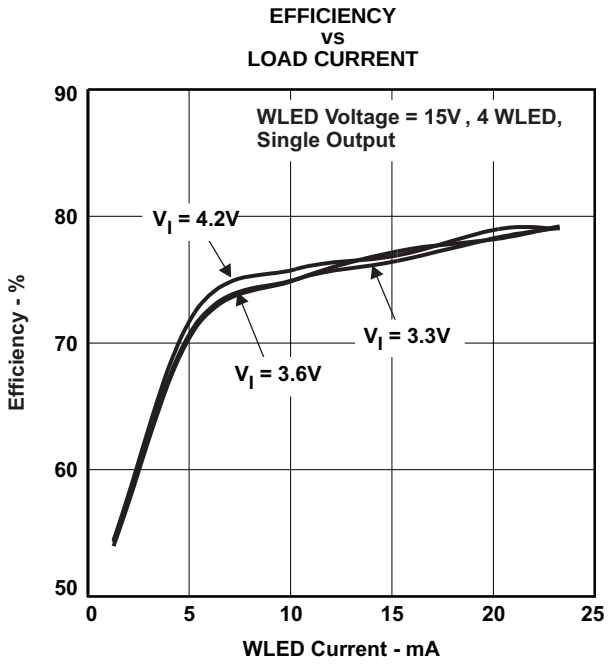


Figure 4.

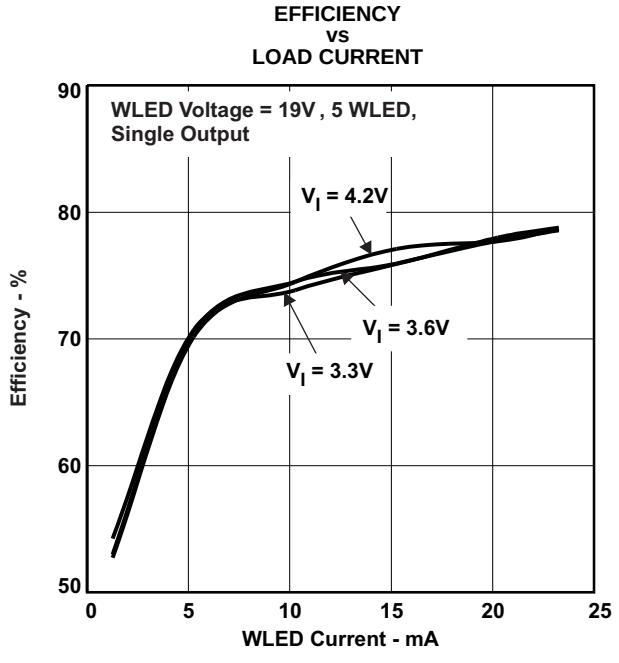


Figure 5.

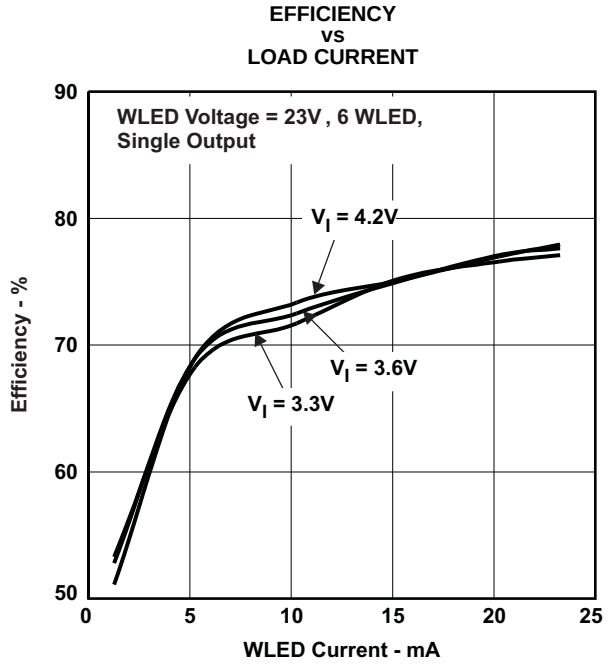


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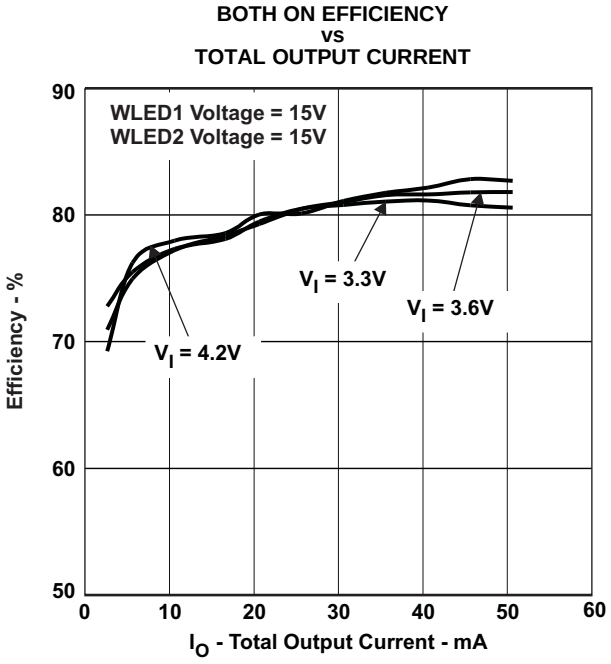


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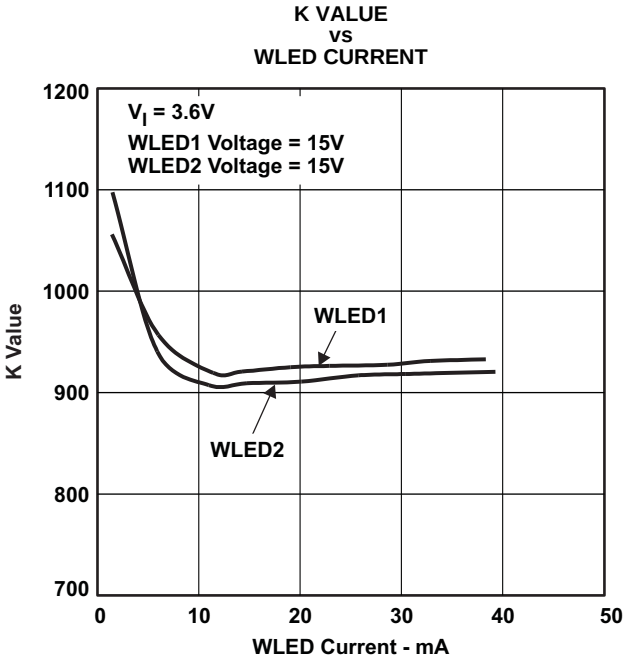


Figure 8.

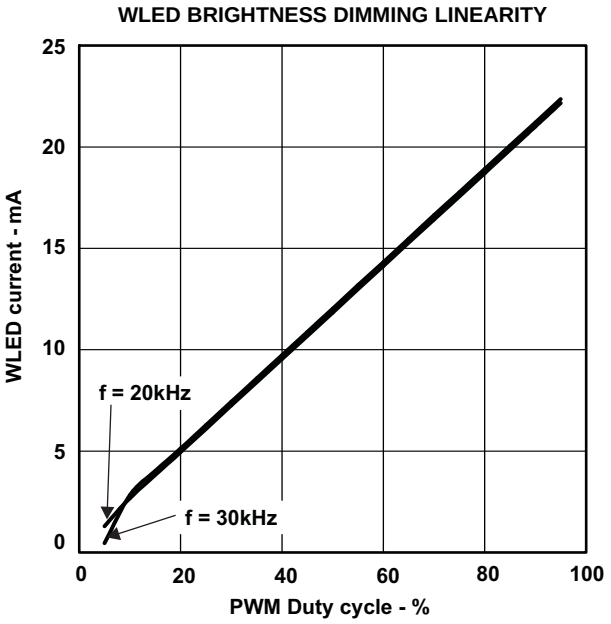


Figure 9.

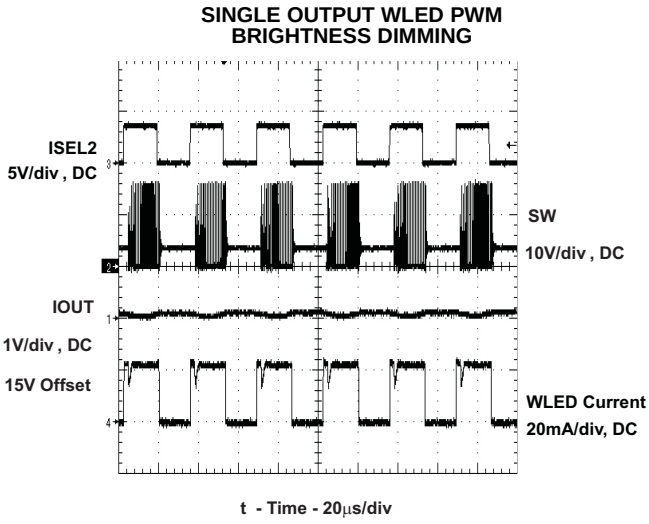


Figure 10.

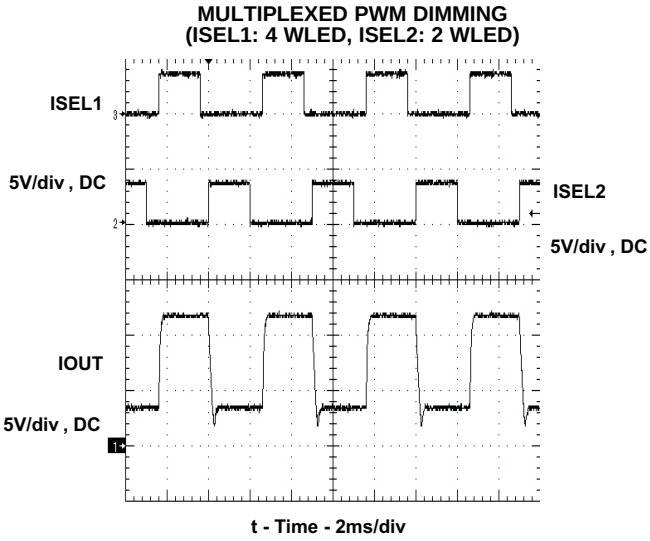


Figure 11.

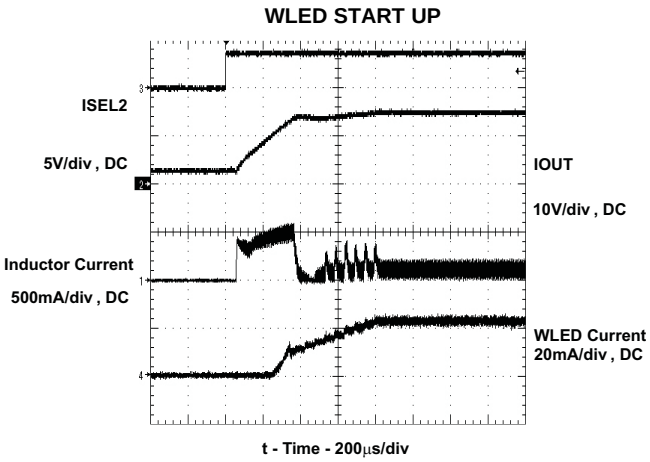


Figure 12.

DETAILED DESCRIPTION

CURRENT REGULATION

The TPS61150A uses a single boost regulator to drive 2 WLED strings whose current can be programmed independently. The boost converter adopts PWM control which is ideal for high output current and low output ripple noises. The feedback loop regulates the IFB pin to a threshold voltage (330mV typical), giving the current sink circuit just enough headroom to operate.

The regulation current is set by the resistor on the Iset pin based on

$$I_O = \frac{V_{ISET}}{R_{SET}} \times K_{ISET} \quad (1)$$

where

I_O = output current

V_{ISET} = Iset pin voltage (1.229V typical)

R_{SET} = Iset pin resistor value

K_{ISET} = current multiplier (920 typical)

When both outputs are enabled, the boost converter regulates to the IFB pin that demands higher Iout pin voltage, $V_{(IOUT)}$, and let the other IFB pin rise above its regulation voltage. The feedback path dynamically switches to the other IFB pin if its voltage drops more than the IFB low hysterisis (60mV typical) below it's regulation voltage. This ensures proper current regulation for both outputs. When both IFB voltages are low, IFB1 is used for regulation. Once IFB1 reaches its regulation voltage, the feedback path may hand over to IFB2 if it is still low, and the boost output will continue to rise.

The overall efficiency in this mode depends on the voltage different between the IFB1 and IFB2. A large difference reduces the efficiency due to power losses across the current sink circuit. To improve the efficiency of the both-on mode, the two current outputs can be turned on complimentarily by applying out of phase enable signal to the SEL pins. The ISET pin resistors need to be recalculated to compensate for the reduced DC current.

START UP

During start up, both the boost converter and the current sink circuitry are trying to establish steady state simultaneously. The current sink circuitry ramps up current in 16 steps, with each step taking 64 clock cycles. This ensures that the current sink loop is slower than the boost converter response during startup. Therefore, the boost converter output comes up slowly as current sink circuitry ramps up the current. This ensures smooth start up and minimizes in-rush current.

OVERVOLTAGE PROTECTION

To prevent the boost output run away as the result of WLED disconnection, there is an overvoltage protection circuit which stops the boost converter from switching as soon as its output exceeds the OVP threshold. When the voltage falls below the OVP threshold, the converter resumes switching. TPS61150A provides 28V(typical) OVP to prevent a 25V rated output capacitor or the internal 30V FET from breaking down.

UNDERVOLTAGE LOCKOUT

An undervoltage lockout prevents mis-operation of the device for input voltages below 1.65V (typical). When the input voltage is below the undervoltage threshold, the device remains off and both the boost converter and current sink circuit are turned off, providing isolation between input and output.

THERMAL SHUTDOWN

An internal thermal shutdown turns off the IC when the typical junction temperature of 160°C is exceeded. The thermal shutdown has a hysteresis of typically 15°C.

DETAILED DESCRIPTION (continued)

ENABLE

Pulling either the SEL1 or SEL2 pin low turns off the corresponding output. If both SEL1 and SEL2 are low for more than 40ms, the IC shuts down and consumes less than 2μA (room temperature) current. The SEL pin can also be used for PWM brightness dimming. To improve PWM dimming linearity, soft start is disabled if the time between falling and rising edges of two adjacent SELx pulses is less than 40ms. See *APPLICATION INFORMATION* for details.

Each SEL input pin has an internal pull down resistor to disable the device when the pin is floating.

APPLICATION INFORMATION

MAXIMUM OUTPUT CURRENT

The over-current limit in a boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit, input voltage, output voltage and efficiency can all change maximum current output. Since current limit clamps peak inductor current, ripple has to be subtracted to derive maximum DC current. The ripple current is a function of switching frequency, inductor value and duty cycle. The following equations take into account of all the above factors for maximum output current calculation.

$$I_p = \frac{1}{\left[L \times \left(\frac{1}{Viout + Vf - Vin} + \frac{1}{Vin}\right) \times Fs\right]} \quad (2)$$

where

Ip = inductor peak-to-peak ripple

L = inductor value

Vf = power diode forward voltage

Fs = switching frequency

Viout = boost output voltage. It is equal to 330mV + voltage drop across WLED.

$$Iout_max = \frac{Vin \times \left(Ilim - \frac{I_p}{2}\right) \times \eta}{Viout} \quad (3)$$

where

Iout_max = maximum output current of the boost converter

Ilim = overcurrent limit

η = efficiency

To keep a tight range of the overcurrent limit, The TPS61150A uses the Vin and Iout pin voltage to compensate for the overcurrent limit variation caused by the slope compensation. However, the current threshold still has residual dependency on the VIN and IOUT voltage. Use Figure 1 and Figure 2 to identify the typical overcurrent limit in your application, and use ±25% tolerance to account for temperature dependency and process variations.

The maximum output current can also be limited by the current capability of the current sink circuitry. It is designed to provide maximum 35mA current regardless of the current capability of the boost converter.

WLED BRIGHTNESS DIMMING

There are three ways to change the output current *on the fly* for WLED dimming. The first method parallels an additional resistor with the ISET pin resistor as shown in Figure 13 . The switch (Q1) can change the ISET pin resistance and therefore, modify the output current. This method is very simple, but can only provide limited dimming steps.

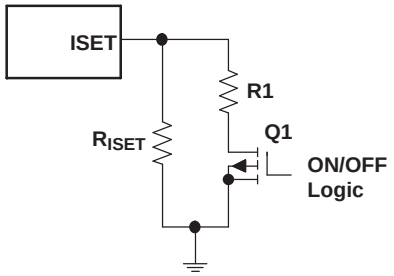


Figure 13. Switching In/Out an Additional Resistor to Change Output Current

APPLICATION INFORMATION (continued)

Alternatively, a PWM dimming signal at the SEL pin can modulate the output current by the duty cycle of the signal. The logic high of the signal turns on the current sink circuit, while the logic low turns it off. This operation creates an averaged DC output current proportional to the duty cycle of the PWM signal. The frequency of the PWM signal has to be high enough to avoid flashing of the WLEDs. The soft start of the current sink circuit is disabled during the PWM dimming to improve linearity.

The major concern of the PWM dimming is the creation of audible noises which can come from the inductor and/or output capacitor of the boost converter. The audible noises on the output capacitor are created by the presence of voltage ripple in range of audible frequencies. The TPS61150A alleviates the problem by disconnecting the WLEDs from the output capacitor when the SEL pin is low. Therefore, the output capacitor is not discharged by the WLEDs, which reduces the voltage ripple during PWM dimming.

The audible noises can be eliminated by using PWM dimming frequency above or below the audible frequency range. The maximum PWM dimming frequency of the TPS61150A is determined by the current settling time (t_{isink}) which is the time required for the circuit sink circuit to reach steady state after the SEL pin transitions from low to high. The maximum dimming frequency can be calculated by

$$F_{PWM_MAX} = \frac{D_{min}}{T_{isink}} \quad (4)$$

D_{min} = min duty cycle of the PWM dimming required in the application.

For 20% D_{min}, PWM dimming frequency up to 33kHz is possible, making the noise frequency above the audible range.

The third method uses an external DC voltage and resistor as shown in Figure 14 to change the ISET pin current, and thus control the output current. The DC voltage can be the output of a filtered PWM signal. The equation to calculate the output current is

$$I_{WLED} = K_{ISET} \times \left(\frac{1.229}{R_{ISET}} + \frac{1.229 - V_{DC}}{R_1} \right) \text{ for DC voltage input} \quad (5)$$

$$I_{WLED} = K_{ISET} \times \left(\frac{1.229}{R_{ISET}} + \frac{1.229 - V_{DC}}{R_1 + 10K} \right) \text{ for PWM signal input} \quad (6)$$

K_{ISET} = current multiplier between the ISET pin current and the IFB pin current.

VDC= voltage of the DC voltage source or the DC voltage of the PWM signal.



Figure 14. Analog Dimming Uses an External Voltage Source to Control the Output Current

INDUCTOR SELECTION

Because the selection of the inductor affects power supplies steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three specifications most important to the performance of the inductor, inductor value, DC resistance, and saturation current. Considering inductor value alone is not enough.

The inductors inductance value determines the inductor ripple current. It is generally recommended to set peak-to-peak ripple current given by Equation 2 to 30–40% of DC current. It is a good compromise of power losses and inductor size. For this reason, 10µH inductors are recommended for TPS61150A. Inductor DC current can be calculated as

APPLICATION INFORMATION (continued)

$$I_{L_DC} = \frac{V_{iout} \times I_{out}}{V_{in} \times \eta} \quad (7)$$

Use the maximum load current and minimum V_I for calculation.

The internal loop compensation for PWM control is optimized for the external component shown in the typical application circuit with consideration of component tolerance. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20 to 35% from the 0A value depending on how the inductor vendor defines saturation. Using an inductor with a smaller inductance value forces discontinuous PWM in which inductor current ramps down to zero before the end of each switching cycle. It reduces the boost converter's maximum output current, and causes large input voltage ripple. An inductor with larger inductance reduces the gain and phase margin of the feedback loop, possibly resulting in instability

Regulator efficiency is dependent on the resistance of its high current path and switching losses associated with the PWM switch and power diode. Although the TPS61150A has optimized the internal switches, the overall efficiency still relies on inductors DC resistance (DCR); Lower DCR improves efficiency. However, there is a trade off between DCR and inductor size, and shielded inductors typically have higher DCR than unshielded ones. DCR in range of 150mΩ to 350mΩ is suitable for applications requiring both on mode. DCR is the range of 250mΩ to 450mΩ is a good choice for single output application. Table 2 and Table 3 list recommended inductor models.

Table 2. Recommended Inductors for Single Output

	L (µH)	DCR Typ (mΩ)	Isat (A)	SIZE (L×W×H mm)
TDK				
VLF3012AT-100MR49	10	360	0.49	2.8×3.0×1.2
VLCF4018T-100MR74-2	10	163	0.74	4.0×4.0×1.8
Sumida				
CDRH2D11/HP	10	447	0.52	3.2×3.2×1.2
CDRH3D16/HP	10	230	0.84	4.0×4.0×1.8

Table 3. Recommended Inductors for Dual Output

	L (µH)	DCR Typ (mΩ)	Isat (A)	SIZE (L×W×H mm)
TDK				
VLCF4018T-100MR74-2	10	163	0.74	4.0×4.0×1.8
VLF4012AT-100MR79	10	300	0.85	3.5×3.7×1.2
Sumida				
CDRH3D16/HP	10	230	0.84	4.0×4.0×1.8
CDRH4D11/HP	10	340	0.85	4.8×4.8×1.2

INPUT AND OUTPUT CAPACITOR SELECTION

The output capacitor is mainly selected for the output ripple of the converter. This ripple voltage is the sum of the ripple caused by the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by

$$C_{out} = \frac{\left(V_{iout} - V_{in}\right) I_{out}}{V_{iout} \times Fs \times V_{ripple}} \quad (8)$$

V_{ripple} = Peak-to-peak output ripple.

For V_I = 3.6V, V_{iout} = 20V, and F_s = 1.2MHz, 0.1% ripple (20mV) would require 1.0µF capacitor. For this value, ceramic capacitors are the best choice for its size, cost and availability.

The additional output ripple component caused by ESR is calculated using:

$$V_{ripple_ESR} = I_{out} \times R_{ESR}$$

Due to it's low ESR, V_{ripple_ESR} can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

During a load transient, the capacitor at the output of the boost converter has to supply or absorb additional current before the inductor current ramps up the steady state value. Larger capacitors always help to reduce the voltage over and under shoot during a load transient. A larger capacitor also helps loop stability.

Care must be taken when evaluating a ceramic capacitor's derating due to applied dc voltage, aging and frequency response. For example, larger form factor capacitors (in 1206 size) have their self-resonant frequencies in the range of TPS61150A's switching frequency, so the effective capacitance is significantly lower. Therefore, it may be necessary to use small capacitors in parallel instead of one large capacitor.

The popular vendors for high value ceramic capacitors are:

TDK (http://www.component.tdk.com/components.php)

Murata (http://www.murata.com/cap/index.html)

Table 4. Recommended Input and Output Capacitors

	Capacitance (µF)	Voltage (V)	Case
TDK			
C3216X5R1E475K	4.7	25	1206
C2012X5R1E105K	1	25	805
C1005X5R0J105K	1	6.3	402
Murata			
GRM319R61E475KA12D	4.7	25	1206
GRM216R61E105KA12D	1	25	805
GRM155R60J105KE19D	1	6.3	402

LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems, therefore, use wide and short traces for high current paths. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce the input ripple seen by the IC. The VIN and SW pins are conveniently located on the edges of the IC, therefore the inductor can be placed close to the IC. The output capacitor needs to be placed near the load to minimize ripple and maximize transient performance.

It is also beneficial to have the ground of the output capacitor close to the GND pin since there will be large ground return current flowing between them. When laying out signal ground, it is recommended to use short traces separated from power ground traces, and connect them together at a single point.

ADDITIONAL APPLICATION CIRCUIT

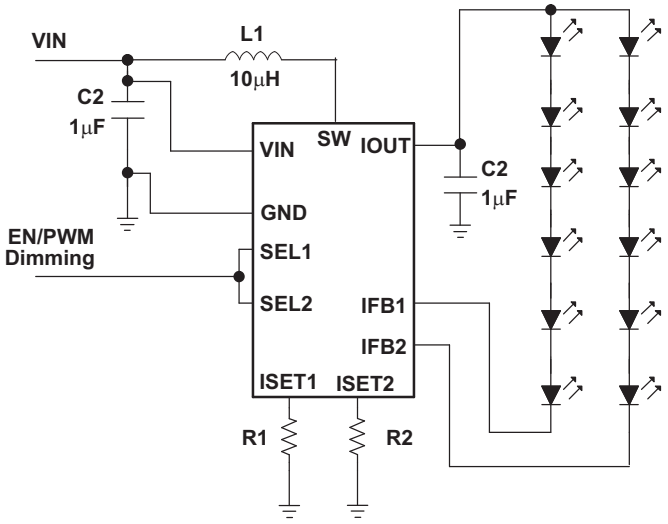


Figure 15. Driving Up to 12 WLEDs With One LCD Backlight

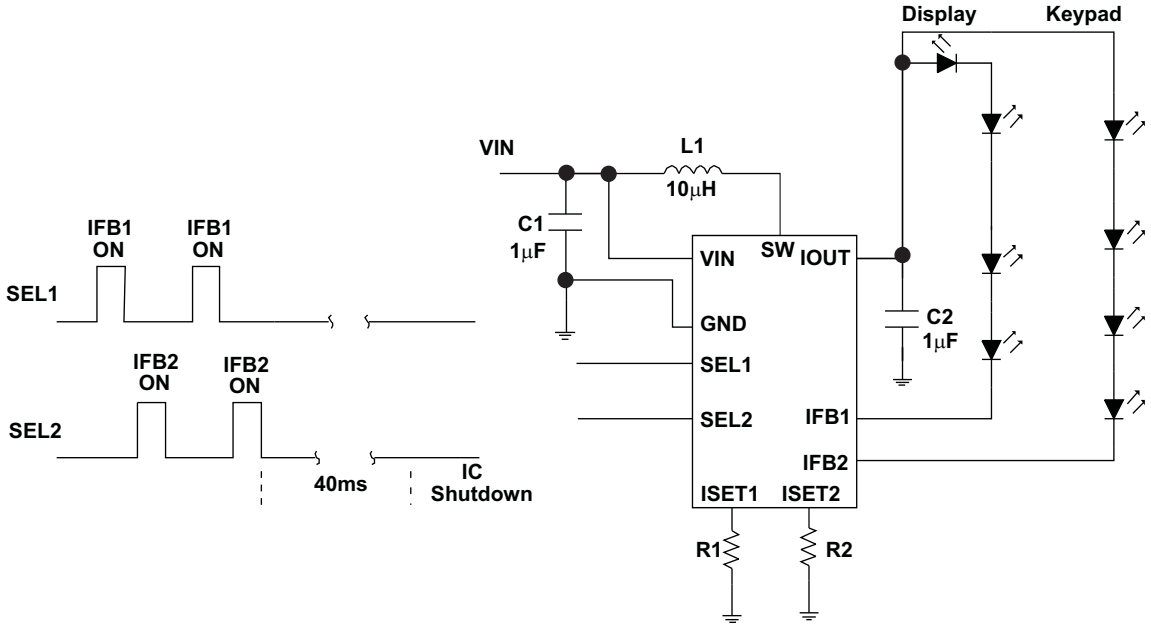


Figure 16. Driving a Keypad and LCD Backlight by applying interleaved PWM signal to the SEL1 and SEL2 pins. The duty cycle of the PWM signal controls brightness dimming

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61150ADRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BTK	Samples
TPS61150ADRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BTK	Samples
TPS61150ADRCTG4	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BTK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

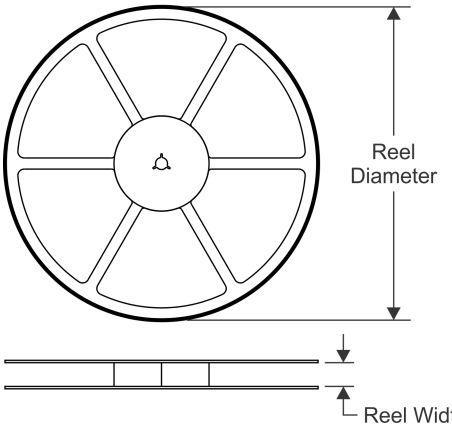
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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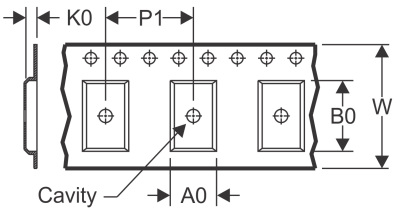
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

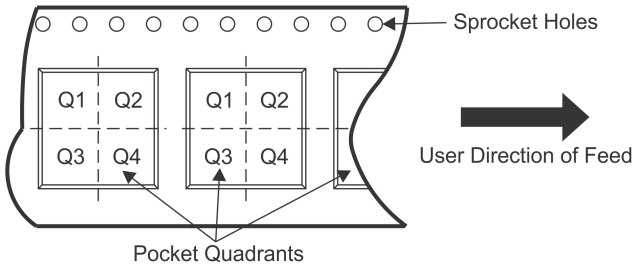


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

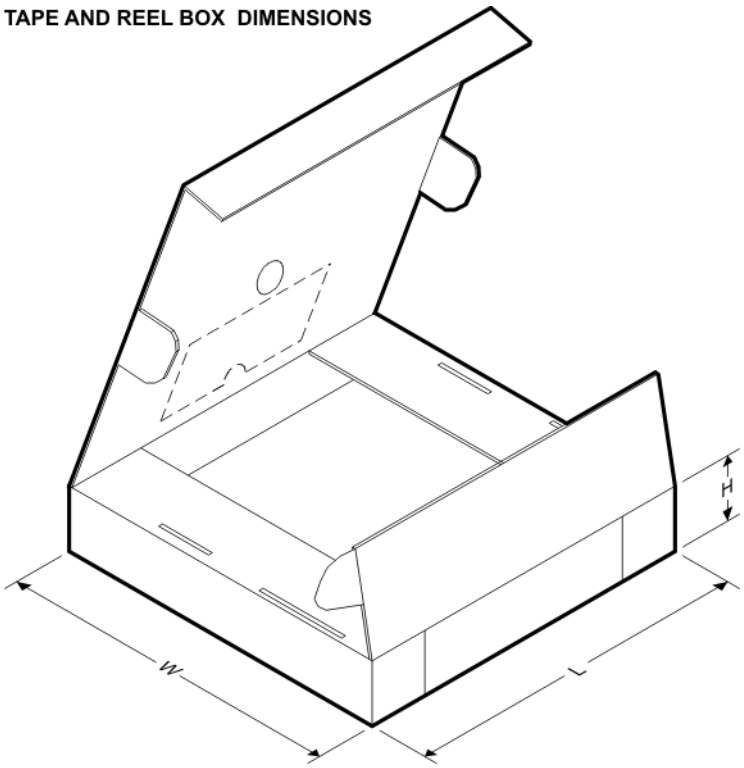
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61150ADRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61150ADRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61150ADRCR	VSON	DRC	10	3000	853.0	449.0	35.0
TPS61150ADRCT	VSON	DRC	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

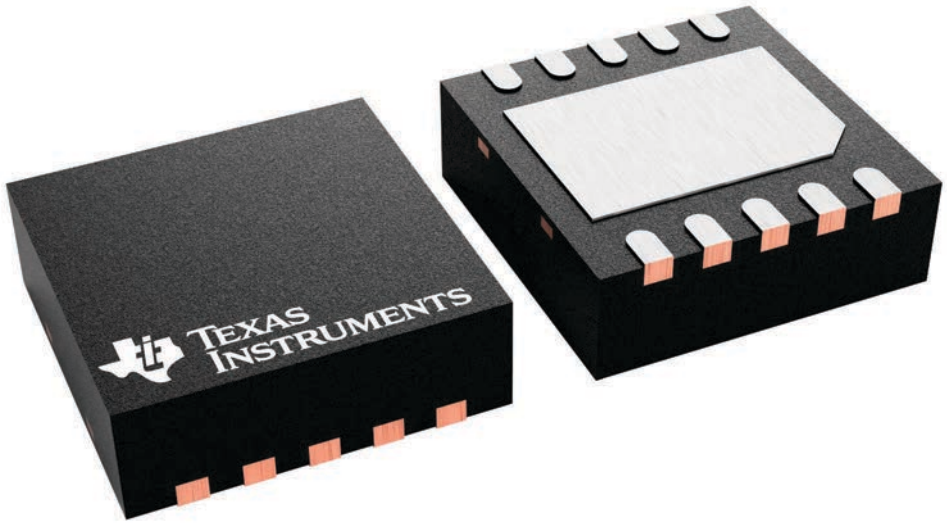
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



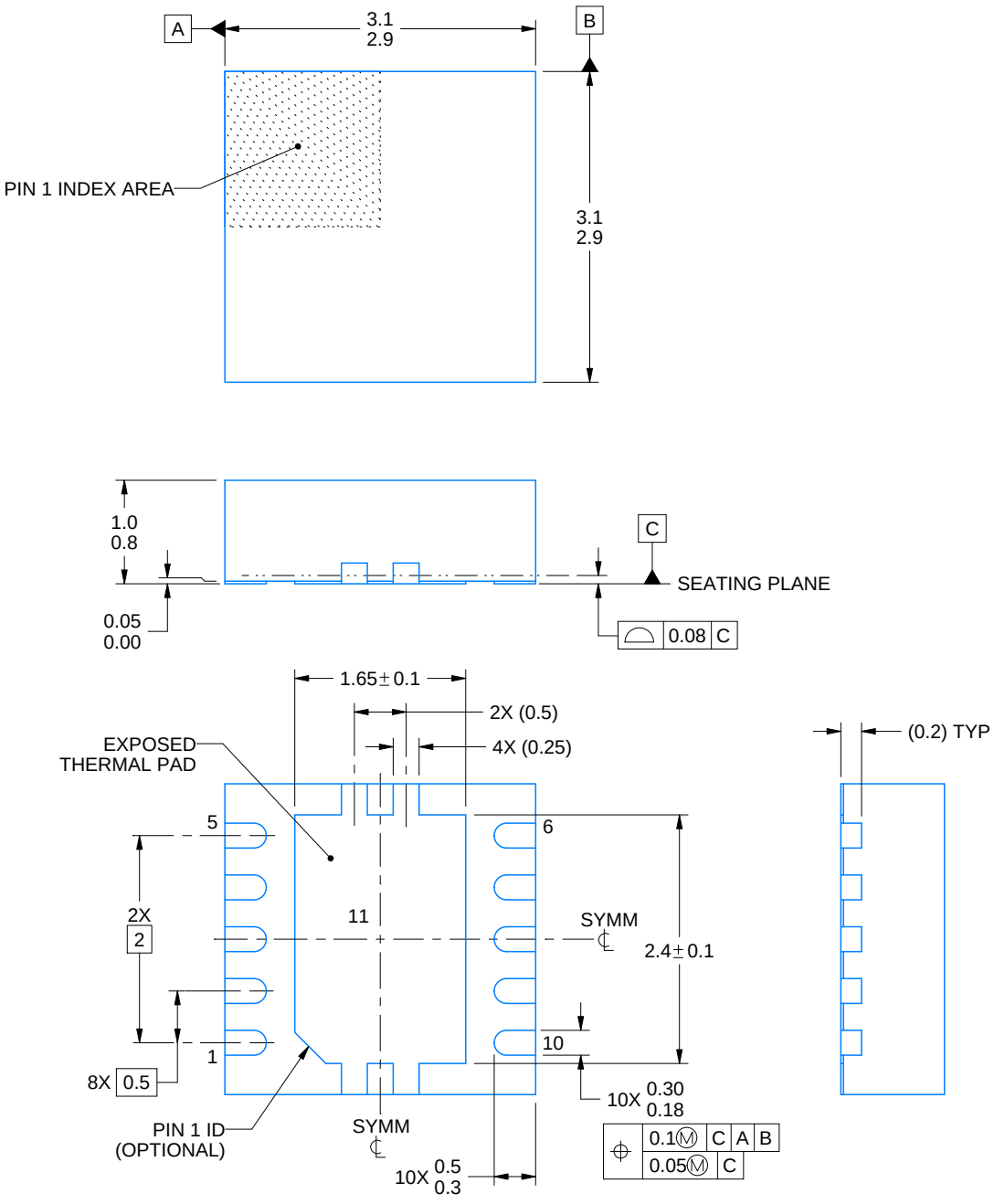
4226193/A

DRC0010J

PACKAGE OUTLINE

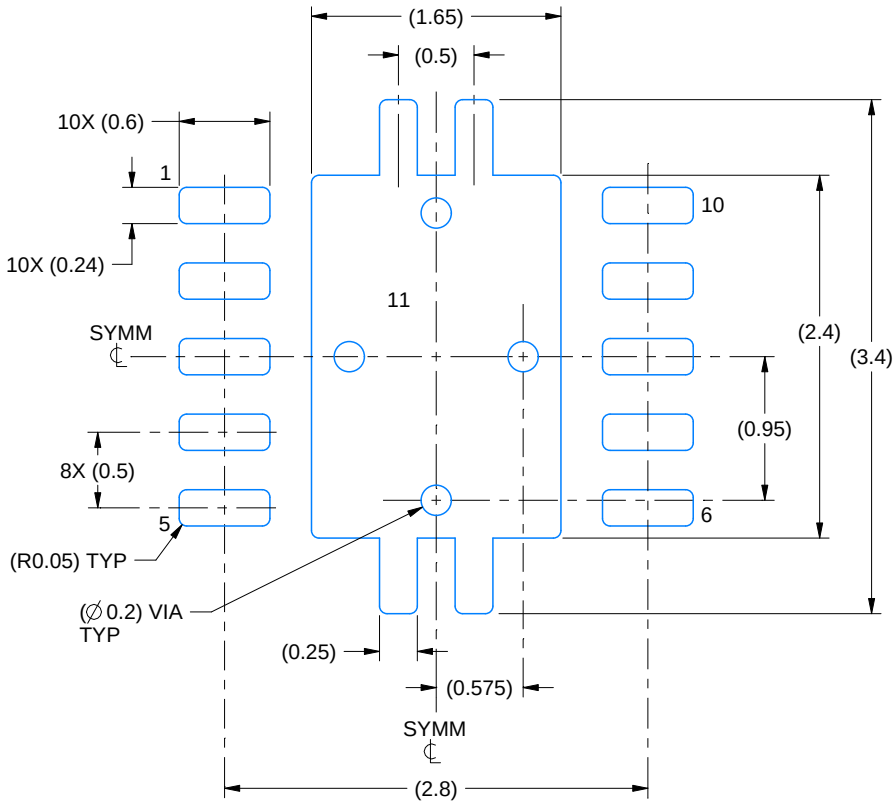
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

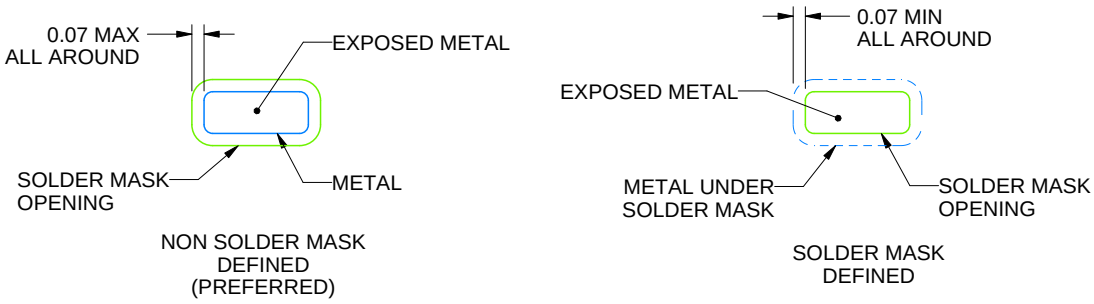


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

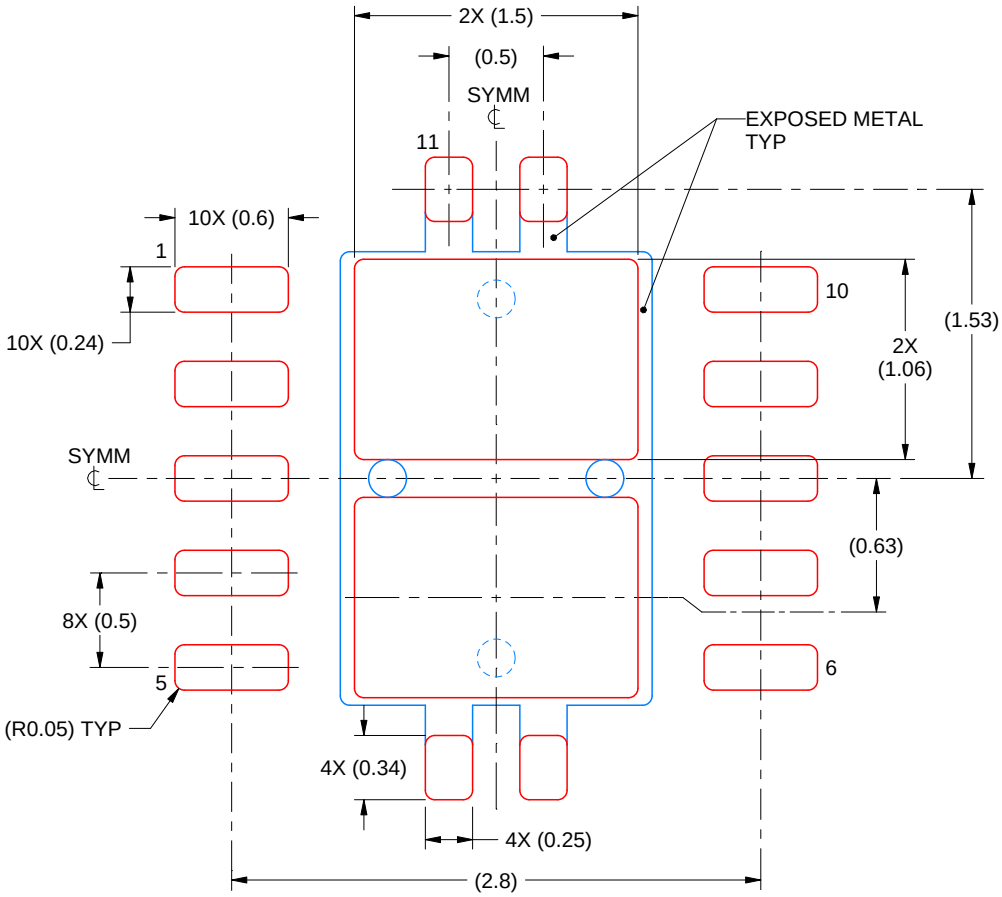
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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