

SN54LVTZ244, SN74LVTZ244 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS302C – SEPTEMBER 1993 – REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

description

These octal buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation with the capability to provide a TTL interface to a 5-V system environment.

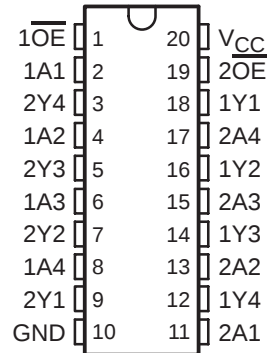
These devices are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

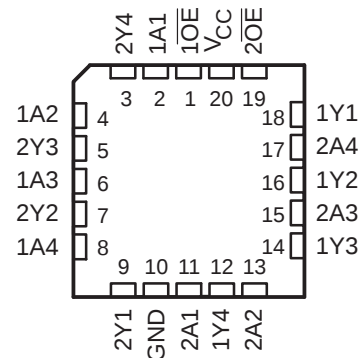
The SN74LVTZ244 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVTZ244 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTZ244 is characterized for operation from -40°C to 85°C .

SN54LVTZ244 . . . J PACKAGE
SN74LVTZ244 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTZ244 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

Copyright © 1995, Texas Instruments Incorporated

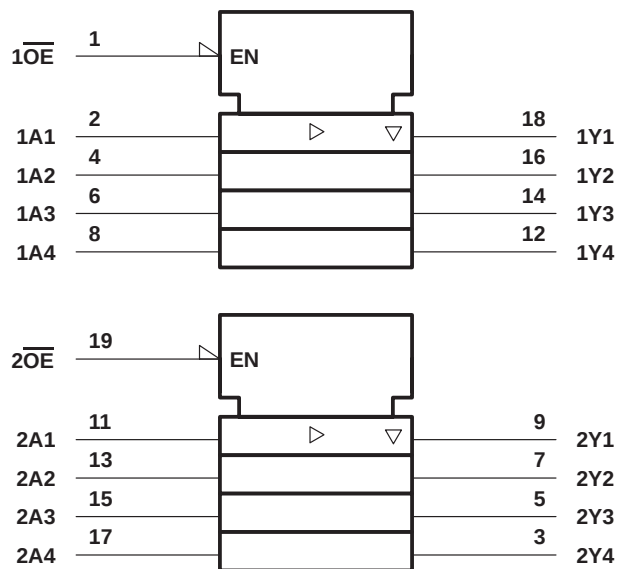
SN54LVTZ244, SN74LVTZ244

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

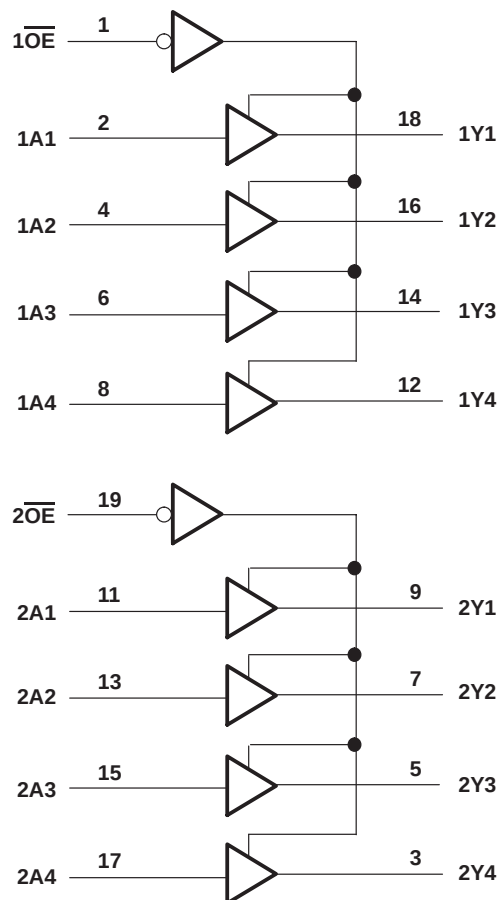
SCBS302C – SEPTEMBER 1993 – REVISED JULY 1995

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTZ244, SN74LVTZ244

3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS302C – SEPTEMBER 1993 – REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVTZ244	96 mA
SN74LVTZ244	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTZ244	48 mA
SN74LVTZ244	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Operating free-air temperature range, T_A : SN54LVTZ244	–55°C to 125°C
SN74LVTZ244	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

		SN54LVTZ244		SN74LVTZ244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

SN54LVTZ244, SN74LVTZ244

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCBS302C – SEPTEMBER 1993 – REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVTZ244			SN74LVTZ244			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$				-1.2			-1.2	V
V_{OH}	$V_{CC} = \text{MIN to MAX}^\ddagger$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4			2.4			
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2						
		$I_{OH} = -32\text{ mA}$				2			
V_{OL}	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$			0.2			0.2	V
		$I_{OL} = 24\text{ mA}$			0.5			0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$			0.4			0.4	
		$I_{OL} = 32\text{ mA}$			0.5			0.5	
		$I_{OL} = 48\text{ mA}$			0.55				
		$I_{OL} = 64\text{ mA}$						0.55	
I_I	$V_{CC} = 0\text{ or MAX}^\ddagger$, $V_I = 5.5\text{ V}$				10			10	μA
	$V_{CC} = 0\text{ to }3.6\text{ V}$	$V_I = V_{CC}\text{ or GND}$	Control inputs		± 1			± 1	
		$V_I = V_{CC}$			1			1	
		$V_I = 0$	Data inputs		-5			-5	
I_{off}	$V_{CC} = 0\text{ V}$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$							± 100	μA
$I_{OZPU}^\S$	$V_{CC} = 0\text{ V to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE} = X$							± 50	μA
$I_{OZPD}^\S$	$V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE} = X$							± 50	μA
$I_I(\text{hold})$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	A inputs		75	75			μA
		$V_I = 2\text{ V}$			-75	-75			
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$				5			5	μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$				-5			-5	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$, $I_O = 0$	Outputs high	0.12	0.5		0.12	0.225		mA
		Outputs low	8.6	15		8.6	15		
		Outputs disabled	0.12	0.5		0.12	0.225		
$\Delta I_{CC}^\P$	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.3			0.2		mA
C_i	$V_I = 3\text{ V or }0$			4			4		pF
C_O	$V_O = 3\text{ V or }0$			8			8		pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This parameter is specified by characterization.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

SN54LVTZ244, SN74LVTZ244

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCBS302C – SEPTEMBER 1993 – REVISED JULY 1995

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTZ244				SN74LVTZ244				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP [†]	MAX	MIN		MAX
t _{PLH}	A	Y	1	4.7		5.2	1	2.5	4.1		5	ns
t _{PHL}			1	4.4		5.4	1	2.5	4.1		5.2	
t _{PZH}	$\overline{\text{OE}}$	Y	1	5.4		6.5	1	2.7	5.2		6.3	ns
t _{PZL}			1.1	5.4		7.6	1.1	3.1	5.2		6.7	
t _{PHZ}	$\overline{\text{OE}}$	Y	1.9	6.2		6.9	1.9	3.9	5.6		6.3	ns
t _{PLZ}			1.8	5.5		6	1.8	3.2	5.1		5.6	

[†] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

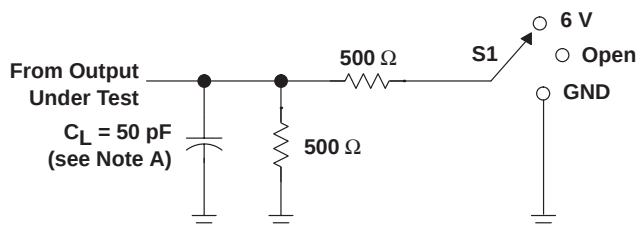
SN54LVTZ244, SN74LVTZ244

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

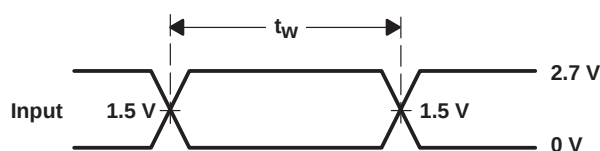
SCBS302C – SEPTEMBER 1993 – REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION

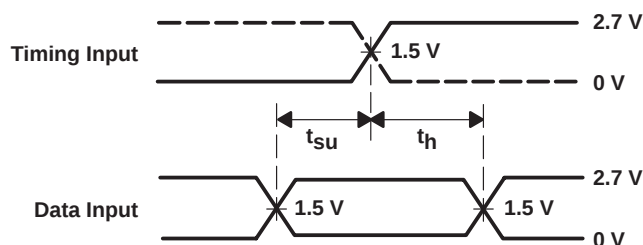


LOAD CIRCUIT FOR OUTPUTS

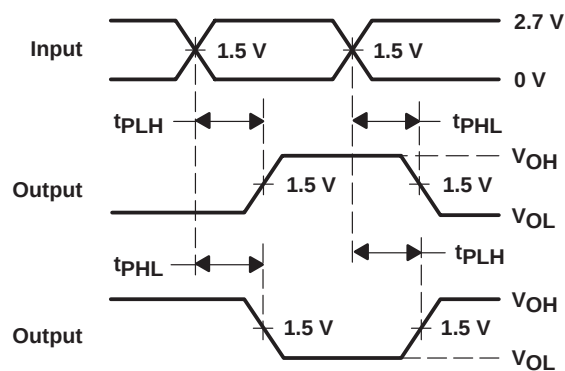
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



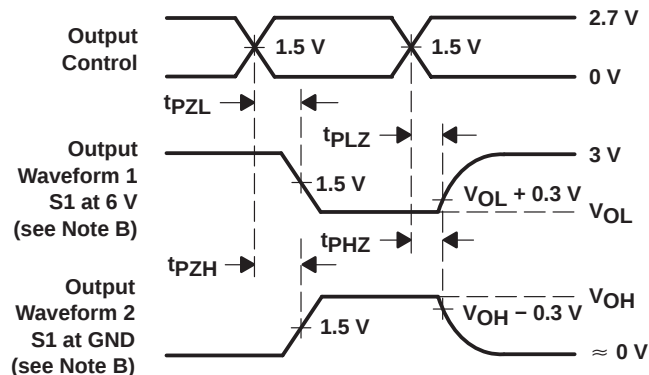
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVTZ244DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXZ244	Samples
SN74LVTZ244DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTZ244	Samples
SN74LVTZ244DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTZ244	Samples
SN74LVTZ244PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXZ244	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

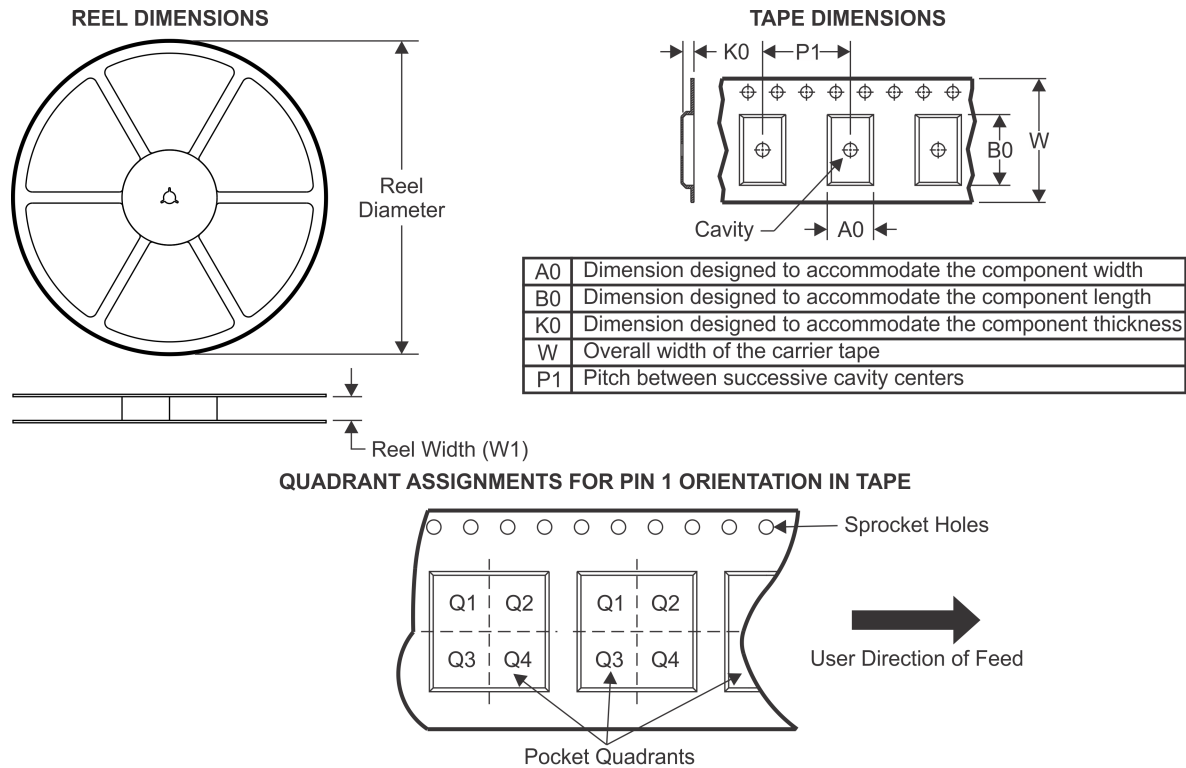
⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

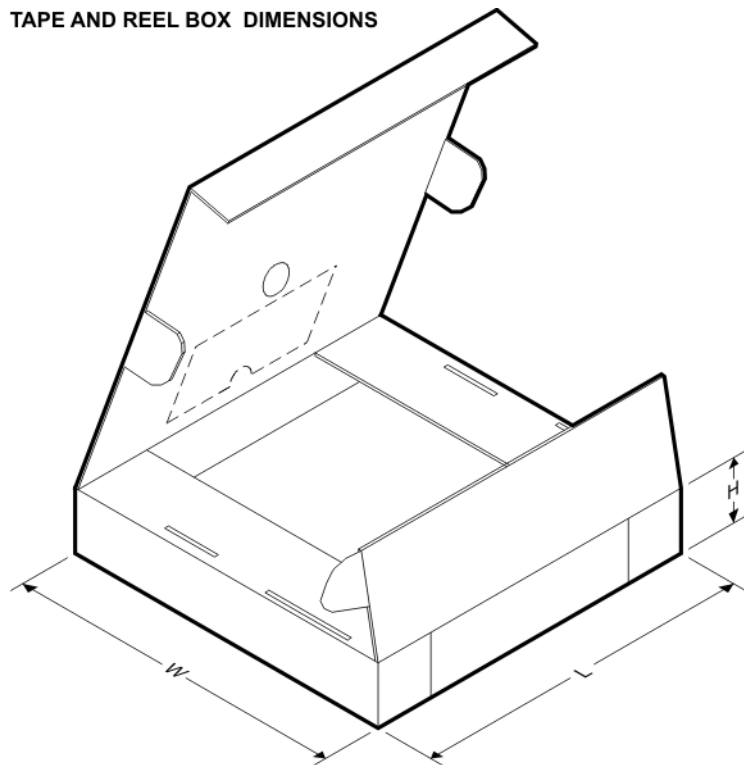
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTZ244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVTZ244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVTZ244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

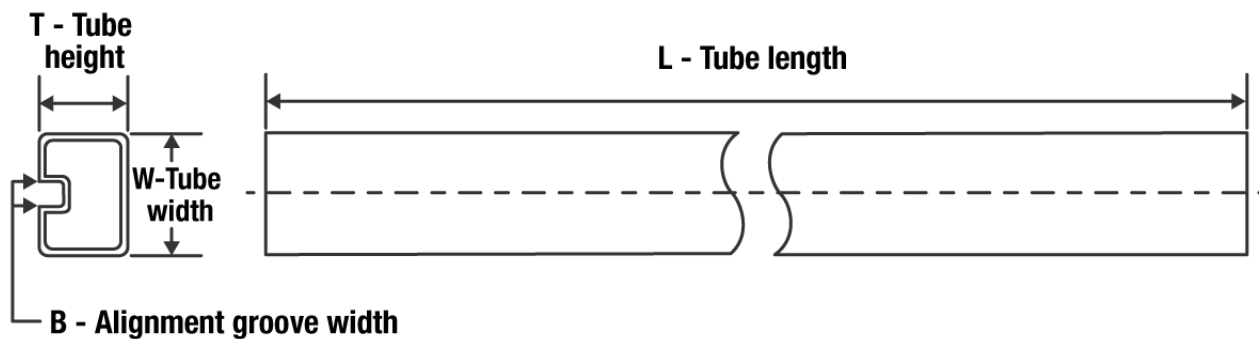
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

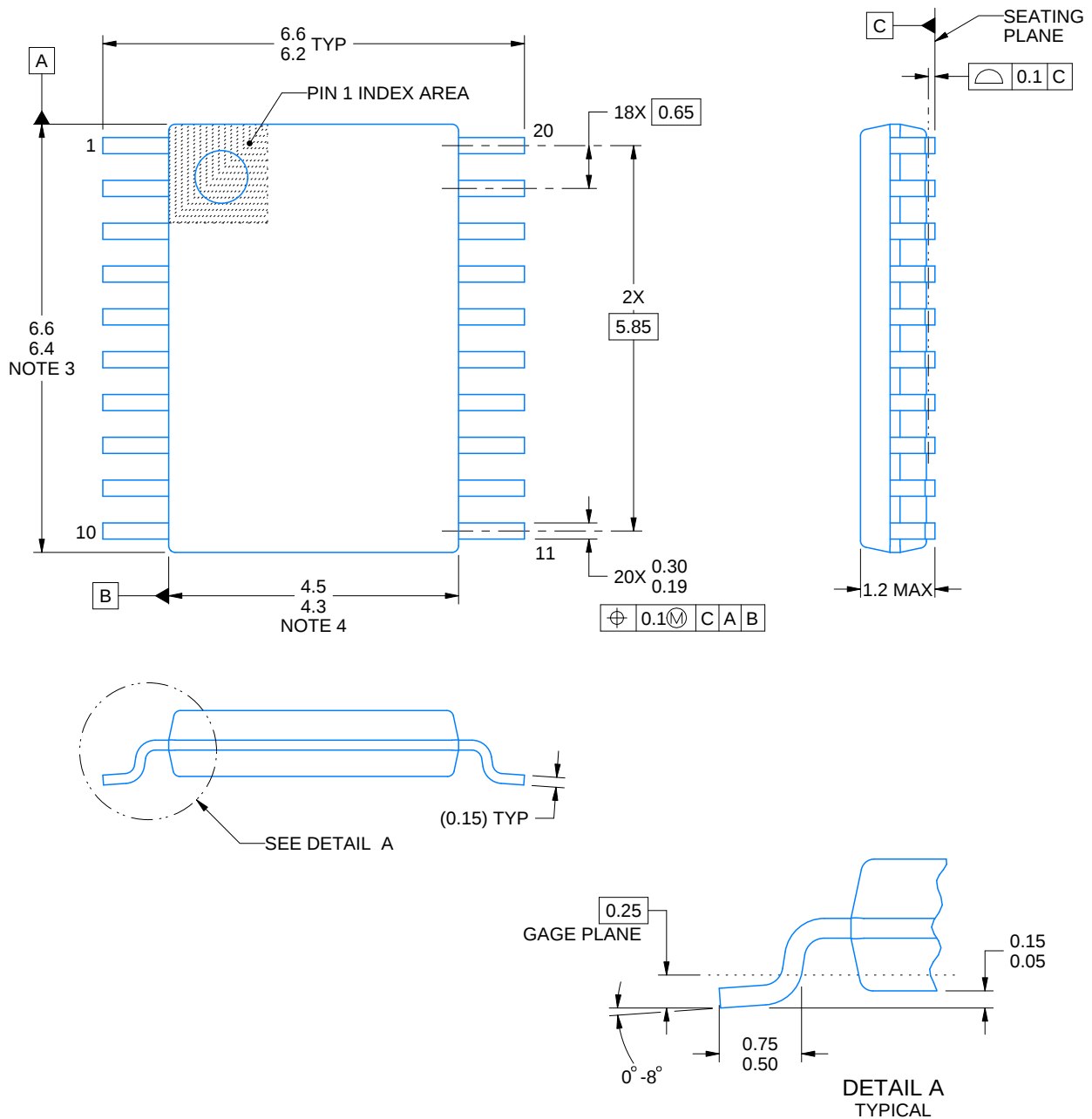
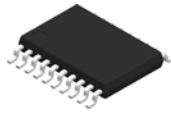
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTZ244DBR	SSOP	DB	20	2000	853.0	449.0	35.0
SN74LVTZ244DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVTZ244PWR	TSSOP	PW	20	2000	853.0	449.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVTZ244DW	DW	SOIC	20	25	507	12.83	5080	6.6



4220206/A 02/2017

NOTES:

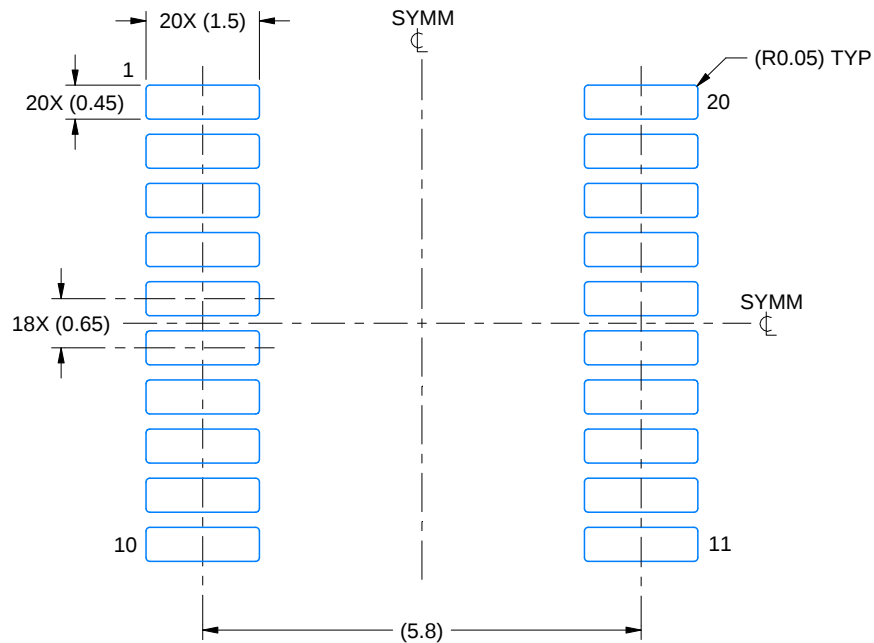
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

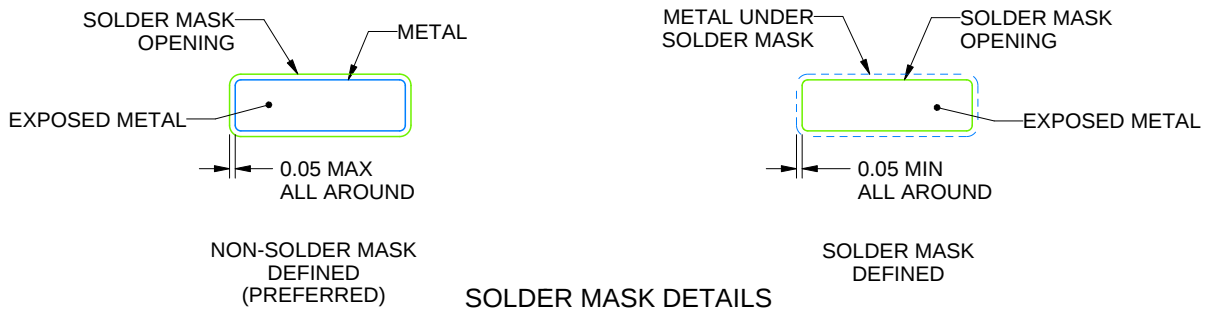
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

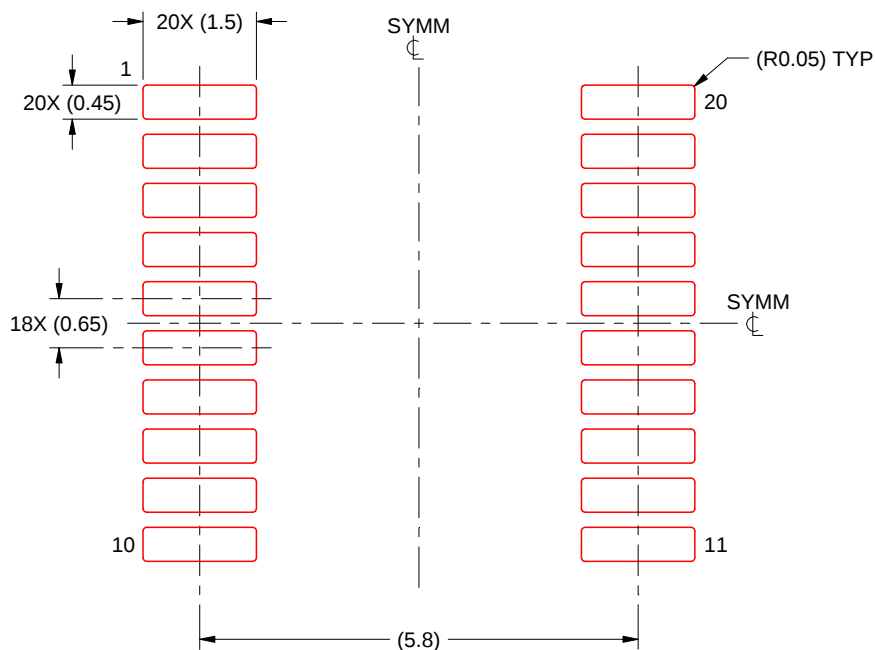
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

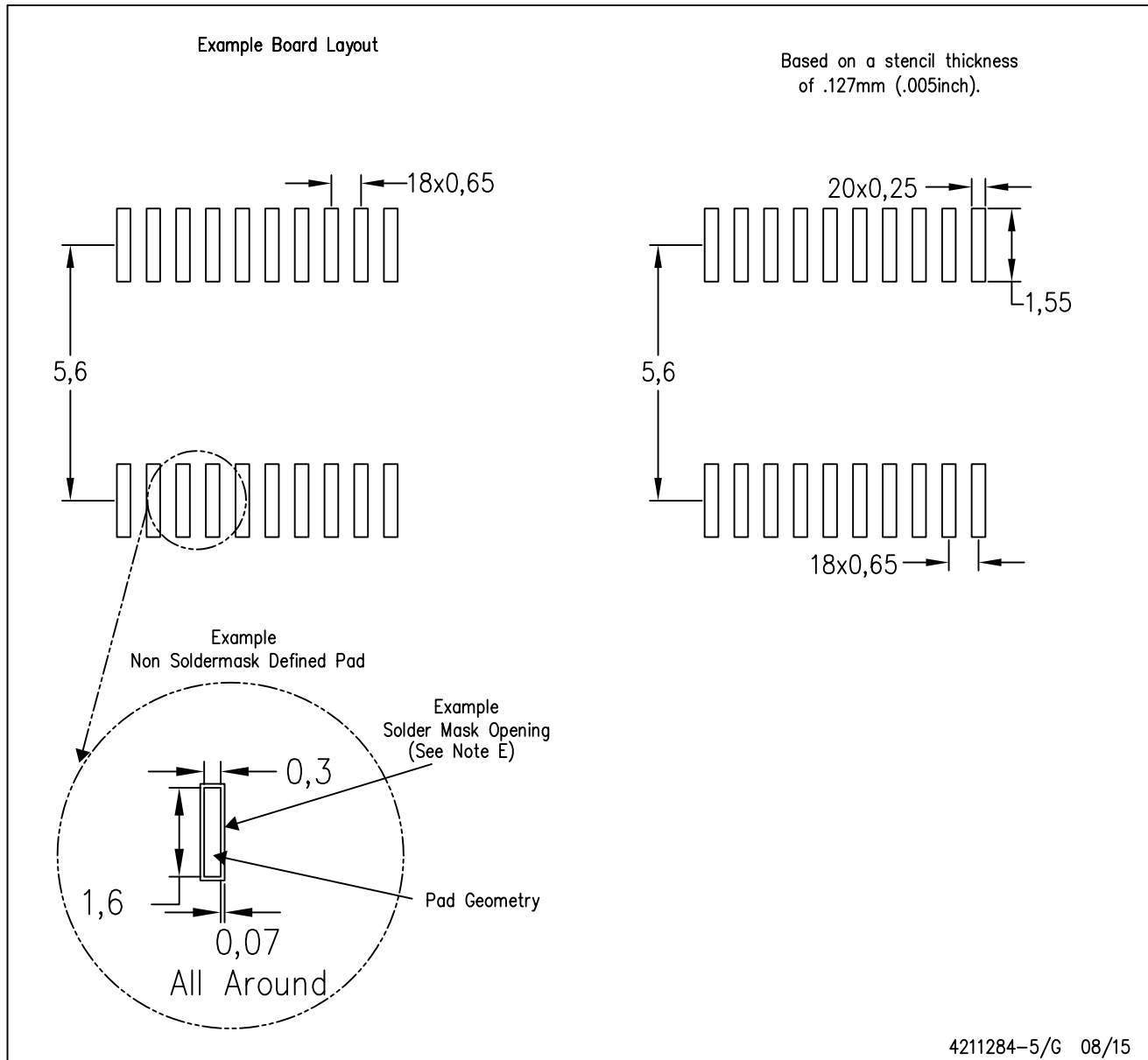
4220206/A 02/2017

NOTES: (continued)

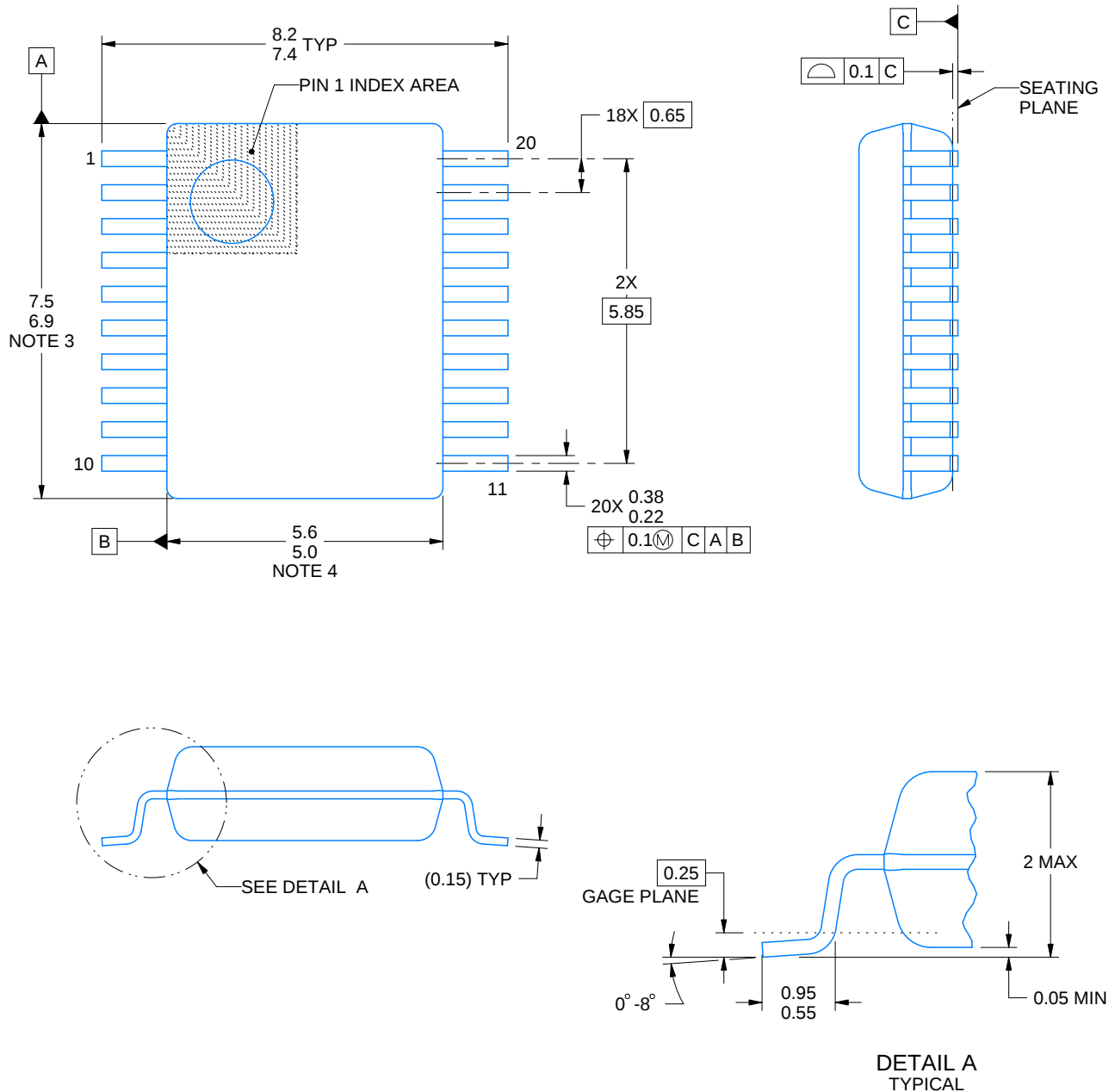
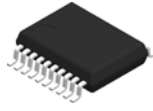
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4214851/B 08/2019

NOTES:

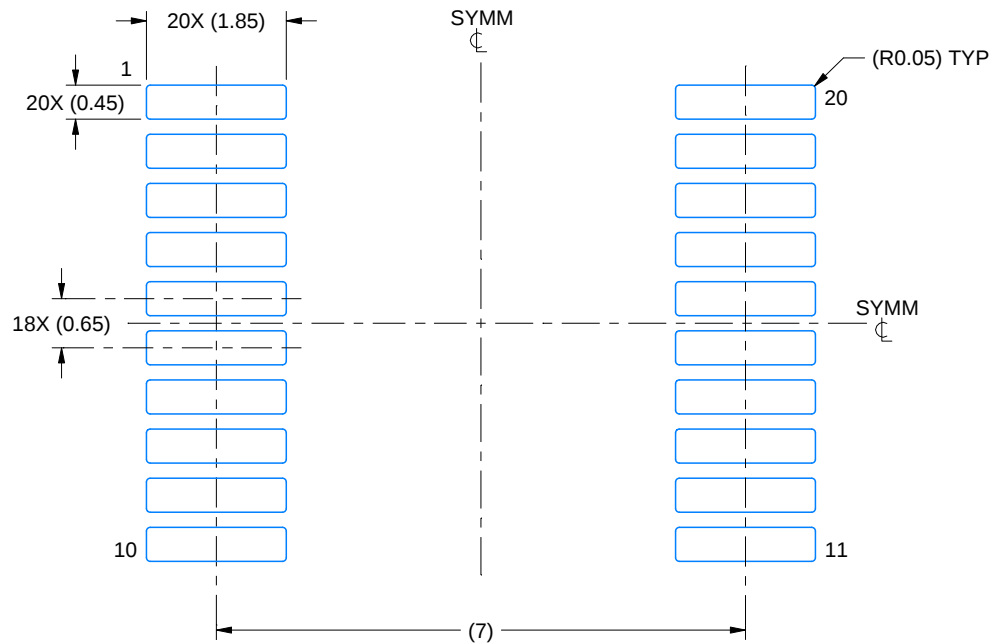
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

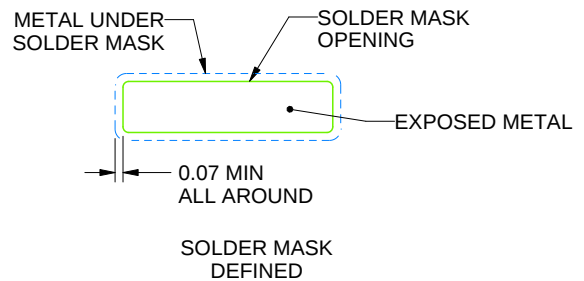
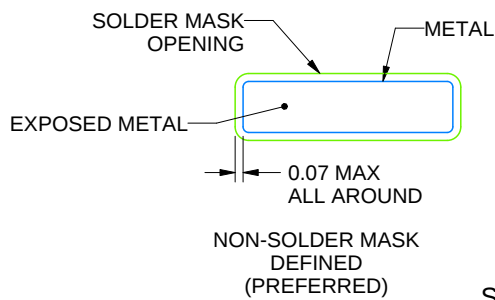
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

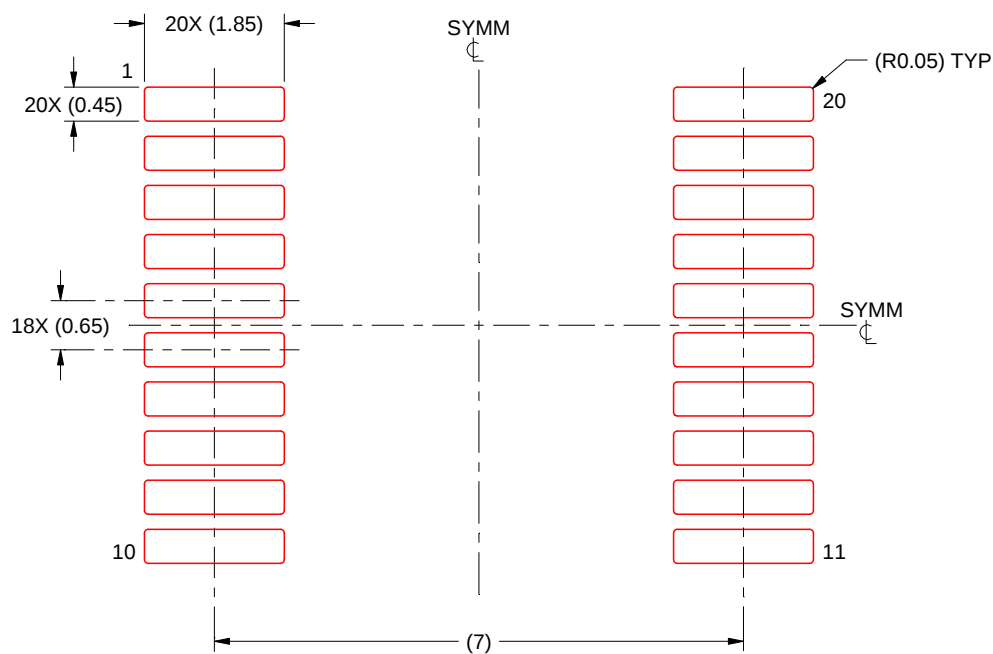
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

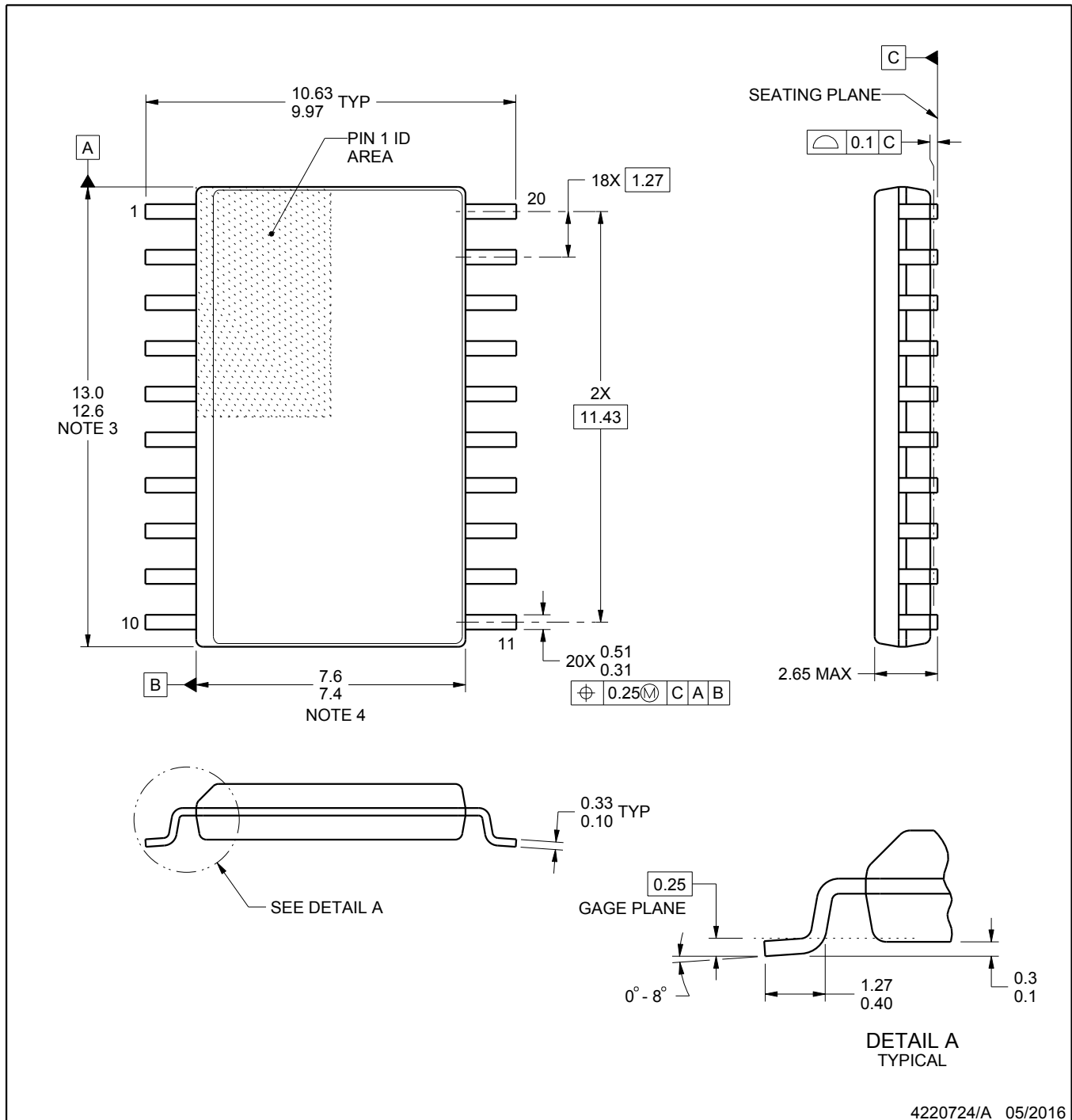
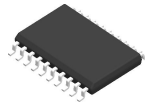


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



NOTES:

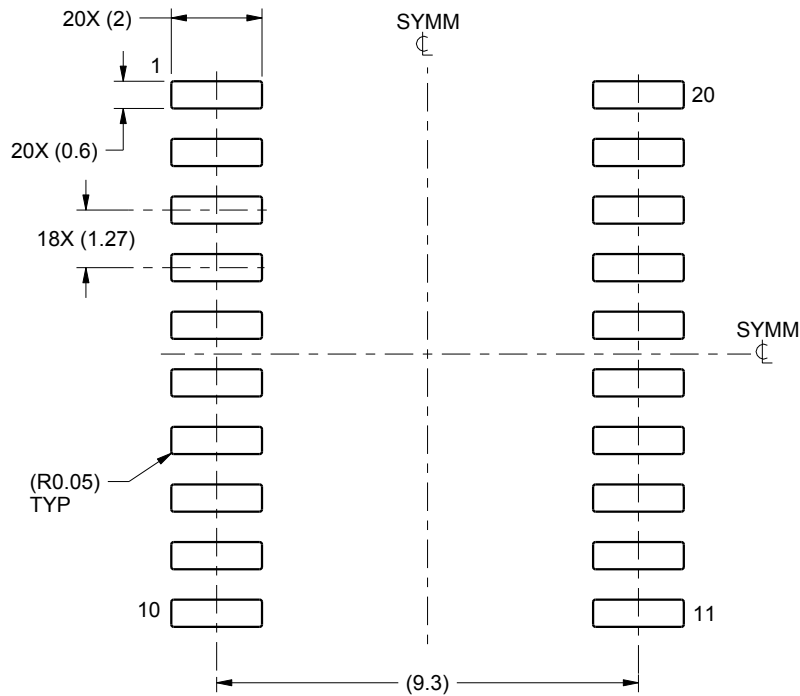
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

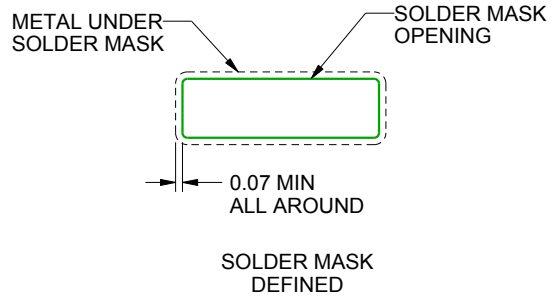
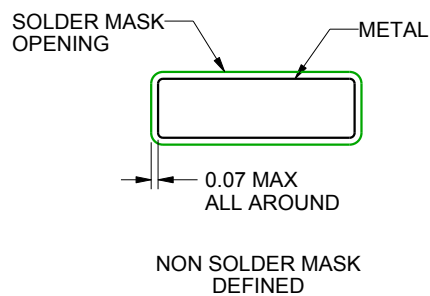
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

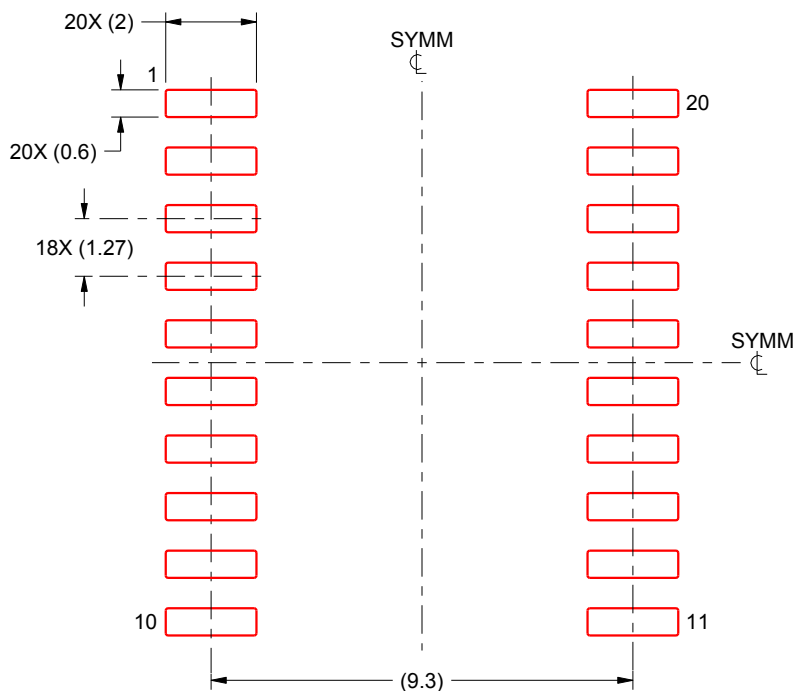
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated