UA78L00 Series Positive-Voltage Linear Regulators

1 Features

- 3-Terminal Linear Regulators
- Output Current Up to 100 mA
- No External Components
- Internal Thermal-Overload Protection
- Internal Short-Circuit Current Limiting

2 Applications

- Computing and Servers
- On-Card Regulation
- Telecommunications
- White Goods
- Chemical or Gas Sensors
- Field Transmitter: Temperature Sensors
- Flow Meters

3 Description

The UA78L00 series of fixed-voltage linear regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation as well as for voltage regulation in major appliances. In addition, they can be used with power-pass elements to make high-current voltage regulators. One of these regulators can deliver up to 100 mA of output current. The internal limiting and thermal-shutdown features of these regulators help to protect the device from overload.

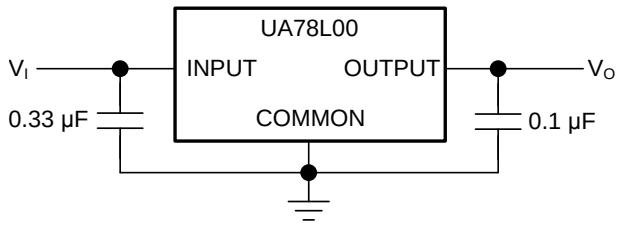
The UA78L00C and UA78L00AC series devices are characterized for operation over the virtual junction temperature range of 0°C to 125°C. The UA78L05AI device is characterized for operation over the virtual junction temperature range of −40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UA78L00D, UA78L00AD	SOIC (8)	4.90 mm × 3.91 mm
UA78L00LP, UA78L00ALP	TO-92 (3)	4.30 mm × 4.30 mm
UA78L00PK, UA78L00APK	SOT-89 (3)	4.50 mm × 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision U (January 2014) to Revision V	Page
• Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added Applications	1
• Changed θ_{JA} values in *Thermal Information* table From: 97 To: 115 (D), From: 140 To: 143.6 (LP), and From: 52 To: 54.7 (PK)	4
• Changed θ_{JC} values in *Thermal Information* table From: 39 To: 60.3 (D), From: 55 To: 74.4 (LP), and From: 9 To: 88.1 (PK)	4

Changes from Revision T (May 2011) to Revision U	Page
• Deleted *Ordering Information* table; see *Product Option Addendum* at the end of the data sheet	1
• Updated document to new TI data sheet format - no specification changes	1

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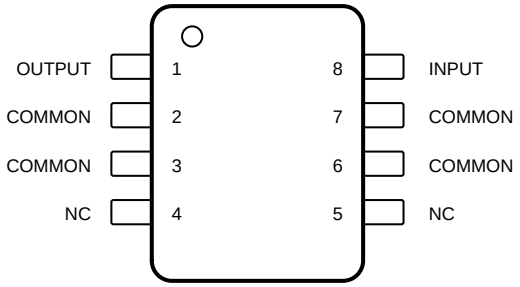
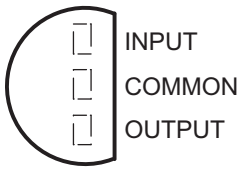
5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View

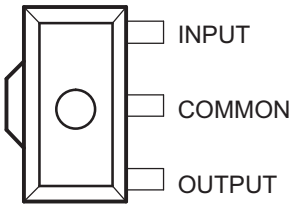


Not to scale

LP Package
3-Pin TO-92
Top View



PK Package
3-Pin SOT-89
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	SOIC	TO-92	SOT-89		
COMMON	2, 3, 6, 7	2	2	—	Ground
INPUT	8	3	3	I	Supply input
OUTPUT	1	1	1	O	Voltage output
NC	4, 5	—	—	—	No internal connection

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage, V_I	UA78L02AC, UA78L05C, UA78L09C, and UA78L10AC		30	V
	UA78L12C, UA78L12AC, UA78L15C, and UA78L15AC		35	
Virtual junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	1000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_I Input voltage	UA78L02AC	4.75	20	V
	UA78L05C and UA78L05AC	7	20	
	UA78L06C and UA78L06AC	8.5	20	
	UA78L08C and UA78L08AC	10.5	23	
	UA78L09C and UA78L09AC	11.5	24	
	UA78L10AC	12.5	25	
	UA78L12C and UA78L12AC	14.5	27	
	UA78L15C and UA78L15AC	17.5	30	
I_O Output current			100	mA
T_J Operating virtual junction temperature	UA78L00C and UA78L00AC series	0	125	°C
	UA78L05AI	–40	125	

6.4 Thermal Information

THERMAL METRIC[1]		UA78L00			UNIT
		D (SOIC)	LP (TO-92)	PK (SOT-89)	
		8 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115	143.6	54.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.3	74.4	88.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.6	—	9.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.2	24.2	6.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55	120.9	9.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	7.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics: UA78L02

at specified virtual junction temperature, V_I = 9 V, and I_O = 40 mA (unless otherwise noted)[1]

PARAMETER	TEST CONDITIONS[2]		MIN	TYP	MAX	UNIT
Output voltagef	V_I = 4.75 V to 20 V, and I_O = 1 mA to 40 mA	T_J = 25°C	2.5	2.6	2.7	V
		T_J = 0°C to 125°C	2.45		2.75	
	I_O = 1 mA to 70 mA, and T_J = 0°C to 125°C		2.45		2.75	
Input voltage regulation	V_I = 4.75 V to 20 V, and T_J = 25°C			20	100	mV
	V_I = 5 V to 20 V, and T_J = 25°C			16	75	
Ripple rejection	V_I = 6 V to 20 V, f = 120 Hz, and T_J = 25°C		43	51		dB
Output voltage regulation	I_O = 1 mA to 100 mA, and T_J = 25°C			12	50	mV
	I_O = 1 mA to 40 mA, and T_J = 25°C			6	25	
Output noise voltage	f = 10 Hz to 100 kHz, and T_J = 25°C			30		µV
Dropout voltage	T_J = 25°C			1.7		V
Bias current	T_J = 25°C			3.6	6	mA
	T_J = 125°C				5.5	
Bias current change	V_I = 5 V to 20 V, and T_J = 0°C to 125°C				2.5	mA
	I_O = 1 mA to 40 mA, and T_J = 0°C to 125°C				0.1	

(1) Applies to UA78L02AC.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

6.6 Electrical Characteristics: UA78L05

at specified virtual junction temperature, V_I = 10 V, and I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
Output voltage	V_I = 7 V to 20 V, and I_O = 1 mA to 40 mA	T_J = 25°C	UA78L05C	4.6	5	5.4	V
			UA78L05AC and UA78L05AI	4.8	5	5.2	
		T_J = full range	UA78L05C	4.5		5.5	
			UA78L05AC and UA78L05AI	4.75		5.25	
	I_O = 1 mA to 70 mA, and T_J = full range	UA78L05C		4.5		5.5	
		UA78L05AC and UA78L05AI		4.75		5.25	
Input voltage regulation	V_I = 7 V to 20 V, and T_J = 25°C	UA78L05C			32	200	mV
		UA78L05AC and UA78L05AI			32	150	
	V_I = 8 V to 20 V, and T_J = 25°C	UA78L05C			26	150	
		UA78L05AC and UA78L05AI			26	100	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz, and T_J = 25°C	UA78L05C		40	49		dB
		UA78L05AC and UA78L05AI		41	49		
Output voltage regulation	I_O = 1 mA to 100 mA, and T_J = 25°C				15	60	mV
	I_O = 1 mA to 40 mA, and T_J = 25°C				8	30	
Output noise voltage	f = 10 Hz to 100 kHz, and T_J = 25°C				42		µV
Dropout voltage	T_J = 25°C				1.7		V
Bias current	T_J = 25°C				3.8	6	mA
	T_J = 125°C					5.5	
Bias current change	V_I = 8 V to 20 V, and T_J = full range					1.5	mA
	I_O = 1 mA to 40 mA, and T_J = full range	UA78L05C				0.2	
		UA78L05AC and UA78L05AI				0.1	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output. Full range for the UA78L05AC is T_J = 0°C to 125°C, and full range for the UA78L05AI is T_J = –40°C to 125°C.

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6.7 Electrical Characteristics: UA78L06

at specified virtual junction temperature, V_I = 12 V, and I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 8.5 V to 20 V, I_O = 1 mA to 40 mA	T_J = 25°C	UA78L06C	5.7	6.2	6.7	V
			UA78L06AC	5.95	6.2	6.45	
		T_J = 0°C to 125°C	UA78L06C	5.6		6.8	
			UA78L06AC	5.9		6.5	
	T_J = 0°C to 125°C, and I_O = 1 mA to 70 mA		UA78L06C	5.6		6.8	
			UA78L06AC	5.9		6.5	
Input voltage regulation	T_J = 25°C	V_I = 8.5 V to 20 V	UA78L06C		35	200	mV
			UA78L06AC		35	175	
		V_I = 9 V to 20 V	UA78L06C		29	150	
			UA78L06AC		29	125	
Ripple rejection	T_J = 25°C, V_I = 10 V to 20 V, and f = 120 Hz		UA78L06C	39	48		dB
			UA78L06AC	40	48		
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA			16	80	mV
		I_O = 1 mA to 40 mA			9	40	
Output noise voltage	T_J = 25°C, and f = 10 Hz to 100 kHz				46		µV
Dropout voltage	T_J = 25°C				1.7		V
Bias current	T_J = 25°C				3.9	6	mA
	T_J = 125°C					5.5	
Bias current change	T_J = 0°C to 125°C	V_I = 9 V to 20 V				1.5	mA
		I_O = 1 mA to 40 mA	UA78L06C			0.2	
			UA78L06AC			0.1	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

6.8 Electrical Characteristics: UA78L08

at specified virtual junction temperature, V_I = 14 V, and I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 10.5 V to 23 V, I_O = 1 mA to 40 mA	T_J = 25°C	UA78L08C	7.36	8	8.64	V
			UA78L08AC	7.7	8	8.3	
		T_J = 0°C to 125°C	UA78L08C	7.2		8.8	
			UA78L08AC	7.6		8.4	
	I_O = 1 mA to 70 mA	T_J = 0°C to 125°C	UA78L08C	7.2		8.8	
			UA78L08AC	7.6		8.4	
Input voltage regulation	T_J = 25°C	V_I = 10.5 V to 23 V	UA78L08C		42	200	mV
			UA78L08AC		42	175	
		V_I = 11 V to 23 V	UA78L08C		36	150	
			UA78L08AC		36	125	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz, and T_J = 25°C		UA78L08C	36	46		dB
			UA78L08AC	37	46		
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA			18	80	mV
		I_O = 1 mA to 40 mA			10	40	
Output noise voltage	f = 10 Hz to 100 kHz, and T_J = 25°C				54		µV
Dropout voltage	T_J = 25°C				1.7		V
Bias current	T_J = 25°C				4	6	mA
	T_J = 125°C					5.5	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

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Electrical Characteristics: UA78L08 (continued)

at specified virtual junction temperature, V_I = 14 V, and I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)			MIN	TYP	MAX	UNIT
Bias current change	T_J = 0°C to 125°C	V_I = 11 V to 23 V				1.5	mA
		I_O = 1 mA to 40 mA	UA78L08C			0.2	
			UA78L08AC			0.1	

6.9 Electrical Characteristics: UA78L09

at specified virtual junction temperature, V_I = 16 V, and I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 12 V to 24 V, I_O = 1 mA to 40 mA	T_J = 25°C	UA78L09C	8.3	9	9.7	V
			UA78L09AC	8.6	9	9.4	
		T_J = 0°C to 125°C	UA78L09C	8.1		9.9	
			UA78L09AC	8.55		9.45	
	I_O = 1 mA to 70 mA, and T_J = 0°C to 125°C		UA78L09C	8.1		9.9	
			UA78L09AC	8.55		9.45	
Input voltage regulation	T_J = 25°C	V_I = 12 V to 24 V	UA78L09C		45	225	mV
			UA78L09AC		45	175	
		V_I = 13 V to 24 V	UA78L09C		40	175	
			UA78L09AC		40	125	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz, and T_J = 25°C		UA78L09C	36	45		dB
			UA78L09AC	38	45		
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA			19	90	mV
		I_O = 1 mA to 40 mA			11	40	
Output noise voltage	f = 10 Hz to 100 kHz, and T_J = 25°C				58		µV
Dropout voltage	T_J = 25°C				1.7		V
Bias current	T_J = 25°C				4.1	6	mA
	T_J = 125°C					5.5	
Bias current change	T_J = 0°C to 125°C	V_I = 13 V to 24 V				1.5	mA
		I_O = 1 mA to 40 mA	UA78L09C			0.2	
			UA78L09AC			0.1	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

6.10 Electrical Characteristics: UA78L10

at specified virtual junction temperature, V_I = 14 V, and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 13 V to 25 V, and I_O = 1 mA to 40 mA	T_J = 25°C	9.6	10	10.4	V
		T_J = 0°C to 125°C	9.5		10.5	
	T_J = 0°C to 125°C, and I_O = 1 mA to 70 mA		9.5		10.5	
Input voltage regulation	T_J = 25°C	V_I = 13 V to 25 V		51	175	mV
		V_I = 14 V to 25 V		42	125	
Ripple rejection	T_J = 25°C, V_I = 15 V to 25 V, and f = 120 Hz		37	44		dB
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA		20	90	mV
		I_O = 1 mA to 40 mA		11	40	
Output noise voltage	T_J = 25°C, and f = 10 Hz to 100 kHz			62		µV
Dropout voltage	T_J = 25°C			1.7		V

(1) Applies to UA78L10AC.
(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

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Electrical Characteristics: UA78L10 (continued)

at specified virtual junction temperature, V_I = 14 V, and I_O = 40 mA (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(2)		MIN	TYP	MAX	UNIT
Bias current	T_J = 25°C			4.2	6	mA
	T_J = 125°C				5.5	
Bias current change	T_J = 0°C to 125°C	V_I = 14 V to 25 V			1.5	mA
		I_O = 1 mA to 40 mA			0.1	

6.11 Electrical Characteristics: UA78L12

at specified virtual junction temperature, V_I = 19 V, and I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 14 V to 27 V, and I_O = 1 mA to 40 mA	T_J = 25°C	UA78L12C	11.1	12	12.9	V
			UA78L12AC	11.5	12	12.5	
		T_J = 0°C to 125°C	UA78L12C	10.8		13.2	
			UA78L12AC	11.4		12.6	
	T_J = 0°C to 125°C, and I_O = 1 mA to 70 mA		UA78L12C	10.8		13.2	
			UA78L12AC	11.4		12.6	
Input voltage regulation	T_J = 25°C	V_I = 14.5 V to 27 V			55	250	mV
		V_I = 16 V to 27 V			49	200	
Ripple rejection	T_J = 25°C	V_I = 15 V to 25 V, and f = 120 Hz	UA78L12C	36	42		dB
			UA78L12AC	37	42		
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA			22	100	mV
		I_O = 1 mA to 40 mA			13	50	
Output noise voltage	T_J = 25°C, and f = 10 Hz to 100 kHz				70		µV
Dropout voltage	T_J = 25°C				1.7		V
Bias current	T_J = 25°C				4.3	6.5	mA
	T_J = 125°C					6	
Bias current change	T_J = 0°C to 125°C	V_I = 16 V to 27 V				1.5	mA
		I_O = 1 mA to 40 mA	UA78L12C			0.2	
			UA78L12AC			0.1	

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

6.12 Electrical Characteristics: UA78L15

at specified virtual junction temperature, V_I = 23 V, and I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)			MIN	TYP	MAX	UNIT
Output voltage	V_I = 17.5 V to 30 V, and I_O = 1 mA to 40 mA	T_J = 25°C	UA78L15C	13.8	15	16.2	V
			UA78L15AC	14.4	15	15.6	
		T_J = 0°C to 125°C	UA78L15C	13.5		16.5	
			UA78L15AC	14.25		15.75	
	T_J = 0°C to 125°C, and I_O = 1 mA to 70 mA		UA78L15C	13.5		16.5	
			UA78L15AC	14.25		15.75	
Input voltage regulation	T_J = 25°C	V_I = 17.5 V to 30 V			65	300	mV
		V_I = 20 V to 30 V			58	250	
Ripple rejection	T_J = 25°C	V_I = 18.5 V to 28.5 V, and f = 120 Hz	UA78L15C	33	39		dB
			UA78L15AC	34	39		

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

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Electrical Characteristics: UA78L15 (continued)

at specified virtual junction temperature, V_I = 23 V, and I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[(1)]			MIN	TYP	MAX	UNIT
Output voltage regulation	T_J = 25°C	I_O = 1 mA to 100 mA			25	150	mV
		I_O = 1 mA to 40 mA			15	75	
Output noise voltage	T_J = 25°C, and f = 10 Hz to 100 kHz				82		µV
Dropout voltage	T_J = 25°C				1.7		V
Bias current	T_J = 25°C				4.6	6.5	mA
	T_J = 125°C					6	
Bias current change	T_J = 0°C to 125°C	V_I = 10 V to 30 V				1.5	mA
		I_O = 1 mA to 40 mA	UA78L15C			0.2	
			UA78L15AC			0.1	

6.13 Typical Characteristics

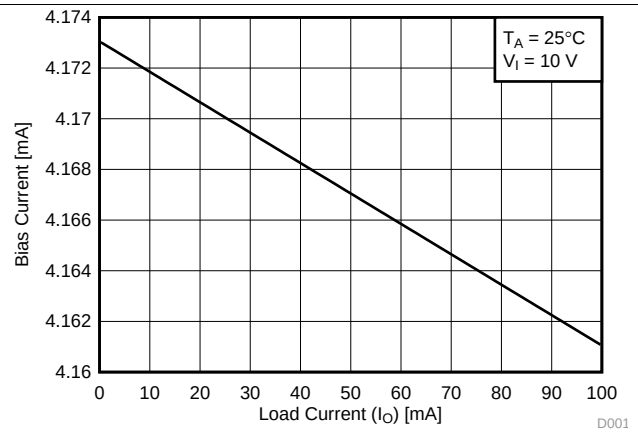


Figure 1. Bias Current vs Load Current

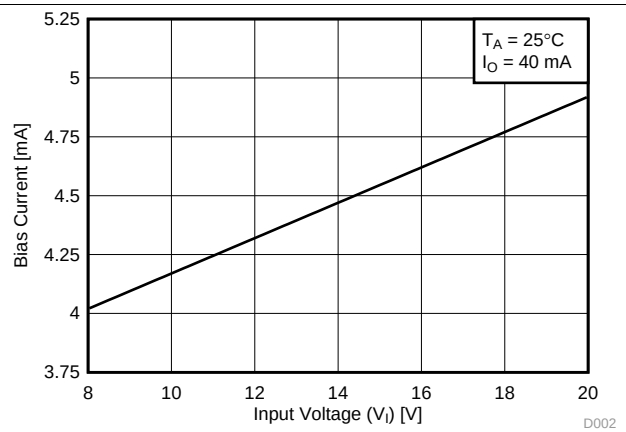


Figure 2. Bias Current vs Input Voltage

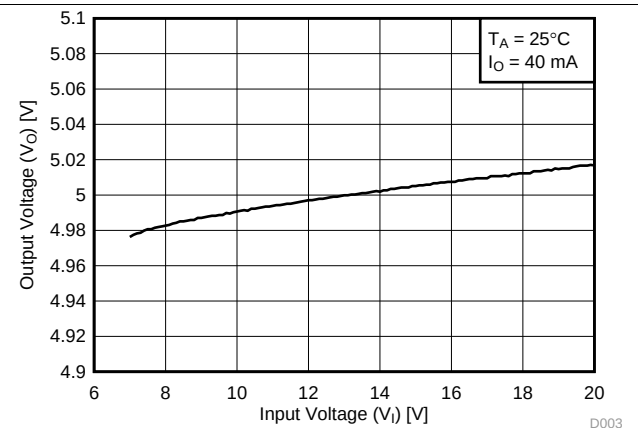


Figure 3. Line Regulation

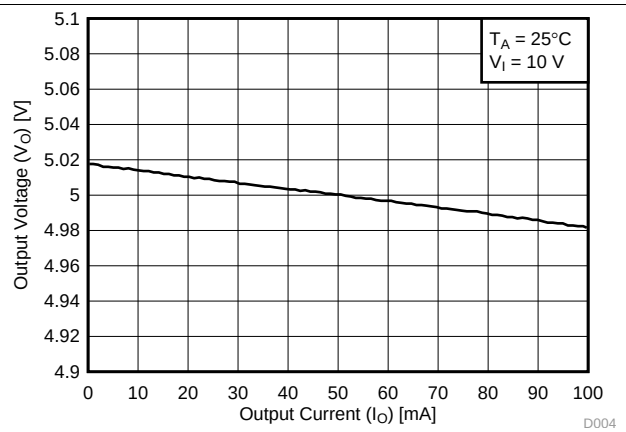


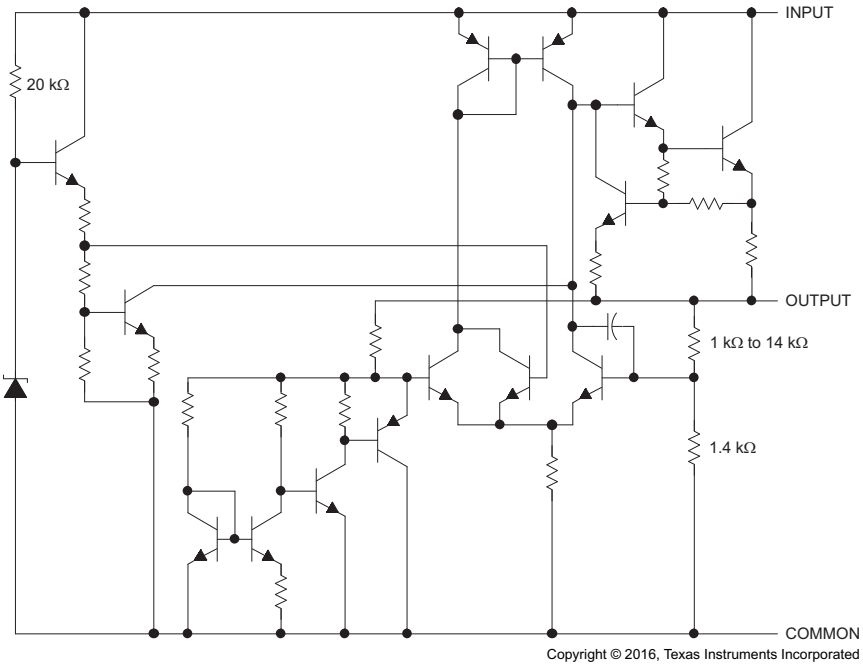
Figure 4. Load Regulation

7 Detailed Description

7.1 Overview

The UA78L00 series of fixed-voltage integrated-circuit voltage regulators is designed for a wide range of applications. Each of these regulators can deliver up to 100 mA of output current at a fixed output voltage depending on the device variant.

7.2 Functional Block Diagram



NOTE: Resistor values shown are nominal.

7.3 Feature Description

The UA78L00 series of linear regulators are easy-to-use, fixed-output voltage regulators. The devices enable up to 100 mA of current and feature short-circuit current limiting and thermal overload protection.

7.4 Device Functional Modes

7.4.1 Fixed-Output Mode

These devices are available in fixed-output voltages. Table 1 describes the typical output voltage provided by each device variation.

Table 1. UA78L00 Typical Device Voltage Outputs

DEVICE	TYPICAL OUTPUT VOLTAGE (V)
UA78L02	2.6
UA78L05	5
UA78L06	6.2
UA78L08	8
UA78L09	9
UA78L10	10
UA78L12	12
UA78L15	15

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8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UA78L00 devices are ideal for use as linear regulators with only a few external components needed. The UA78L00 devices can also be used to clean power supply noise by attenuating ripple on the input signal.

8.2 Typical Application

The UA78L00 devices are typically used as fixed-output linear regulators, sourcing current up to 100 mA into a load.

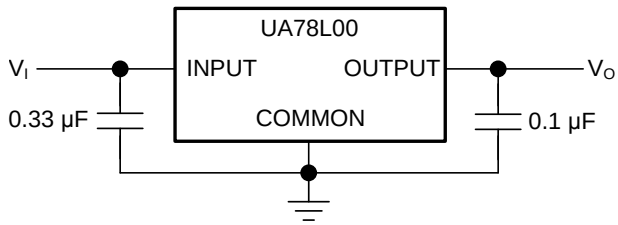

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Figure 5. Fixed Output Regulator

8.2.1 Design Requirements

The COMMON pin must be tied to ground to set the OUTPUT pin to the desired fixed output voltage.

Although not required, a 0.33-µF bypass capacitor is recommended on the input, and a 0.1-µF bypass capacitor is recommend on the output.

8.2.2 Detailed Design Procedure

Occasionally, the input voltage to the regulator can collapse faster than the output voltage. For example, this can occur when the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series-pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed as shown in Figure 6.

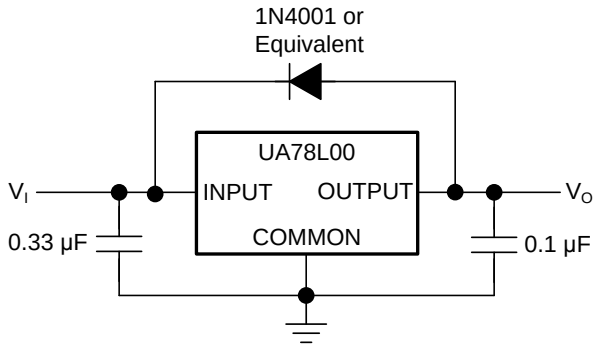

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Figure 6. Reverse-Bias-Protection Circuit

Typical Application (continued)

In many cases, a regulator powers a load that is not connected to ground, but instead, is connected to a voltage source of opposite polarity (for example, operational amplifiers, level-shifting circuits, and so on). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 7. This protects the regulator from output polarity reversals during startup and short-circuit operation.

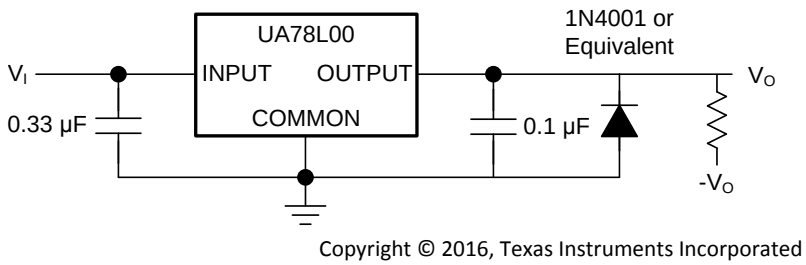

Figure 7. Output Polarity-Reversal-Protection Circuit

8.2.3 Application Curves

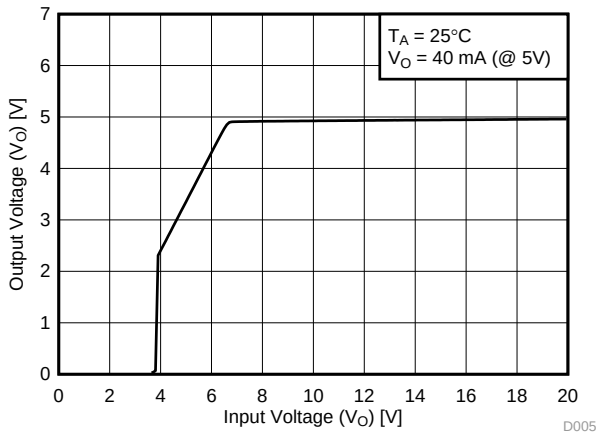

Figure 8. Output Voltage vs Input Voltage

8.3 System Examples

8.3.1 Positive Regulator in Negative Configuration

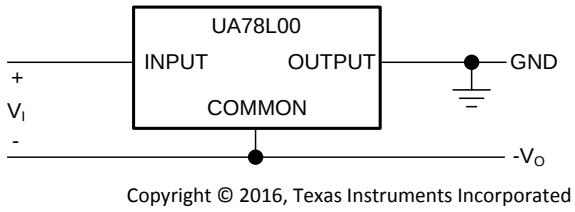

Figure 9. Positive Regulator in Negative Configuration (V_I Must Float)

8.3.2 Current Limiter Circuit

Figure 10 shows an example of using the UA78L00 as a current limiter. The output current limit is set by Equation 1.

$$I_O = \left(\frac{V_O}{R1}\right) + I_O \text{ Bias Current} \tag{1}$$

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System Examples (continued)

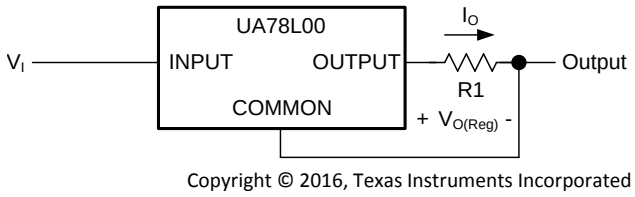

Figure 10. Current Limiter Example

9 Power Supply Recommendations

See *Recommended Operating Conditions* for the recommended power supply voltages for each variation of the UA78L00. Note that each device variant may have a different recommended maximum operating voltage.

10 Layout

10.1 Layout Guidelines

Keep trace widths large enough to eliminate problematic I×R voltage drops at the input and output terminals. Bypass capacitors should be placed as close to the UA78L00 as possible. Additional copper and vias connected to ground facilitate additional thermal dissipation, preventing the device from reaching thermal overload.

10.2 Layout Example

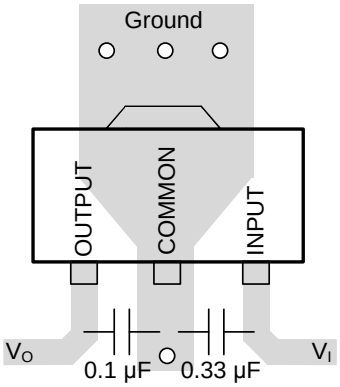

Figure 11. Example Layout for PK Package

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UA78L02A	Click here	Click here	Click here	Click here	Click here
UA78L05	Click here	Click here	Click here	Click here	Click here
UA78L05A	Click here	Click here	Click here	Click here	Click here
UA78L06A	Click here	Click here	Click here	Click here	Click here
UA78L08A	Click here	Click here	Click here	Click here	Click here
UA78L09A	Click here	Click here	Click here	Click here	Click here
UA78L10A	Click here	Click here	Click here	Click here	Click here
UA78L12A	Click here	Click here	Click here	Click here	Click here
UA78L15A	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA78L02ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L02A	Samples
UA78L02ACDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L02A	Samples
UA78L02ACLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L02AC	Samples
UA78L02ACLPE3	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L02AC	Samples
UA78L05ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05A	Samples
UA78L05ACLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L05AC	Samples
UA78L05ACLPE3	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L05AC	Samples
UA78L05ACLPM	ACTIVE	TO-92	LP	3	2000	RoHS & Non-Green	SN	N / A for Pkg Type	0 to 125	78L05AC	Samples
UA78L05ACLPME3	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L05AC	Samples
UA78L05ACLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L05AC	Samples
UA78L05ACLPRE3	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L05AC	Samples
UA78L05ACPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F5	Samples
UA78L05ACPKE6	ACTIVE	SOT-89	PK	3	1000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	0 to 125	F5	Samples
UA78L05ACPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F5	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA78L05AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI	Samples
UA78L05AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI	Samples
UA78L05AIDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	78L05AI	Samples
UA78L05AILP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	78L05AI	Samples
UA78L05AILPE3	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	78L05AI	Samples
UA78L05AILPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	78L05AI	Samples
UA78L05AILPRE3	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	78L05AI	Samples
UA78L05AIPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	J5	Samples
UA78L05AIPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	J5	Samples
UA78L05CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C	Samples
UA78L05CDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C	Samples
UA78L05CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C	Samples
UA78L05CDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L05C	Samples
UA78L05CLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L05C	Samples
UA78L05CLPE3	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L05C	Samples
UA78L05CLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L05C	Samples
UA78L05CPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	B5	Samples
UA78L05CPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	B5	Samples
UA78L06ACLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L06AC	Samples
UA78L06ACLPE3	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L06AC	Samples
UA78L06ACLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L06AC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA78L06ACLPRE3	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L06AC	Samples
UA78L06ACPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F6	Samples
UA78L06ACPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F6	Samples
UA78L08ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L08A	Samples
UA78L08ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 125	78L08A	Samples
UA78L08ACDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L08A	Samples
UA78L08ACLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L08AC	Samples
UA78L08ACLPE3	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L08AC	Samples
UA78L08ACLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L08AC	Samples
UA78L08ACLPRE3	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L08AC	Samples
UA78L08ACPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F8	Samples
UA78L08ACPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F8	Samples
UA78L09ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L09A	Samples
UA78L09ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L09A	Samples
UA78L09ACDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L09A	Samples
UA78L09ACLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L09AC	Samples
UA78L09ACLPE3	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L09AC	Samples
UA78L09ACLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L09AC	Samples
UA78L09ACLPRE3	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L09AC	Samples
UA78L09ACPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F9	Samples
UA78L09ACPKE6	ACTIVE	SOT-89	PK	3	1000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	0 to 125	F9	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA78L09ACPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	F9	Samples
UA78L10ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A	Samples
UA78L10ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A	Samples
UA78L10ACDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L10A	Samples
UA78L10ACLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L10AC	Samples
UA78L10ACLPE3	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L10AC	Samples
UA78L10ACLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L10AC	Samples
UA78L10ACLPRE3	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L10AC	Samples
UA78L10ACPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	FA	Samples
UA78L10ACPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	FA	Samples
UA78L12ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A	Samples
UA78L12ACDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A	Samples
UA78L12ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 125	78L12A	Samples
UA78L12ACDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A	Samples
UA78L12ACDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L12A	Samples
UA78L12ACLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L12AC	Samples
UA78L12ACLPE3	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L12AC	Samples
UA78L12ACLPM	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L12AC	Samples
UA78L12ACLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L12AC	Samples
UA78L12ACPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	FC	Samples
UA78L12ACPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	FC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA78L15ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L15A	Samples
UA78L15ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L15A	Samples
UA78L15ACDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	78L15A	Samples
UA78L15ACLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L15AC	Samples
UA78L15ACLPE3	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L15AC	Samples
UA78L15ACLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L15AC	Samples
UA78L15ACLPRE3	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 125	78L15AC	Samples
UA78L15ACPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	FF	Samples
UA78L15ACPKG3	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	FF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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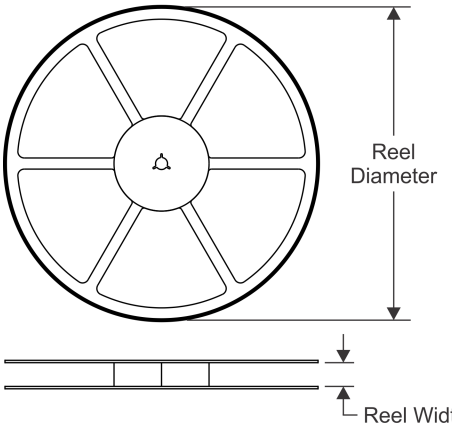
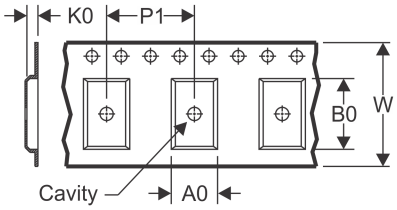
TAPE AND REEL INFORMATION

REEL DIMENSIONS

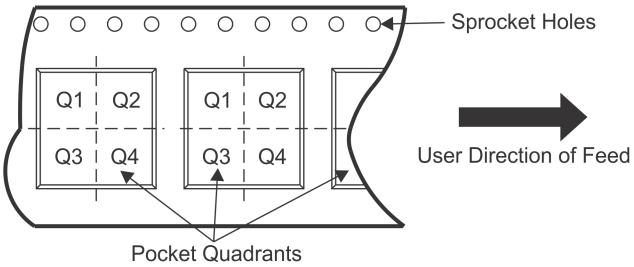


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

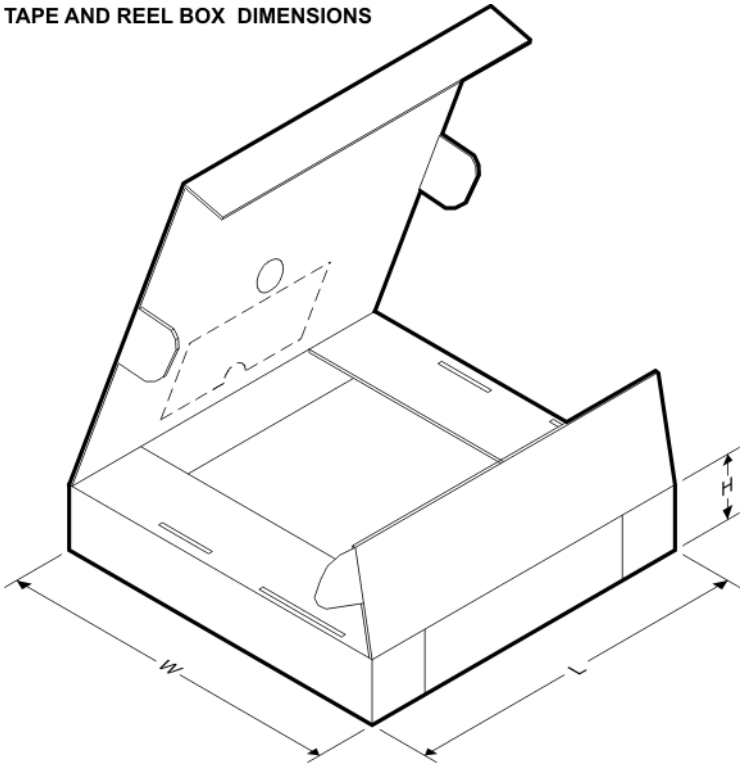


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA78L05ACDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05ACPKE6	SOT-89	PK	3	1000	180.0	13.0	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05AIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L05CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L05CPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L06ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L08ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L08ACDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
UA78L08ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L08ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L09ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L09ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L09ACPKE6	SOT-89	PK	3	1000	180.0	13.0	4.91	4.52	1.9	8.0	12.0	Q3
UA78L10ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA78L10ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L12ACDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
UA78L12ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L12ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L12ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
UA78L15ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA78L15ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS

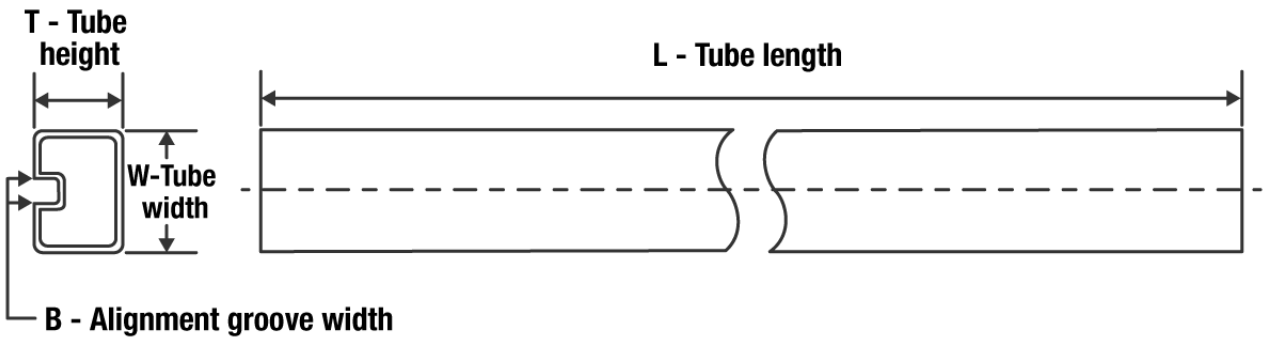


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA78L05ACDR	SOIC	D	8	2500	364.0	364.0	27.0
UA78L05ACDR	SOIC	D	8	2500	340.5	336.1	25.0
UA78L05ACDRG4	SOIC	D	8	2500	340.5	336.1	25.0
UA78L05ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L05ACPKE6	SOT-89	PK	3	1000	182.0	182.0	20.0
UA78L05AIDR	SOIC	D	8	2500	340.5	336.1	25.0
UA78L05AIPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L05CDR	SOIC	D	8	2500	340.5	336.1	25.0
UA78L05CPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L06ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA78L08ACDR	SOIC	D	8	2500	340.5	336.1	25.0
UA78L08ACDR	SOIC	D	8	2500	364.0	364.0	27.0
UA78L08ACDRG4	SOIC	D	8	2500	340.5	336.1	25.0
UA78L08ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L09ACDR	SOIC	D	8	2500	340.5	336.1	25.0
UA78L09ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L09ACPKE6	SOT-89	PK	3	1000	182.0	182.0	20.0
UA78L10ACDR	SOIC	D	8	2500	340.5	336.1	25.0
UA78L10ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L12ACDR	SOIC	D	8	2500	364.0	364.0	27.0
UA78L12ACDR	SOIC	D	8	2500	340.5	336.1	25.0
UA78L12ACDRG4	SOIC	D	8	2500	340.5	336.1	25.0
UA78L12ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
UA78L15ACDR	SOIC	D	8	2500	340.5	336.1	25.0
UA78L15ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0

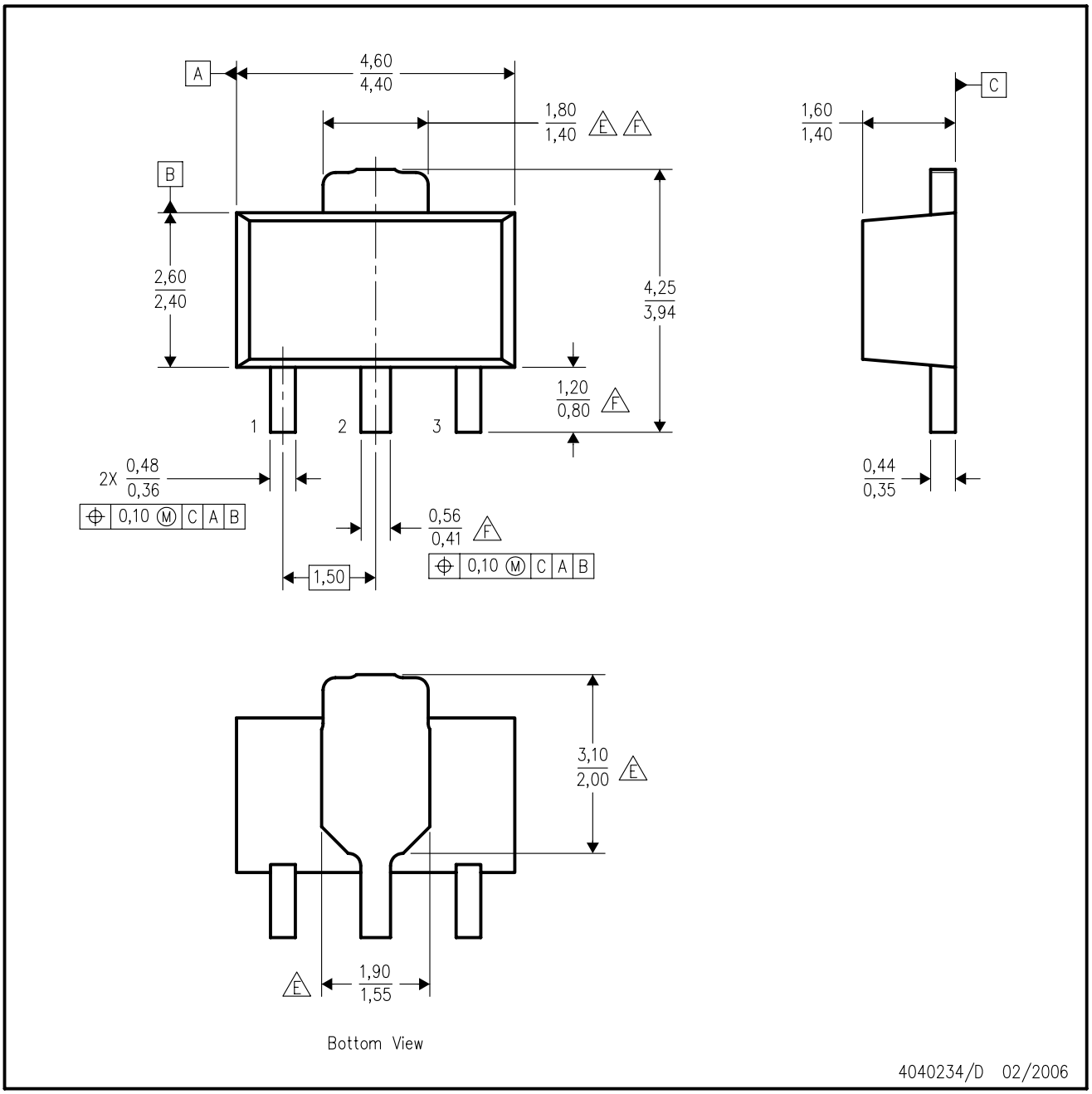
TUBE



*All dimensions are nominal

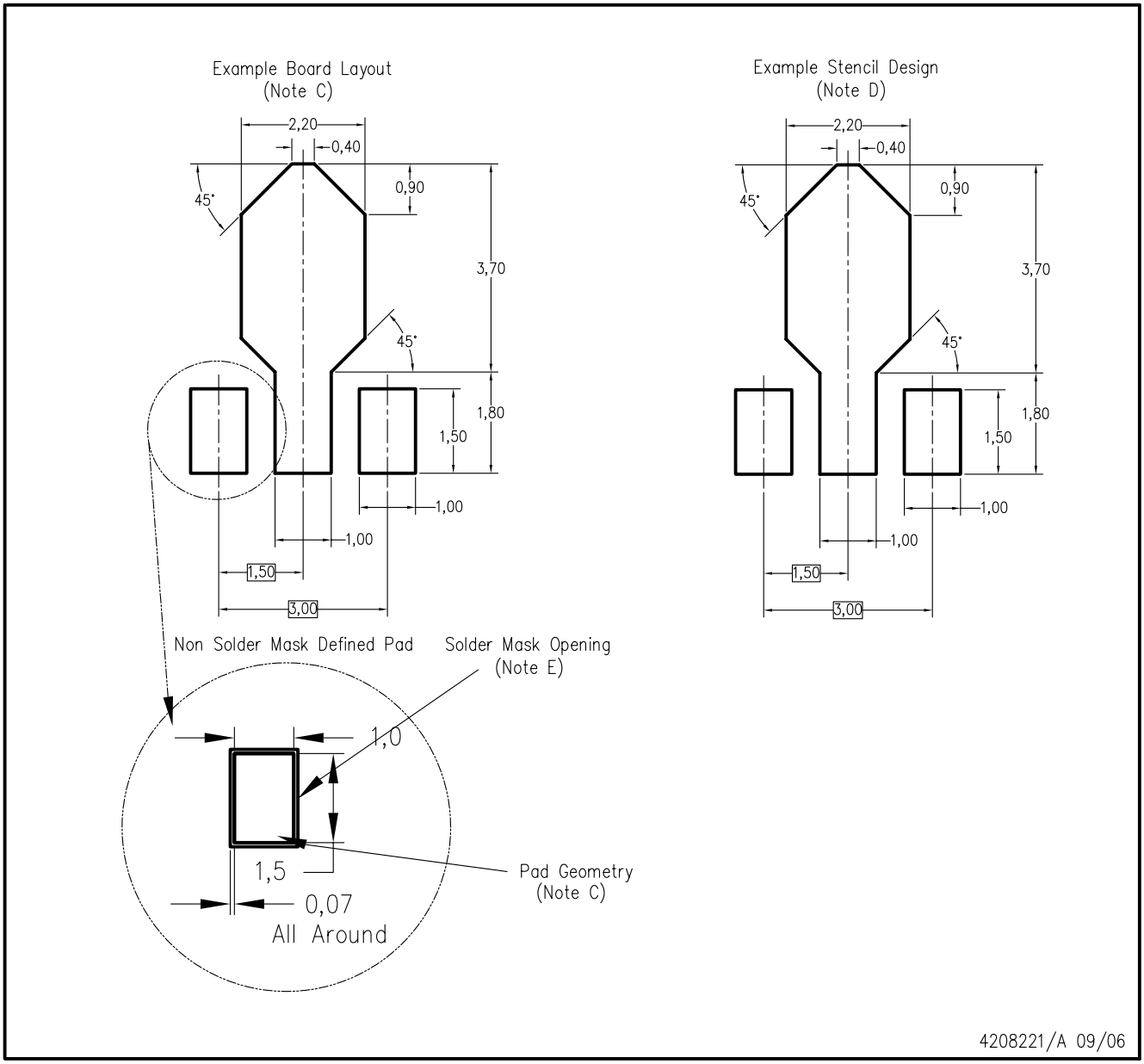
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UA78L02ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L02ACDG4	D	SOIC	8	75	507	8	3940	4.32
UA78L05ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L05ACDE4	D	SOIC	8	75	507	8	3940	4.32
UA78L05ACDG4	D	SOIC	8	75	507	8	3940	4.32
UA78L05AID	D	SOIC	8	75	507	8	3940	4.32
UA78L05CD	D	SOIC	8	75	507	8	3940	4.32
UA78L05CDG4	D	SOIC	8	75	507	8	3940	4.32
UA78L08ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L09ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L10ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L12ACD	D	SOIC	8	75	507	8	3940	4.32
UA78L12ACDG4	D	SOIC	8	75	507	8	3940	4.32
UA78L15ACD	D	SOIC	8	75	507	8	3940	4.32

PK (R–PSSO–F3) PLASTIC SINGLE–IN–LINE PACKAGE

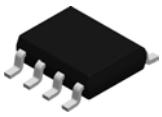


NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. The center lead is in electrical contact with the tab.
- D. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
- E. Thermal pad contour optional within these dimensions.
- F. Falls within JEDEC TO–243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

PK (R–PDSO–G3)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

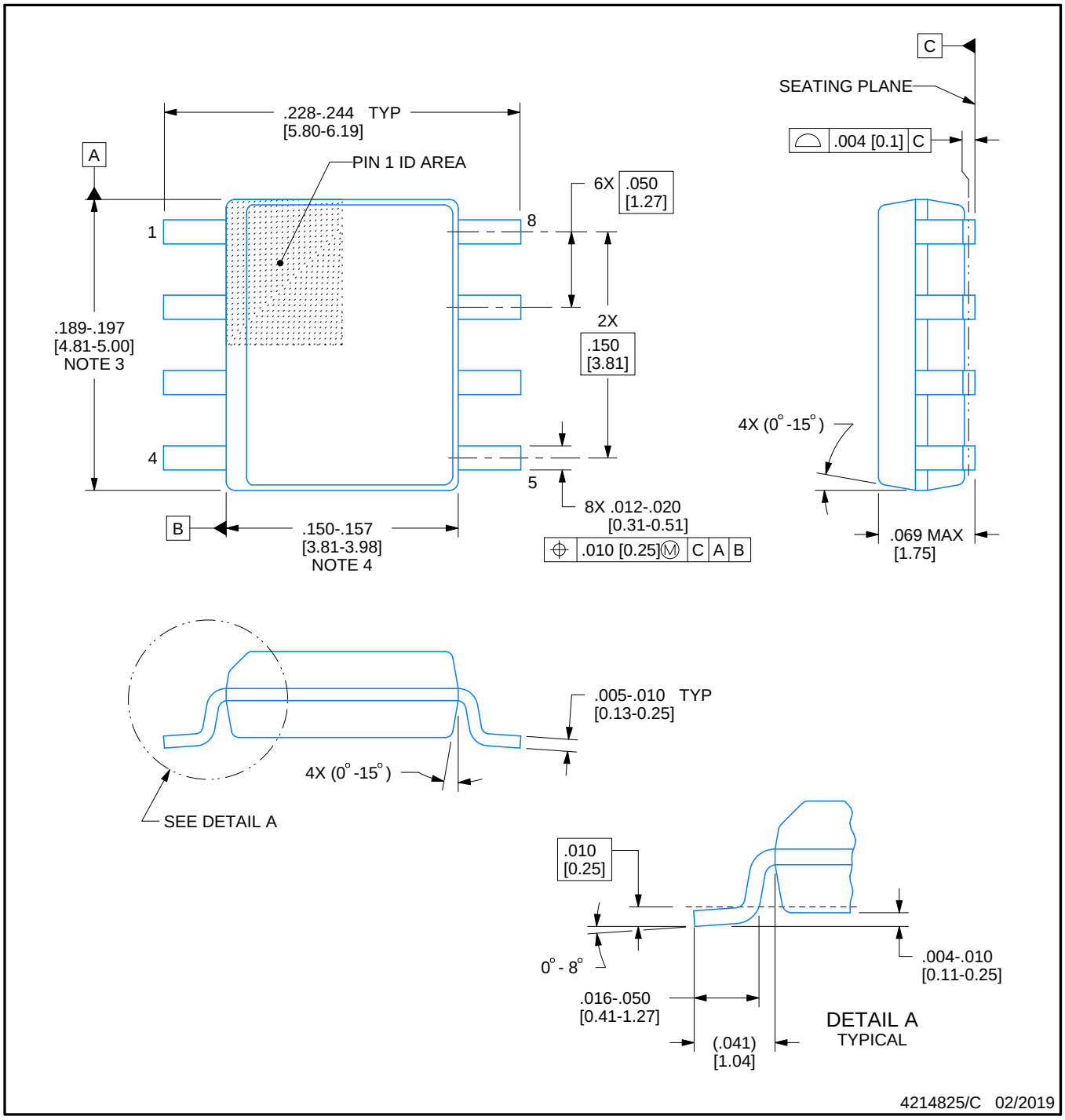


PACKAGE OUTLINE

D0008A

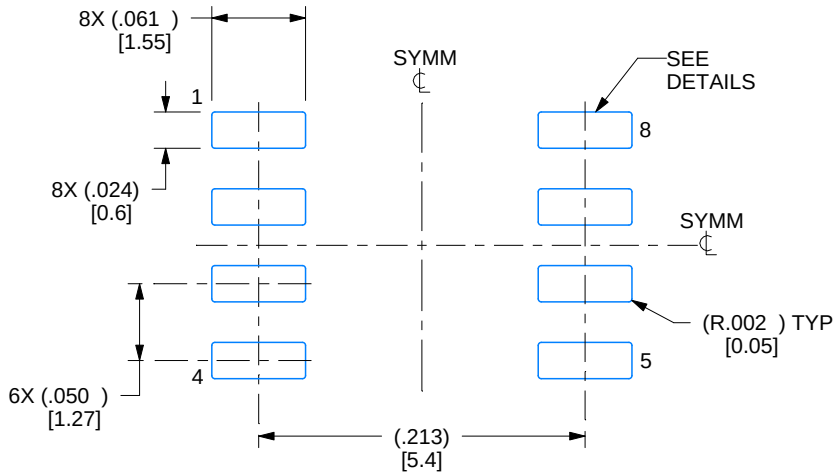
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

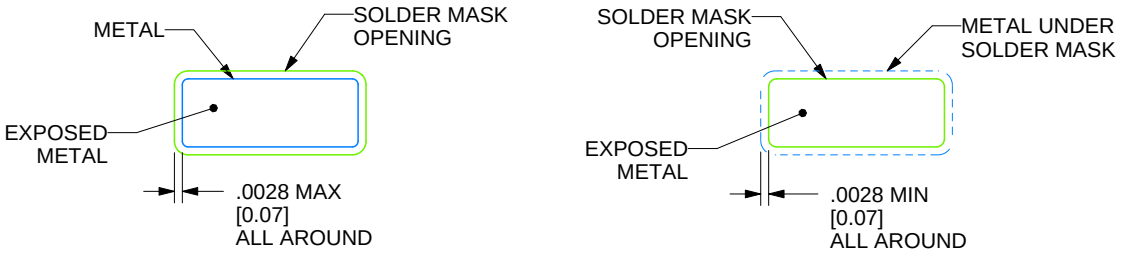


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

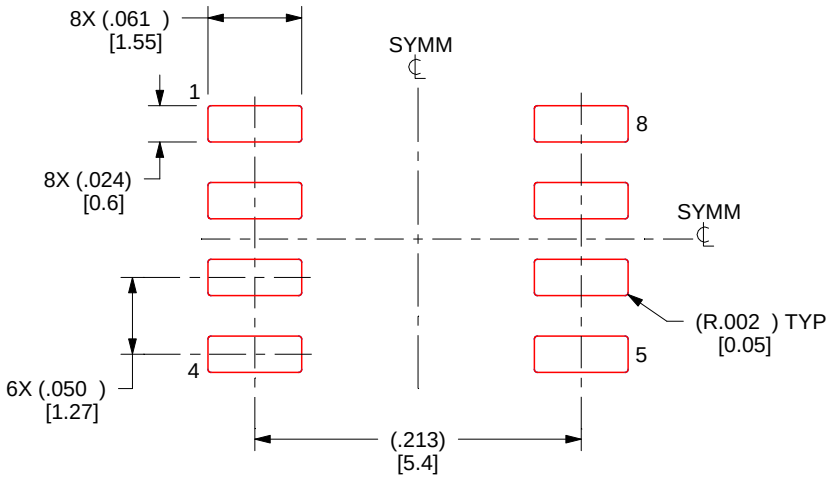


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



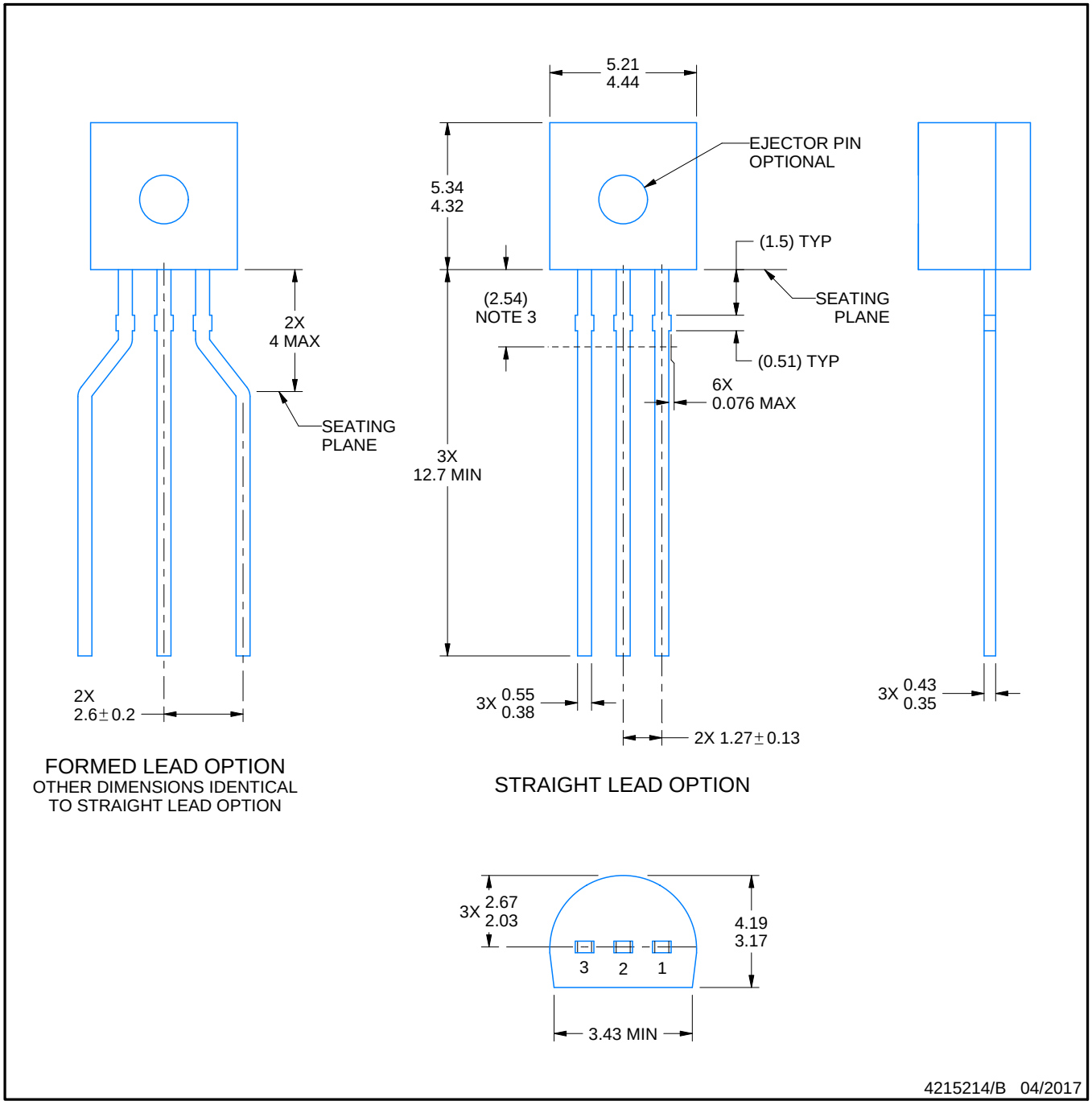
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

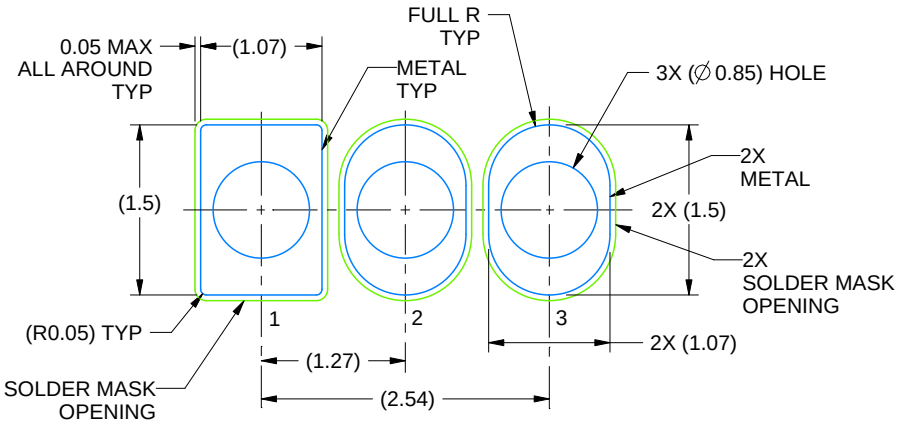
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

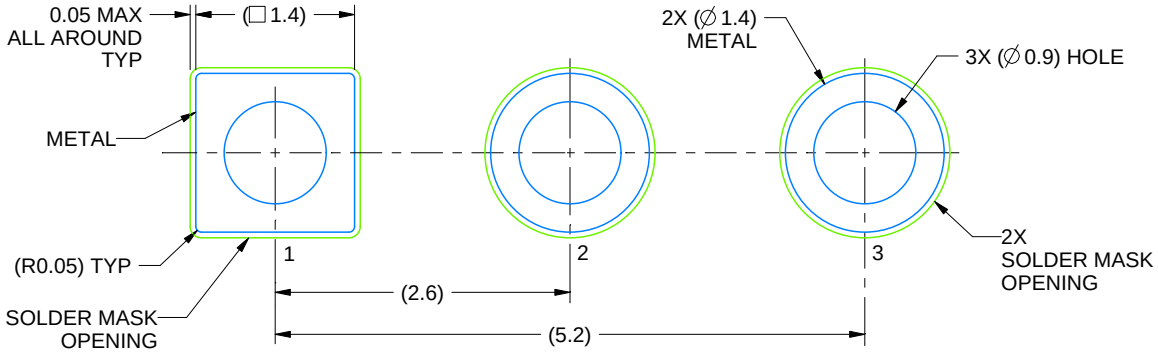


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



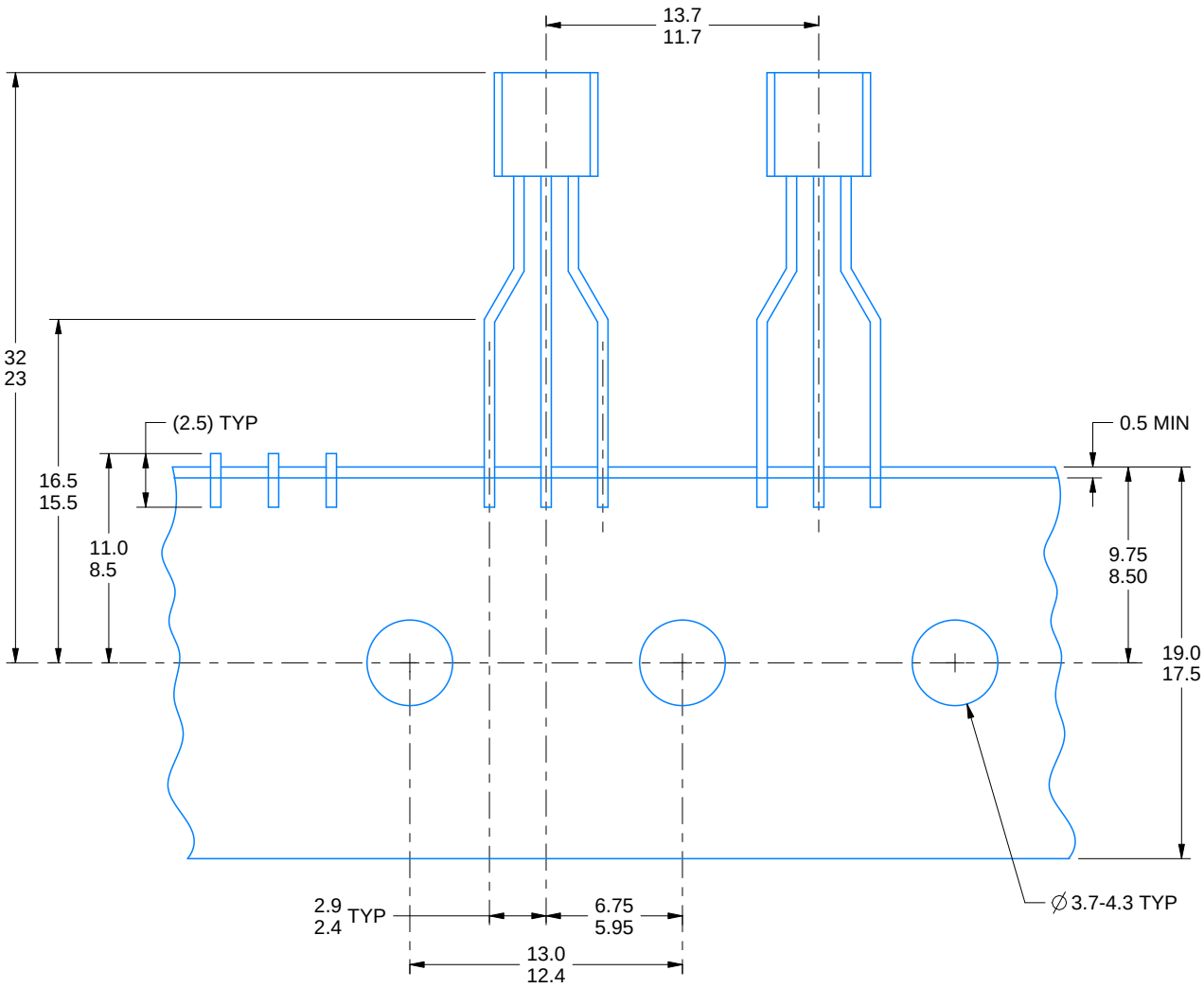
LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

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