

SN54ABT16823, SN74ABT16823 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS217C – JUNE 1992 – REVISED JANUARY 1997

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- High-Impedance State During Power Up and Power Down
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

These 18-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The 'ABT16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ($\overline{\text{CLKEN}}$) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high disables the clock buffer, latching the outputs. Taking the clear ($\overline{\text{CLR}}$) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{\text{OE}}$) input can be used to place the nine outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{\text{OE}}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54ABT16823 . . . WD PACKAGE
SN74ABT16823 . . . DGG OR DL PACKAGE
(TOP VIEW)

$\overline{\text{CLR}}$	1	56	1CLK
$\overline{\text{OE}}$	2	55	1CLKEN
1Q1	3	54	1D1
GND	4	53	GND
1Q2	5	52	1D2
1Q3	6	51	1D3
V_{CC}	7	50	V_{CC}
1Q4	8	49	1D4
1Q5	9	48	1D5
1Q6	10	47	1D6
GND	11	46	GND
1Q7	12	45	1D7
1Q8	13	44	1D8
1Q9	14	43	1D9
2Q1	15	42	2D1
2Q2	16	41	2D2
2Q3	17	40	2D3
GND	18	39	GND
2Q4	19	38	2D4
2Q5	20	37	2D5
2Q6	21	36	2D6
V_{CC}	22	35	V_{CC}
2Q7	23	34	2D7
2Q8	24	33	2D8
GND	25	32	GND
2Q9	26	31	2D9
$\overline{\text{OE}}$	27	30	2CLKEN
2CLR	28	29	2CLK



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**TEXAS
INSTRUMENTS**

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SN54ABT16823, SN74ABT16823

18-BIT BUS-INTERFACE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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description (continued)

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54ABT16823 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16823 is characterized for operation from -40°C to 85°C .

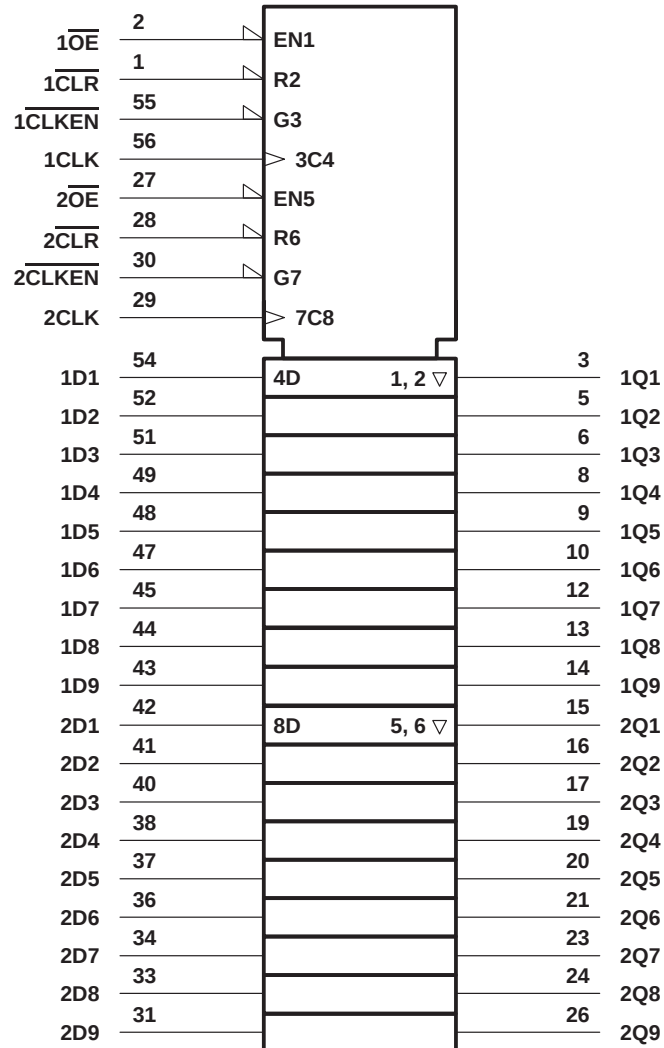
FUNCTION TABLE
(each 9-bit flip-flop)

INPUTS					OUTPUT Q
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	
L	L	X	X	X	L
L	H	L	$\uparrow$	H	H
L	H	L	$\uparrow$	L	L
L	H	L	L	X	Q_0
L	H	H	X	X	Q_0
H	X	X	X	X	Z

SN54ABT16823, SN74ABT16823
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logic symbol[†]



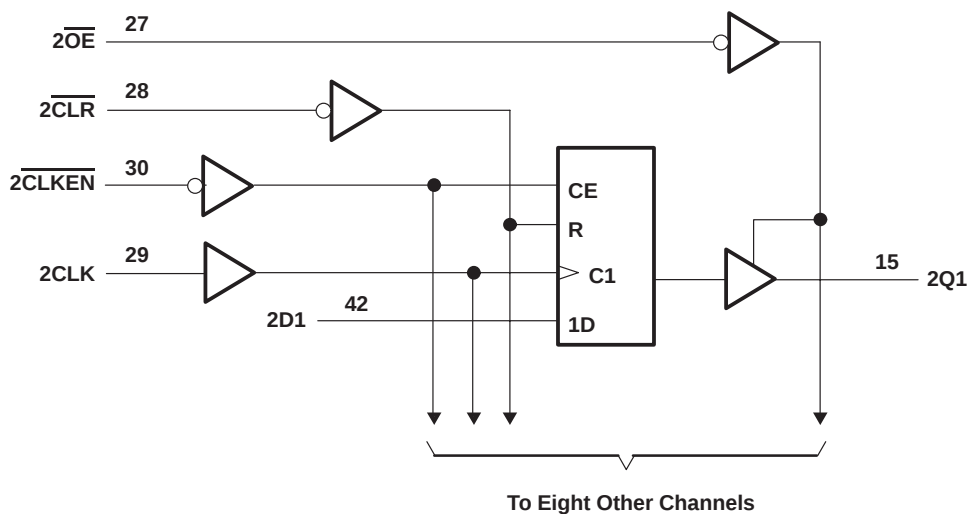
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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The diagram illustrates the internal logic of a single channel of a 10-bit counter. It features a 74163 counter with the following inputs and outputs:

- Inputs:**
 - $\overline{1OE}$ (pin 2)
 - $\overline{1CLR}$ (pin 1)
 - $\overline{1CLKEN}$ (pin 55)
 - $1CLK$ (pin 56)
 - $1D1$ (pin 54)
- Counter Outputs:**
 - CE (Carry Enable)
 - R (Reset)
 - $C1$ (Carry 1)
 - $1D$ (Data 1)
- Logic:**
 - $\overline{1OE}$ is inverted and connected to the CE input.
 - $\overline{1CLR}$ is inverted and connected to the R input.
 - $\overline{1CLKEN}$ is inverted and connected to the $1CLK$ input.
 - $1CLK$ is connected to the $1D$ input.
 - The output $1Q1$ (pin 3) is connected to the $1D$ input via a feedback loop.
 - The output $1Q1$ is also connected to the $1D1$ input.
 - The output $1Q1$ is connected to the $1D$ input via a feedback loop.
- Output:** $1Q1$ (pin 3)

A bracket at the bottom indicates that this circuit is repeated for eight other channels, totaling nine channels.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16823	96 mA
SN74ABT16823	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

			SN54ABT16823		SN74ABT16823		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT16823		SN74ABT16823		UNIT
		MIN	TYP [†]	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = –18 mA			–1.2		–1.2		–1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = –3 mA		2.5			2.5		2.5	V
	V _{CC} = 5 V, I _{OH} = –3 mA		3			3		3	
	V _{CC} = 4.5 V		2			2			
			2*					2	
V _{OL}	V _{CC} = 4.5 V			0.55		0.55			V
				0.55*				0.55	
V _{hys}			100						mV
I _I	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
I _{OZPU}	V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I _{OZPD}	V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I _{OZH}	V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V			10**		50		10	μA
I _{OZL}	V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2$ V			–10**		–50		–10	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}	Outputs high			50		50		50	μA
I _O [‡]	V _{CC} = 5.5 V, V _O = 2.5 V	–50	–100	–200	–50	–200	–50	–200	mA
I _{CC}	Outputs high			0.5		0.5		0.5	mA
	Outputs low			80		80		80	
	Outputs disabled			0.5		0.5		0.5	
ΔI _{CC} [§]	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA
C _i	V _I = 2.5 V or 0.5 V		3.5						pF
C _O	V _O = 2.5 V or 0.5 V		7.5						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

** These limits apply only to the SN74ABT16823.

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		SN54ABT16823		SN74ABT16823		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration	$\overline{\text{CLR}}$ low	3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		
t_{su}	Setup time before CLK $\uparrow$	$\overline{\text{CLR}}$ inactive	1.6		2		1.6		ns
		Data	1.7		1.7		1.7		
		CLKEN low	2.8		2.8		2.8		
t_h	Hold time after CLK $\uparrow$	Data	1.2		1.2		1.2		ns
		CLKEN low	0.6		0.6		0.6		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16823					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f _{max}			150			150		MHz
t _{PLH}	CLK	Q	1.6	3.9	5.5	1.6	7.7	ns
t _{PHL}			2.1	3.9	5.4	2.1	6.4	
t _{PHL}	$\overline{\text{CLR}}$	Q	1.9	4.1	5.3	1.9	6.3	ns
t _{PZH}	$\overline{\text{OE}}$	Q	1	3.1	4.2	1	5.1	ns
t _{PZL}			1.5	3.5	4.6	1.5	5.7	
t _{PHZ}	$\overline{\text{OE}}$	Q	2.2	4.3	6	2.2	6.8	ns
t _{PLZ}			1.6	4.3	6.4	1.6	9.9	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16823					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f _{max}			150			150		MHz
t _{PLH}	CLK	Q	1.6	3.9	5.5	1.6	6.8	ns
t _{PHL}			2.1	3.9	5.4	2.1	6	
t _{PHL}	$\overline{\text{CLR}}$	Q	1.9	4.1	5.3	1.9	6.1	ns
t _{PZH}	$\overline{\text{OE}}$	Q	1	3.1	4.2	1	4.9	ns
t _{PZL}			1.5	3.5	4.6	1.5	5.5	
t _{PHZ}	$\overline{\text{OE}}$	Q	2.2	4.3	5.6	2.2	6.1	ns
t _{PLZ}			1.6	4.3	6.4	1.6	8.7	



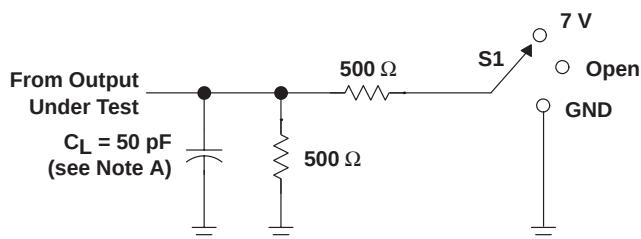
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18-BIT BUS-INTERFACE FLIP-FLOPS

WITH 3-STATE OUTPUTS

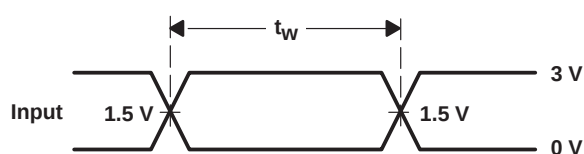
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PARAMETER MEASUREMENT INFORMATION

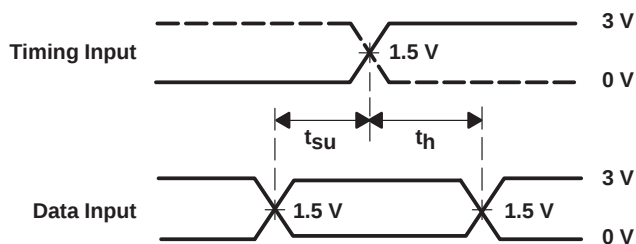


LOAD CIRCUIT

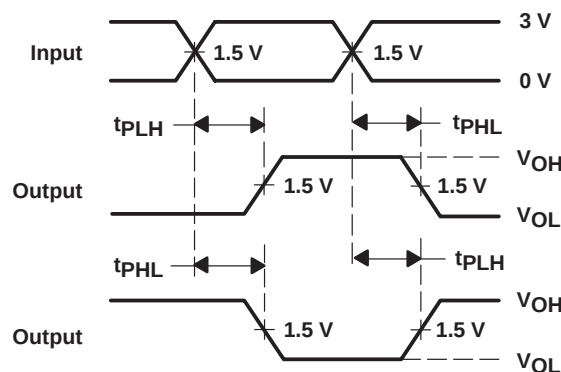
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



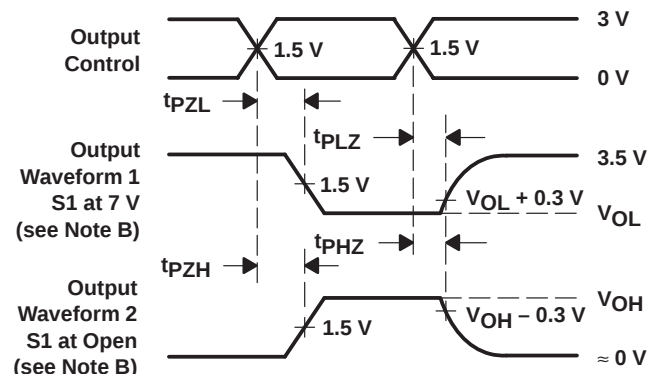
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT16823DGGR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16823	Samples
SN74ABT16823DGVR	ACTIVE	TVSOP	DGV	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AH823	Samples
SN74ABT16823DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16823	Samples
SN74ABT16823DLG4	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16823	Samples
SN74ABT16823DLR	ACTIVE	SSOP	DL	56	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16823	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

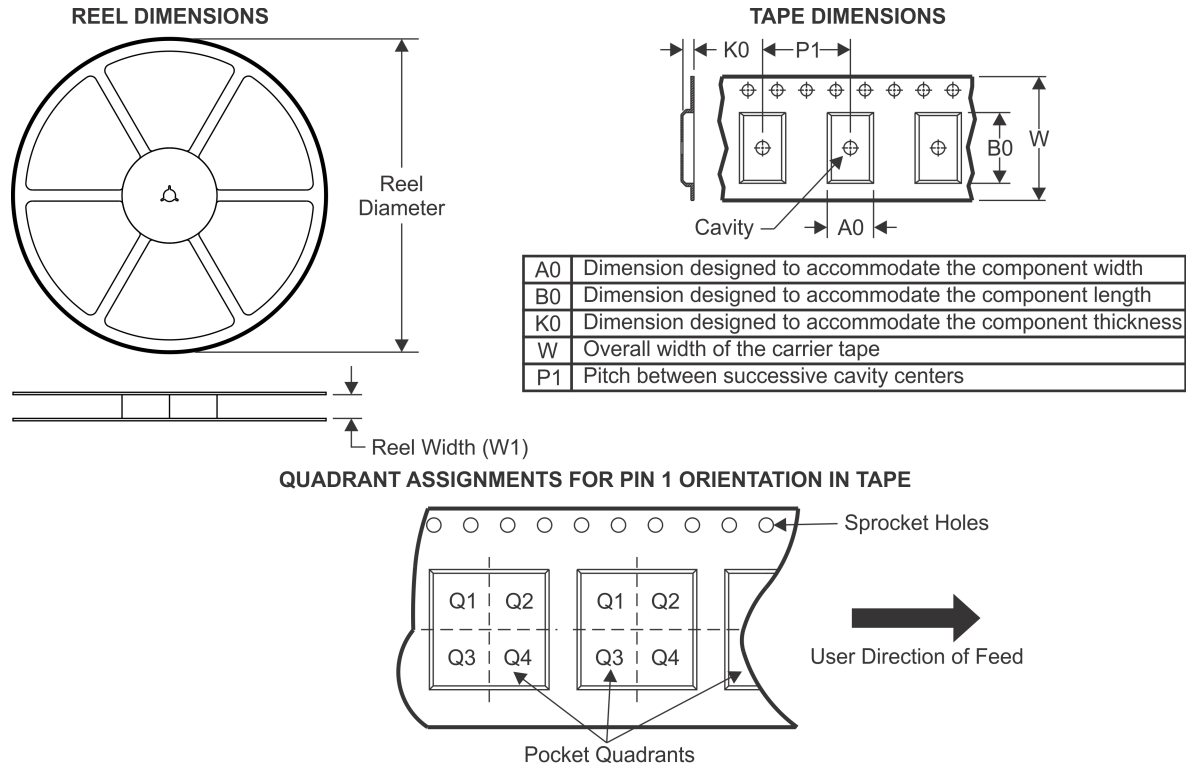
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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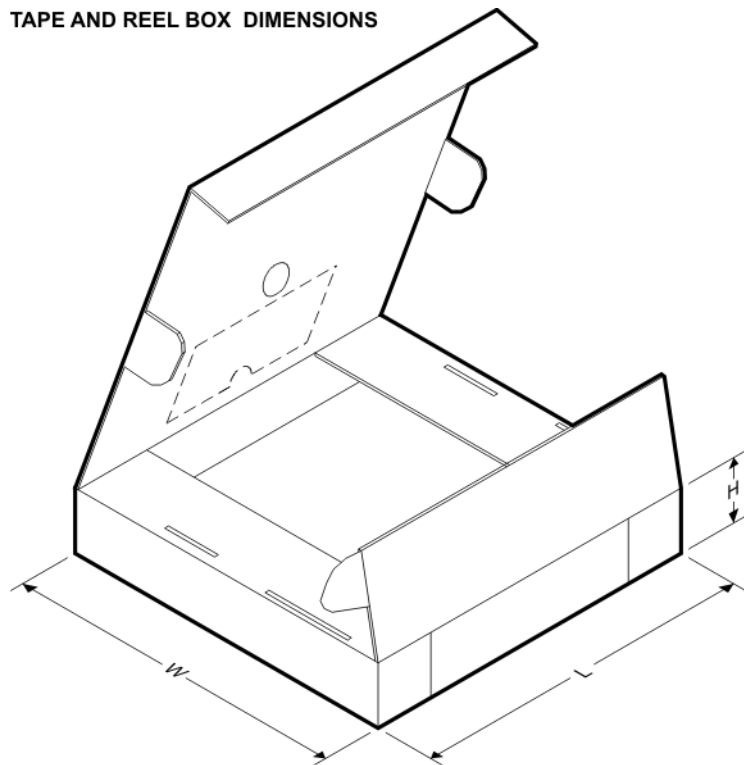
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16823DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ABT16823DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74ABT16823DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

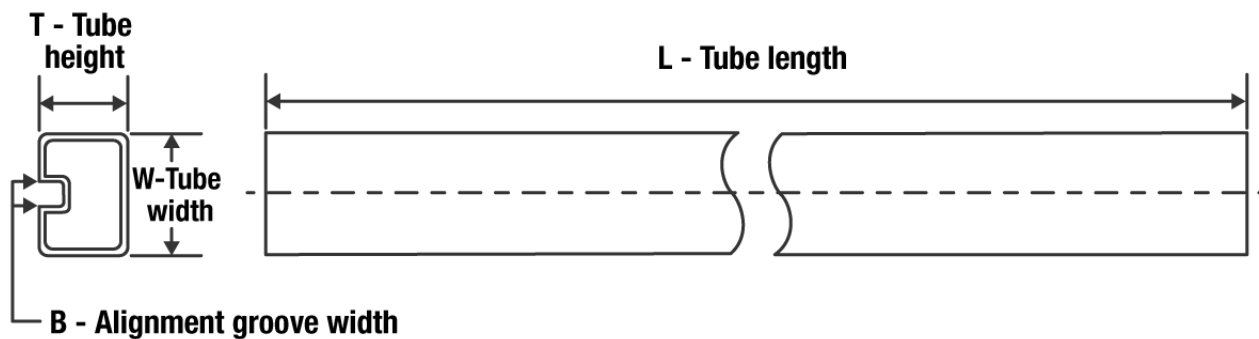
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16823DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74ABT16823DGVR	TVSOP	DGV	56	2000	367.0	367.0	45.0
SN74ABT16823DLR	SSOP	DL	56	1000	367.0	367.0	55.0

TUBE



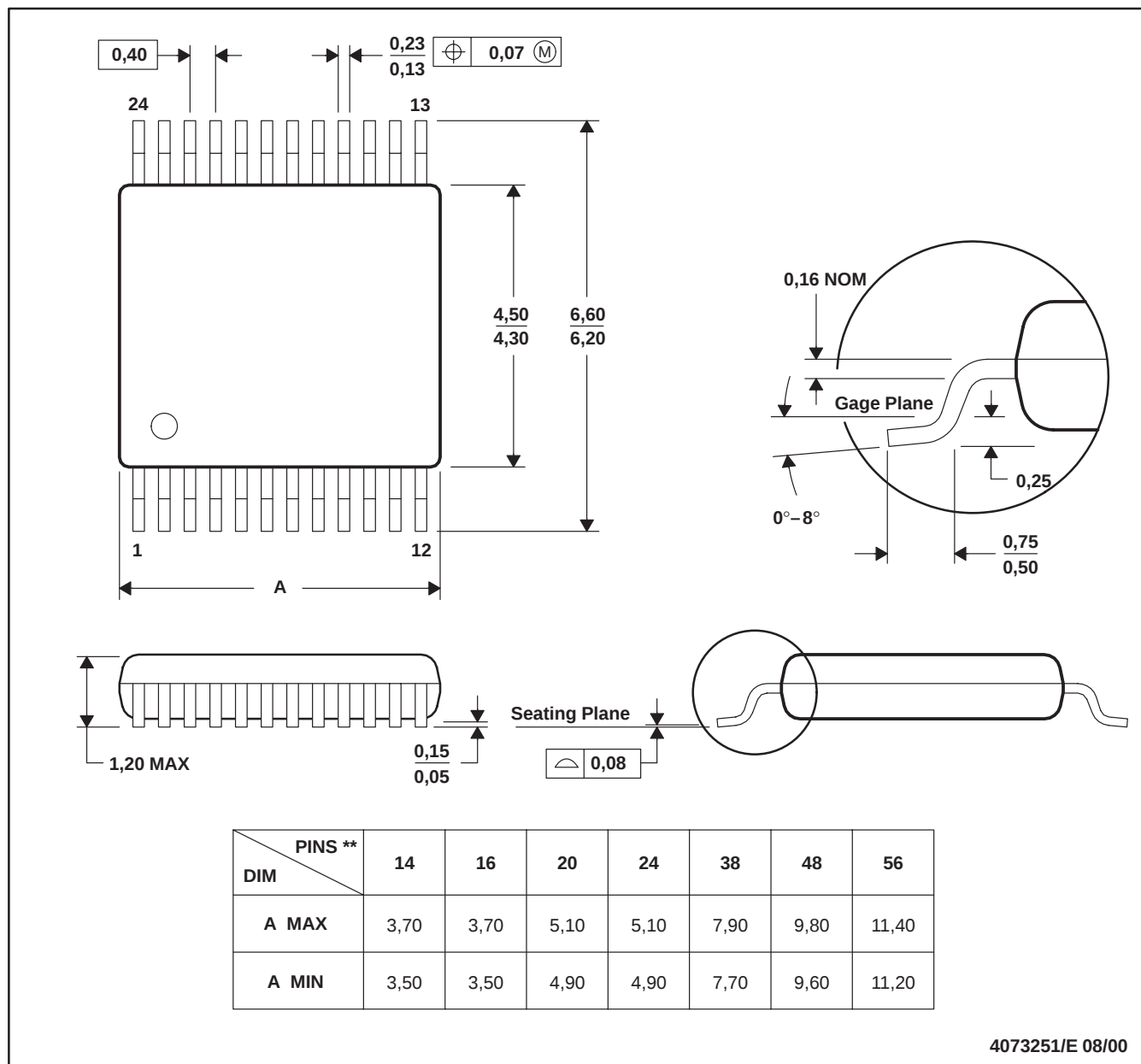
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT16823DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ABT16823DLG4	DL	SSOP	56	20	473.7	14.24	5110	7.87

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

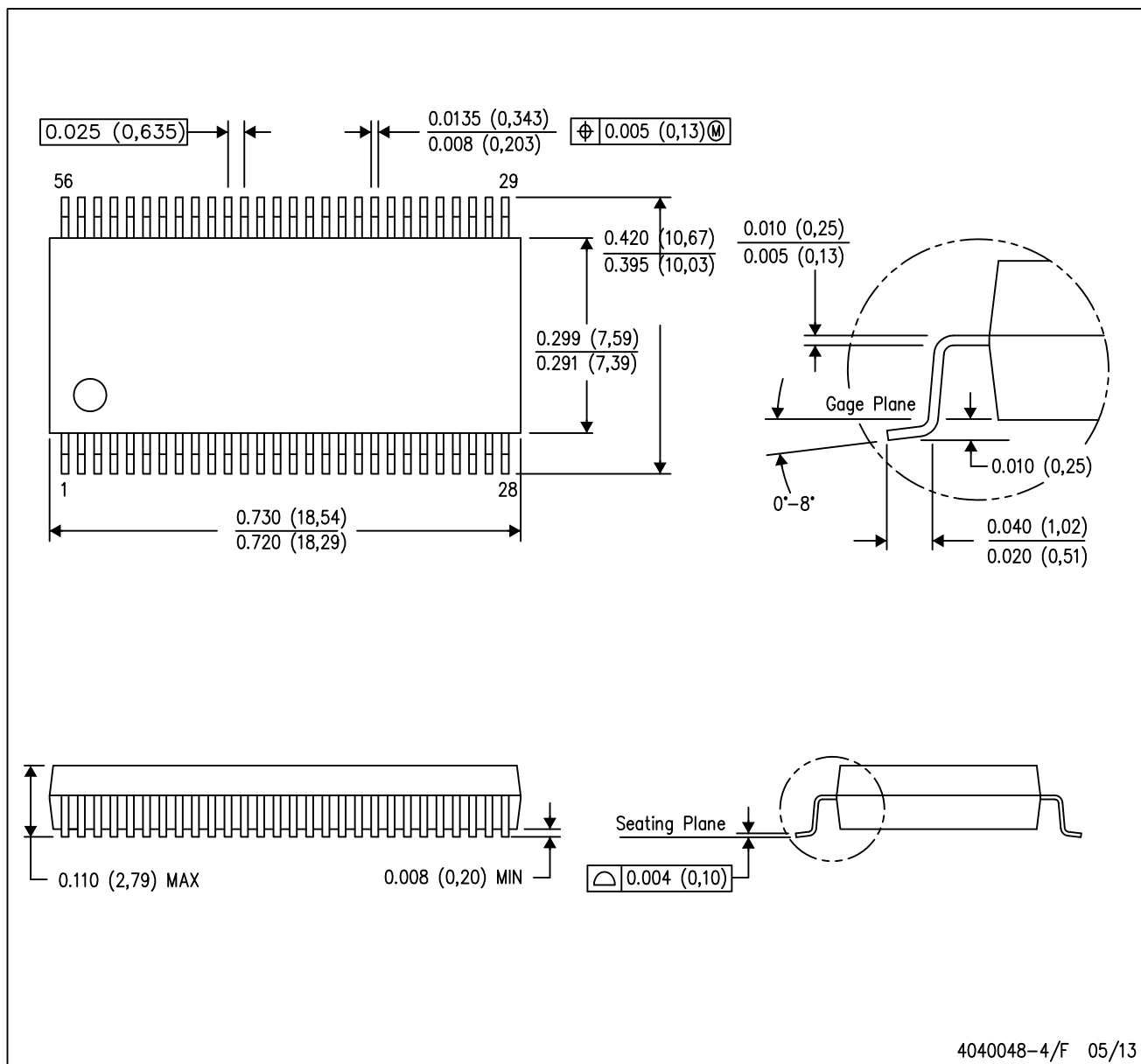
24 PINS SHOWN



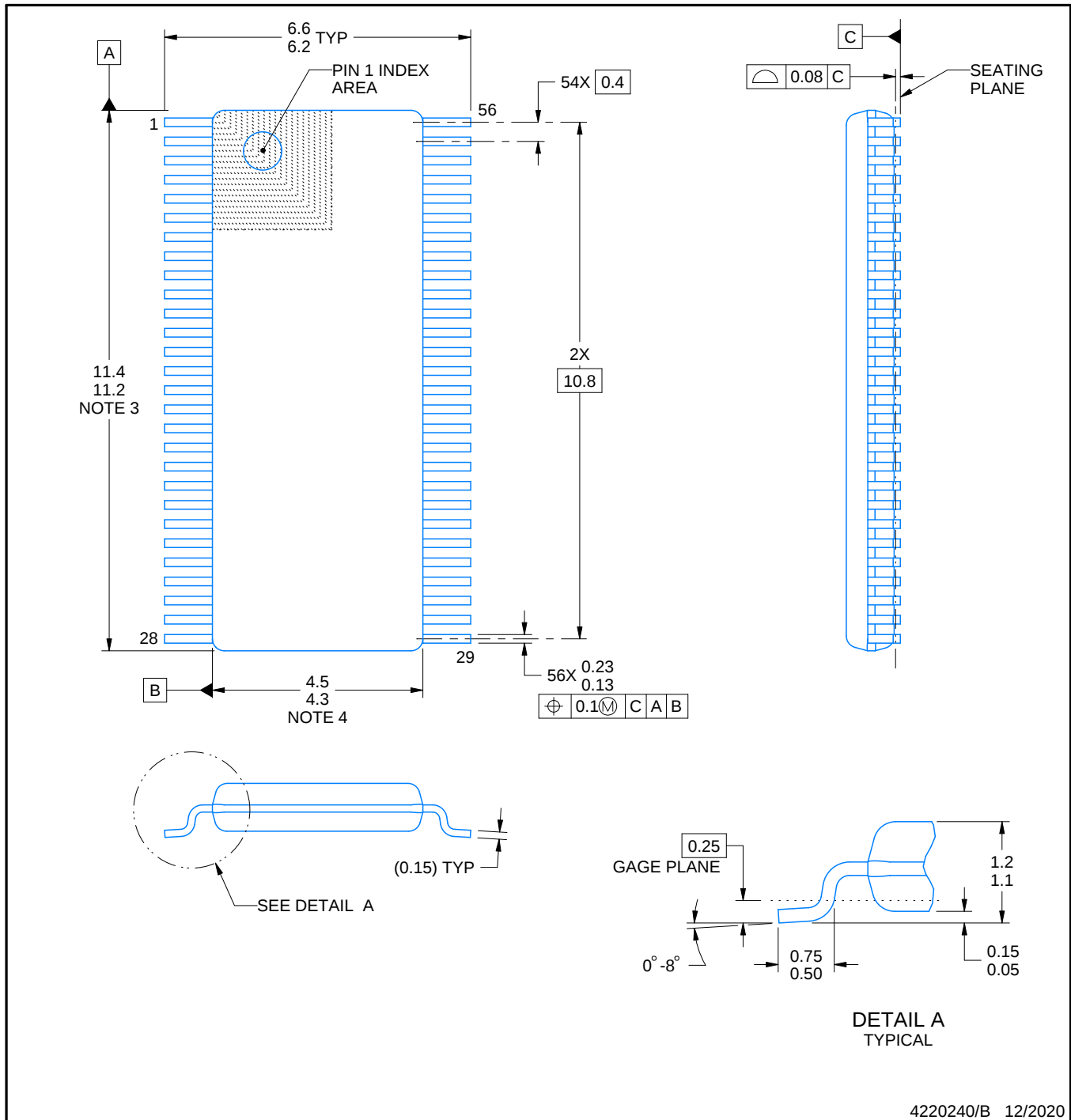
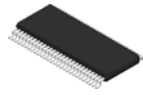
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118



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NOTES:

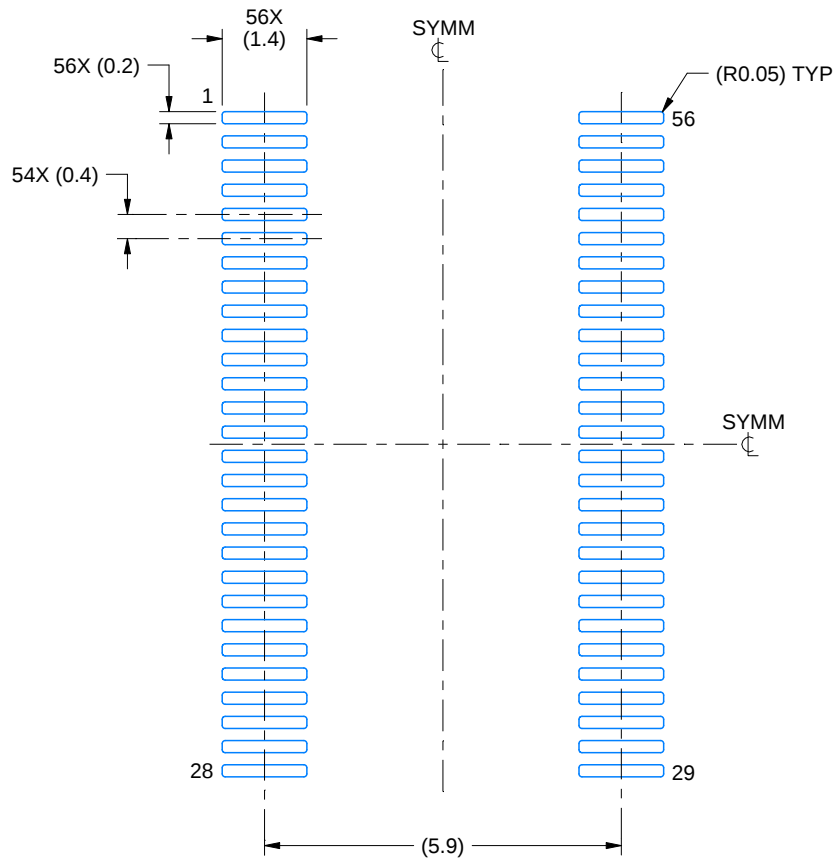
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-194.

EXAMPLE BOARD LAYOUT

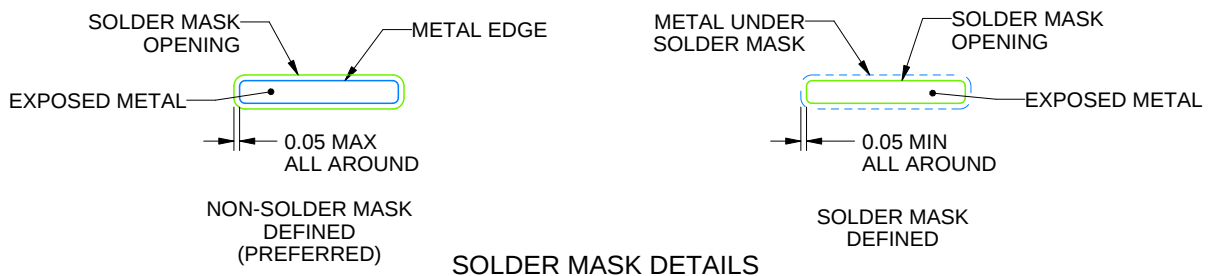
DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

4220240/B 12/2020

NOTES: (continued)

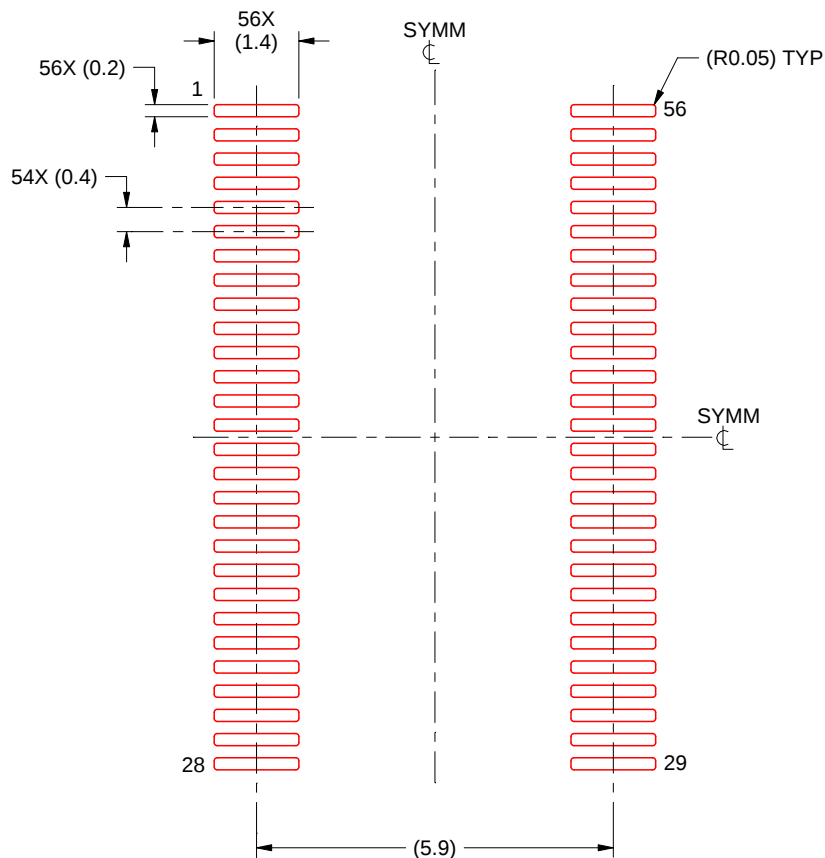
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

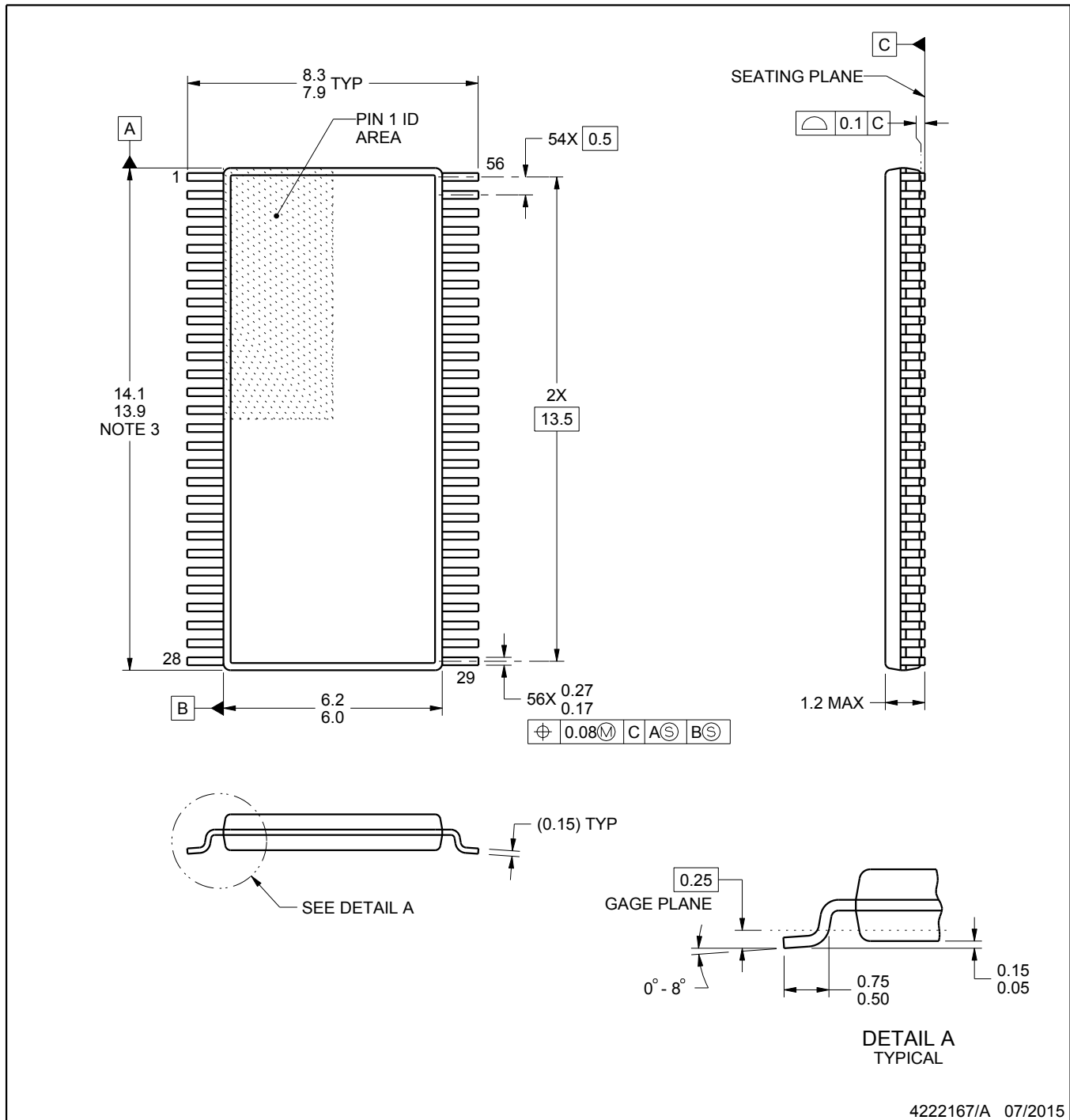


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4220240/B 12/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4222167/A 07/2015

NOTES:

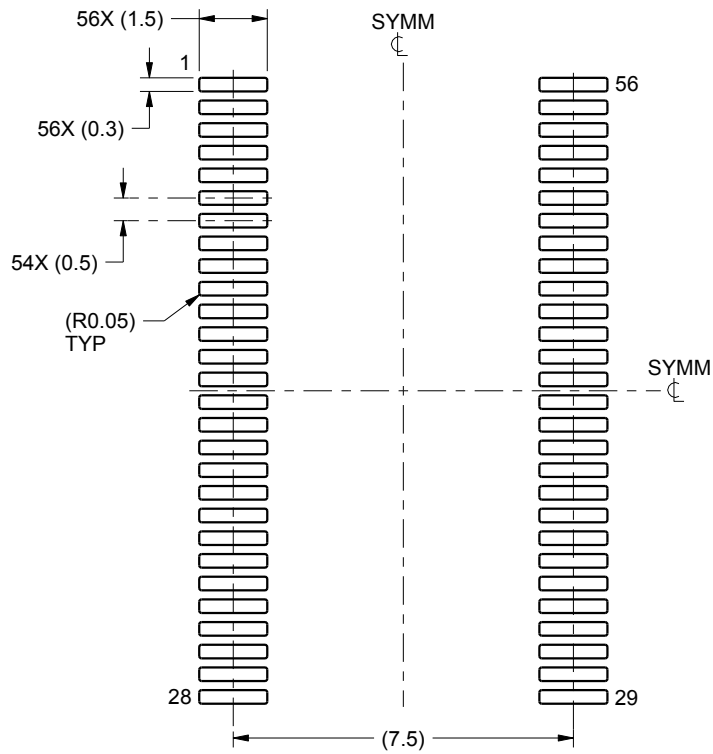
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

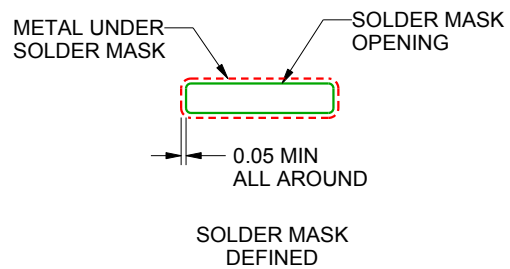
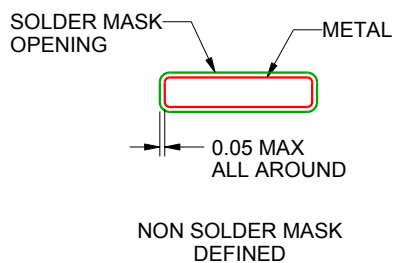
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

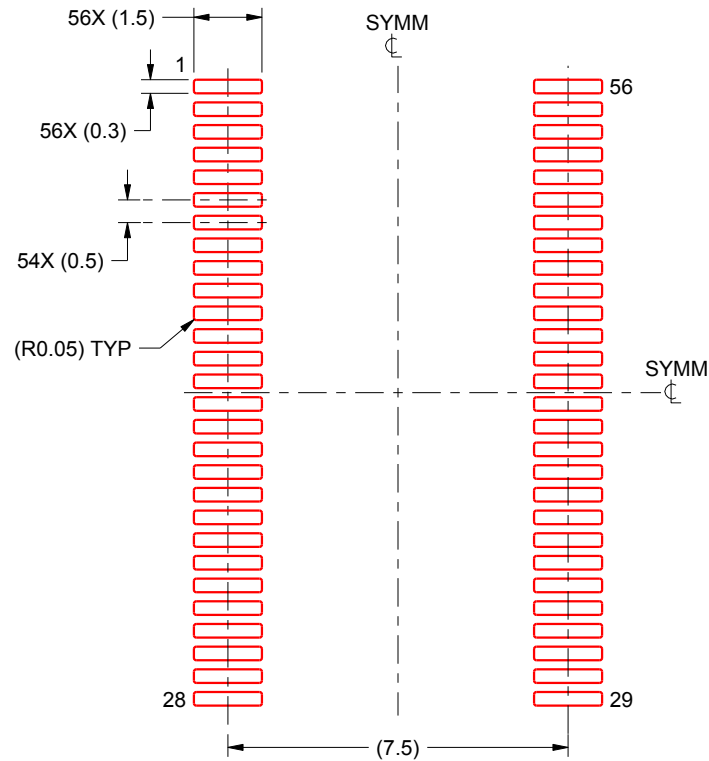
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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