具有使能功能的 TPS709-Q1 150mA、30V、1μA I_Q 稳压器

1 特性

- 符合汽车应用 标准
- 具有符合 AEC Q100 标准的下列结果：
  - 器件温度等级 1：环境工作温度范围为 –40°C 至 125°C
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 2
  - 器件 CDM ESD 分类等级 C4B
- 输入电压范围：2.7V 至 30V
- 超低 I_Q：1μA
- 反向电流保护
- 低 $I_{SHUTDOWN}$：150nA
- 支持 200mA 峰值输出
- 在温度范围内精度为 2%
- 可提供固定输出电压：1.2V 至 6.5V
- 热关断及过流保护
- 封装：小外形尺寸晶体管 (SOT)-23-5 封装、晶圆级小外形无引线 (WSON)

2 应用

- 汽车
- 信息娱乐系统
- 车身控制模块
- 导航系统
- 微控制器备用电源

3 说明

TPS709-Q1 系列线性稳压器是针对功耗敏感型应用设计的超低静态电流 器件。一个精密带隙和误差放大器在温度范围内的精度为 2%。只有 1μA 的静态电流使得此器件成为由电池供电、要求非常小闲置状态功率耗散的常开系统的理想解决方案。为了增加安全性，这些器件还具有热关断、电流限制和反向电流保护功能。

通过将 EN 引脚拉为低电平，可将该系列稳压器置于关断模式。这个模式的关断电流低至 150nA（典型值）。

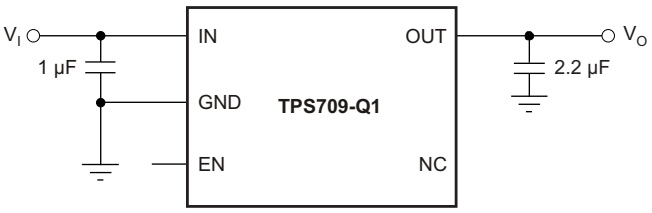
TPS709-Q1 系列可提供 WSON-6 和 SOT-23-5 封装。

器件信息(1)

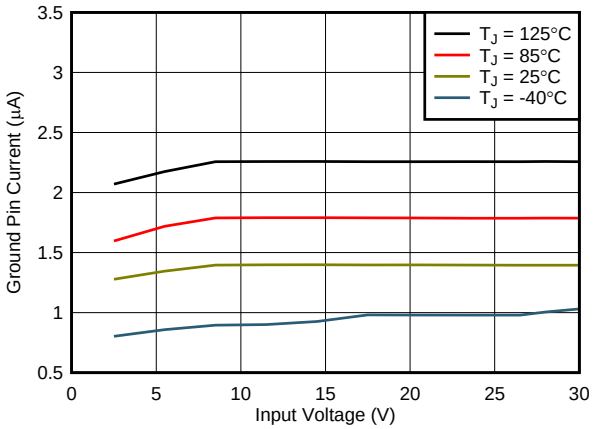
器件型号	封装	封装尺寸（标称值）
TPS709-Q1	SOT-23 (5)	2.90mm × 1.60mm
	WSON (6)	2.00mm x 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路



接地电流与 V_{IN} 和温度间的关系



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (March 2015) to Revision C — **Page**

- Changed from: Dropout Voltage (V) to: Dropout Voltage (mV) in Figure 8, Figure 9, and Figure 10 ... 7
- Deleted last sentence from *Shutdown* section ... 14
- Changed text From: "input supply range of 2.7 V to 6.5 V:" To: " input supply range of 2.7 V to 30 V." in the *Power Supply Recommendations* section ... 18

Changes from Revision A (December 2013) to Revision B — **Page**

- 在文档中增加了 DRV 封装、*ESD 额定值*、*建议运行条件*、*时序要求* 表、*概述*、*器件功能模式*、*典型应用*、*器件和文档支持* 以及*机械、封装和可订购信息* 部分 ... 1
- 更改了*应用信息*、*特性* *说明*、*电源建议* 和*布局* 部分 ... 1
- 已删除*低压降* 特性 要点 ... 1
- 更改了*应用*部分 ... 1
- 更改了*说明*部分的最后一句 ... 1
- 添加了器件信息表 ... 1
- 添加了首页曲线 ... 1
- Added DRV package drawing to *Pin Configuration and Functions* section ... 4
- Changed *Pin Functions* table: added DRV and I/O columns, added Thermal pad row, and changed EN pin description ... 4
- Changed *Recommended Operating Conditions* table ... 5
- Added DRV column to *Thermal Information* table ... 5
- Changed *Electrical Characteristics* conditions ... 6
- Changed V_{OUT}, I_{CL}, I_{SHDN}, and I_{REV} symbols in *Electrical Characteristics* table ... 6
- Changed $V_{EN(HI)}$ parameter into $V_{EN(HI)}$ and $V_{EN(LO)}$ parameters in *Electrical Characteristics* table ... 6
- Changed T_A parameter to T_J in *Electrical Characteristics* table ... 6
- Changed *Typical Characteristics* section ... 7
- Changed junction temperature values in first paragraph of *Thermal Protection* section ... 15
- Changed 6.3-V to 10-V in second sentence of *Detailed Design Procedure* section ... 18

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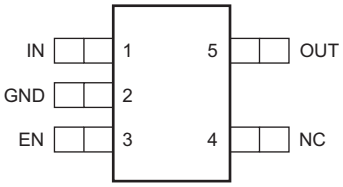
Changes from Original (December 2013) to Revision A **Page**

- 已发布至生产 1

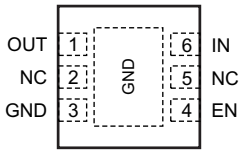
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5 Pin Configuration and Functions

DBV Package
SOT-23-5
(Top View)



DRV Package
WSON-6
(Top View)



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO. DRV	NO. DBV		
EN	4	3	I	Enable pin. Driving this pin high enables the device. Driving this pin low puts the device into low current shutdown. This pin can be left floating to enable the device. The maximum voltage must remain below 6.5 V.
GND	3	2	—	Ground
IN	6	1	I	Unregulated input to the device
NC	2, 5	4	—	No internal connection
OUT	1	5	O	Regulated output voltage. Connect a small 2.2-µF or greater ceramic capacitor from this pin to ground to assure stability.
Thermal pad		—	—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

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6 Specifications

6.1 Absolute Maximum Ratings

specified at T_J = –40°C to 125°C, unless otherwise noted; all voltages are with respect to GND(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	32	V
	V_{EN}	–0.3	7	V
	V_{OUT}	–0.3	7	V
Maximum output current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Junction temperature, T_J		–55	150	°C
Ambient temperature, T_A		–40	125	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		30	V
V_{OUT}	Output voltage	1.2		6.5	V
I_{OUT}	Output current	0		150	mA
V_{EN}	Enable voltage	0		6.5	V
C_{IN}	Input capacitor		1		µF
C_{OUT}	Output capacitor	2	2.2	47	µF
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS709-Q1		UNIT
		DBV (SOT-23)	DRV (WSON)	
		5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.9	73.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	127.4	97.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.4	42.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.8	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.4	42.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	12.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

At –40°C ≤ T_J, T_A ≤ 125°C, V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = 2 V, and C_{IN} = C_{OUT} = 2.2-µF ceramic, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2.7		30	V
V_{OUT}	Output voltage range		1.2		6.5	V
V_{OUT}	DC output accuracy	V_{OUT} < 3.3 V	–2%		2%	
		V_{OUT} ≥ 3.3 V	–1%		1%	
ΔV_{OUT}	Line regulation	($V_{OUT(nom)}$ + 1 V, 2.7 V) ≤ V_{IN} ≤ 30 V		3	10	mV
	Load regulation	V_{IN} = $V_{OUT(nom)}$ + 1.5 V or 3 V (whichever is greater), 100 µA ≤ I_{OUT} ≤ 150 mA		20	50	mV
V_{DO}	Dropout voltage(1)(2)	TPS70933-Q1, I_{OUT} = 50 mA		295	650	mV
		TPS70933-Q1, I_{OUT} = 150 mA		975	1540	
		TPS70950-Q1, I_{OUT} = 50 mA		245	500	
		TPS70950-Q1, I_{OUT} = 150 mA		690	1200	
I_{CL}	Output current limit(3)	V_{OUT} = 0.9 × $V_{OUT(nom)}$	200	320	500	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA, V_{OUT} ≤ 3.3 V		1.3	2.55	µA
		I_{OUT} = 0 mA, V_{OUT} > 3.3 V		1.4	2.7	
		I_{OUT} = 100 µA, V_{IN} = 30 V		6.7	10	
		I_{OUT} = 150 mA		350		
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.4 V, V_{IN} = 2.7 V		150		nA
PSRR	Power-supply rejection ratio	f = 10 Hz		80		dB
		f = 100 Hz		62		
		f = 1 kHz		52		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, I_{OUT} = 10 mA, V_{IN} = 2.7 V, V_{OUT} = 1.2 V		190		μV_{RMS}
$V_{EN(HI)}$	Enable pin high (enabled)		0.9			V
$V_{EN(LO)}$	Enable pin high (disabled)		0		0.4	V
I_{EN}	Enable pin current	EN = 1.0 V, V_{IN} = 5.5 V		300		nA
I_{REV}	Reverse current (flowing out of IN pin)	V_{OUT} = 3 V, V_{IN} = V_{EN} = 0 V		10		nA
	Reverse current (flowing into OUT pin)	V_{OUT} = 3 V, V_{IN} = V_{EN} = 0 V		100		nA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		158		°C
		Reset, temperature decreasing		140		
T_J	Operating junction temperature		–40		125	°C

(1) V_{DO} is measured with V_{IN} = 0.98 × $V_{OUT(nom)}$.
(2) Dropout is only valid when V_{OUT} ≥ 2.8 V because of the minimum input voltage limits.
(3) Measured with V_{IN} = V_{OUT} + 3 V for V_{OUT} ≤ 2.5 V. Measured with V_{IN} = V_{OUT} + 2.5 V for V_{OUT} > 2.5 V.

6.6 Timing Requirements

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), R_L = 47 Ω, V_{EN} = 2 V, and C_{IN} = C_{OUT} = 2.2-µF ceramic, unless otherwise noted. Typical values are at T_J = 25°C.

			MIN	NOM	MAX	UNIT
t_{STR}	Start-up time(1)	$V_{OUT(nom)}$ ≤ 3.3 V		200	600	µs
		$V_{OUT(nom)}$ > 3.3 V		500	1500	µs

(1) Startup time = time from EN assertion to 0.95 × $V_{OUT(nom)}$ and load = 47 Ω.

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6.7 Typical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.

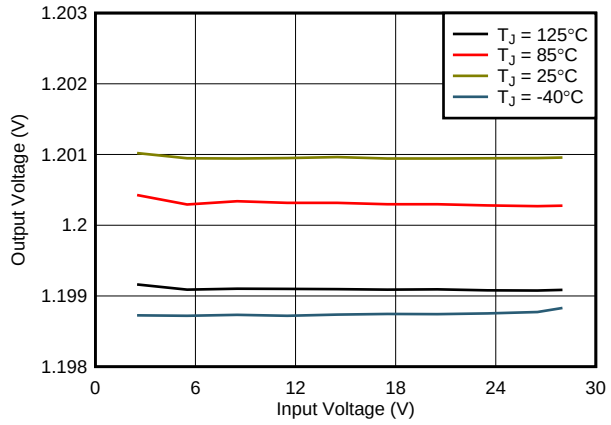


Figure 1. 1.2-V Line Regulation vs V_{IN} and Temperature

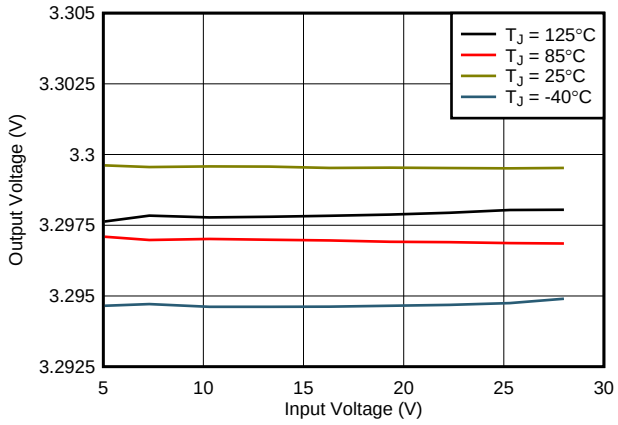


Figure 2. 3.3-V Line Regulation vs V_{IN} and Temperature

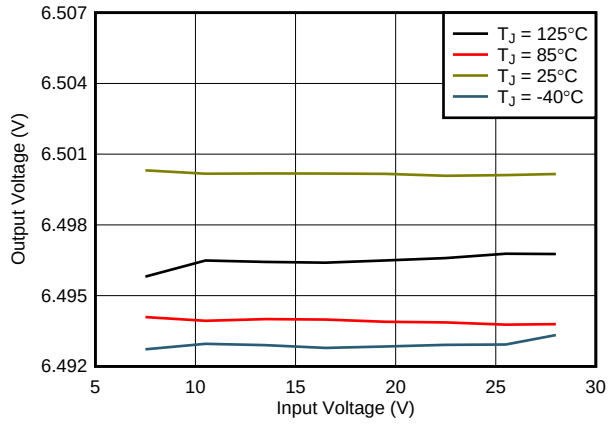


Figure 3. 6.5-V Line Regulation vs V_{IN} and Temperature

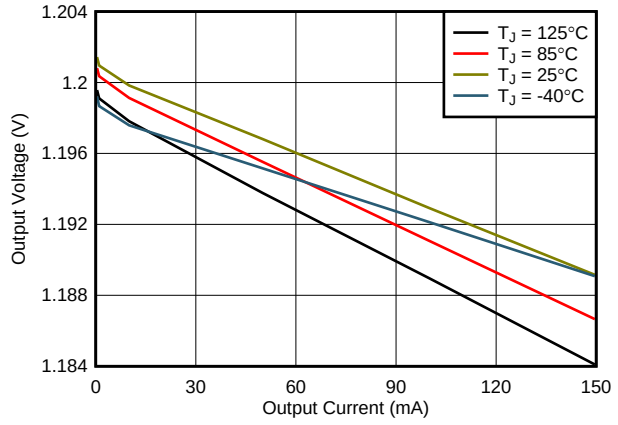


Figure 4. 1.2-V Load Regulation vs I_{OUT} and Temperature

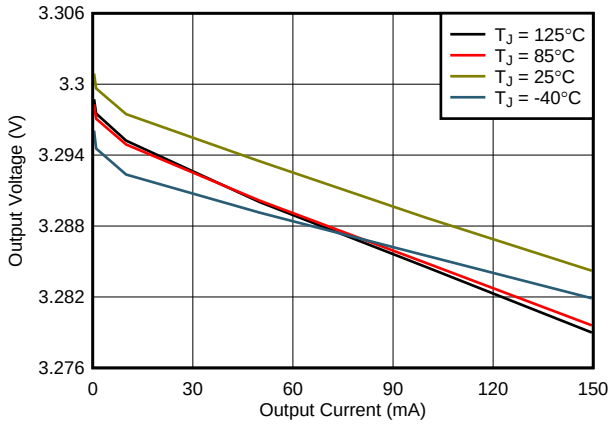


Figure 5. 3.3-V Load Regulation vs I_{OUT} and Temperature

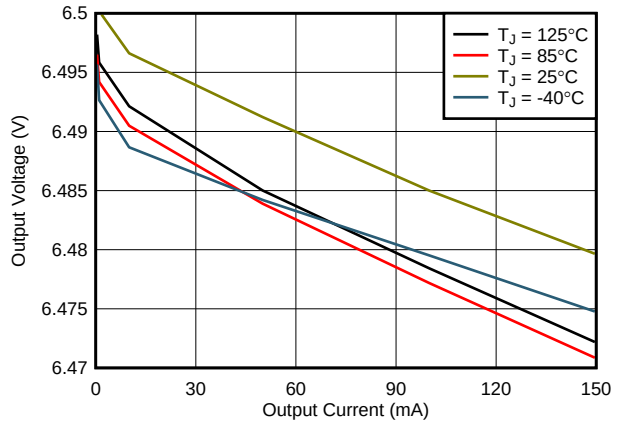


Figure 6. 6.5-V Load Regulation vs I_{OUT} and Temperature

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Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.

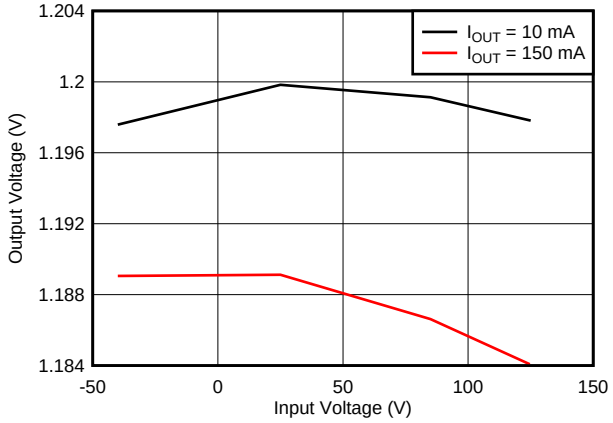


Figure 7. 1.2-V Output Voltage vs Temperature

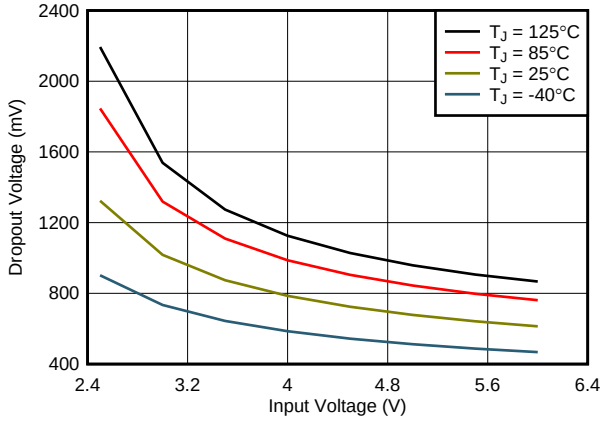


Figure 8. 6.5-V Dropout Voltage vs V_{IN} and Temperature

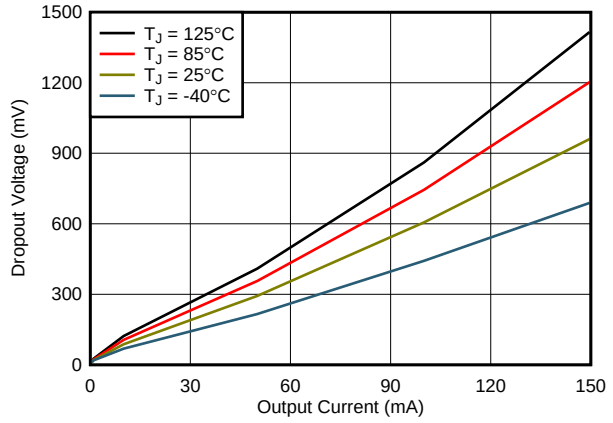


Figure 9. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

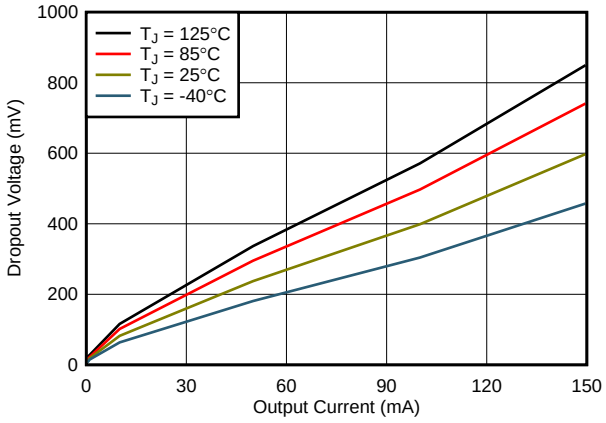


Figure 10. Dropout Voltage vs I_{OUT} and Temperature

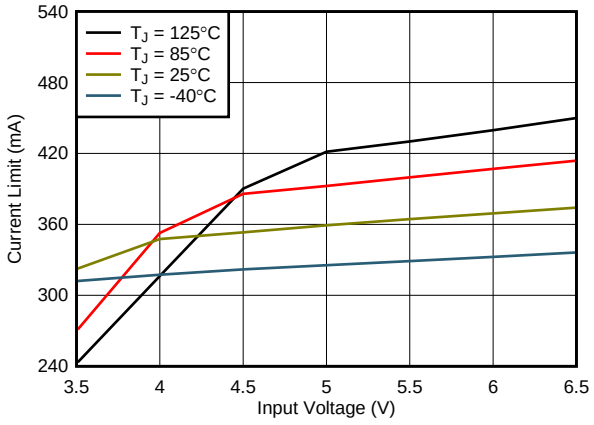


Figure 11. 1.2-V Current Limit vs V_{IN} and Temperature

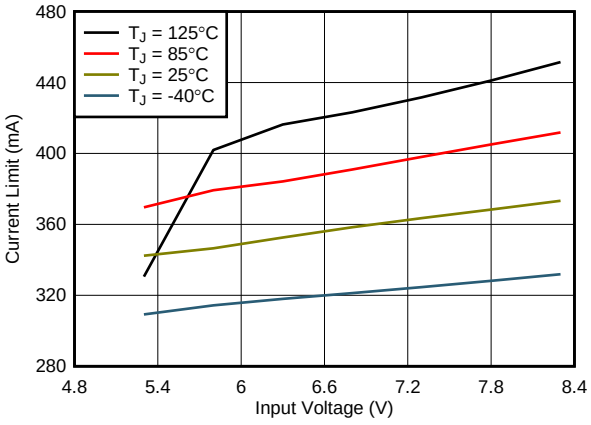


Figure 12. 3.3-V Current Limit vs V_{IN} and Temperature

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Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.

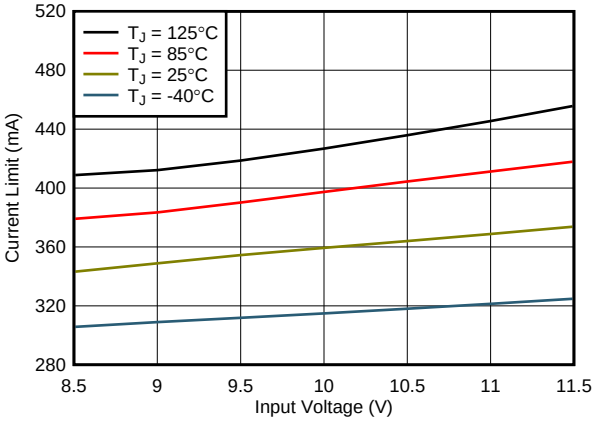


Figure 13. 6.5-V Current Limit vs V_{IN} and Temperature

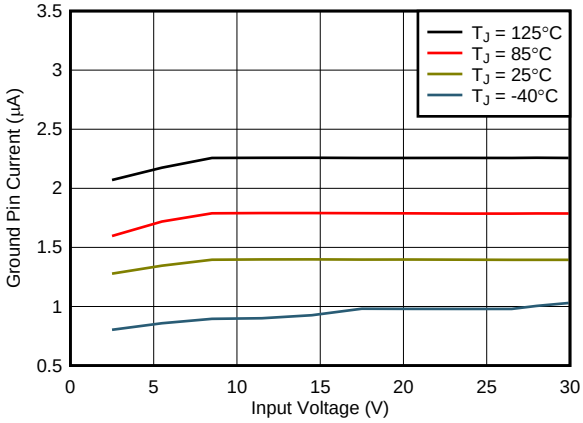


Figure 14. 1.2-V Ground Pin Current vs V_{IN} and Temperature

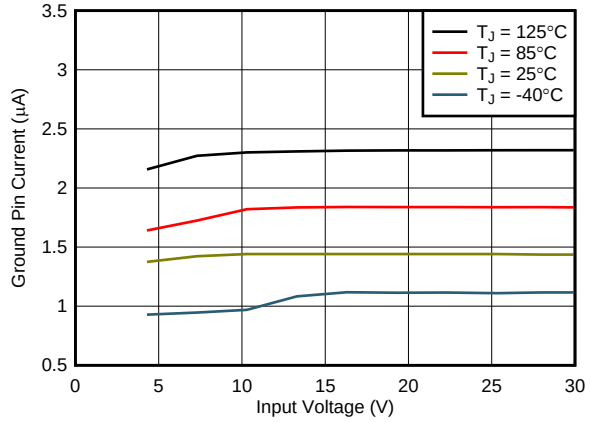


Figure 15. 3.3-V Ground Pin Current vs V_{IN} and Temperature

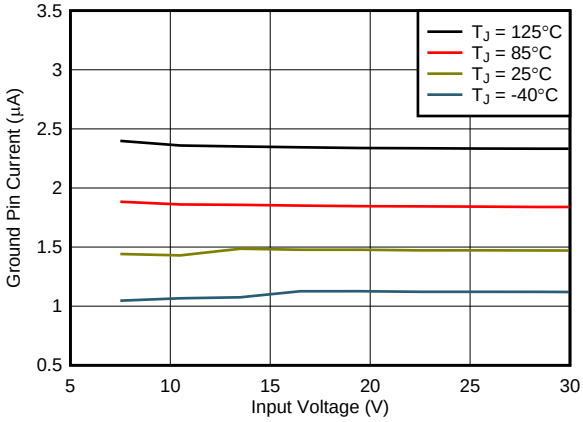


Figure 16. 6.5-V Ground Pin Current vs V_{IN} and Temperature

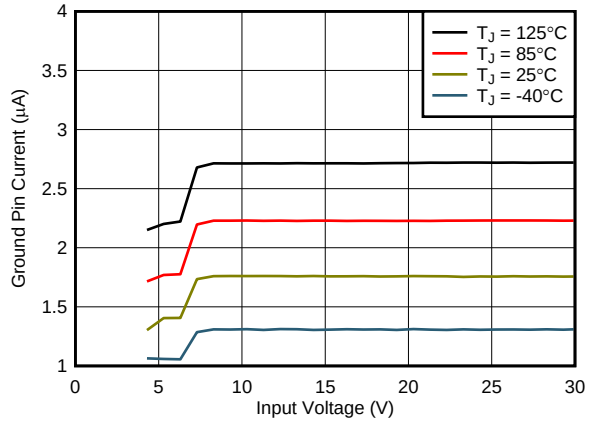


Figure 17. 3.3-V Ground Current vs V_{IN} and Temperature with EN Floating

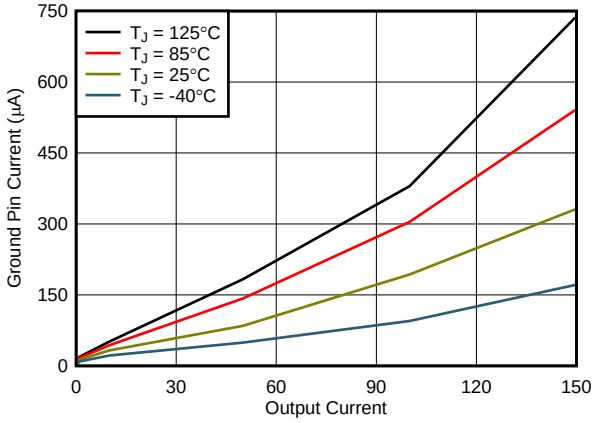


Figure 18. 1.2-V Ground Pin Current vs I_{OUT} and Temperature

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Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.

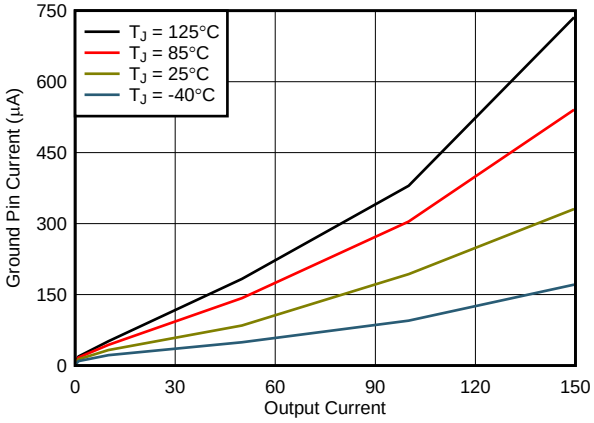


Figure 19. 3.3-V Ground Pin Current vs I_{OUT} and Temperature

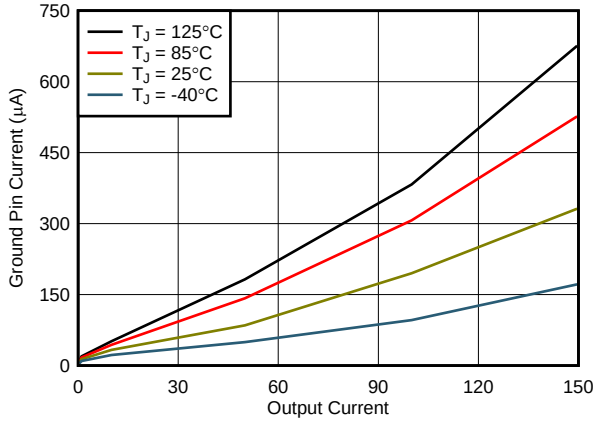


Figure 20. 6.5-V Ground Pin Current vs I_{OUT} and Temperature

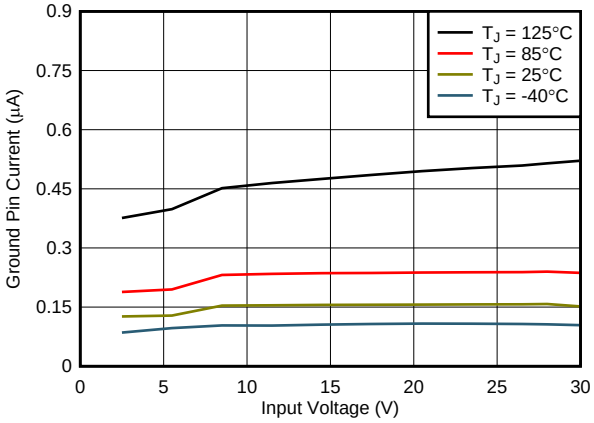


Figure 21. 1.2-V Shutdown Current vs V_{IN} and Temperature

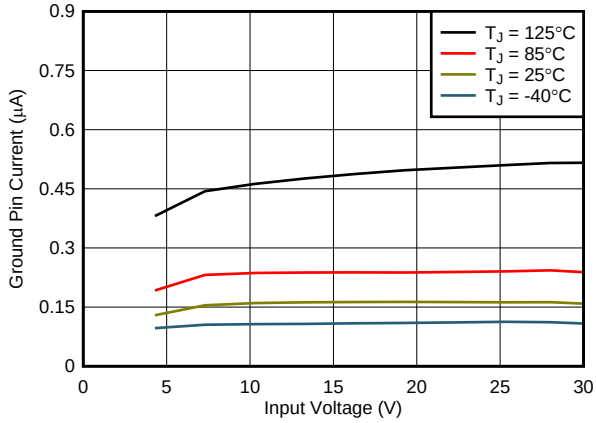


Figure 22. 3.3-V Shutdown Current vs V_{IN} and Temperature

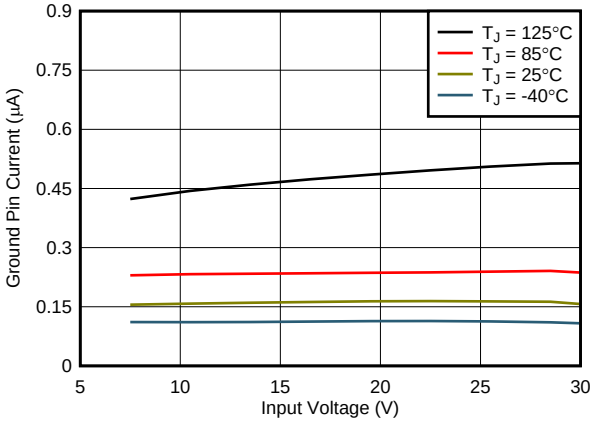


Figure 23. 6.5-V Shutdown Current vs V_{IN} and Temperature

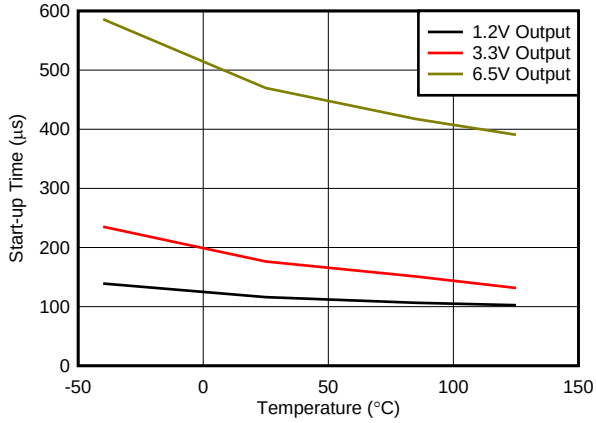


Figure 24. Start-Up Time vs Temperature

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Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.

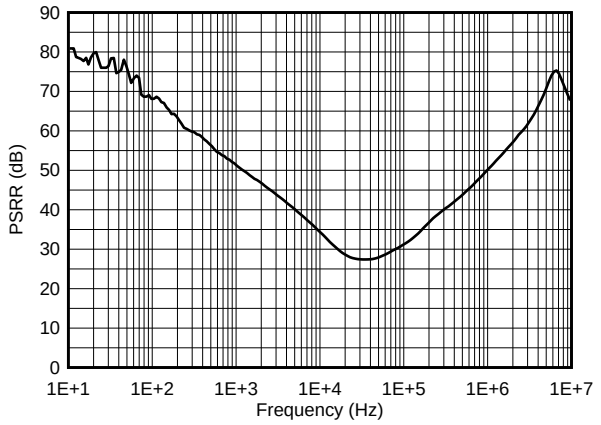


Figure 25. Power-Supply Rejection Ratio vs Frequency

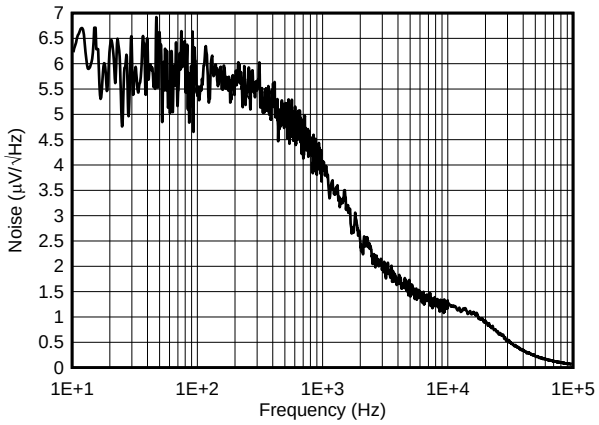
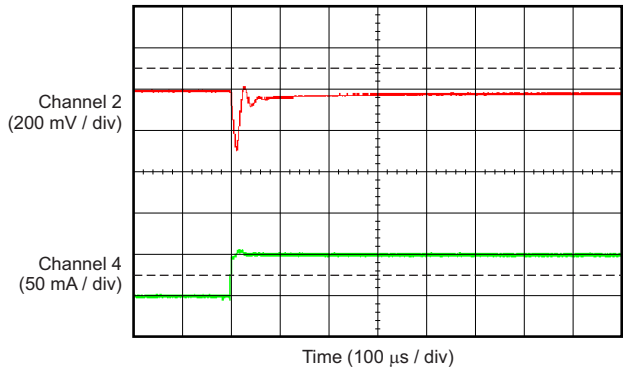
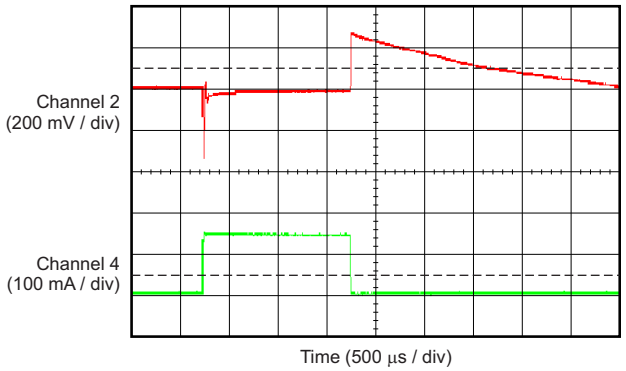


Figure 26. Noise



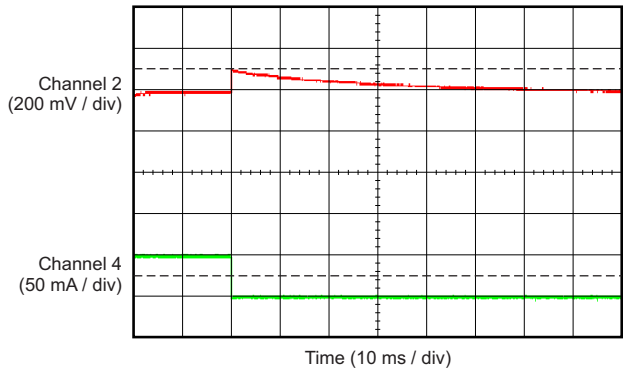
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 2.7 V

Figure 27. TPS70912-Q1 Load Transient (0 mA to 50 mA)



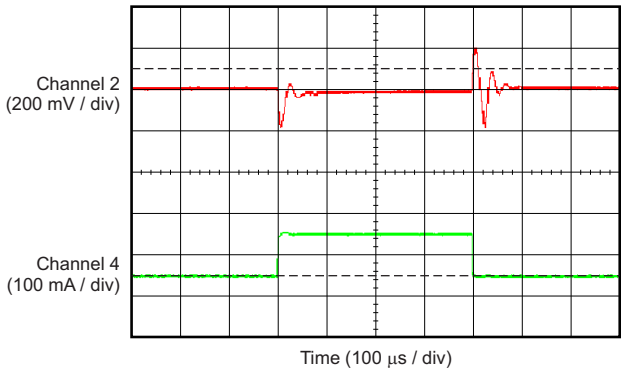
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 2.7 V

Figure 28. TPS70912-Q1 Load Transient (1 mA to 150 mA)



Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 2.7 V

Figure 29. TPS70912-Q1 Load Transient (50 mA to 0 mA)



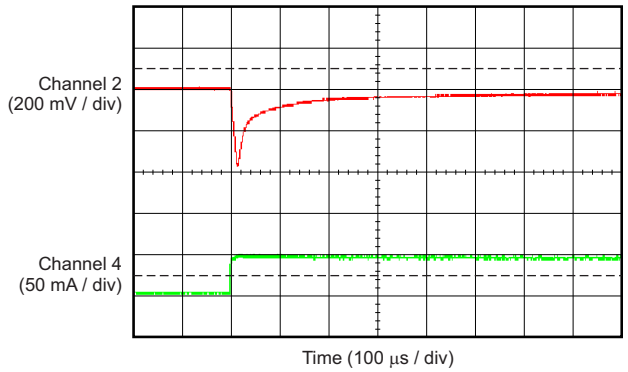
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 2.7 V

Figure 30. TPS70912-Q1 Load Transient (50 mA to 150 mA)

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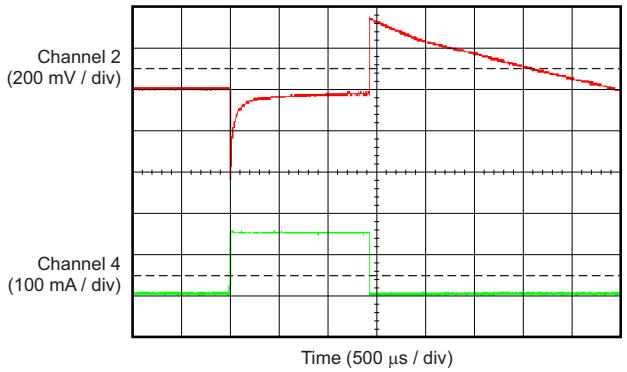
Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.



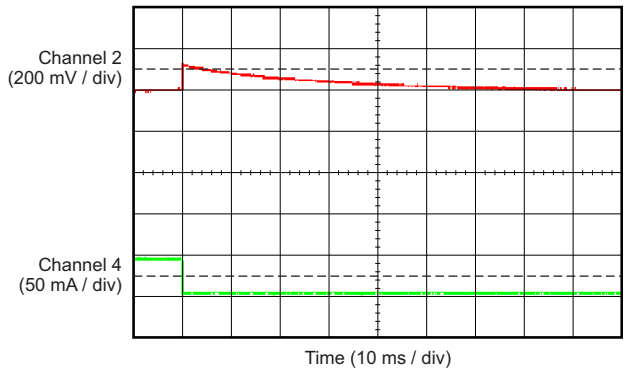
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 4.3 V

Figure 31. TPS70933-Q1 Load Transient (0 mA to 50 mA)



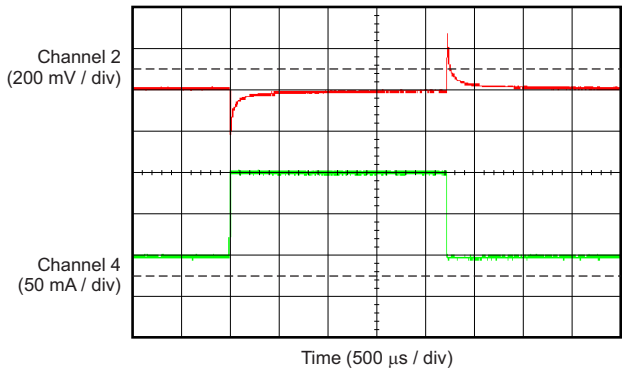
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 4.3 V

Figure 32. TPS70933-Q1 Load Transient (1 mA to 150 mA)



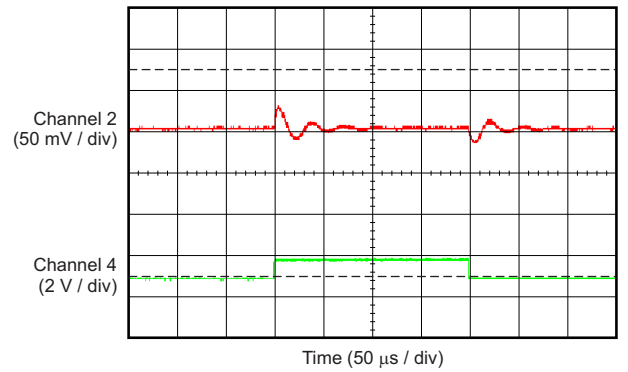
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 4.3 V

Figure 33. TPS70933-Q1 Load Transient (50 mA to 0 mA)



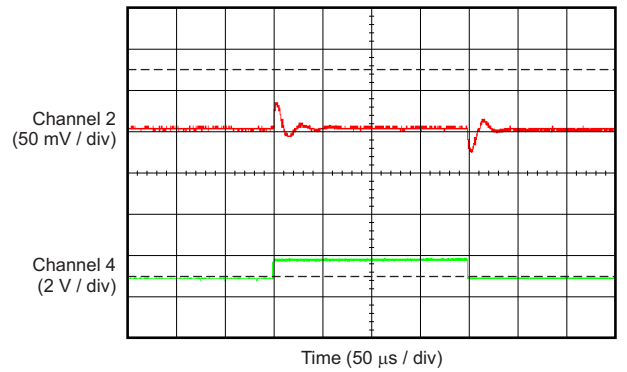
Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 4.3 V

Figure 34. TPS70933-Q1 Load Transient (50 mA to 150 mA)



Channel 2 = V_{OUT}, channel 4 = V_{IN}, I_{OUT} = 10 mA

Figure 35. TPS70912-Q1 Line Transient (2.7 V to 3.7 V)



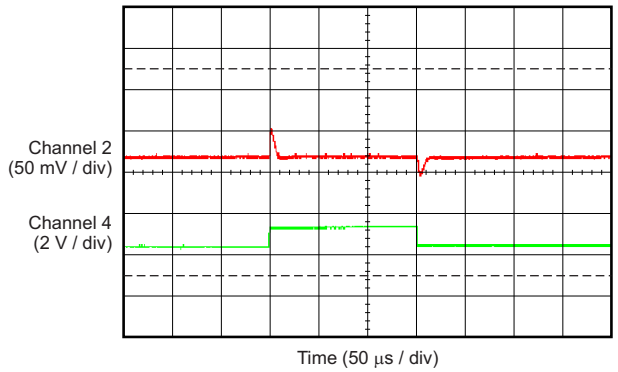
Channel 2 = V_{OUT}, channel 4 = V_{IN}, I_{OUT} = 50 mA

Figure 36. TPS70912-Q1 Line Transient (2.7 V to 3.7 V)

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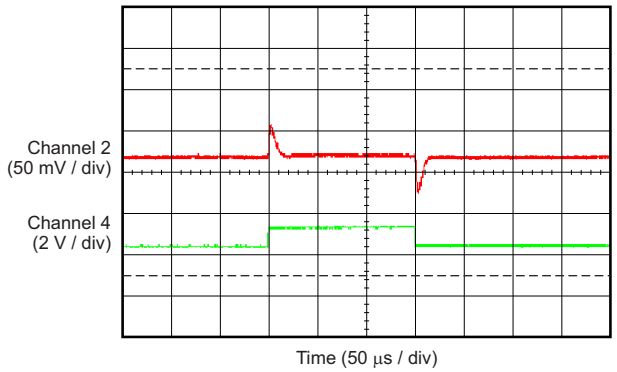
Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(nom)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = 25°C.



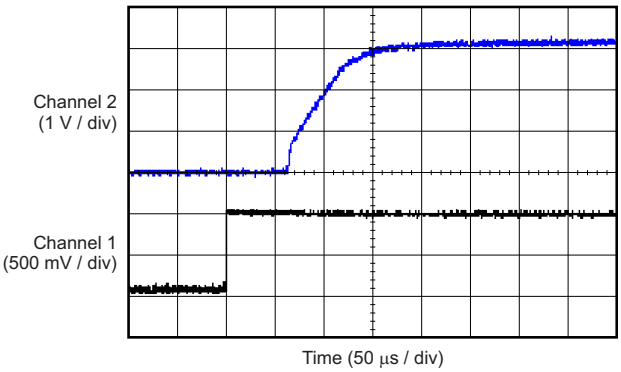
Channel 2 = V_{OUT}, channel 4 = V_{IN}, I_{OUT} = 10 mA

Figure 37. TPS70933-Q1 Line Transient (4.3 V to 5.3 V)



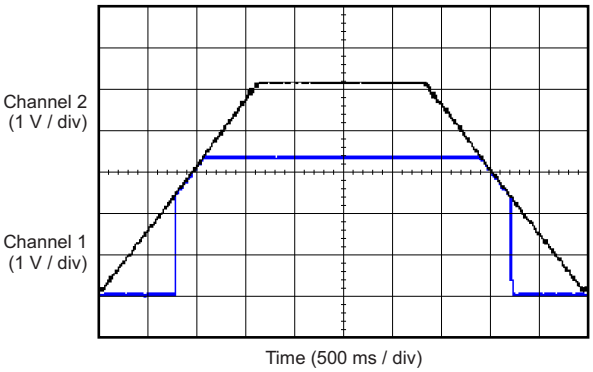
Channel 2 = V_{OUT}, channel 4 = V_{IN}, I_{OUT} = 50 mA

Figure 38. TPS70933-Q1 Line Transient (4.3 V to 5.3 V)



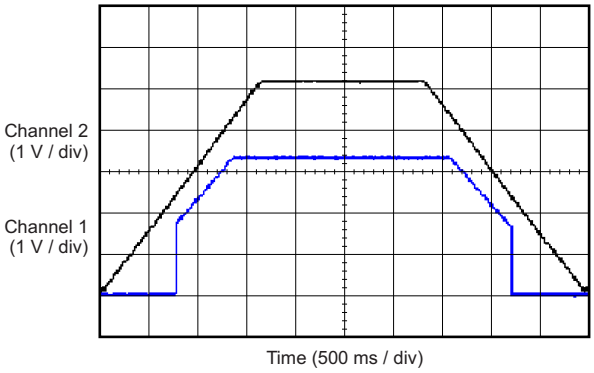
Channel 1 = EN, channel 2 = V_{OUT}, V_{IN} = 4.3 V, C_{OUT} = 2.2 µF, TPS70633

Figure 39. Power-Up with Enable



Channel 1 = V_{IN}, channel 2 = V_{OUT}, I_{OUT} = 3 mA, TPS70633

Figure 40. Power-Up and Power-Down Response



Channel 1 = V_{IN}, channel 2 = V_{OUT}, I_{OUT} = 150 mA, TPS70633

Figure 41. Power-Up and Power-Down Response

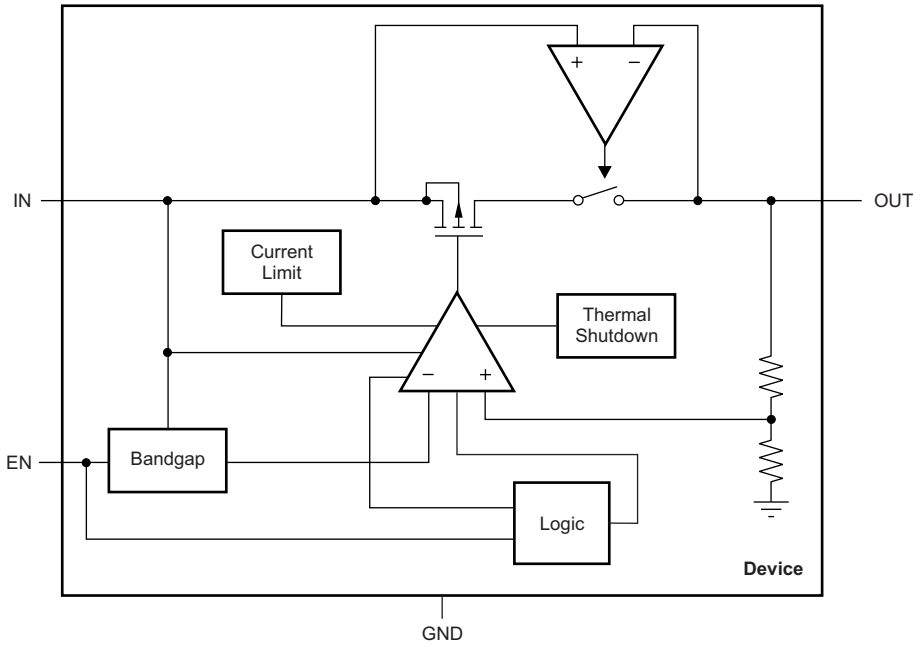
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7 Detailed Description

7.1 Overview

The TPS709-Q1 series are ultralow quiescent current, low-dropout (LDO) linear regulators. The TPS709-Q1 offers reverse current protection to block any discharge current from the output into the input. The TPS709-Q1 also features current limit and thermal shutdown for reliable operation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TPS709-Q1 uses an undervoltage lockout (UVLO) circuit to keep the output shut off until the internal circuitry operates properly.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(HI)}$ (0.9 V, minimum). Turn off the device by forcing the EN pin to drop below 0.4 V.

7.3.3 Reverse Current Protection

The TPS709-Q1 has integrated reverse current protection. Reverse current protection prevents the flow of current from the OUT pin to the IN pin when output voltage is higher than input voltage. The reverse current protection circuitry places the power path in high impedance when the output voltage is higher than the input voltage. This setting reduces leakage current from the output to the input to 10 nA, typical. The reverse current protection is always active regardless of the enable pin logic state or if the OUT pin voltage is greater than 1.8 V. Reverse current can flow if the output voltage is less than 1.8 V and if input voltage is less than the output voltage.

If voltage is applied to the input pin, then the maximum voltage that can be applied to the OUT pin is the lower of three times the nominal output voltage or 6.5 V. For example, if the 1.2-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 3.6 V. If the 3.3-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 6.5 V.

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Feature Description (continued)

7.3.4 Internal Current Limit

The TPS709-Q1 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and can be measured as ($V_{OUT} = I_{LIMIT} \times R_{LOAD}$). The PMOS pass transistor dissipates [($V_{IN} - V_{OUT}$) × I_{LIMIT}] until a thermal shutdown is triggered and the device turns off. When cool, the device is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the *Thermal Information* section for more details.

The TPS709-Q1 is characterized over the recommended operating output current range up to 150 mA. The internal current limit begins to limit the output current at a minimum of 200 mA of output current.

7.3.5 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 158°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C, maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The TPS709-Q1 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS709-Q1 into thermal shutdown degrades device reliability.

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7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{EN(low)}$	—	$T_J > 158°C$

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS709-Q1 consumes low quiescent current and delivers excellent line and load transient performance. This performance, combined with low noise and good PSRR with little (V_{IN} – V_{OUT}) headroom, makes these devices ideal for RF portable applications, current limit, and thermal protection. The TPS709-Q1 devices are specified from –40°C to 125°C.

8.1.1 Input and Output Capacitor Considerations

The TPS709-Q1 devices are stable with output capacitors with an effective capacitance of 2.0 μF or greater for output voltages below 1.5 V. For output voltages equal or greater than 1.5 V, the minimum effective capacitance for stability is 1.5 μF. The maximum capacitance for stability is 47 μF. The equivalent series resistance (ESR) of the output capacitor must be between 0 Ω and 0.2 Ω for stability.

The effective capacitance is the minimum capacitance value of a capacitor after taking into account variations resulting from tolerances, temperature, and dc bias effects. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and ESR over temperature.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-μF to 2.2-μF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR.

8.1.2 Dropout Voltage

The TPS709-Q1 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with the output current because the PMOS device functions like a resistor in dropout.

The ground pin current of many linear voltage regulators increases substantially when the device is operated in dropout. This increase in ground pin current while operating in dropout can be several orders of magnitude larger than when the device is not in dropout. The TPS709-Q1 employs a special control loop that limits the increase in ground pin current while operating in dropout. This functionality allows for the most efficient operation while in dropout conditions that can greatly increase battery run times.

8.1.3 Transient Response

As with any regulator, increasing the output capacitor size reduces over- and undershoot magnitude, but increases transient response duration.

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8.2 Typical Application

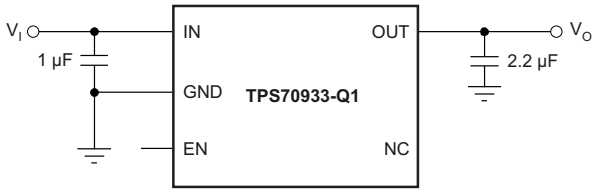


Figure 42. 3.3-V, Low-I_Q Rail

8.2.1 Design Requirements

Table 2 summarizes the design requirements for Figure 42.

Table 2. Design Requirements for a 3.3-V, Low-I_Q Rail Application

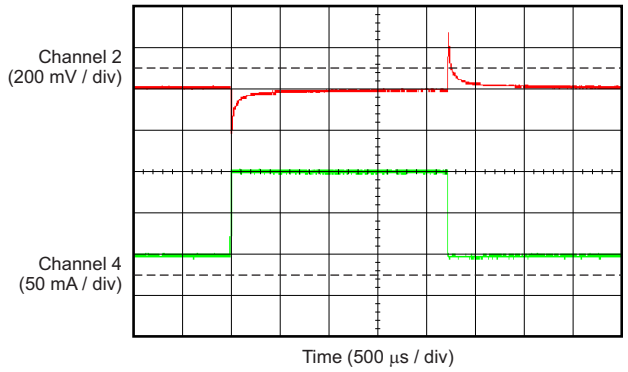
PARAMETER	DESIGN SPECIFICATION
V_{IN}	4.3 V
V_{OUT}	3.3 V
$I_{(IN)}$ (no load)	< 5 µA
I_{OUT} (max)	150 mA

8.2.2 Detailed Design Procedure

Select a 2.2-µF, 10-V X7R output capacitor to satisfy the minimum output capacitance requirement with a 3.3-V dc bias.

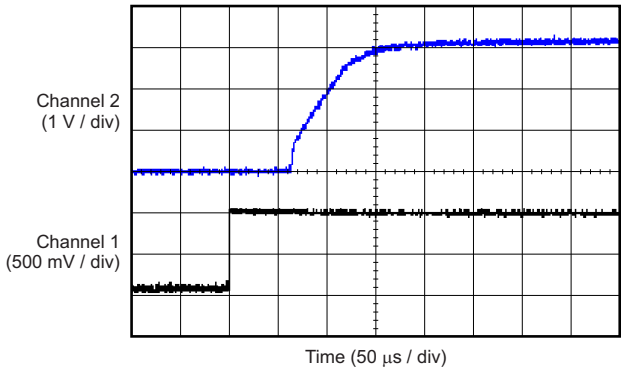
Select a 1.0-µF, 10-V X7R input capacitor to provide input noise filtering and eliminate high-frequency voltage transients.

8.2.3 Application Curves



Channel 2 = V_{OUT}, channel 4 = I_{OUT}, V_{IN} = 4.3 V

Figure 43. TPS70933-Q1 Load Transient (50 mA to 150 mA)



Channel 1 = EN, channel 2 = V_{OUT}, V_{IN} = 4.3 V, C_{OUT} = 2.2 µF, TPS70933-Q1

Figure 44. Power-Up with Enable

9 Power Supply Recommendations

This device is designed to operate with an input supply range of 2.7 V to 30 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

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10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

Input and output capacitors must be placed as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection must be connected directly to the device GND pin. High ESR capacitors may degrade PSRR performance.

10.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 1.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

Figure 45 shows the maximum ambient temperature versus the power dissipation of the TPS709-Q1. This figure assumes the device is soldered on a JEDEC standard, high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to ensure the TPS709-Q1 does not operate above a junction temperature of 125°C.

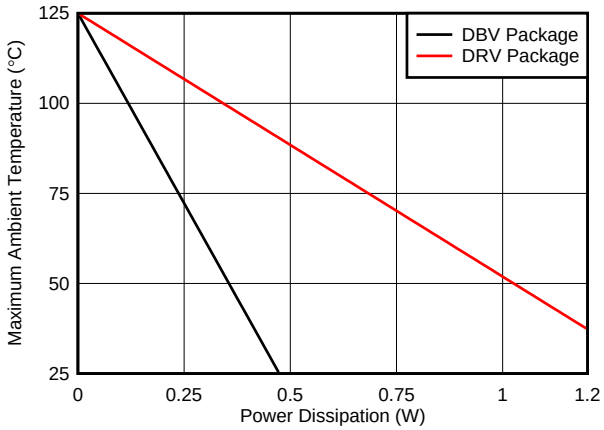


Figure 45. Maximum Ambient Temperature vs Device Power Dissipation

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Layout Guidelines (continued)

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB}, shown in the *Thermal Information*. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 2.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{2}$$

where:

- P_D is the power dissipation shown by Equation 1,
- T_T is the temperature at the center-top of the IC package,
- T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface*.

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

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10.2 Layout Examples

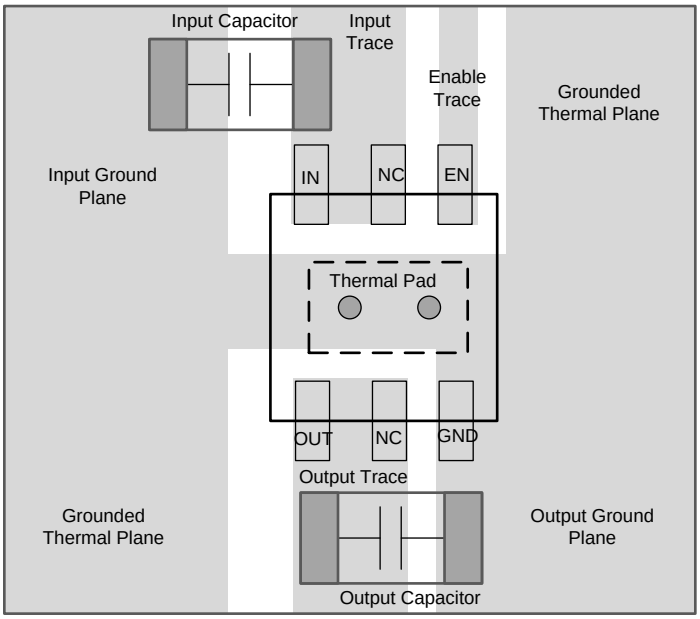


Figure 46. WSON Layout Example

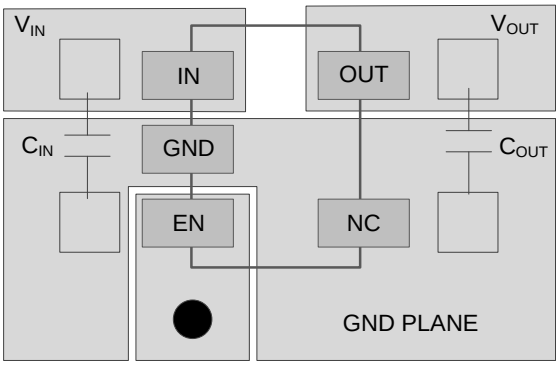


Figure 47. SOT23-5 Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

评估模块 (EVM) 可与 TPS709-Q1 配套使用，帮助评估初始电路性能。TPS70933EVM-110 评估模块（和相关的用户指南）可在德州仪器 (TI) 网站上的产品文件夹中获取，也可直接从 TI 网上商店购买。

11.1.1.2 Spice 模型

分析模拟电路和系统的性能时，使用 SPICE 模型对电路性能进行计算机仿真非常有用。您可以从产品文件夹中的*仿真模型*下获取 TPS709 的 SPICE 模型。

11.1.2 器件命名规则

表 **3.** 器件命名规则(1)

产品	V_{OUT}
TPS709**xx(x)***yyyz*-Q1	**XX(X)** 是标称输出电压。对于分辨率为 100mV 的输出电压，订货编号中使用两位数字；否则，使用三位数字（例如，28 = 2.8V；125 = 1.25V）。 **YYY** 为封装标识符。 **Z** 为卷带数量（R = 3000，T = 250）。

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者登录 TI 的网站 www.ti.com.cn进行查询。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

《TPS70933EVM-110 评估模块用户指南》

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

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11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS70912QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLR	Samples
TPS70912QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJD	Samples
TPS70915QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJE	Samples
TPS70918QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLS	Samples
TPS70918QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJF	Samples
TPS70925QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLT	Samples
TPS70925QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJG	Samples
TPS70927QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJH	Samples
TPS70928QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLU	Samples
TPS70928QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJI	Samples
TPS70930QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLV	Samples
TPS70930QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJJ	Samples
TPS70933QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLJ	Samples
TPS70933QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJK	Samples
TPS70936QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLW	Samples
TPS70950QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLX	Samples
TPS70950QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SJL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

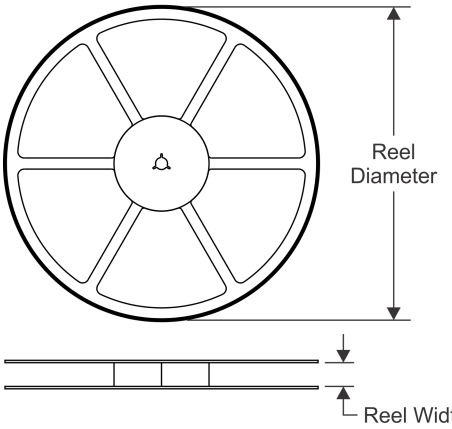
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

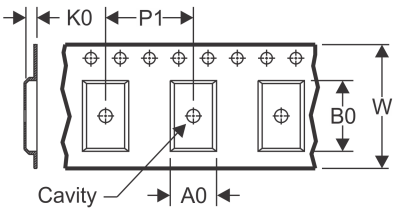
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

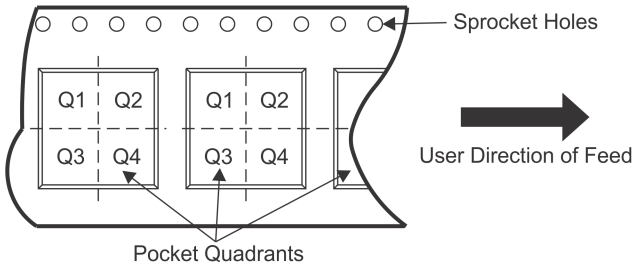


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

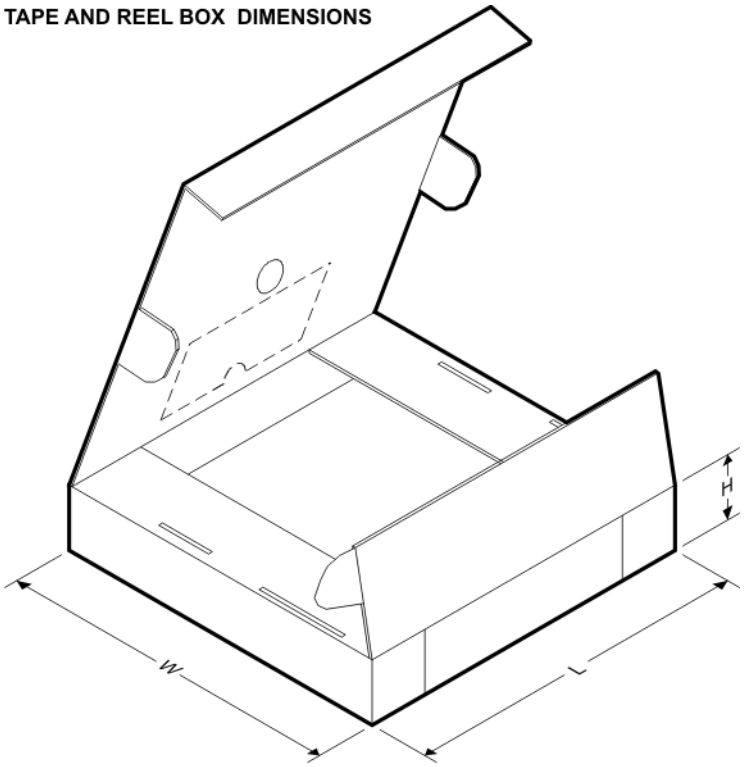
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70912QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70912QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70915QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70918QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70918QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70925QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70925QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70927QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70928QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70928QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70930QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70930QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70933QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70933QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS70936QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

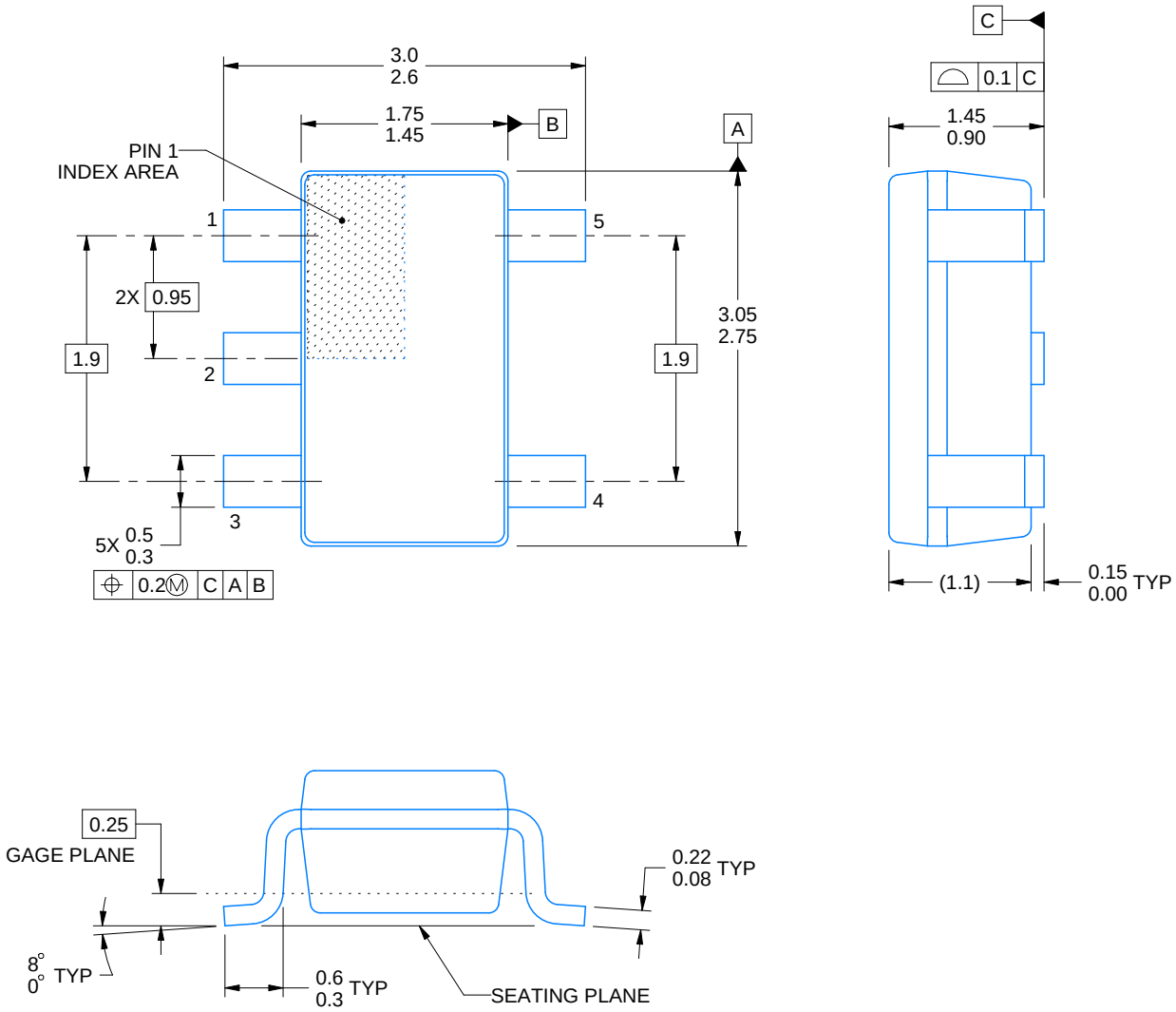
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70912QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70912QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70915QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70918QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70918QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70925QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70925QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70927QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70928QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70928QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70930QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70930QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70933QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70933QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS70936QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70950QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70950QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

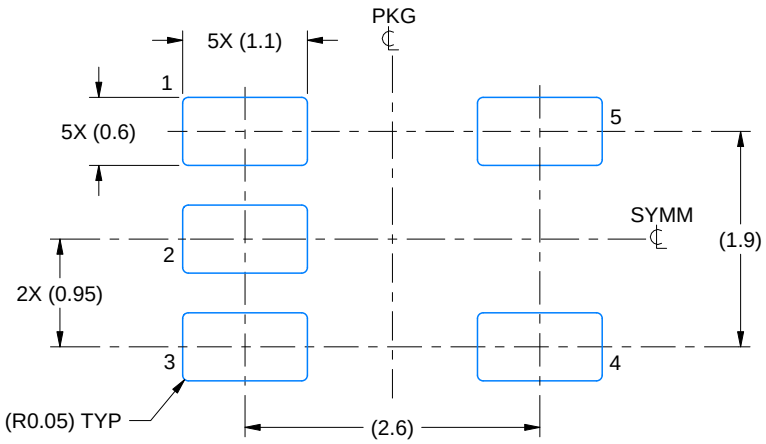
SMALL OUTLINE TRANSISTOR



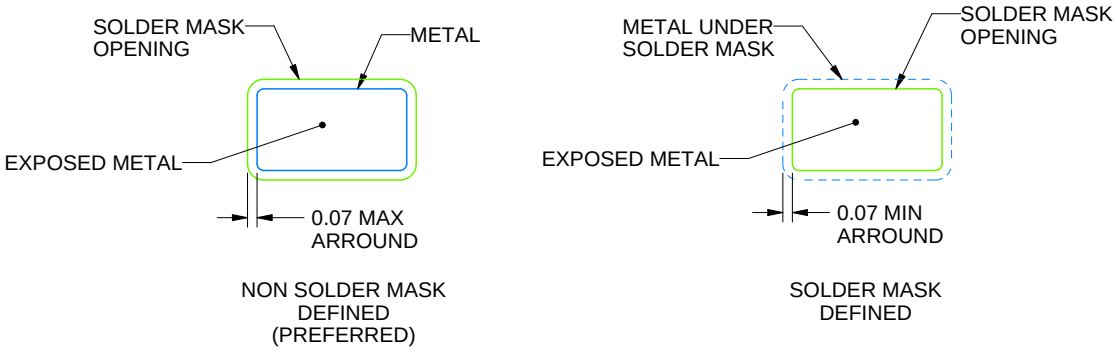
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

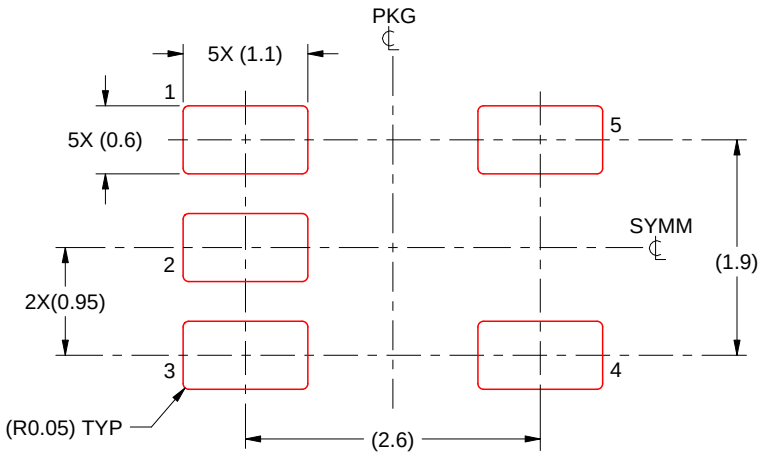


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

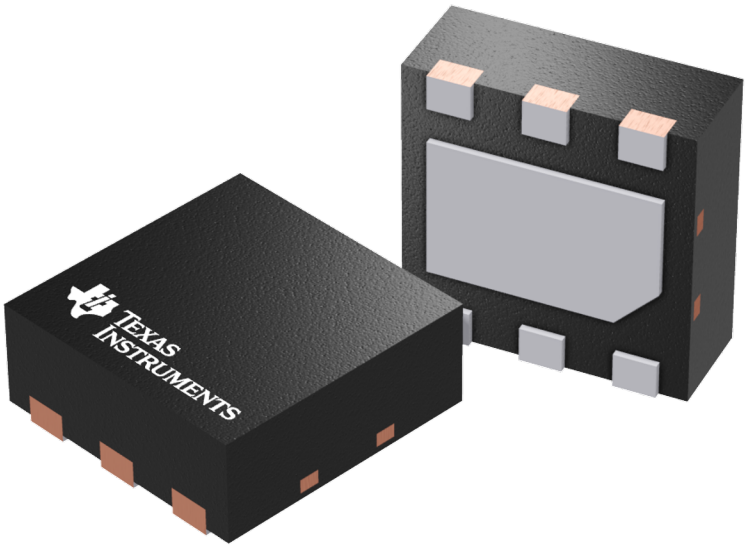
4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



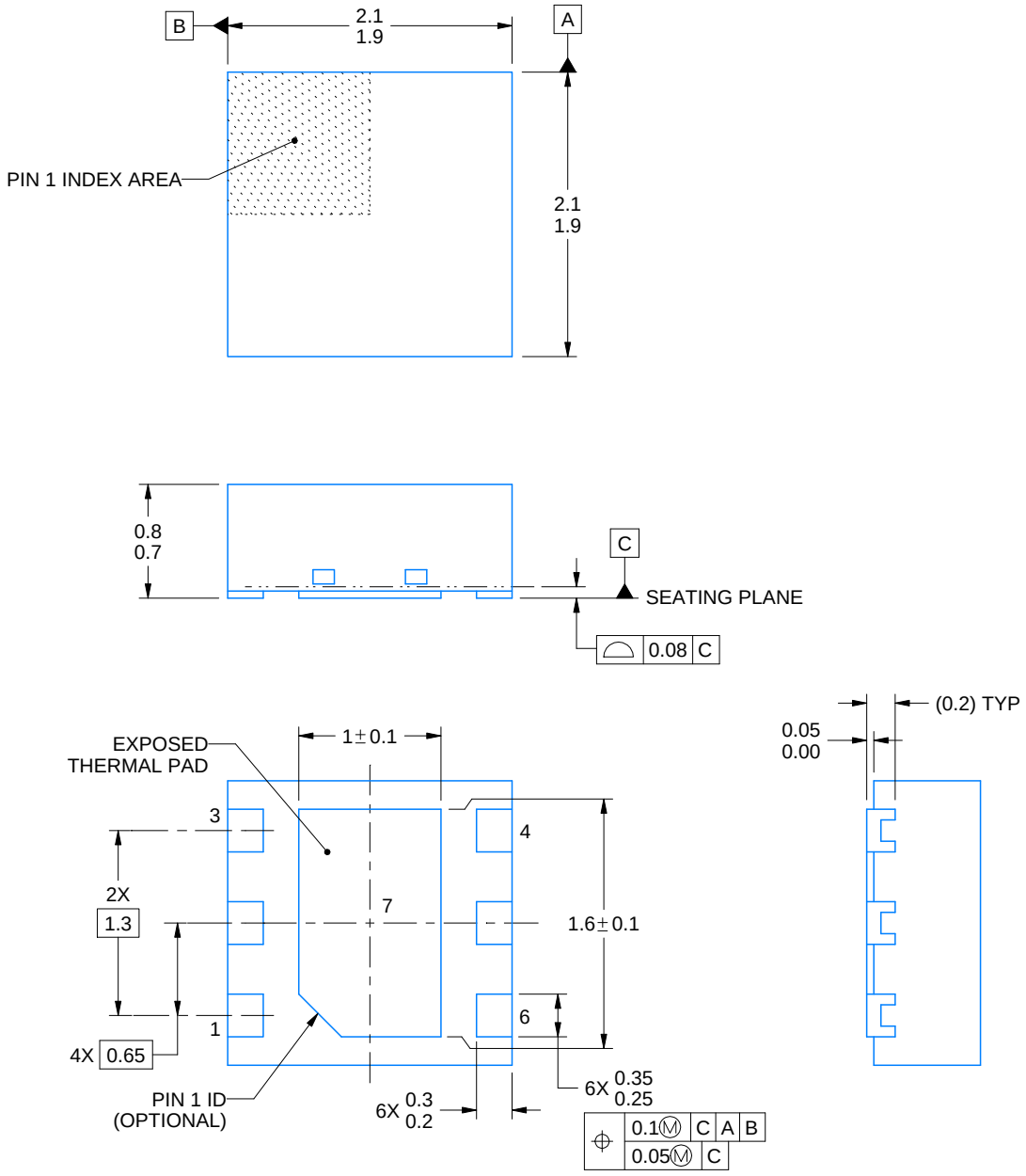
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

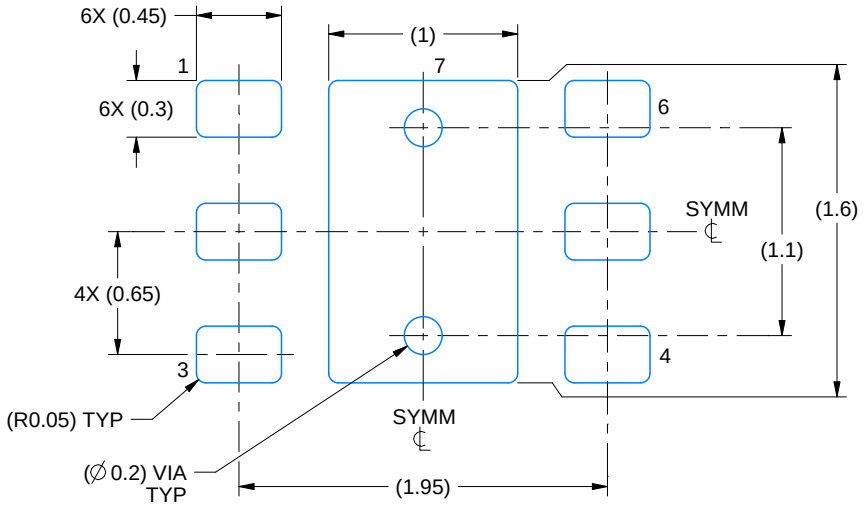
PLASTIC SMALL OUTLINE - NO LEAD



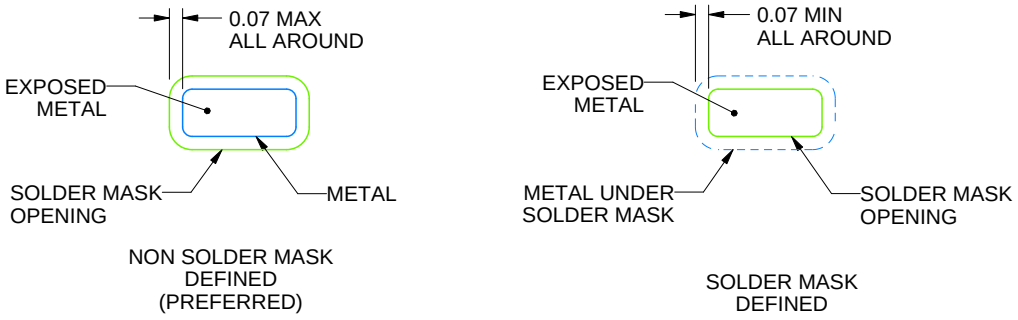
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

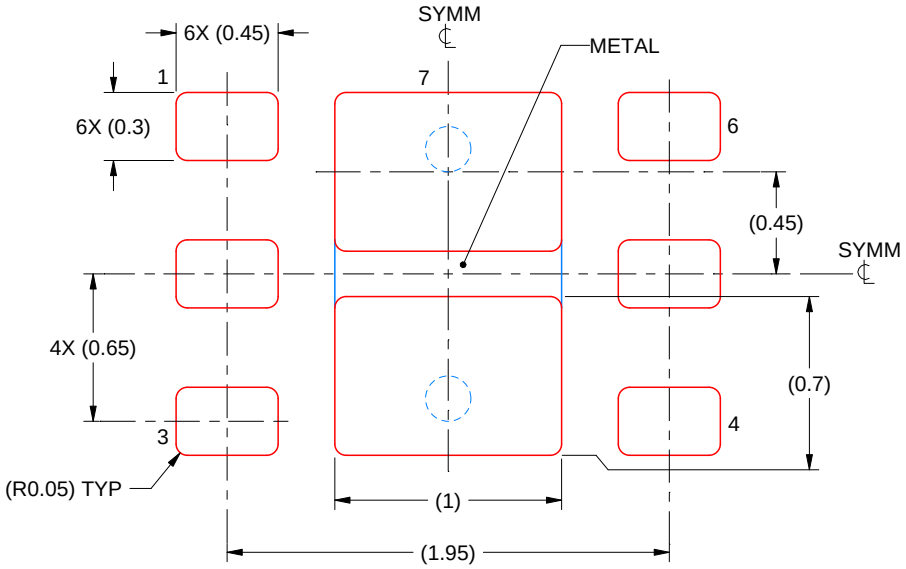


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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