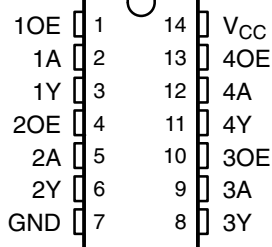


# SN54ABT126, SN74ABT126 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

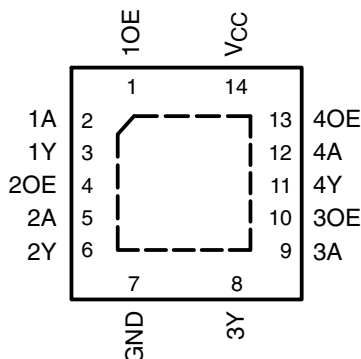
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- Typical  $V_{OLP}$  (Output Ground Bounce)  $<1$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

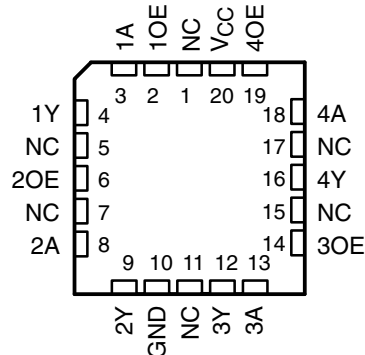
SN54ABT126 ... J PACKAGE  
SN74ABT126 ... D, DB, N, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74ABT126 ... RGY PACKAGE  
(TOP VIEW)



SN54ABT126 ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'ABT126 bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

## ORDERING INFORMATION

| $T_A$          | PACKAGE†   |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| –40°C to 85°C  | QFN – RGY  | Tape and reel | SN74ABT126RGYR        | AB126            |
|                | PDIP – N   | Tube          | SN74ABT126N           | SN74ABT126N      |
|                | SOIC – D   | Tube          | SN74ABT126D           | ABT126           |
|                |            | Tape and reel | SN74ABT126DR          |                  |
|                | SOP – NS   | Tape and reel | SN74ABT126NSR         | ABT126           |
|                | SSOP – DB  | Tape and reel | SN74ABT126DBR         | AB126            |
|                | TSSOP – PW | Tube          | SN74ABT126PW          | AB126            |
|                |            | Tape and reel | SN74ABT126PWR         |                  |
| –55°C to 125°C | CDIP – J   | Tube          | SNJ54ABT126J          | SNJ54ABT126J     |
|                | LCCC – FK  | Tube          | SNJ54ABT126FK         | SNJ54ABT126FK    |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# SN54ABT126, SN74ABT126

## QUADRUPLE BUS BUFFER GATES

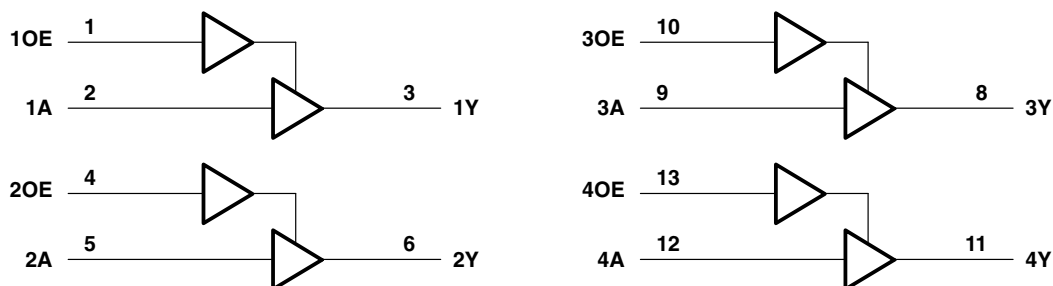
### WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each buffer)

| INPUTS |   | OUTPUT |
|--------|---|--------|
| OE     | A | Y      |
| H      | H | H      |
| H      | L | L      |
| L      | X | Z      |

#### logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and RGY packages.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                           |                 |
|---------------------------------------------------------------------------|-----------------|
| Supply voltage range, $V_{CC}$                                            | –0.5 V to 7 V   |
| Input voltage range, $V_I$ (see Note 1)                                   | –0.5 V to 7 V   |
| Voltage range applied to any output in the high or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$ : SN54ABT126              | 96 mA           |
| SN74ABT126                                                                | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                               | –18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                              | –50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): D package          | 86°C/W          |
| (see Note 2): DB package                                                  | 96°C/W          |
| (see Note 2): N package                                                   | 80°C/W          |
| (see Note 2): NS package                                                  | 76°C/W          |
| (see Note 2): PW package                                                  | 113°C/W         |
| (see Note 3): RGY package                                                 | 47°C/W          |
| Storage temperature range, $T_{stg}$                                      | –65°C to 150°C  |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. The package thermal impedance is calculated in accordance with JESD 51-7.
  3. The package thermal impedance is calculated in accordance with JESD 51-5.



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# SN54ABT126, SN74ABT126 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 4)

|                          |                                    | SN54ABT126 |          | SN74ABT126 |          | UNIT         |
|--------------------------|------------------------------------|------------|----------|------------|----------|--------------|
|                          |                                    | MIN        | MAX      | MIN        | MAX      |              |
| $V_{CC}$                 | Supply voltage                     | 4.5        | 5.5      | 4.5        | 5.5      | V            |
| $V_{IH}$                 | High-level input voltage           | 2          |          | 2          |          | V            |
| $V_{IL}$                 | Low-level input voltage            |            | 0.8      |            | 0.8      | V            |
| $V_I$                    | Input voltage                      | 0          | $V_{CC}$ | 0          | $V_{CC}$ | V            |
| $I_{OH}$                 | High-level output current          |            | -24      |            | -32      | mA           |
| $I_{OL}$                 | Low-level output current           |            | 48       |            | 64       | mA           |
| $\Delta t/\Delta v$      | Input transition rise or fall rate |            | 10       |            | 10       | ns/V         |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate                 | 200        |          | 200        |          | $\mu$ s/V    |
| $T_A$                    | Operating free-air temperature     | -55        | 125      | -40        | 85       | $^{\circ}$ C |

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER            | TEST CONDITIONS                                                                                  | $T_A = 25^{\circ}\text{C}$ |      |           | SN54ABT126 |      | SN74ABT126 |      | UNIT    |
|----------------------|--------------------------------------------------------------------------------------------------|----------------------------|------|-----------|------------|------|------------|------|---------|
|                      |                                                                                                  | MIN                        | TYP† | MAX       | MIN        | MAX  | MIN        | MAX  |         |
| $V_{IK}$             | $V_{CC} = 4.5\text{ V}$ ,<br>$I_I = -18\text{ mA}$                                               |                            |      | -1.2      | -1.2       |      | -1.2       |      | V       |
| $V_{OH}$             | $V_{CC} = 4.5\text{ V}$ ,<br>$I_{OH} = -3\text{ mA}$                                             | 2.5                        |      |           | 2.5        |      | 2.5        |      | V       |
|                      | $V_{CC} = 5\text{ V}$ ,<br>$I_{OH} = -3\text{ mA}$                                               | 3                          |      |           | 3          |      | 3          |      |         |
|                      | $V_{CC} = 4.5\text{ V}$                                                                          |                            |      | 2         | 2          |      |            |      |         |
|                      |                                                                                                  |                            |      | 2*        |            |      | 2          |      |         |
| $V_{OL}$             | $V_{CC} = 4.5\text{ V}$                                                                          |                            |      | 0.55      | 0.55       |      |            |      | V       |
|                      |                                                                                                  |                            |      | 0.55*     |            |      | 0.55       |      |         |
| $V_{hys}$            |                                                                                                  |                            | 100  |           |            |      |            |      | mV      |
| $I_I$                | $V_{CC} = 0\text{ to }5.5\text{ V}$ ,<br>$V_I = V_{CC}\text{ or GND}$                            |                            |      | $\pm 1$   | $\pm 1$    |      | $\pm 1$    |      | $\mu$ A |
| $I_{OZPU}$           | $V_{CC} = 0\text{ to }2.1\text{ V}$ , $V_O = 0.5\text{ V to }2.7\text{ V}$ , $OE = X^{\ddagger}$ |                            |      | $\pm 50$  | $\pm 50$   |      | $\pm 50$   |      | $\mu$ A |
| $I_{OZPD}$           | $V_{CC} = 2.1\text{ V to }0$ , $V_O = 0.5\text{ V to }2.7\text{ V}$ , $OE = X^{\ddagger}$        |                            |      | $\pm 50$  | $\pm 50$   |      | $\pm 50$   |      | $\mu$ A |
| $I_{OZH}$            | $V_{CC} = 2.1\text{ V to }5.5\text{ V}$ , $V_O = 2.7\text{ V}$ , $OE \leq 0.8\text{ V}$          |                            |      | 10        | 10         |      | 10         |      | $\mu$ A |
| $I_{OZL}$            | $V_{CC} = 2.1\text{ V to }5.5\text{ V}$ , $V_O = 0.5\text{ V}$ , $OE \leq 0.8\text{ V}$          |                            |      | -10       | -10        |      | -10        |      | $\mu$ A |
| $I_{off}$            | $V_{CC} = 0$ ,<br>$V_I\text{ or }V_O \leq 4.5\text{ V}$                                          |                            |      | $\pm 100$ |            |      | $\pm 100$  |      | $\mu$ A |
| $I_{CEX}$            | $V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$                                                   |                            |      | 50        | 50         |      | 50         |      | $\mu$ A |
| $I_O^{\S}$           | $V_{CC} = 5.5\text{ V}$ ,<br>$V_O = 2.5\text{ V}$                                                | -50                        | -100 | -200      | -50        | -200 | -50        | -200 | mA      |
| $I_{CC}$             | $V_{CC} = 5.5\text{ V}$ , $I_O = 0$ ,<br>$V_I = V_{CC}\text{ or GND}$                            |                            |      | 1         | 250        | 250  | 250        |      | $\mu$ A |
|                      |                                                                                                  |                            |      | 24        | 30         | 30   | 30         |      | mA      |
|                      |                                                                                                  |                            |      | 0.5       | 250        | 250  | 250        |      | $\mu$ A |
| $\Delta I_{CC}^{\P}$ | $V_{CC} = 5.5\text{ V}$ ,<br>One input at 3.4 V,<br>Other inputs at $V_{CC}$ or GND              |                            |      | 1.5       | 1.5        | 1.5  | 1.5        |      | mA      |
|                      |                                                                                                  |                            |      | 50        | 50         | 50   | 50         |      | $\mu$ A |
| $C_i$                | $V_I = 2.5\text{ V or }0.5\text{ V}$                                                             |                            | 3    |           |            |      |            |      | pF      |
| $C_o$                | $V_O = 2.5\text{ V or }0.5\text{ V}$                                                             |                            | 7    |           |            |      |            |      | pF      |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at  $V_{CC} = 5\text{ V}$ .

‡ For  $V_{CC}$  between 2.1 V and 4 V, OE should be less than or equal to 0.5 V to ensure a low state.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

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# SN54ABT126, SN74ABT126

## QUADRUPLE BUS BUFFER GATES

### WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 5 and Figure 1)

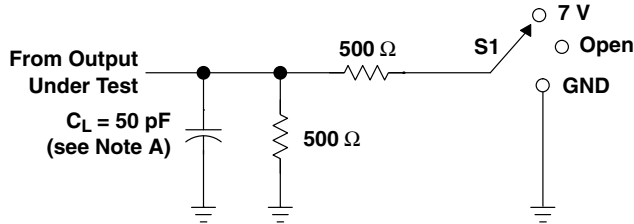
| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 5\text{ V},$<br>$T_A = 25^\circ\text{C}$ |     |     | SN54ABT126 |     | SN74ABT126 |     | UNIT |
|-----------|-----------------|----------------|----------------------------------------------------|-----|-----|------------|-----|------------|-----|------|
|           |                 |                | MIN                                                | TYP | MAX | MIN        | MAX | MIN        | MAX |      |
| $t_{PLH}$ | A               | Y              | 1                                                  | 2.9 | 4.9 | 1          | 7.3 | 1          | 6.3 | ns   |
| $t_{PHL}$ |                 |                | 1                                                  | 2.5 | 5.1 | 1          | 5.9 | 1          | 5.7 |      |
| $t_{PZH}$ | OE              | Y              | 1                                                  | 4.4 | 5.8 | 1          | 5.3 | 1          | 6.5 | ns   |
| $t_{PZL}$ |                 |                | 1                                                  | 4.4 | 5.9 | 1          | 6.4 | 1          | 6.5 |      |
| $t_{PHZ}$ | OE              | Y              | 1                                                  | 3   | 5.7 | 1          | 6.9 | 1          | 6.8 | ns   |
| $t_{PLZ}$ |                 |                | 1                                                  | 3   | 5.8 | 1          | 7.2 | 1          | 6.7 |      |

NOTE 5: Limits may vary among suppliers.

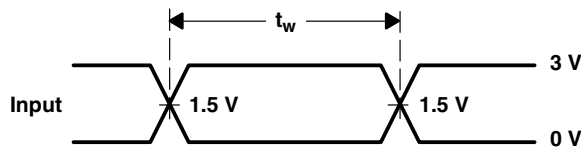
# SN54ABT126, SN74ABT126 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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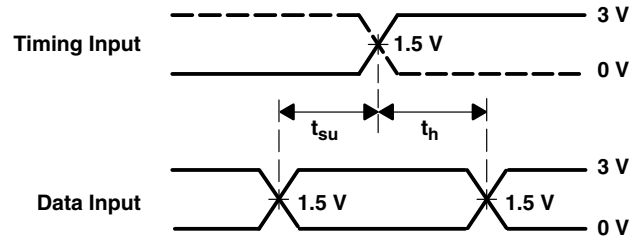
## PARAMETER MEASUREMENT INFORMATION



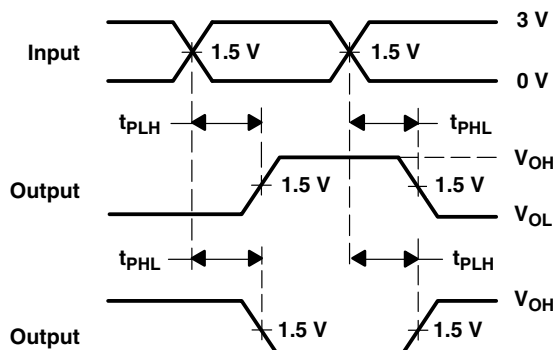
LOAD CIRCUIT



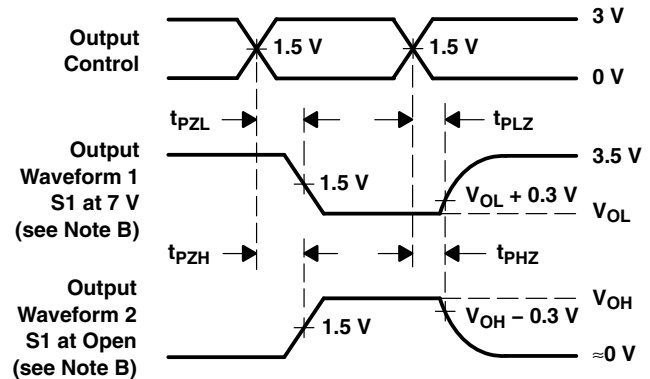
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74ABT126D      | ACTIVE        | SOIC         | D                  | 14   | 50             | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ABT126                  | <a href="#">Samples</a> |
| SN74ABT126DBR    | ACTIVE        | SSOP         | DB                 | 14   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AB126                   | <a href="#">Samples</a> |
| SN74ABT126DR     | ACTIVE        | SOIC         | D                  | 14   | 2500           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ABT126                  | <a href="#">Samples</a> |
| SN74ABT126N      | ACTIVE        | PDIP         | N                  | 14   | 25             | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | SN74ABT126N             | <a href="#">Samples</a> |
| SN74ABT126NSR    | ACTIVE        | SO           | NS                 | 14   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ABT126                  | <a href="#">Samples</a> |
| SN74ABT126PW     | ACTIVE        | TSSOP        | PW                 | 14   | 90             | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AB126                   | <a href="#">Samples</a> |
| SN74ABT126PWR    | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AB126                   | <a href="#">Samples</a> |
| SN74ABT126RGYR   | ACTIVE        | VQFN         | RGY                | 14   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | AB126                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT126DBR  | SSOP         | DB              | 14   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN74ABT126DR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74ABT126NSR  | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74ABT126PWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74ABT126RGYR | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT126DBR  | SSOP         | DB              | 14   | 2000 | 853.0       | 449.0      | 35.0        |
| SN74ABT126DR   | SOIC         | D               | 14   | 2500 | 853.0       | 449.0      | 35.0        |
| SN74ABT126NSR  | SO           | NS              | 14   | 2000 | 853.0       | 449.0      | 35.0        |
| SN74ABT126PWR  | TSSOP        | PW              | 14   | 2000 | 853.0       | 449.0      | 35.0        |
| SN74ABT126RGYR | VQFN         | RGY             | 14   | 3000 | 853.0       | 449.0      | 35.0        |

## TUBE

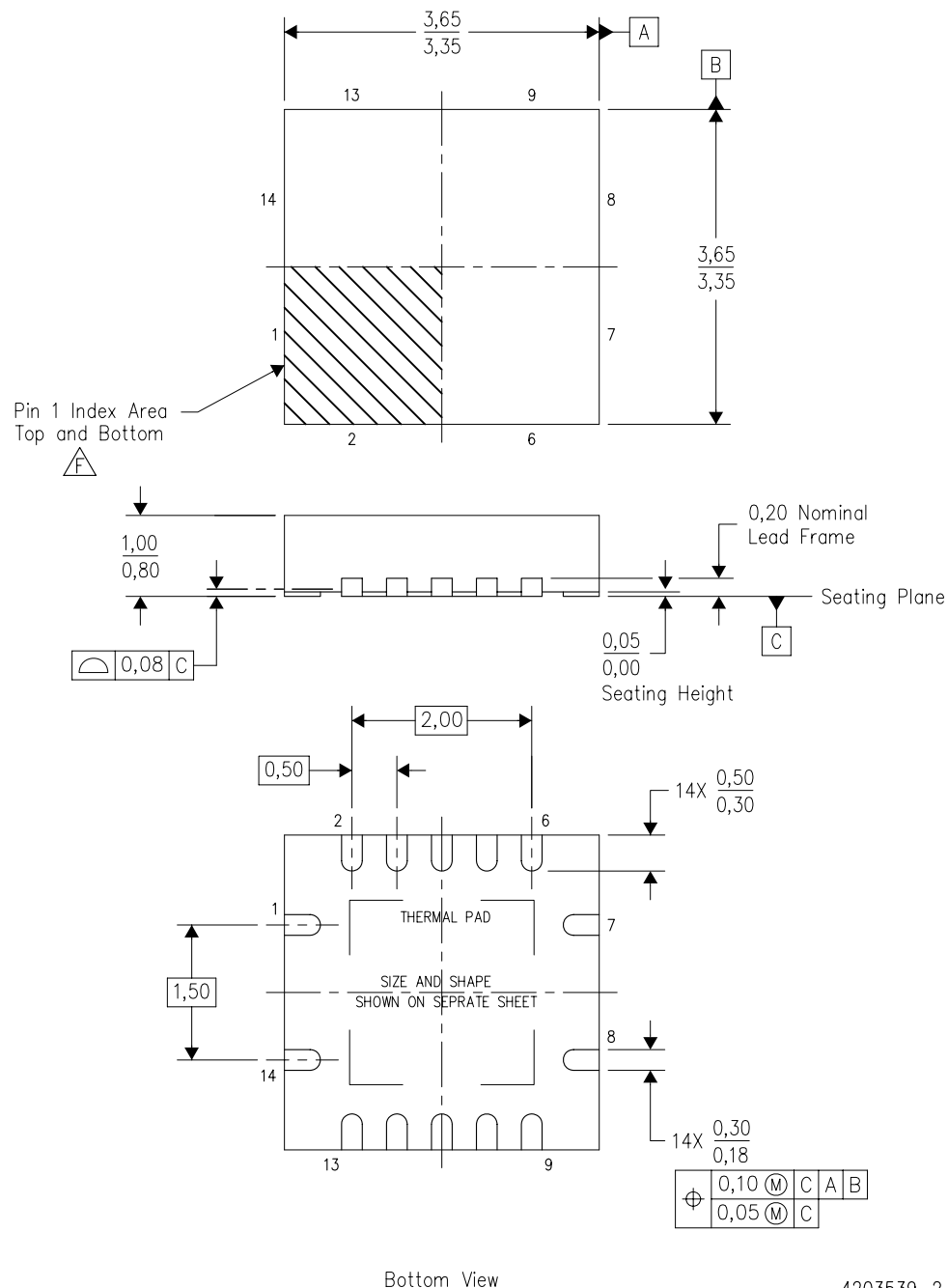


\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74ABT126D  | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74ABT126N  | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74ABT126N  | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74ABT126PW | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

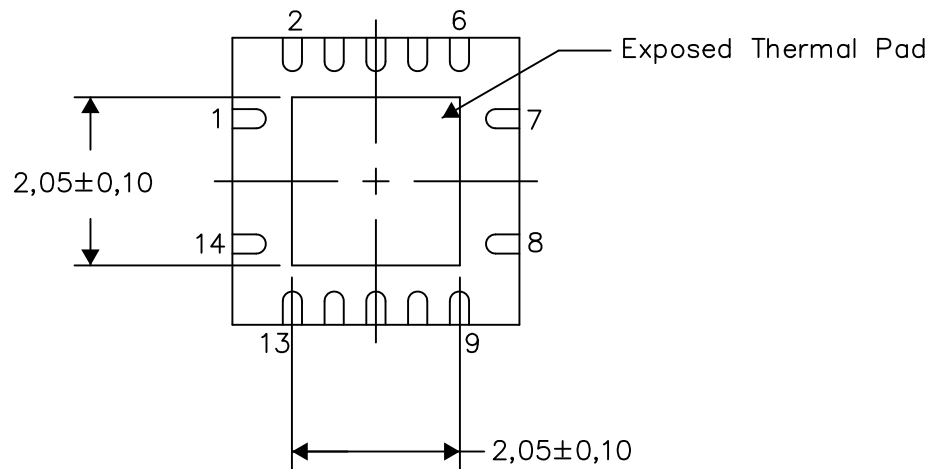
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

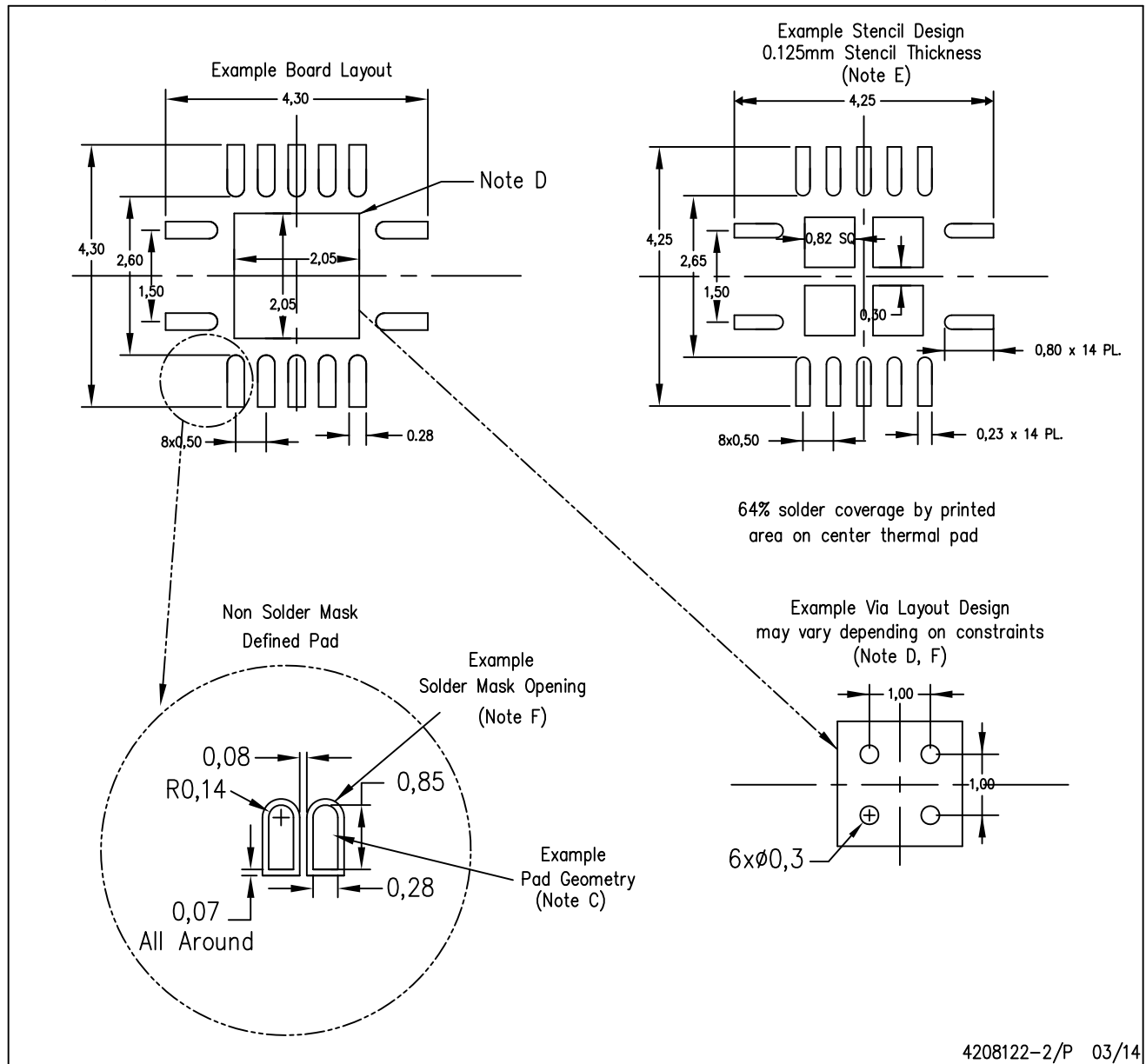
Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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