

FEATURES

- **Single Chip With Easy Interface Between UART and Serial-Port Connector of IBM™ PC/AT™ and Compatibles**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Supports Data Rates up to 120 kbit/s**
- **ESD Protection Meets or Exceeds 10 kV on RS-232 Pins and 3.5 kV on All Other Pins (Human-Body Model)**
- **Pin-to-Pin Compatible With the SN75C185**

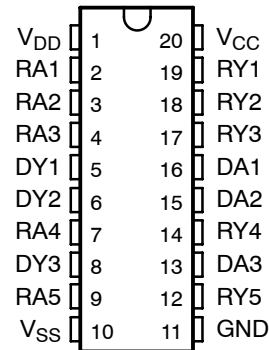
DESCRIPTION/ORDERING INFORMATION

The SN75185 combines three drivers and five receivers from the TI SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The pinout matches the flow-through design of the SN75C185 to decrease the part count, reduce the board space required, and allow easy interconnection of the UART and serial-port connector of IBM™ PC/AT™ and compatibles. The bipolar circuits and processing of the SN75185 provide a rugged low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C185.

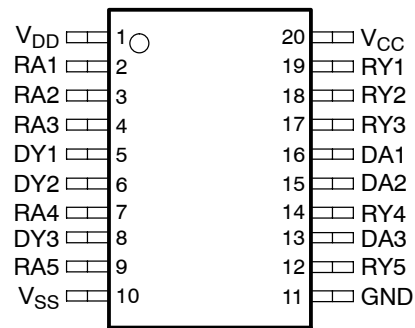
The SN75185 complies with the requirements of the TIA/EIA-232-F and ITU v.28 standards. These standards are for data interchange between a host computer and peripheral at signaling rates up to 20 kbit/s. The switching speeds of the SN75185 are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be assured unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates to 120 kbit/s, use of TIA/EIA-423-B (ITU v.10) and TIA/EIA-422-B (ITU v.11) standards is recommended.

The SN75185 is characterized for operation over the temperature range of 0°C to 70°C.

**N PACKAGE
(TOP VIEW)**



**DB, DW, OR PW PACKAGE
(TOP VIEW)**



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SN75185 MULTIPLE RS-232 DRIVERS AND RECEIVERS

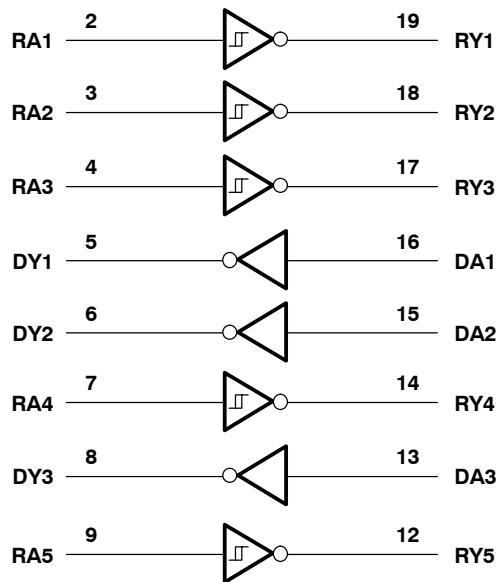
SLLS181D–DECEMBER 1994–REVISED JANUARY 2006

ORDERING INFORMATION

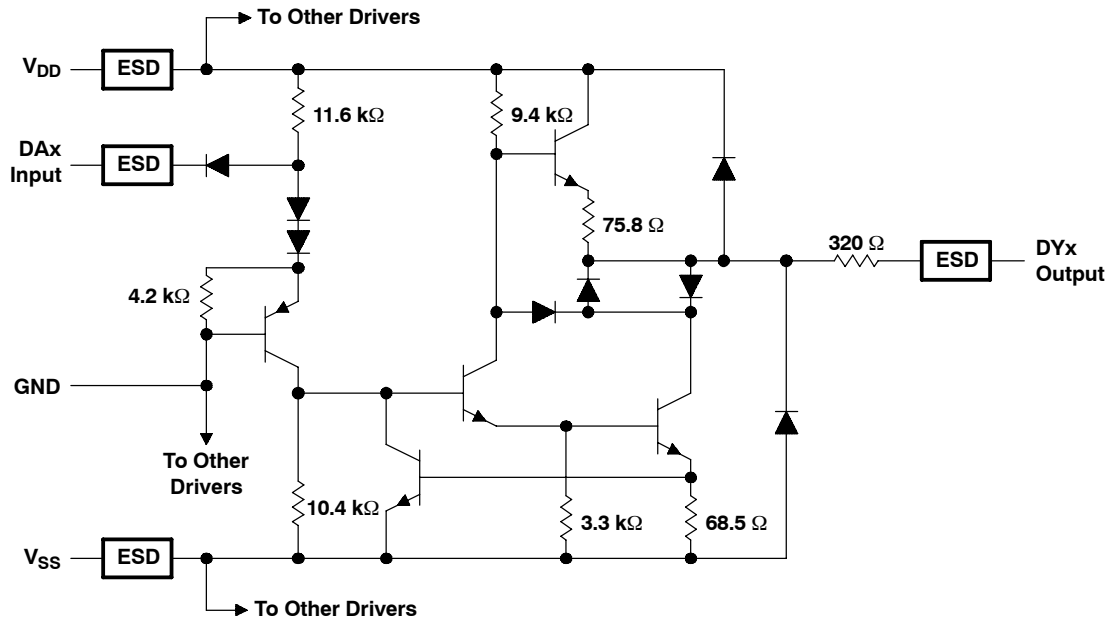
T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 20	SN75185N	SN75185N
	SOIC – DW	Tube of 25	SN75185DW	SN75185
		Reel of 2000	SN75185DWR	
	SSOP – DB	Tube of 70	SN75185DB	A185
		Reel of 2000	SN75185DBR	
	TSSOP – PW	Tube of 70	SN75185PW	A185
		Reel of 2000	SN75185PWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

LOGIC DIAGRAM (POSITIVE LOGIC)

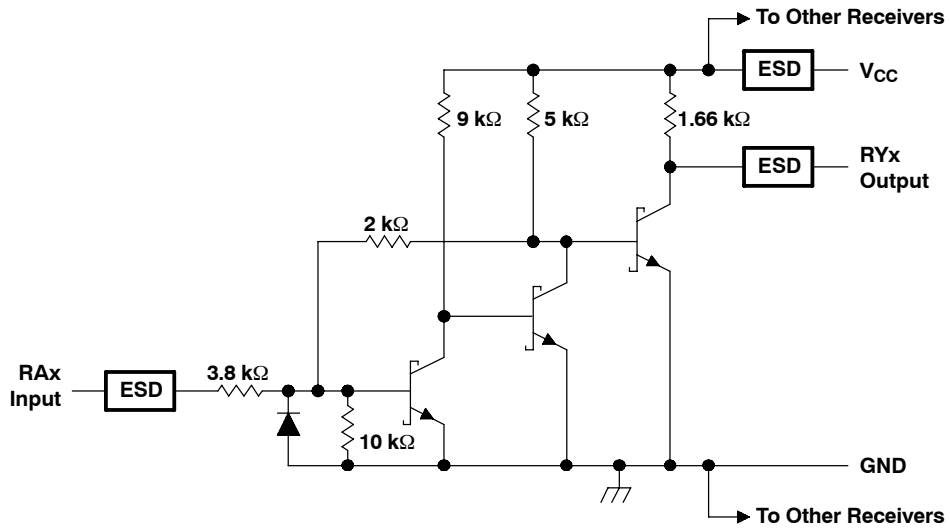


SCHEMATIC OF DRIVERS



Resistor values shown are nominal.

SCHEMATIC (EACH RECEIVER)



Resistor values shown are nominal.

SN75185 MULTIPLE RS-232 DRIVERS AND RECEIVERS

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾		10	V
V _{DD}	Supply voltage ⁽²⁾		15	V
V _{SS}	Supply voltage ⁽²⁾		-15	V
Input voltage range	Driver	-15	7	V
	Receiver	-30	30	
Driver output voltage range		-15	15	V
Receiver low-level output current			20	mA
θ _{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	DB package		°C/W
		DW package		
		N package		
		PW package		
T _J	Operating virtual junction temperature		150	°C
Electrostatic discharge	Human-Body Model	RS-232 pins, class 3, A ⁽⁵⁾		kV
		All pins, class 3, A ⁽⁶⁾		
	Machine Model	RS-232 pins, class 3, B ⁽⁷⁾		V
		All pins, class 3, B ⁽⁵⁾		
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the network ground terminal.
- (3) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) RS-232 pins are tested with respect to ground and to each other.
- (6) Per MIL-PRF-38535
- (7) RS-232 pins are tested with respect to ground.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{DD}	Supply voltage	7.5	9	15	V
V_{SS}	Supply voltage	-7.5	-9	-15	V
V_{IH}	High-level input voltage (drivers only)	1.9			V
V_{IL}	Low-level input voltage (drivers only)			0.8	V
I_{OH}	High-level output current	Drivers		-6	mA
		Receivers		-0.5	
I_{OL}	Low-level output current	Drivers		6	mA
		Receivers		16	
T_A	Operating free-air temperature	0		70	°C

Supply Currents

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{CC}	Supply current from V_{CC}	All inputs at 5 V,	No load,	$V_{CC} = 5\text{ V}$		30	mA
I_{DD}	Supply current from V_{DD}	All inputs at 1.9 V,	No load	$V_{DD} = 9\text{ V}, V_{SS} = -9\text{ V}$		15	
				$V_{DD} = 12\text{ V}, V_{SS} = -12\text{ V}$		19	
				$V_{DD} = 15\text{ V}, V_{SS} = -15\text{ V}$		25	
		All inputs at 0.8 V,	No load	$V_{DD} = 9\text{ V}, V_{SS} = -9\text{ V}$		4.5	
				$V_{DD} = 12\text{ V}, V_{SS} = -12\text{ V}$		5.5	
				$V_{DD} = 15\text{ V}, V_{SS} = -15\text{ V}$		9	
I_{SS}	Supply current from V_{SS}	All inputs at 1.9 V,	No load	$V_{DD} = 9\text{ V}, V_{SS} = -9\text{ V}$		-15	
				$V_{DD} = 12\text{ V}, V_{SS} = -12\text{ V}$		-19	
				$V_{DD} = 15\text{ V}, V_{SS} = -15\text{ V}$		-25	
		All inputs at 0.8 V,	No load	$V_{DD} = 9\text{ V}, V_{SS} = -9\text{ V}$		-3.2	
				$V_{DD} = 12\text{ V}, V_{SS} = -12\text{ V}$		-3.2	
				$V_{DD} = 15\text{ V}, V_{SS} = -15\text{ V}$		-3.2	

DRIVER SECTION

Electrical Characteristics

over recommended operating free-air temperature range, $V_{DD} = 9\text{ V}$, $V_{SS} = -9\text{ V}$, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	$V_{IL} = 0.8\text{ V}$, $R_L = 3\text{ k}\Omega$, See Figure 1	6	7.5		V
V_{OL} Low-level output voltage ⁽¹⁾	$V_{IH} = 1.9\text{ V}$, $R_L = 3\text{ k}\Omega$, See Figure 1		-7.5	-6	V
I_{IH} High-level input current	$V_I = 5\text{ V}$, See Figure 2			10	μA
I_{IL} Low-level input current	$V_I = 0$, See Figure 2			-1.6	mA
$I_{OS(H)}$ High-level short-circuit output current ⁽²⁾	$V_{IL} = 0.8\text{ V}$, $V_O = 0$, See Figure 1	-4.5	-12	-19.5	mA
$I_{OS(L)}$ Low-level short-circuit output current	$V_{IH} = 2\text{ V}$, $V_O = 0$, See Figure 1	4.5	12	19.5	mA
r_o Output resistance ⁽³⁾	$V_{CC} = V_{DD} = V_{SS} = 0$, $V_O = -2\text{ V to } 2\text{ V}$	300			Ω

- (1) The algebraic convention, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g., if -10 V is maximum, the typical value is a more negative voltage).
- (2) Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
- (3) Test conditions are those specified by TIA/EIA-232-F and as listed above.

Switching Characteristics

$V_{CC} = 5\text{ V}$, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, $C_L = 15\text{ pF}$		315	500	ns
t_{PHL} Propagation delay time, high- to low-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, $C_L = 15\text{ pF}$		75	175	ns
t_{TLH} Transition time, low- to high-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, $C_L = 15\text{ pF}$		60	100	ns
	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, $C_L = 2500\text{ pF}$ ⁽¹⁾		1.7	2.5	μs
t_{THL} Transition time, high- to low-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, $C_L = 15\text{ pF}$		40	75	ns
	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, $C_L = 2500\text{ pF}$ ⁽²⁾		1.5	2.5	μs

- (1) Measured between -3-V and 3-V points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.
- (2) Measured between 3-V and -3-V points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.

RECEIVER SECTION

Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{T+}	Positive-going threshold voltage	See Figure 5	T _A = 25°C	1.75	1.9	2.3	V
			T _A = 0°C to 70°C	1.55		2.3	
V _{T-}	Negative-going threshold voltage			0.75	0.97	1.25	V
V _{hys}	Input hysteresis (V _{T+} – V _{T-})			0.5			V
V _{OH}	High-level output voltage	I _{OH} = –0.5 mA	V _{IH} = 0.75 V	2.6	4	5	V
			Inputs open	2.6			
V _{OL}	Low-level input voltage	I _{OL} = 10 mA,	V _I = 3 V		0.2	0.45	V
I _{IH}	High-level input current	V _I = 25 V,	See Figure 5	3.6		8.3	mA
		V _I = 3 V,	See Figure 5	0.43			
I _{IL}	Low-level output current	V _I = –25 V,	See Figure 5	–3.6		–8.3	mA
		V _I = –3 V,	See Figure 5	–0.43			
I _{OS}	Short-circuit output current	See Figure 4			–3.4	–12	mA

(1) All typical values are at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 9 V, and V_{SS} = –9 V.

Switching Characteristics

V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V, T_A = 25°C (see Figure 6)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 50 pF,	R _L = 5 kΩ		107	500	ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 50 pF,	R _L = 5 kΩ		42	150	ns
t _{TLH}	Transition time, low- to high-level output	C _L = 50 pF,	R _L = 5 kΩ		175	525	ns
t _{THL}	Transition time, high- to low-level output	C _L = 50 pF,	R _L = 5 kΩ		16	60	ns

PARAMETER MEASUREMENT INFORMATION

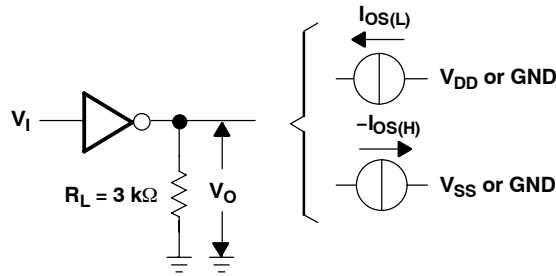


Figure 1. Driver Test Circuit for V_{OH} , V_{OL} , $I_{OS(H)}$, and $I_{OS(L)}$

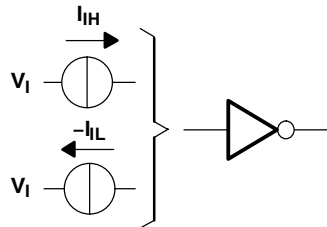
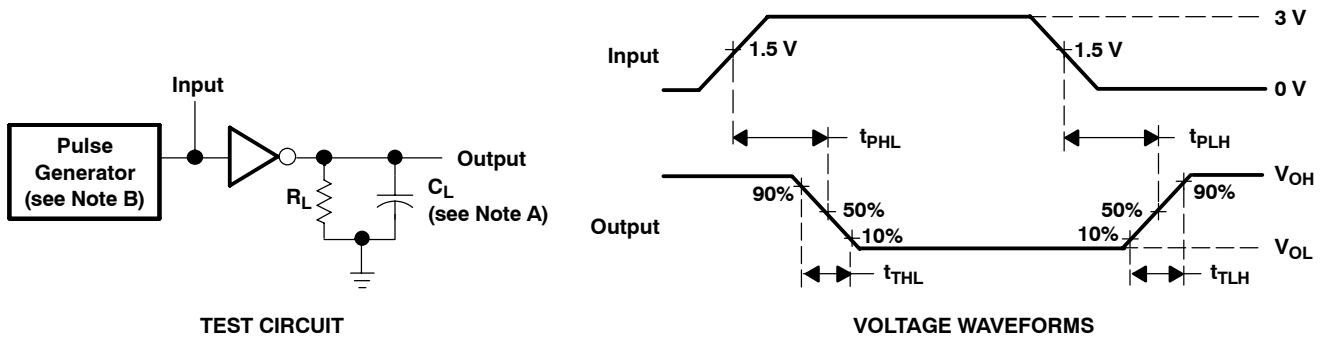


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $t_w = 25\ \mu\text{s}$, $\text{PRR} = 20\ \text{kHz}$, $Z_O = 50\ \Omega$, $t_r = t_f < 50\ \text{ns}$.

Figure 3. Driver Test Circuit and Voltage Waveforms

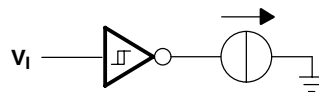


Figure 4. Receiver Test Circuit for I_{OS}

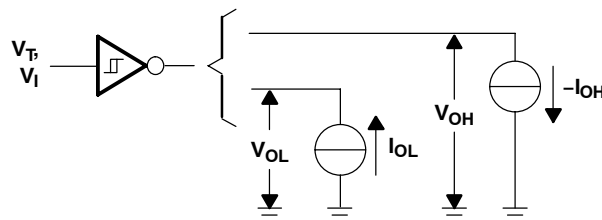
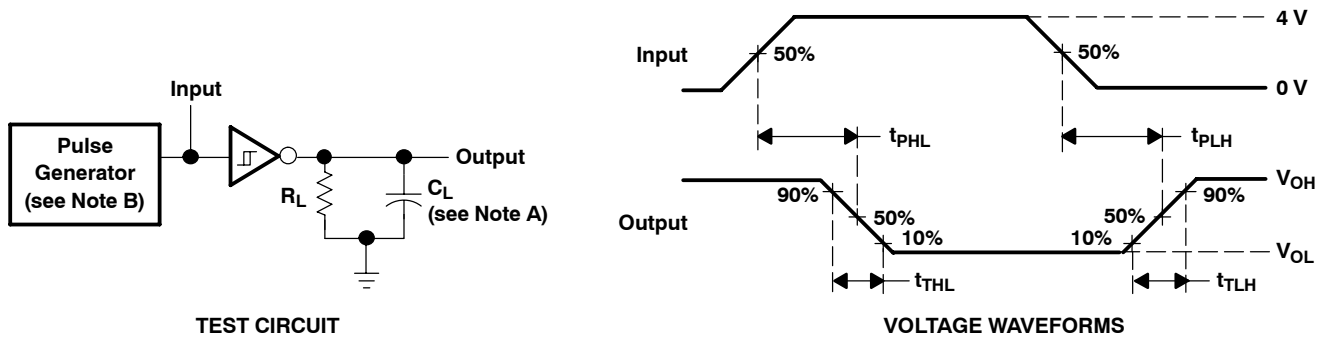


Figure 5. Receiver Test Circuit for V_T , V_{OH} , and V_{OL}

PARAMETER MEASUREMENT INFORMATION (continued)



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $t_w = 25 \mu\text{s}$, $\text{PRR} = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f < 50 \text{ ns}$.

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS
 DRIVER SECTION

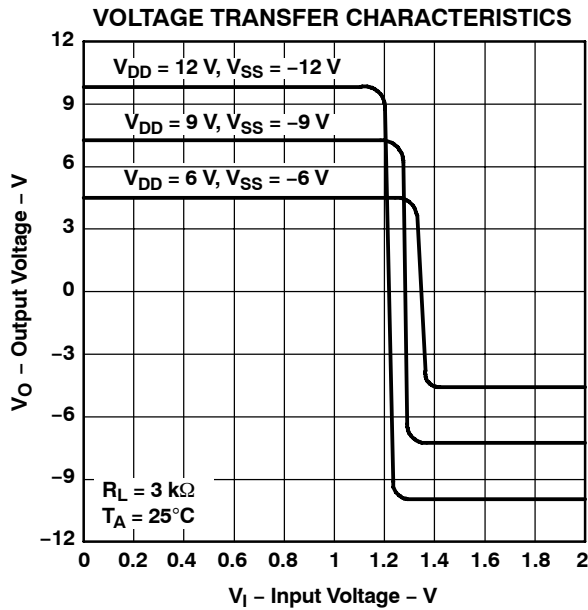


Figure 7.

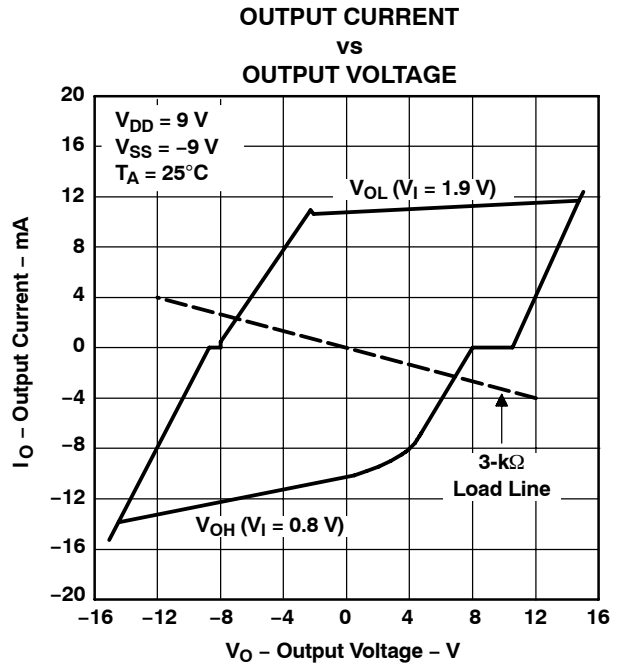


Figure 8.

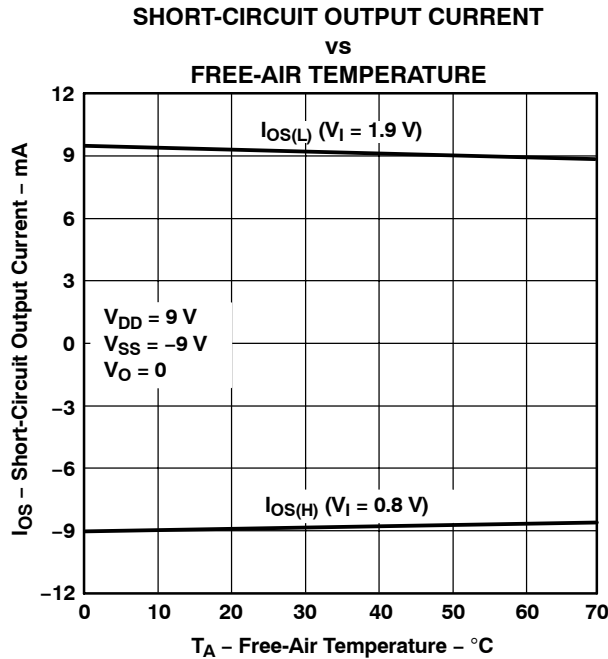


Figure 9.

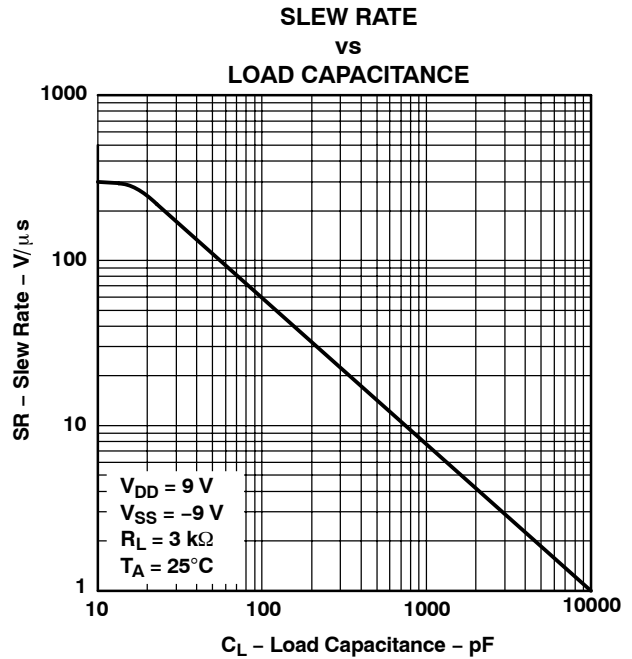


Figure 10.

TYPICAL CHARACTERISTICS
RECEIVER SECTION

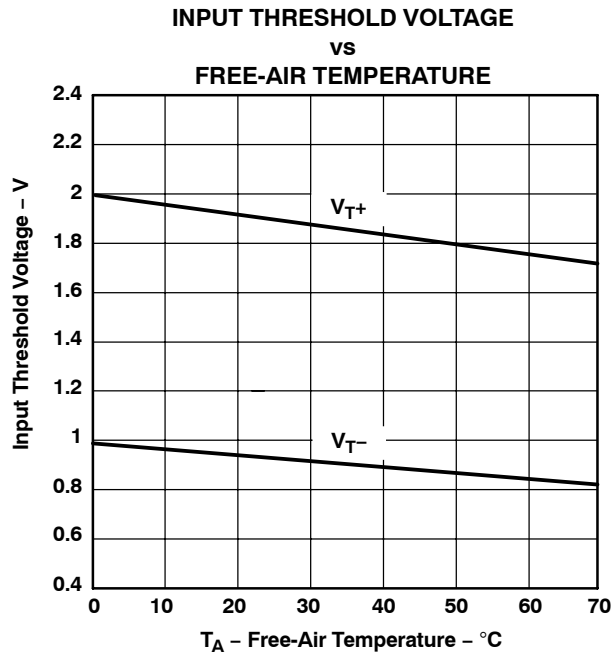


Figure 11.

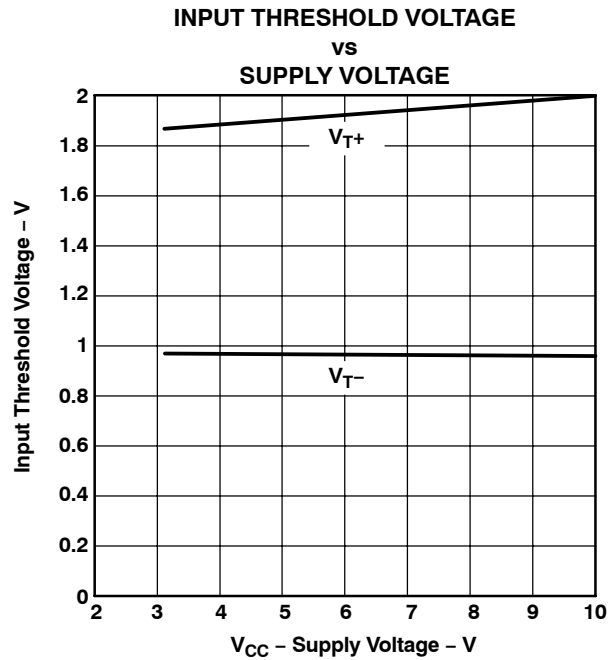
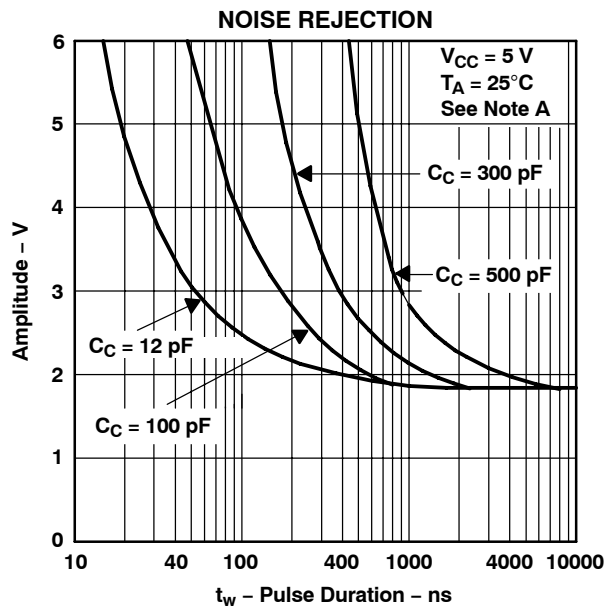


Figure 12.



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.

Figure 13.

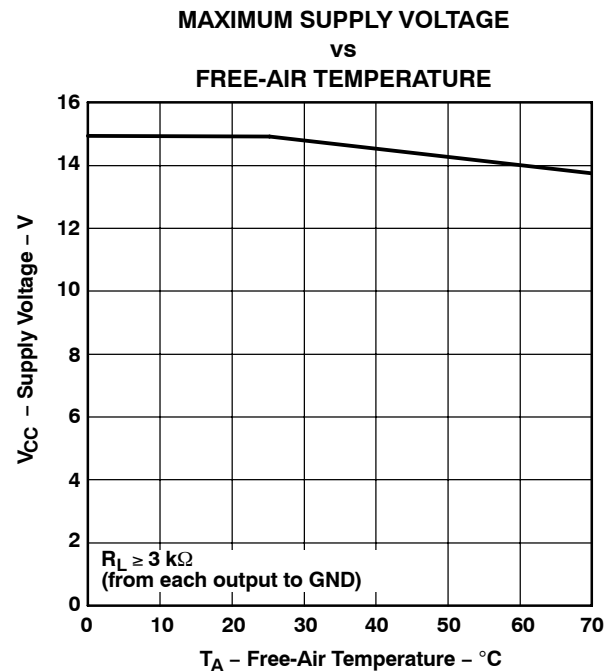


Figure 14.

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the SN75185 in the fault condition. In the fault condition, the device outputs are shorted to ± 15 V, and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).

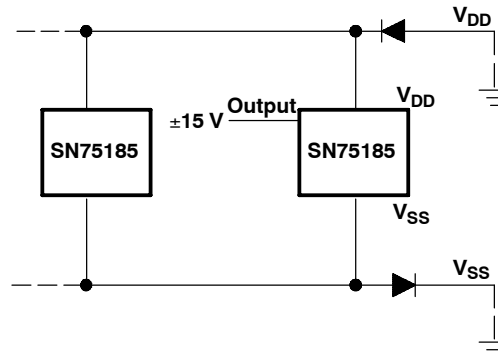
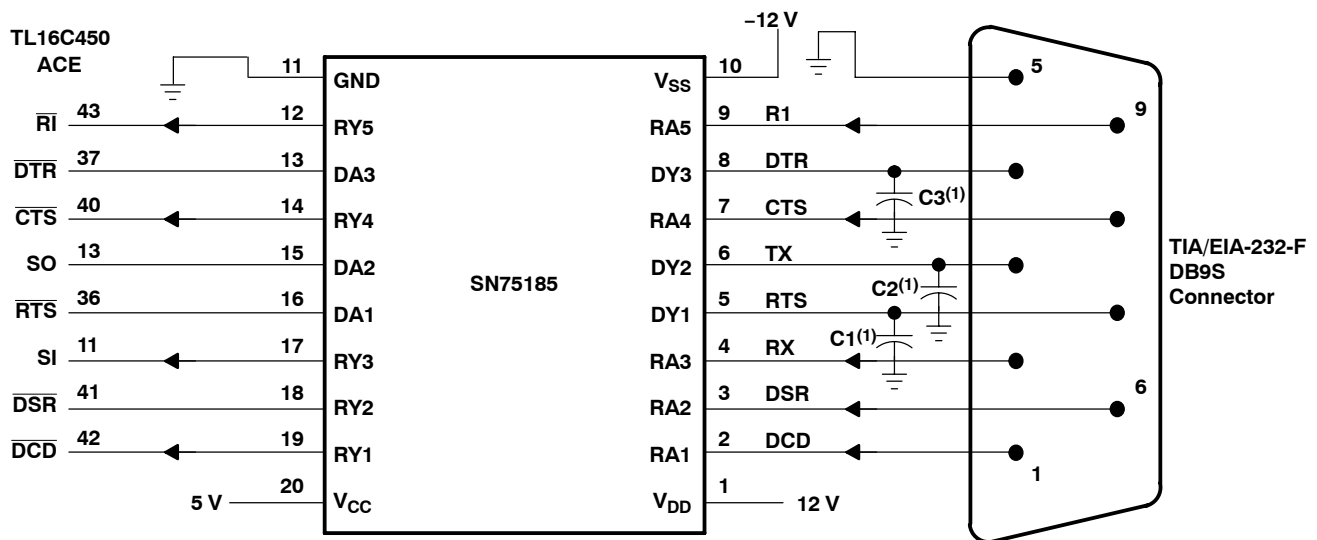


Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F



- (1) See Figure 10 to select the correct values for the loading capacitors (C1, C2, and C3), which are required to meet the RS-232 maximum slew-rate requirement of $30 \text{ V}/\mu\text{s}$. The value of the loading capacitors required depends on the line length and desired slew rate, but typically is 330 pF.

Figure 16. Typical Connection

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75185DB	ACTIVE	SSOP	DB	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A185	Samples
SN75185DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A185	Samples
SN75185DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185	Samples
SN75185DWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185	Samples
SN75185DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185	Samples
SN75185DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185	Samples
SN75185N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75185N	Samples
SN75185PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A185	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

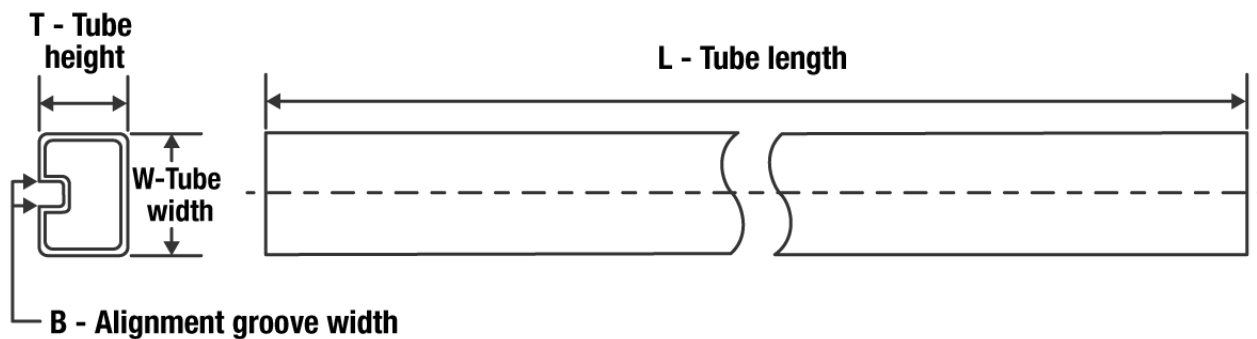

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75185DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN75185DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75185PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75185DBR	SSOP	DB	20	2000	853.0	449.0	35.0
SN75185DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75185PWR	TSSOP	PW	20	2000	853.0	449.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75185DB	DB	SSOP	20	70	530	10.5	4000	4.1
SN75185DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN75185DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75185DWG4	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75185DWG4	DW	SOIC	20	25	507	12.83	5080	6.6
SN75185N	N	PDIP	20	20	506	13.97	11230	4.32

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

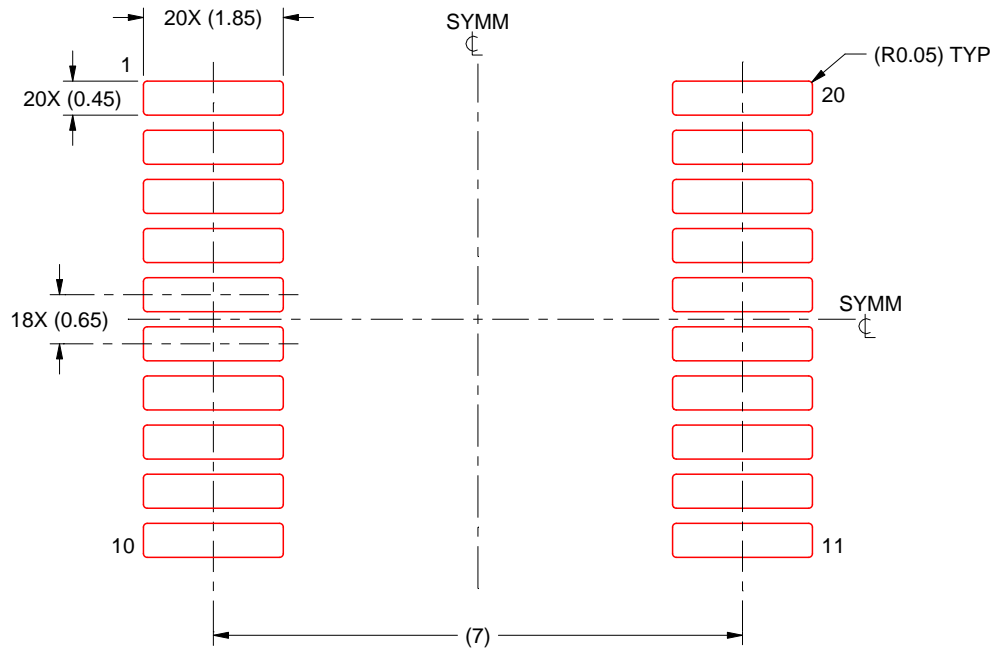
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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