

## 具有过流限制的 3.3V 至 18V 电源多路复用器 (MUX)

 查询样品: [TPS22980](#)

### 特性

- 3.3V 电源供电
- 4.5V 至 19.8V 高电压开关
- 3V 至 3.6V 开关
- 可调节限流
- 热关断
- 先合后断开关
- 低电压闭合之前的高电压放电
- 反向电流阻断

### 应用

- 笔记本电脑
- 台式机
- 电源管理系统

### 说明

TPS22980 是一款限流型电源 mux，此器件可从一个低电压电源（3.0V 到最高 3.6V）或者一个高电压电源（5V 到最高 18V）提供到一个外围器件的连接。由数字控制信号选择所需的输出。

高电压 (VHV) 和低电压 (V3P3) 开关电流限值由外部电阻设定。一旦达到电流限值，TPS22980 将控制此开关以将电流保持在限值上。

当此高电压电源不在时，TPS22980 将保持到低电压电源输出的连接。高电压线路和高压使能信号出现时，此高压开关将会与低电压开关一同打开直到在低压开关上侦测到反向电流。这一功能能在最小下降电流和击穿电流的情况下实现低压电源至高压电源的无缝转换。

为了防止 VHV 连接到 V3P3 连接转换期间的电流回流，TPS22980 将断开 VHV 连接并将输出放电至接近 3.3V。一旦输出达到 3.3V，此器件将接通 V3P3 开关。如果负载出现，则此输出在返回 3.3V 前转换为 0V。

TPS22980 采用 4mm x 4mm x 1mm 四方平面无引线 (QFN) 封装。

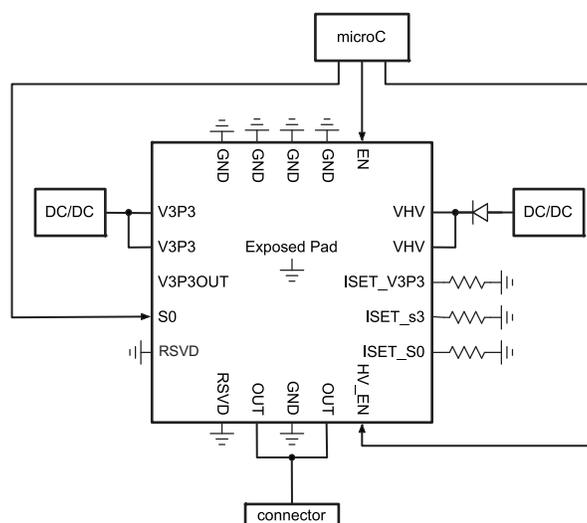


图 1. 典型应用



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# TPS22980

ZHCS595B – DECEMBER 2011 – REVISED APRIL 2012

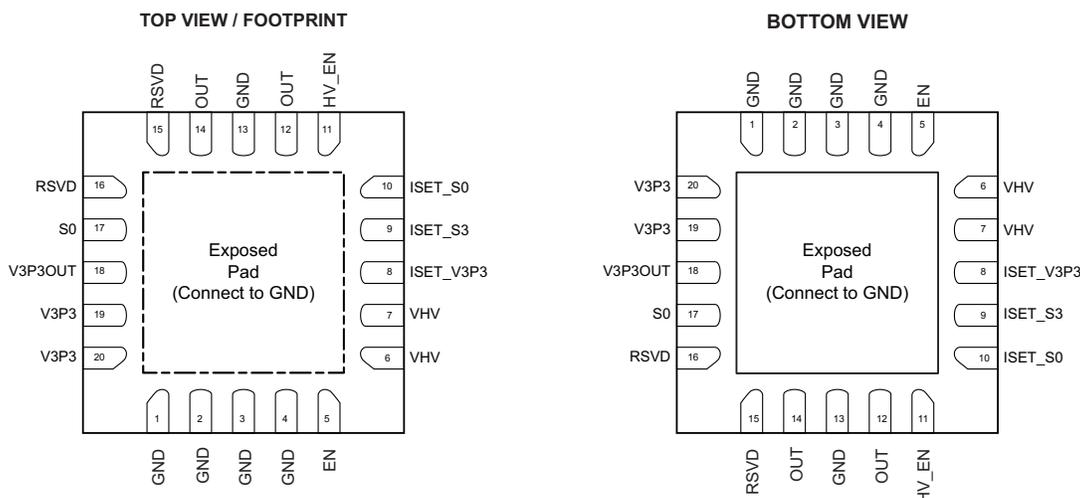
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE	DEVICE SPECIFIC FEATURES
TPS22980RGP	PS22980	RGP	Tape and Reel



Package Size: 4mm x 4mm x 1mm height, Pad Pitch: 0.5mm

## PIN FUNCTIONS

PIN		DESCRIPTION
NO.	NAME	
1	GND	Device ground
2		
3		
4		
5	EN	Device Enable.
6	VHV	High voltage power supply input. Place a minimum of 0.1µF capacitor as close to this pin as possible.
7		
8	ISET_V3P3	Sets the current limit for V3P3. Place resistor between this pin and GND. See Equation 1 to calculate resistor value.
9	ISET_S3	Sets the current limit for VHV in S3 mode. Place resistor between this pin and GND. See Equation 1 to calculate resistor value.
10	ISET_S0	Sets the current limit for VHV in S0 mode. Place resistor between this pin and GND. See Equation 1 to calculate resistor value.
11	HV_EN	High voltage output enable.
12, 14	OUT	Power output. Place a minimum of 1µF capacitor as close to this pin as possible.
13	GND	Device ground.
15	RSVD	Reserved. Must Tie to GND.
16		
17	S0	When this pin is asserted, the device is put in S0 mode. Otherwise the device operates in S3 mode.
18	V3P3OUT	3.3V bypass output. Place a minimum of 0.1µF capacitor as close to this pin as possible.
19	V3P3	3.3V power supply input. Place a minimum of 0.1µF capacitor as close to this pin as possible.
20		
EP	GND	

## ABSOLUTE MAXIMUM RATINGS

 over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		VALUE	UNIT
V <sub>I</sub>	Input voltage range on V3P3 (VDD) <sup>(3)</sup>	–0.3 to 3.6	V
	Input voltage range on EN, HVEN, ISET_V3P3, ISET_S0, ISET_S3, S0 <sup>(3)</sup>	–0.3 to V3P3+0.3	
	Input voltage range on VHV <sup>(3)</sup>	–0.3 to 20	
	Output voltage range at OUT <sup>(3)</sup>	–0.3 to 20	
	Output voltage range at V3P3OUT <sup>(3)</sup>	–0.3 to V3P3+0.3	
T <sub>A</sub>	Operating ambient temperature range	–40 to 85	°C
T <sub>J (MAX)</sub>	Maximum operating junction temperature	110	°C
T <sub>stg</sub>	Storage temperature range	–65 to 150	°C
ESD Rating	Charge Device Model (JESD 22 C101)	500	V
	Human Body Model (JESD 22 A114)	2	kV

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature [T<sub>A(max)</sub>] is dependent on the maximum operating junction temperature [T<sub>J(max)</sub>], the maximum power dissipation of the device in the application [P<sub>D(max)</sub>], and the junction-to-ambient thermal resistance of the part/package in the application (θ<sub>JA</sub>), as given by the following equation: T<sub>A(max)</sub> = T<sub>J(max)</sub> – (θ<sub>JA</sub> × P<sub>D(max)</sub>)
- (3) All voltage values are with respect to network ground terminal.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TPS22980	UNITS
		RGP	
		16 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	38.9	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance	30.7	
θ <sub>JB</sub>	Junction-to-board thermal resistance	11.5	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	11.4	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	2.2	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

**RECOMMENDED OPERATING CONDITIONS**

			MIN	MAX	UNIT
V <sub>3P3</sub>	Supply voltage range		3.0	3.6	V
V <sub>HV</sub>			4.5	19.8	V
I <sub>LIM3P3OUT</sub>	V3P3OUT Switch current range		0	500	mA
V <sub>IH</sub>	Input logic high	EN, HV_EN, S0	V3P3-0.6	V3P3	V
V <sub>IL</sub>	Input logic low	EN, HV_EN, S0	0	0.6	V
R <sub>SET_V3P3</sub>	3.3V switch current limit set resistance		25.3	402	kΩ
R <sub>SET_S0</sub>	VHV switch current limit in S0 mode set resistance		25.3	402	kΩ
R <sub>SET_S3</sub>	VHV switch current limit in S3 mode set resistance		25.3	402	kΩ

**ELECTRICAL CHARACTERISTICS**

Unless otherwise noted the specification applies over the V<sub>DD</sub> range and operating junction temp  $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ . Typical values are for V<sub>3P3</sub> = 3.3V, V<sub>HV</sub> = 15V, and T<sub>J</sub> = 25°C.

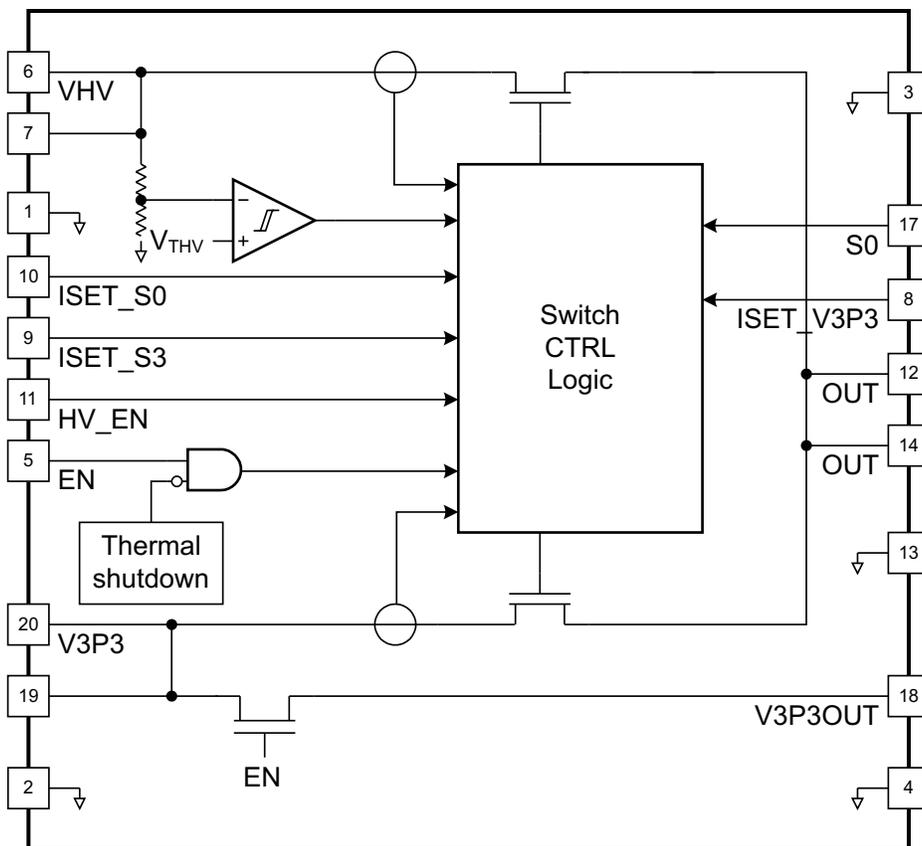
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLIES AND CURRENTS</b>						
V <sub>3P3</sub>	V3P3 Input voltage range		3	3.3	3.6	V
V <sub>HV</sub>	VHV Input voltage range		4.5		19.8	V
I <sub>VHVACT</sub>	Active quiescent current from VHV	HV_EN = 1, EN = 1			150	μA
I <sub>VHVSD</sub>	Shutdown leakage current from VHV	HV_EN = 0, EN = 0 or 1			30	μA
I <sub>DDACT</sub>	Active quiescent current from V3P3	EN = 1, HV_EN = 0			200	μA
I <sub>DDACTHV</sub>	Active quiescent current from V3P3	EN = 1, HV_EN = 1			150	μA
I <sub>DDSD</sub>	Shutdown Quiescent Current from V3P3	EN = 0, OUT = 0V			10	μA
I <sub>DIS</sub>	OUT Discharge Current	EN = 1, V <sub>HV</sub> = 5V HV_EN = 1 → 0	5		10	mA
I <sub>IN</sub>	HV_EN, EN, S0, S3 Input pin leakage	V = 0 V			1	μA
		V = V3P3			1	μA
<b>SWITCH AND RESISTANCE CHARACTERISTICS</b>						
R <sub>SHV</sub>	VHV Switch resistance	V <sub>HV</sub> = 5 V to 18V, I <sub>VHV</sub> = 1.5 A			250	mΩ
R <sub>S3P3</sub>	V3P3 Switch resistance	V <sub>3P3</sub> = 3.3 V, I <sub>V3P3</sub> = 1.5 A			250	mΩ
R <sub>S3P3BYP</sub>	V3P3 Bypass switch resistance	V <sub>3P3</sub> = 3.3 V, I <sub>V3P3</sub> = 500 mA			500	mΩ
<b>VOLTAGE THRESHOLDS</b>						
V <sub>HVUVLO</sub>	VHV Under voltage lockout	VHV Input Falling	3.6	4		V
		VHV Input Rising		4	4.3	
V <sub>3P3UVLO</sub>	V3P3 Under voltage lockout	V3P3 Input Falling	1.8	2.25		V
		V3P3 Input Rising		2.25	2.5	
<b>THERMAL SHUTDOWN</b>						
T <sub>SD</sub>	Shutdown Temperature		110	120	130	°C
T <sub>SDHYST</sub>	Shutdown Hysteresis			10		°C

**ELECTRICAL CHARACTERISTICS (continued)**

Unless otherwise noted the specification applies over the  $V_{DD}$  range and operating junction temp  $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ . Typical values are for  $V_{3P3} = 3.3\text{V}$ ,  $V_{HV} = 15\text{V}$ , and  $T_J = 25^{\circ}\text{C}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CURRENT LIMIT</b>						
$I_{LIMHV}$	VHV Switch current limit state S0 or S3	$R_{SET\_S0,3} = 402\text{ k}\Omega$	100	110	150	mA
		$R_{SET\_S0,3} = 80.6\text{ k}\Omega$	495	525	555	
		$R_{SET\_S0,3} = 26.7\text{ k}\Omega$	1515	1575	1635	
$I_{LIM3P3}$	V3P3 Switch current limit	$R_{SET\_V3P3} = 402\text{ k}\Omega$	100	110	150	mA
		$R_{SET\_V3P3} = 80.6\text{ k}\Omega$	495	525	555	
		$R_{SET\_V3P3} = 26.7\text{ k}\Omega$	1515	1575	1635	
$I_{REV3P3}$	V3P3 Switch Reverse Current Limit		10	27	45	mA
$T_{V3P3RC}$	V3P3 Switch Reverse Current Response Time	$V_{OUT} = V_{3P3} \rightarrow V_{3P3} + 20\text{mV}$			100	$\mu\text{S}$
$T_{VHVSC}$	VHV Switch short circuit response time	$C_{OUT} = 20\text{ pF}$		8		$\mu\text{s}$
$T_{V3P3SC}$	V3P3 Switch short circuit response time	$C_{OUT} = 20\text{ pF}$		8		$\mu\text{s}$
<b>TRANSITION DELAYS</b>						
$T_{3P3OFF}$	VHV to V3P3 off time	$C_{OUT} = 1.1\mu\text{F}$ , $EN = 1$ , $HV\_EN = 1 \rightarrow 0$			6	ms
$T_{0-3.3V}$	0V to 3.3V ramp time	$C_{OUT} \leq 20\text{ pF}$			6	ms
$T_{3.3V-VHV}$	3.3V to VHV ramp time	$C_{OUT} \leq 20\text{ pF}$			6	ms
$T_{VHV-3.3V}$	VHV to 3.3V ramp time	$C_{OUT} \leq 20\text{ pF}$			23	ms
$T_{LIM}$	Overcurrent response time	$C_{OUT} \leq 20\text{ pF}$			0.5	ms

**FUNCTIONAL BLOCK DIAGRAM**



## APPLICATION INFORMATION

### CURRENT LIMIT

The TPS22980 provides current limiting in the power switches. Both the VHV supply current limit and the V3P3 supply current limit are adjustable by external resistors.

Figure 2 shows a simplified view of the TPS22980 current limit function. Both the VHV supply current limit and the V3P3 supply current limit are adjustable by external resistors.

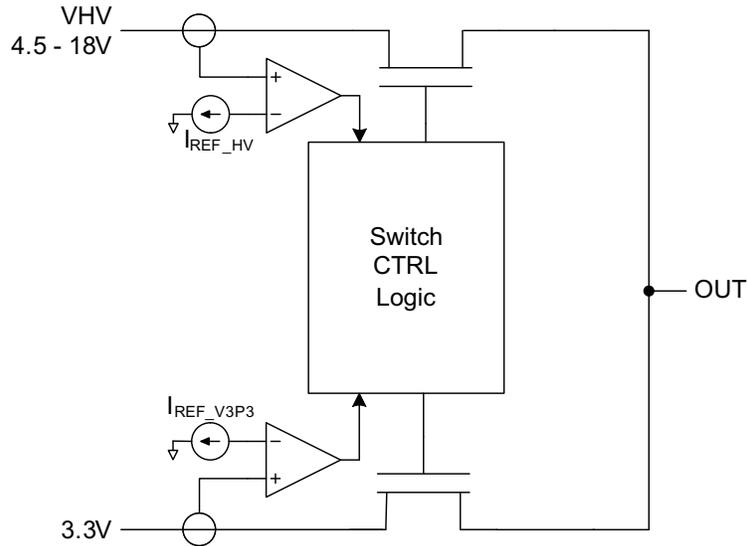


Figure 2. Simplified Current Limit Diagram

The current limit thresholds,  $I_{REF\_HV}$  and  $I_{REF\_V3P3}$ , are set with three external resistors as shown in Figure 3. When the TPS22980 is passes the V3P3 voltage, the current limit is set by  $R_{ISET\_V3P3}$ . The VHV path has two modes that support two different current limits which are selected by the S0 pin. When S0 is asserted high,  $R_{ISET\_S0}$  sets the current limit. When S0 is low,  $R_{ISET\_S3}$  sets the current limit. This allows the system to have two separate VHV current limits for different modes such as active and sleep.

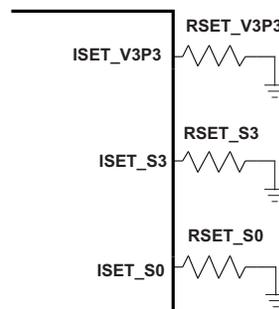


Figure 3. External  $R_{SET}$  Resistances to Set Current Limits

## CURRENT LIMIT THRESHOLD

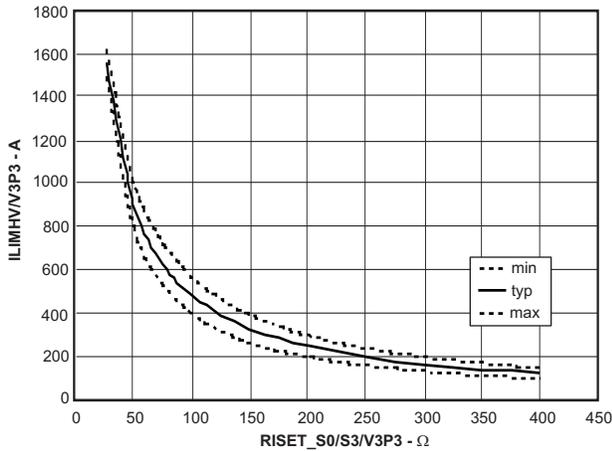


Figure 4.  $I_{LIM}$  vs  $R_{SET}$  for VHV and V3P3

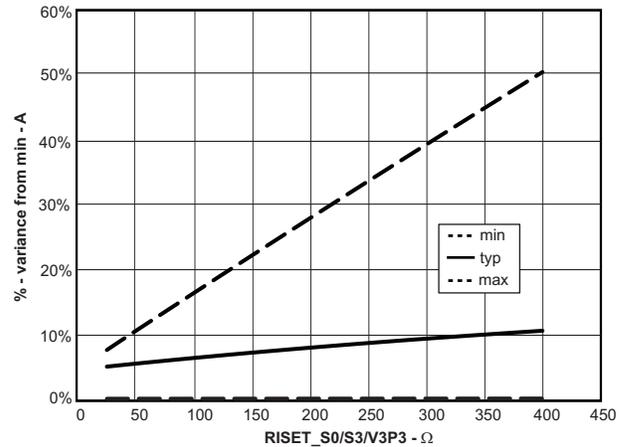


Figure 5. Percent Variance from min  $I_{LIM}$  vs  $R_{SET}$

Figure 4 shows the minimum, typical, and maximum current limit for either supply versus its corresponding  $R_{SET}$  value. Equation 1 is used to determine the  $R_{SET}$  needed to set a minimum  $I_{LIM}$  for a given supply and mode. Figure 5 shows the approximate variation from the set minimum  $I_{LIM}$  value to the typical and maximum  $I_{LIM}$  values.

$$R_{SET} = \frac{40 \text{ k}\Omega \times \text{Amps}}{I_{LIMmin}} \quad (1)$$

where:

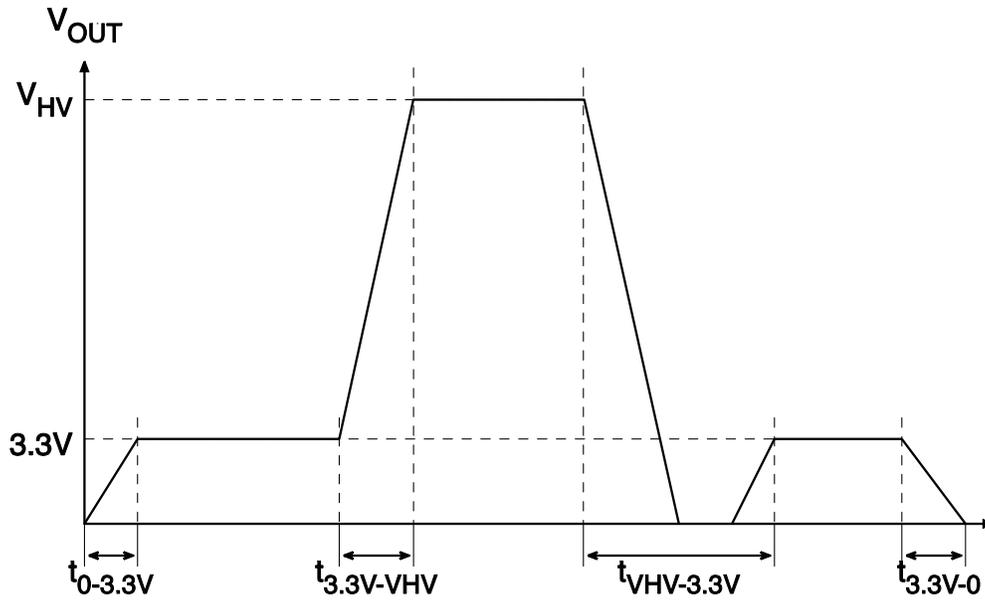
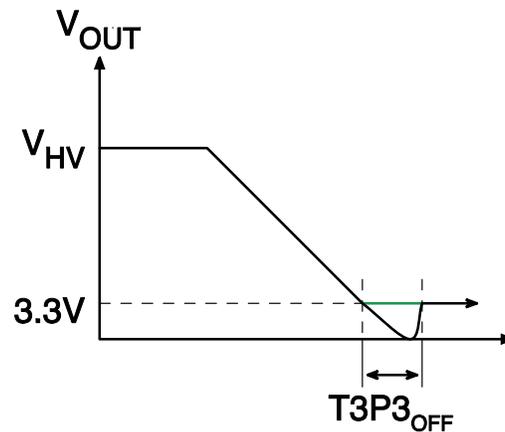
$R_{SET}$  = external resistor used to set the current limit for V3P3, VHV (S0), or VHV (S3), and

$I_{LIMmin}$  = current limit for V3P3, VHV (S0), or VHV (S3) set by the external  $R_{SET}$  resistor.

Each resistor is placed between the corresponding ISET pin and GND, as shown in Figure 3, providing a minimum current limit between 100mA and 1.5A.

## TRANSITION DELAYS

Output transitions of the TPS22980 voltages are shown in Figure 6. When the device transitions from VHV to V3P3 at the output, the power switches both turn off until the output falls to near the V3P3 voltage. During this time, a discharge current ( $I_{DIS}$ ) pulls OUT down. If a load on the line is also pulling OUT down, the output can drop to 0V due to the switch off time of T3P3OFF. Figure 7 shows the voltage drop on the output during this transition with no output capacitance.


**Figure 6. Allowable Voltage Transitions**

**Figure 7. Voltage Drop During Transitions from VHV**

## DIGITAL CONTROL SIGNALS

The voltage at OUT is controlled by two digital logic input signals, EN and HV\_EN. HV\_EN controls the state of the VHV switch and EN controls the state of V3P3 switch. [Table 1](#) lists the possible output states given the conditions of the digital logic signals.

**Table 1. Output State of OUT Given the States EN and HV\_EN**

EN	HV_EN	OUT
0	0	OPEN
0	1	OPEN
1	0	V3P3
1	1	VHV

Figure 8 shows possible combinations of EN and HV\_EN controlling OUT of the TPS22980.

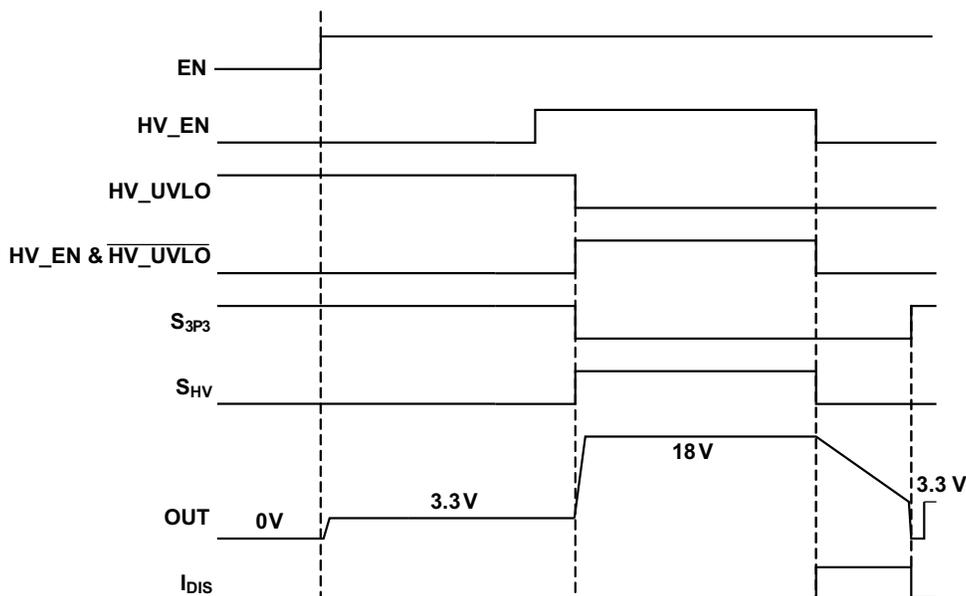


Figure 8. Logic Waveforms Displaying the Transition Between VHV and V3P3

### OVER-CURRENT LIMIT AND SHORT CIRCUIT PROTECTION

When the load at OUT attempts to draw more current than the limit set by the external RISET resistors for the V3P3 switch and VHV switch (for both S0 and S3 modes), the device will operate in a constant current mode while lowering the output voltage. Figure 9 shows the delay,  $t_{LIM}$ , which occurs when an over-current fault is detected until the output current is lowered to  $ILIMHV$  tolerances for VHV or  $ILIM3V3$  tolerances for V3P3 as shown in Figure 4.

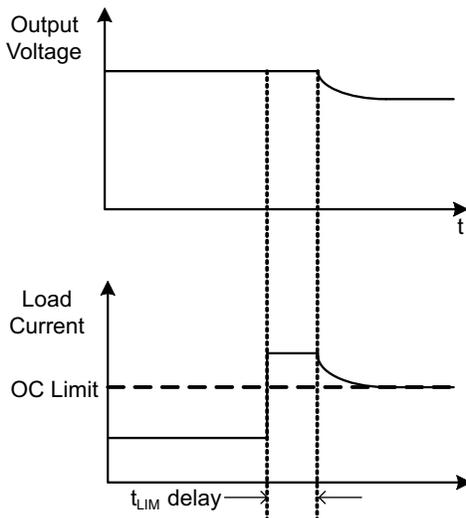


Figure 9. Overcurrent Output Response

All short circuit conditions are treated as over-current conditions. In the event of a short circuit, the device will limit the output current to the corresponding  $R_{SET}$  value and continue to do so until thermal shutdown is encountered or the short circuit condition is removed.

## Reverse Current Protection

Reverse current protection for the V3P3 supply to OUT triggers at  $I_{REV3P3}$  causing the V3P3 supply switch to open. When the HV\_EN signal is not asserted and reverse current protection is triggered, a discharge current source is turned on to bring the output voltage to 3.3V nominal.

## Thermal Shutdown

The device enters thermal shutdown when junction temperature reaches  $T_{SD}$ . The device will resume the previous state on power up once the junction temperature has dropped by  $10^{\circ}\text{C}$ . Connect thermal vias to the exposed GND pad underneath the device package for improved thermal diffusion.

## UVLO

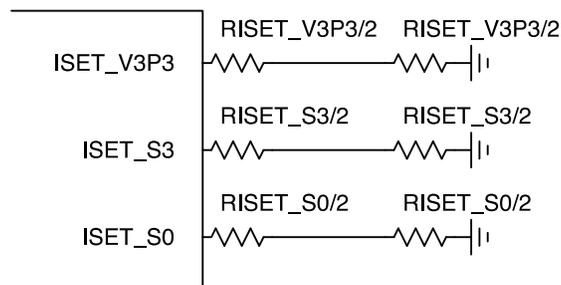
When the VHV rail reaches the under-voltage lockout threshold of  $V_{HVUVLO}$  while HV\_EN is high, the device will switch back to V3P3. Once the UVLO condition has cleared, the device will switch to VHV again. When the V3P3 rail reaches the under-voltage lockout threshold of  $V_{3P3UVLO}$ , regardless of the states of any digital logic controls, the device will open all switches and enter a reset condition.

## Input Inductive Bounce at Short Circuit

When the TPS22980 is operating at high currents and high input voltage on VHV, a short circuit condition can cause the input to exceed the maximum safe operating condition for VHV. When a significant inductance is present at the VHV input, sudden turn off of current through the device may produce a large enough inductive voltage bounce that exceeds the maximum safe operating condition and may damage the TPS22980. To prevent this, reduce any inductance at the input. Input capacitors, such as  $4.7\mu\text{F}$ , can reduce the supply bounce and are recommended.

## Single Point Failure Protection

The TPS22980 current limits are set by the R<sub>ISSET</sub> resistances. Shorting one of these resistance would result in a single point failure that removes the current limiter for that particular input and mode. Without current limiting, an excessive current load may damage the TPS22980 and the system. To prevent a single point failure from occurring, the R<sub>ISSET</sub> resistances can be divided into two series resistances each as shown in [Figure 10](#). Failure of a single resistance will not result in runaway current and damage.



**Figure 10. R<sub>ISSET</sub> Division to Prevent Single Point Failure**

## REVISION HISTORY

<b>Changes from Original (December 2011) to Revision A</b>	<b>Page</b>
• Changed 图1. 典型应用 .....	1
• Added bottom view pin out information. ....	2
• Updated Pin Functions Table. ....	2
• Added reverse current and thermal shutdown parameters to the ELECTRICAL CHARACTERISTICS table. ....	4
• Updated the APPLICATION INFORMATION section. ....	6
<hr/>	
<b>Changes from Revision A (February 2012) to Revision B</b>	<b>Page</b>
• Changed bottom view pin out information. ....	2

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22980RGPR	ACTIVE	QFN	RGP	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS22980	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

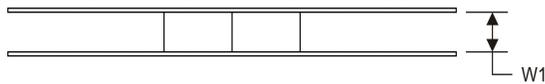
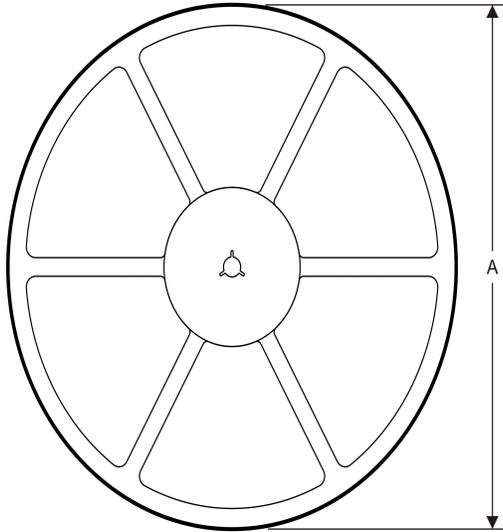
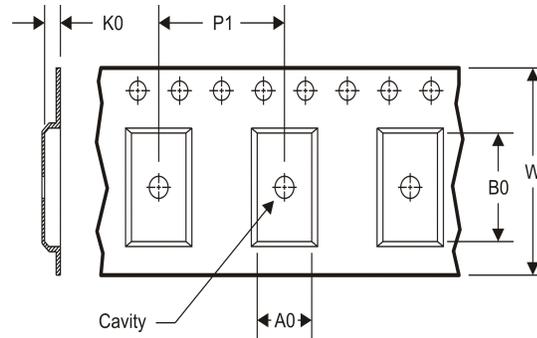
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


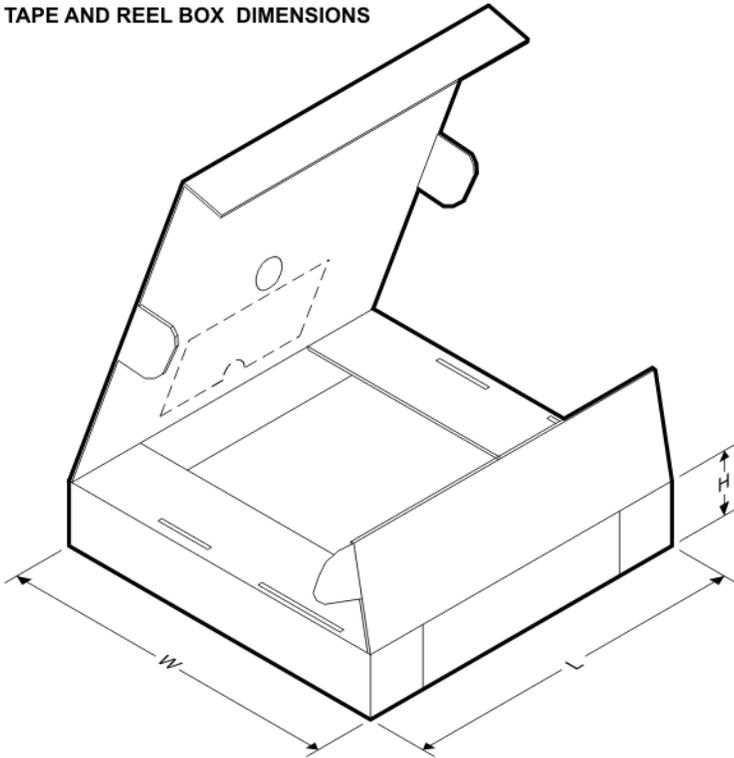
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22980RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22980RGPR	QFN	RGP	20	3000	367.0	367.0	35.0

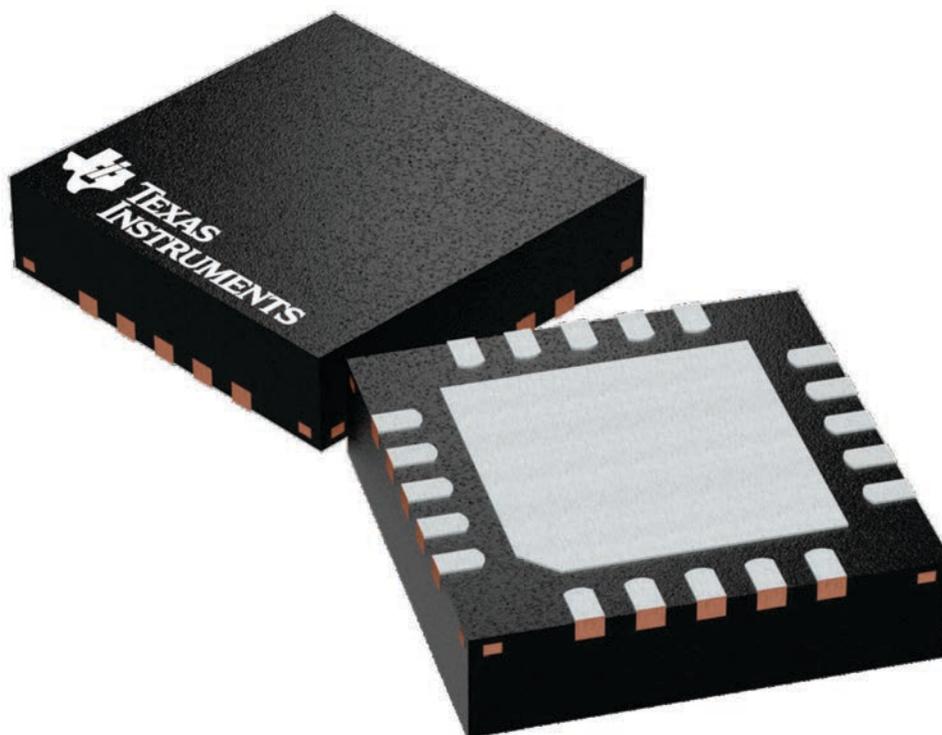
## GENERIC PACKAGE VIEW

**RGP 20**

**VQFN - 1 mm max height**

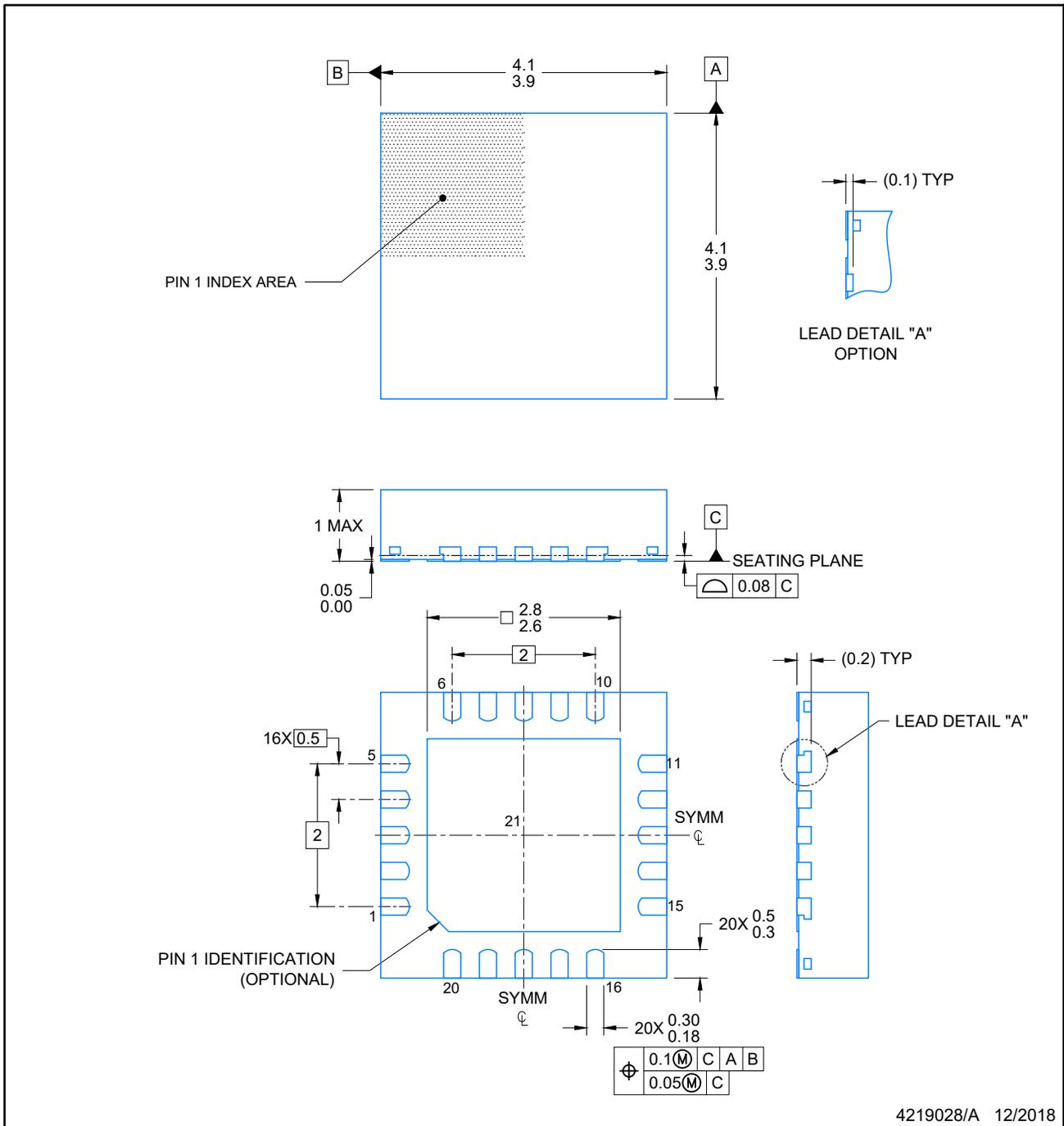
4 x 4, 0.5 mm pitch

VERY THIN QUAD FLATPACK



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224735/A



4219028/A 12/2018

NOTES:

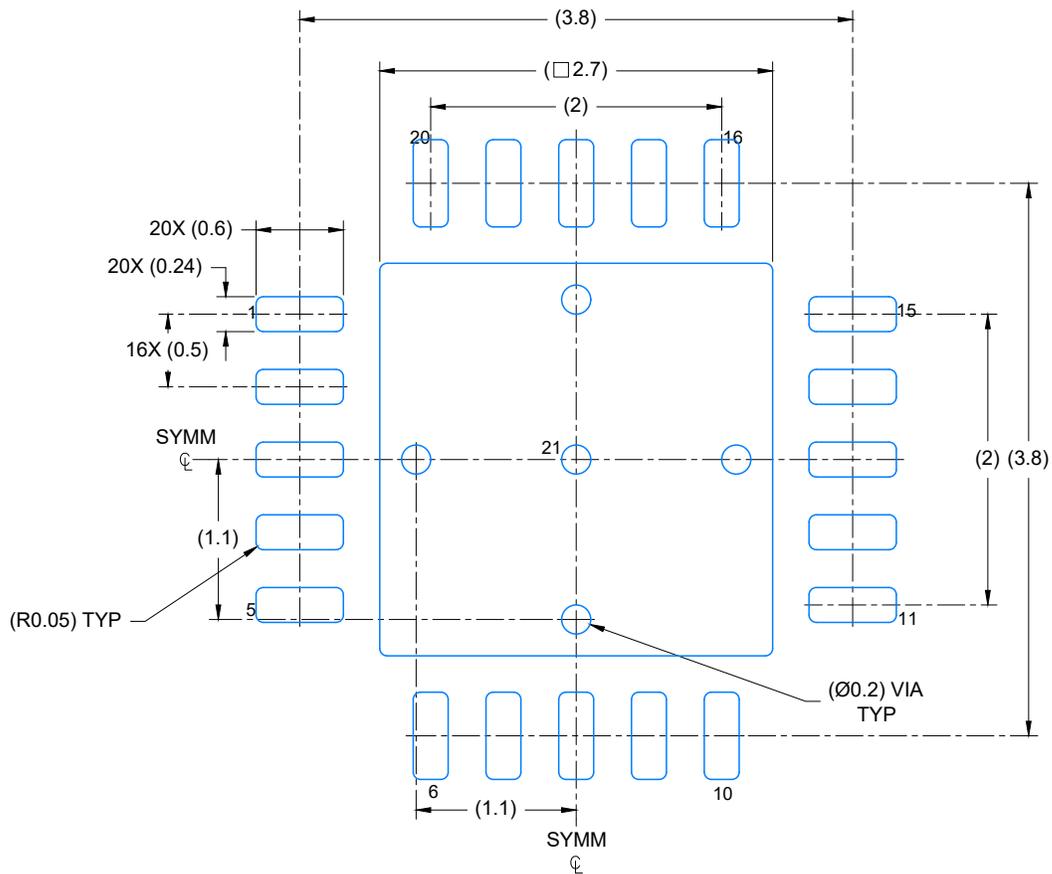
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

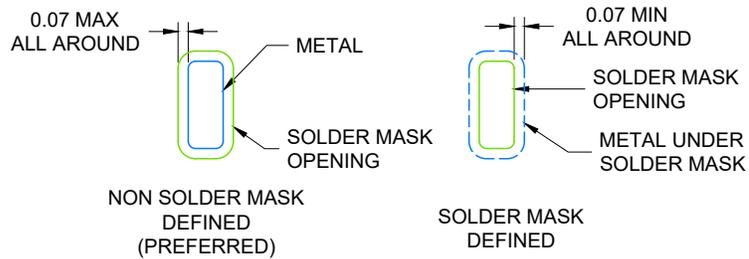
VQFN - 1 mm max height

RGP0020D

PLASTIC QUAD FLATPACK- NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



SOLDER MASK DETAILS

4219028/A 12/2018

NOTES: (continued)

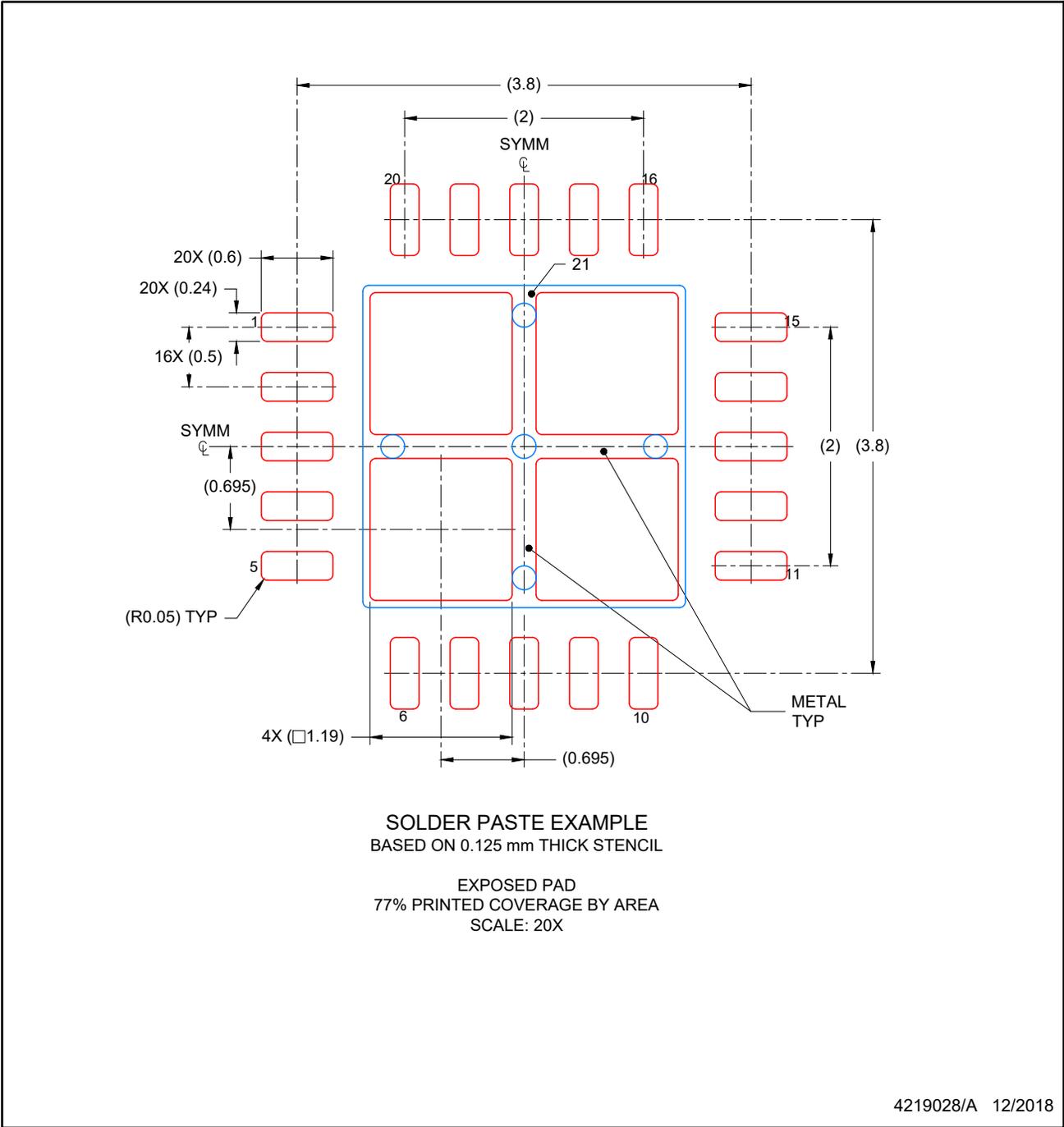
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGP0020D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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