CSD23285F5 -12V P 通道 FemtoFET™ MOSFET

1 特性

- 低导通电阻
- 低 Q_g和 Q_{gd}
- 超小尺寸
  - 1.53mm x 0.77mm
  - 0.5mm 焊盘间距
- 薄型
  - 高度为 0.35mm
- 集成型静电放电 (ESD) 保护二极管
  - 额定值 > 4kV 人体放电模式 (HBM)
  - 额定值 > 2kV 组件充电模式 (CDM)
- 无铅且无卤素
- 符合 RoHS 环保标准

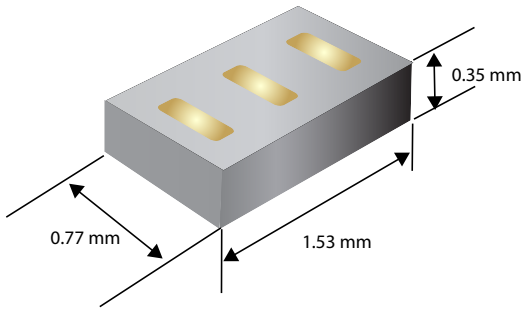
2 应用范围

- 针对负载开关应用进行了 优化
- 针对通用开关应用进行了 应用

3 说明

这款 29mΩ、–12V P 沟道 FemtoFET™MOSFET 技术经过了设计和优化，能够以最大限度减小许多手持式和移动类应用中的 封装尺寸。这项技术能够在替代标准小信号 MOSFET 的同时大幅减小封装尺寸。

典型部件尺寸



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	-12		V
Q_g	栅极电荷总量 (-4.5V)	3.2		nC
Q_{gd}	栅极电荷（栅极到漏极）	0.48		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = –1.5V	64	mΩ
		V_{GS} = -1.8V	49	
		V_{GS} = -2.5V	38	
		V_{GS} = -4.5V	29	
$V_{GS(th)}$	阈值电压	–0.65		V

器件信息(1)

器件	数量	包装介质	封装	运输
CSD23285F5	3000	7 英寸卷带	Femto 1.53mm × 0.77mm SMD 无引线	卷带式
CSD23285F5T	250			

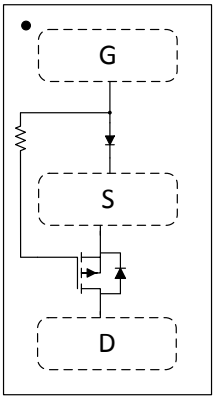
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	-12	V
V_{GS}	栅源电压	-6	V
I_D	持续漏极电流(1)	–3.3	A
	持续漏极电流(2)	–5.4	
I_{DM}	脉冲漏极电流(1)(3)	–31	A
P_D	功率耗散(1)	0.5	W
	功率耗散(2)	1.4	
$V_{(ESD)}$	人体模型 (HBM)	4000	V
	组件充电模式 (CDM)	2000	
T_J, T_{stg}	工作结温，储存温度	-55 至 150	°C

(1) $R_{\theta JA}$ = 245°C/W（覆铜面积最小时的典型值）。
(2) $R_{\theta JA}$ = 90°C/W（覆铜面积最大时的典型值）。
(3) 脉冲持续时间 ≤ 100µs，占空比 ≤ 1%。

顶视图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

目录

1 特性 1
2 应用范围 1
3 说明 1
4 修订历史记录 2
5 **Specifications** 3
5.1 Electrical Characteristics 3
5.2 Thermal Information 3
5.3 Typical MOSFET Characteristics 4
6 器件和文档支持 7
6.1 接收文档更新通知 7
6.2 社区资源 7
6.3 商标 7
6.4 静电放电警告 7
6.5 Glossary 7
7 机械、封装和可订购信息 8
7.1 机械尺寸 8
7.2 推荐的最小 PCB 布局 9
7.3 推荐的模板布局 9

4 修订历史记录

Changes from Original (August 2016) to Revision A **Page**

- 已添加 表 1 添加到了*机械尺寸* 部分 8

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = –250 μA	–12			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –9.6 V			–100	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –5 V			–25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 μA	–0.40	–0.65	–0.95	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.5 V, I_{DS} = –1 A		64	130	mΩ
		V_{GS} = –1.8 V, I_{DS} = –1 A		49	80	
		V_{GS} = –2.5 V, I_{DS} = –1 A		38	47	
		V_{GS} = –4.5 V, I_{DS} = –1 A		29	35	
g_{fs}	Transconductance	V_{DS} = –1.2 V, I_{DS} = –1 A		8.9		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = –6 V, f = 1 MHz		483	628	pF
C_{oss}	Output capacitance			305	397	pF
C_{rss}	Reverse transfer capacitance			37	48	pF
R_G	Series gate resistance			17		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –6 V, I_{DS} = –1 A		3.2	4.2	nC
Q_{gd}	Gate charge gate-to-drain			0.48		nC
Q_{gs}	Gate charge gate-to-source			0.66		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.40		nC
Q_{oss}	Output charge	V_{DS} = –6 V, V_{GS} = 0 V		4.8		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = –6 V, V_{GS} = –4.5 V, I_{DS} = –1 A, R_G = 2 Ω		15		ns
t_r	Rise time			5		ns
$t_{d(off)}$	Turnoff delay time			30		ns
t_f	Fall time			13		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = –1 A, V_{GS} = 0 V		–0.73	–1	V

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)		90		°C/W
	Junction-to-ambient thermal resistance(2)		245		

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

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5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

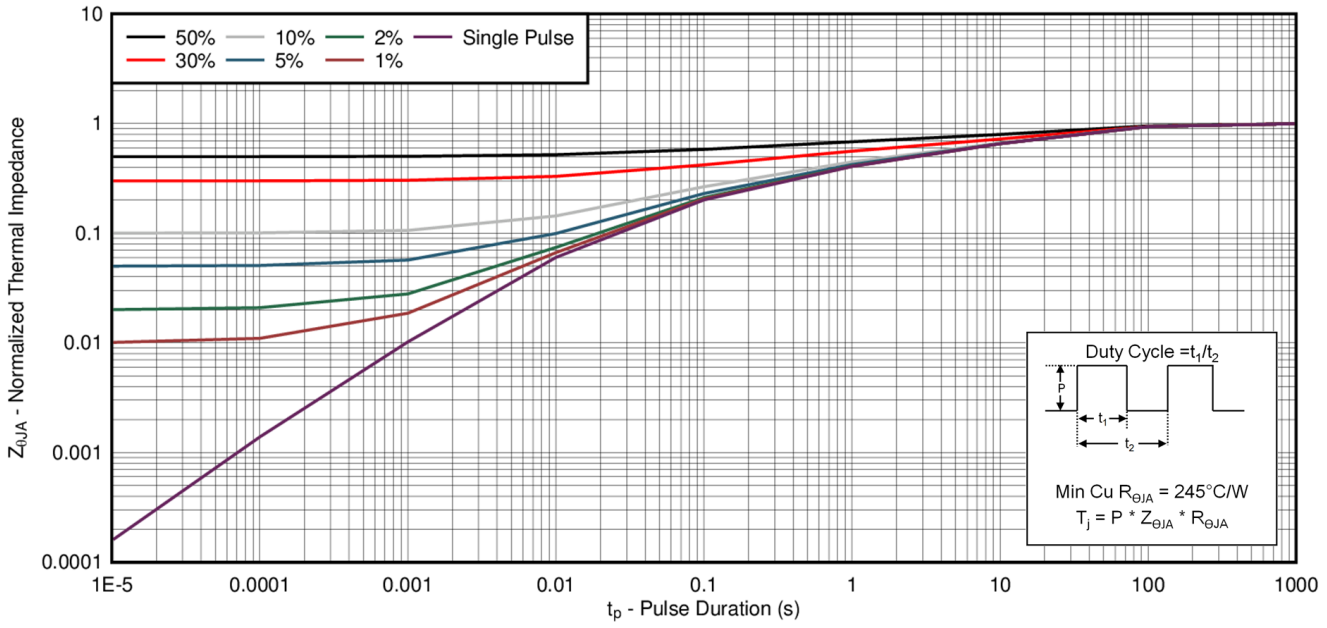


Figure 1. Transient Thermal Impedance

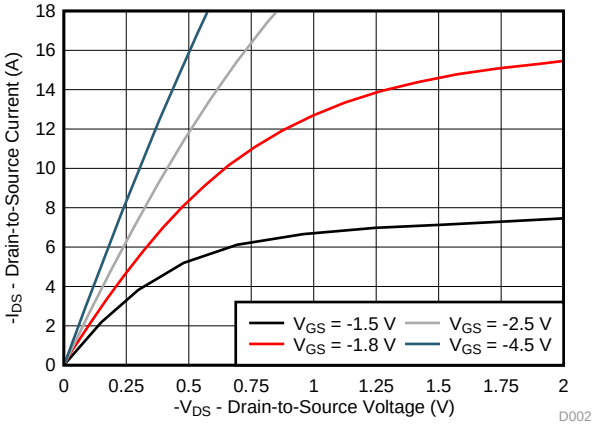


Figure 2. Saturation Characteristics

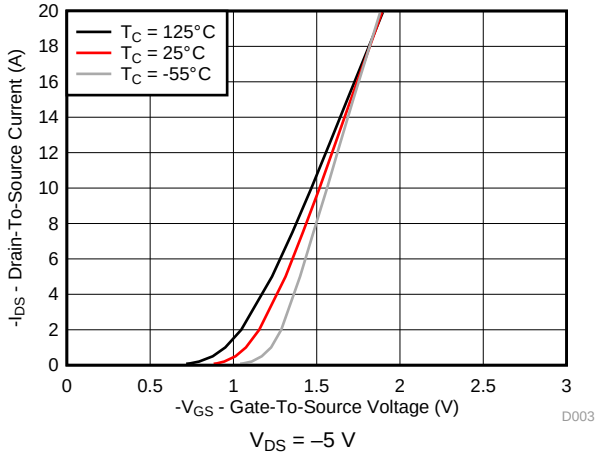


Figure 3. Transfer Characteristics

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Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

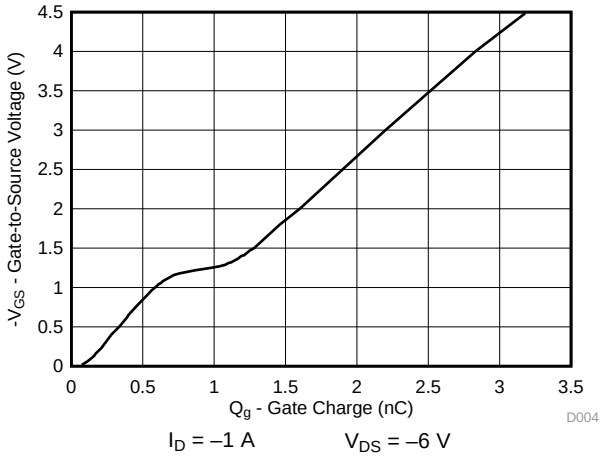


Figure 4. Gate Charge

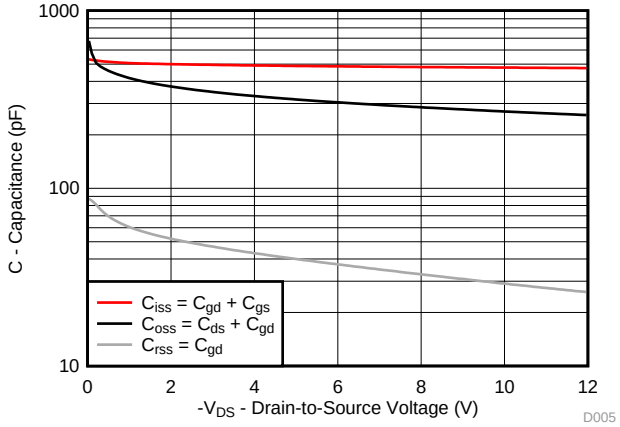


Figure 5. Capacitance

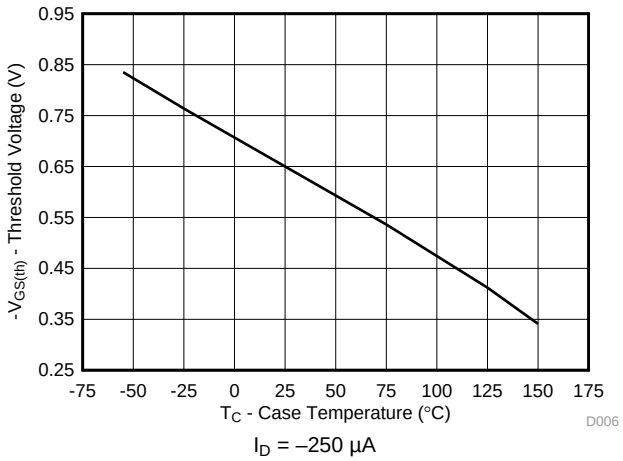


Figure 6. Threshold Voltage vs Temperature

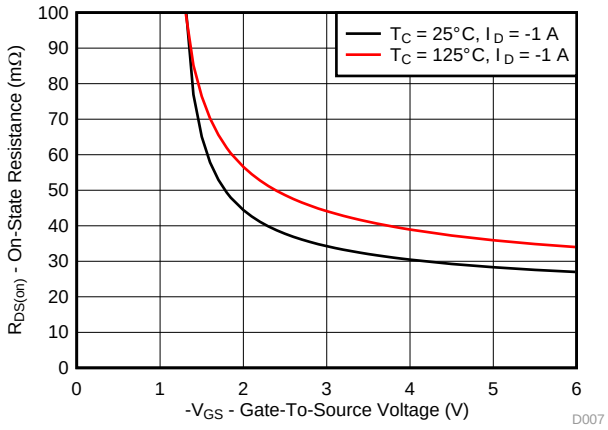


Figure 7. On-State Resistance vs Gate-to-Source Voltage

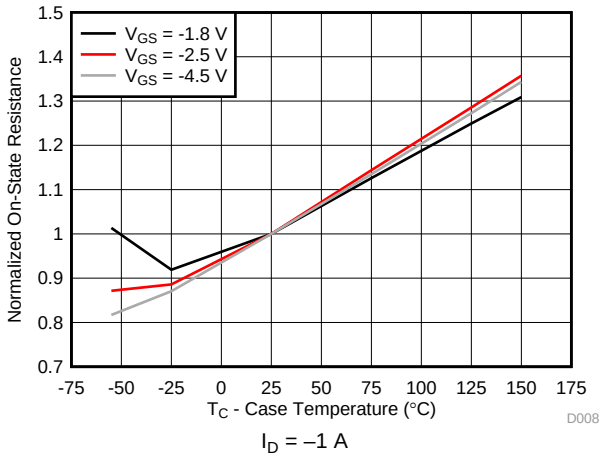


Figure 8. Normalized On-State Resistance vs Temperature

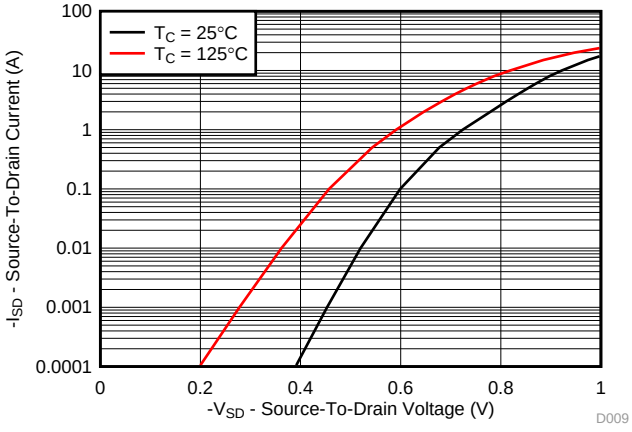
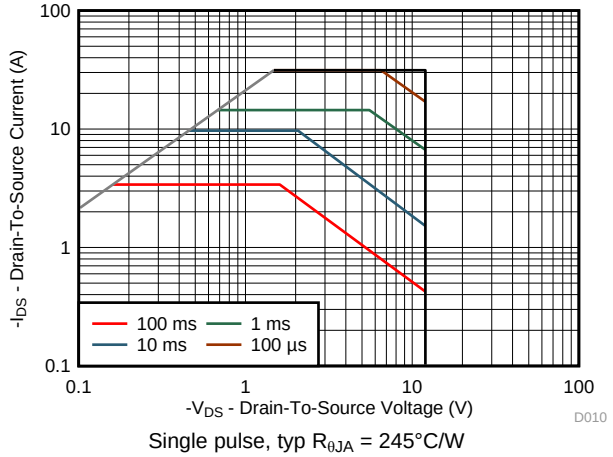


Figure 9. Typical Diode Forward Voltage

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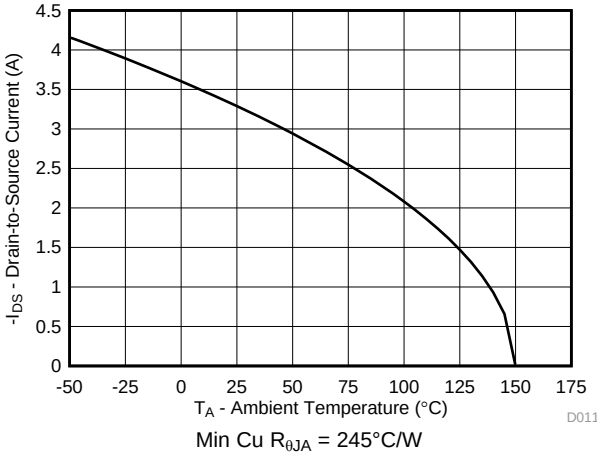
Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



Single pulse, typ $R_{\theta JA}$ = 245°C/W

Figure 10. Maximum Safe Operating Area (SOA)



Min Cu $R_{\theta JA}$ = 245°C/W

Figure 11. Maximum Drain Current vs Temperature

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6 器件和文档支持

6.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的*通知我*进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

6.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

6.3 商标

FemtoFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

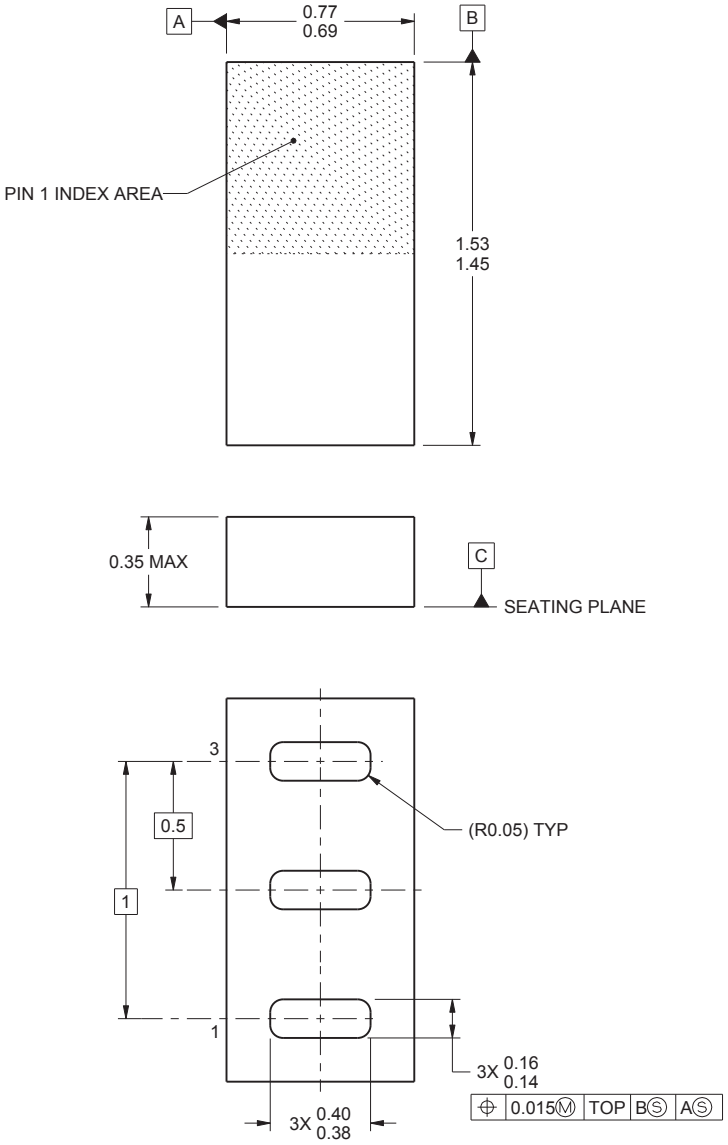
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

7.1 机械尺寸



(1) 所有线性尺寸的单位都是毫米（尺寸和容限值遵循 AME T14.5M-1994）。

(2) 本图纸如有变更，恕不通知。

(3) 此封装采用无铅焊盘设计。

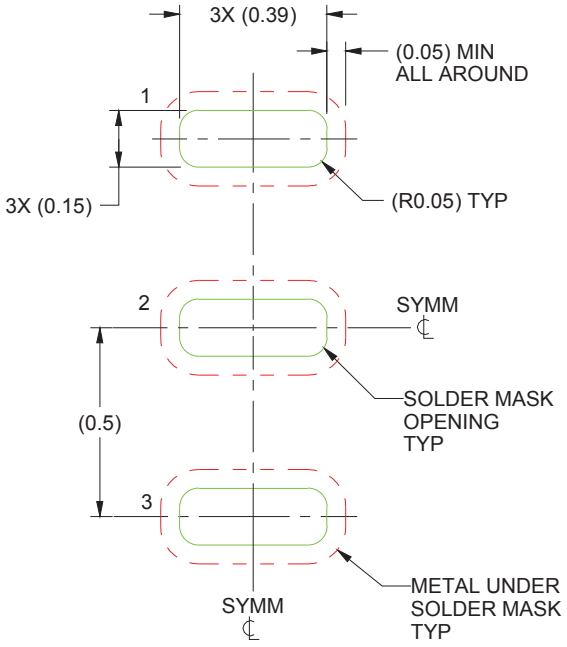
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表 1. 引脚配置

位置	名称
引脚 1	栅极
引脚 2	源极
引脚 3	漏极

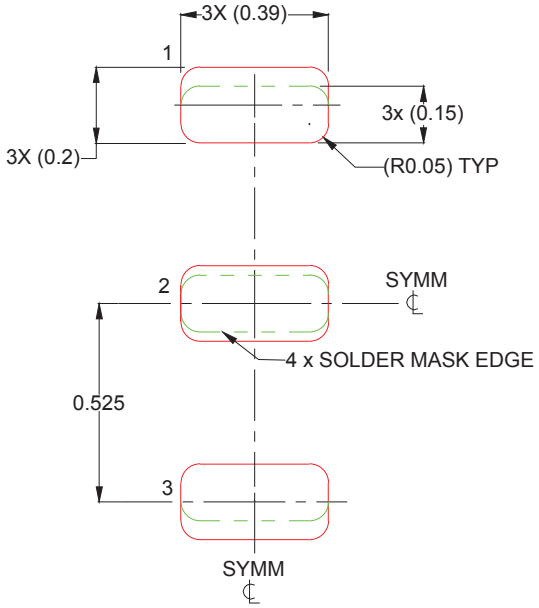
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7.2 推荐的最小 PCB 布局



(1) 所有尺寸的单位都是毫米。

7.3 推荐的模板布局



(1) 所有尺寸的单位都是毫米。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD23285F5	ACTIVE	PICOSTAR	YJK	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	4S	Samples
CSD23285F5T	ACTIVE	PICOSTAR	YJK	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	4S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

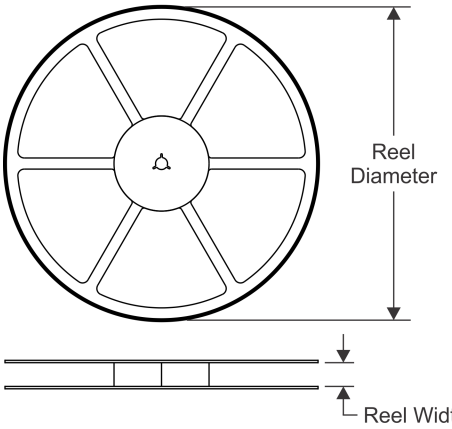
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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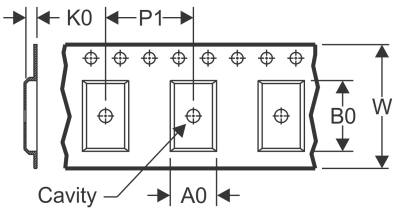
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

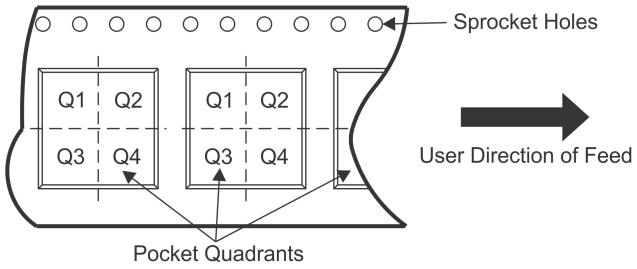


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

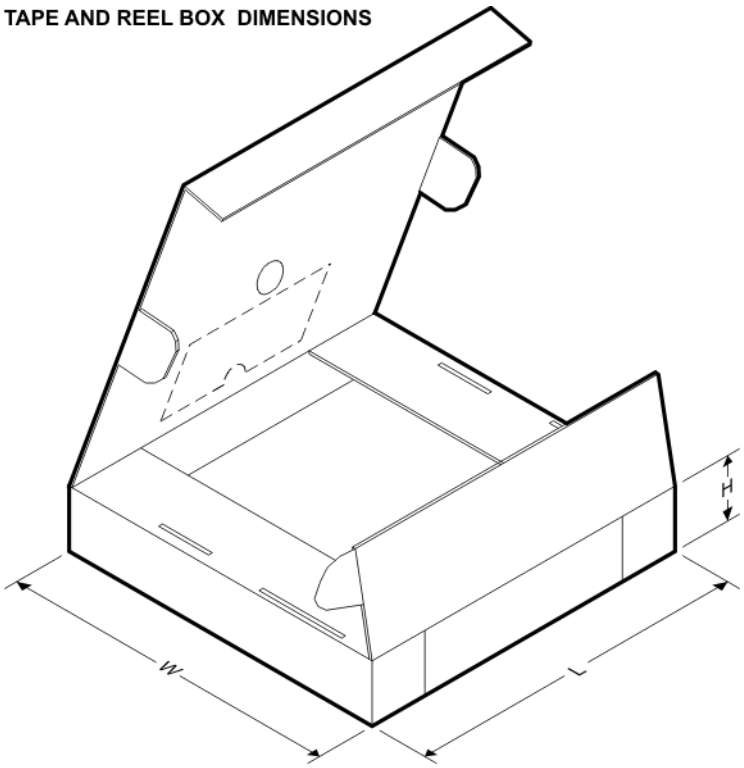
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD23285F5	PICOSTAR	YJK	3	3000	178.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD23285F5	PICOSTAR	YJK	3	3000	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD23285F5T	PICOSTAR	YJK	3	250	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD23285F5T	PICOSTAR	YJK	3	250	178.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD23285F5	PICOSTAR	YJK	3	3000	220.0	220.0	35.0
CSD23285F5	PICOSTAR	YJK	3	3000	182.0	182.0	20.0
CSD23285F5T	PICOSTAR	YJK	3	250	182.0	182.0	20.0
CSD23285F5T	PICOSTAR	YJK	3	250	220.0	220.0	35.0

重要声明和免责声明

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