TPD2E001 Low-Capacitance 2-Channel ESD-Protection for High-Speed Data Interfaces

1 Features

- IEC 61000-4-2 ESD Protection (Level 4)
  - ±8-kV Contact Discharge
  - ±15-kV Air-Gap Discharge
- IO Capacitance: 1.5 pF (Typ)
- Low Leakage Current: 1 nA (Maximum)
- Low Supply Current: 1 nA
- 0.9 V to 5.5 V Supply-Voltage Range
- Space-Saving DRL, DRY, and QFN Package Options
- Alternate 3, 4, 6-Channel options Available: TPD3E001, TPD4E001, TPD6E001

2 Applications

- USB 2.0
- Ethernet
- FireWire™
- LVDS
- SVGA Video Connections
- Glucose Meters
- Medical Imaging

3 Description

The TPD2E001 is a two-channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode array. The TPD2E001 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 Level 4 international standard.

The DRS package (3.00 mm x 3.00 mm) is also available as a non-magnetic package for medical imaging applications.

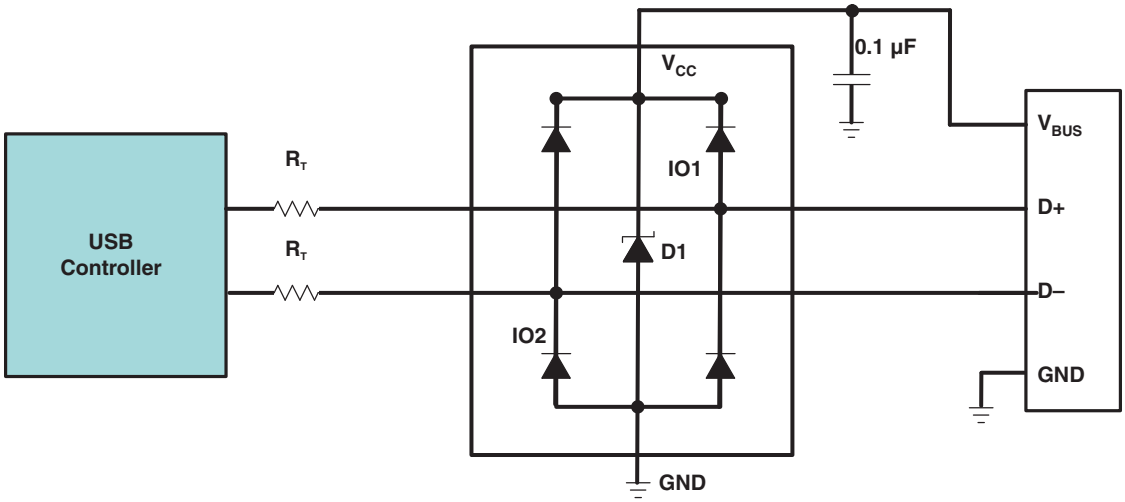
See also TPD2E2U06DRLR which is p2p compatible to TPD2E001DRLR and offers higher IEC ESD Protection, lower clamping voltage, and eliminates the input capacitor requirement.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD2E001	SOT (5)	1.60 mm x 1.20 mm
	WSON (6)	3.00 mm x 3.00 mm
	USON (6)	1.45 mm x 1.00 mm
	SOP (4)	2.90 mm x 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (August 2014) to Revision I	Page
• Updated the *ESDS* section	1
• Updated the *Handling Ratings* table to an *ESD Ratings* table and moved the T_{stg} to the *Absolute Maximum Ratings* table	4
• Added test condition frequency to capacitance	5
• Added note to the *Application and Implementation*	7
• Added *Community Resources*	9

Changes from Revision G (November 2013) to Revision H	Page
• Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision F (Feburary 2012) to Revision G	Page
• Updated document formatting.	1
• Updated Description.	1
• Removed Ordering Information table.	3

Changes from Revision E (June 2008) to Revision F	Page
• Added Medical Imaging to Applications.	1
• Added "The 3x3 mm DRS package is also available as a non-magnetic package for medical imaging application." to the description.	1
• Added 3 x 3 SON – DRS (Non-Magnetic) package to Ordering Information table.	3

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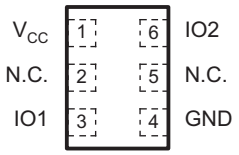
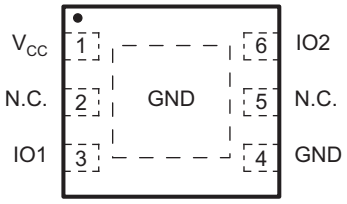
5 Pin Configuration and Functions

DRY Package
6-Pin USON
Top View



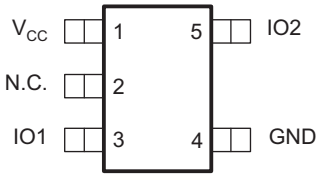
N.C. – Not internally connected

DRS Package
6-Pin WSON
Top View



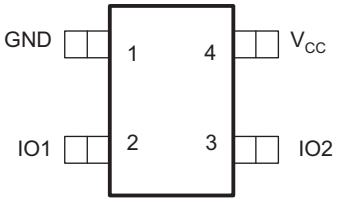
N.C. – Not internally connected

DRL Package
5-Pin SOT
Top View



N.C. – Not internally connected

DZD Package
4-Pin SOP
Top View



Pin Functions

PIN					DESCRIPTION
NAME	DRY NO.	DRL NO.	DRS NO.	DZD NO.	
EP	—	—	EP	—	Exposed pad. Connect to GND.
GND	4	4	4	1	Ground
IOx	3, 6	3, 5	3, 6	2, 3	ESD-protected channel
N.C.	2, 5	2	2, 5	—	No connection. Not internally connected.
V_{CC}	1	1	1	4	Power-supply input. Bypass V_{CC} to GND with a 0.1-µF ceramic capacitor.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Power pin voltage		–0.3	7	V
V_{IO}	IO pin voltage		–0.3	V_{CC} + 0.3	V
T_J	Junction temperature			150	°C
	Bump temperature (soldering)	Infrared (15 s)		220	°C
		Vapor phase (60 s)		215	
	Lead temperature (soldering, 10 s)			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±15000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: Surge Protection

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact	±8000	V
		IEC 61000-4-2 air-gap discharge	±15000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A, operating free-air temperature		–40	85	°C
Operating voltage	V_{CC} pin	0.9	5.5	V
	IO1, IO2 pins	0	V_{CC}	

6.5 Thermal Information

THERMAL METRIC[1]		TPD2E001				UNIT
		DRY (USON)	DRL (SOT)	DRS (WSON)	DZD (SOP)	
		5 PINS	5 PINS	6 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	374.2	257.6	91.9	213.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	223.4	97.6	106.9	93.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	227.8	74.2	64.8	56.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	52.9	7.5	10.2	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	224.8	73.7	64.9	56.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	87.5	N/A	29.9	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.6 Electrical Characteristics

V_{CC} = 5 V ± 10%, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{CC}	Supply voltage			0.9		5.5	V
I_{CC}	Supply current				1	100	nA
V_F	Diode forward voltage	I_F = 10 mA		0.65		0.95	V
V_{BR}	Breakdown voltage	I_{BR} = 10 mA		11			V
V_C	Channel clamp voltage(2)	T_A = 25°C, ±15-kV HBM, I_F = 10 A	Positive transients			V_{CC} + 25	V
			Negative transients			–25	
		T_A = 25°C, ±8-kV contact discharge (IEC 61000-4-2), I_F = 24 A	Positive transients			V_{CC} + 60	
			Negative transients			–60	
		T_A = 25°C, ±15-kV air-gap discharge (IEC 61000-4-2), I_F = 45 A	Positive transients			V_{CC} + 100	
			Negative transients			–100	
I_{IO}	Channel leakage current	$V_{I/O}$ = GND to V_{CC}		–1		1	nA
C_{IO}	Channel input capacitance	V_{CC} = 5 V, bias of V_{CC} / 2; f = 10 MHz			1.5		pF

(1) Typical values are at V_{CC} = 5 V and T_A = 25 °C
(2) Channel clamp voltage is not production tested.

6.7 Typical Characteristics

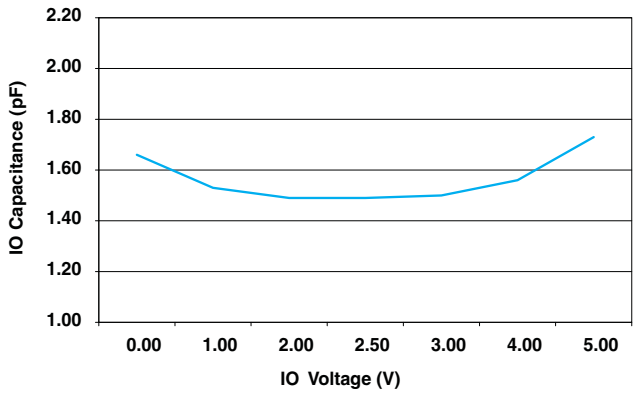


Figure 1. IO Capacitance vs IO Voltage (V_{CC} = 5 V)

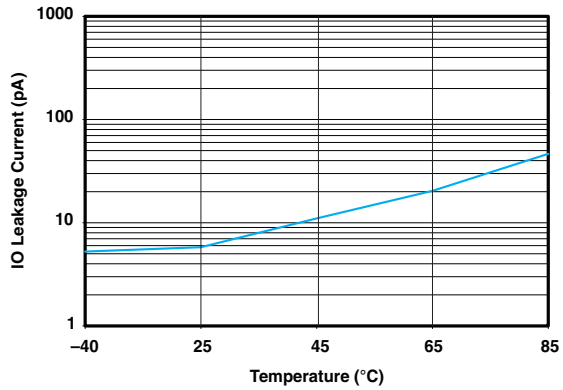


Figure 2. IO Leakage Current vs Temperature (V_{CC} = 5 V)

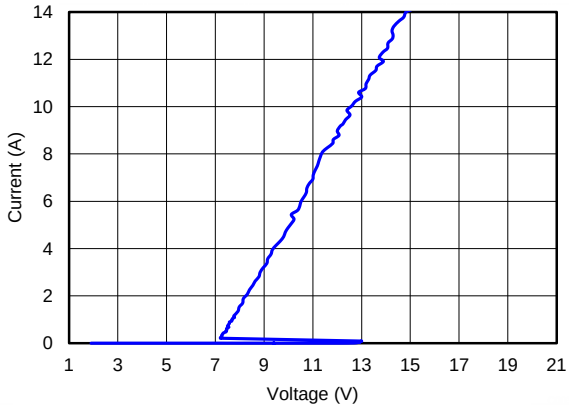


Figure 3. TLP IO to GND (DRS Package)

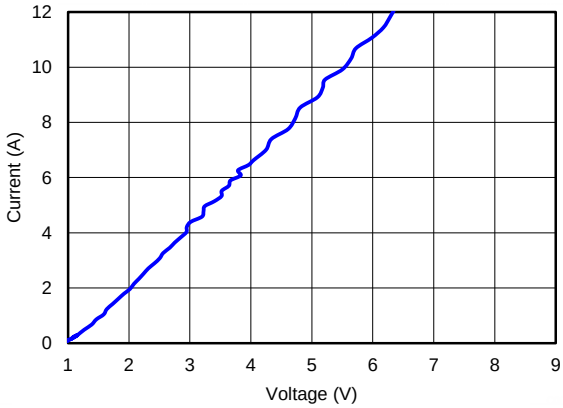


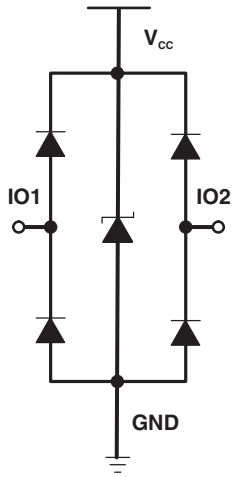
Figure 4. TLP GND to IO (DRS Package)

7 Detailed Description

7.1 Overview

The TPD2E001 is a two-channel transient voltage suppressor (TVS) based ESD protection diode array. The TPD2E001 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 Level 4 international standard.

7.2 Functional Block Diagram



7.3 Feature Description

TPD2E001 is a uni-directional ESD protection device with low capacitance. The device is constructed with a central ESD clamp that features two hiding diodes per line to reduce the capacitive loading. This central ESD clamp is also connected to V_{CC} to provide protection for the V_{CC} line. Each IO line is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 level 4 international standard. The TPD2E001's low loading capacitance makes it ideal for protection high-speed signal terminals.

7.4 Device Functional Modes

TPD2E001 is a passive integrated circuit that activates whenever voltages above V_{BR} or below the lower diodes $V_{forward}$ (–0.6V) are present upon the circuit being protected. During ESD events, voltages as high as ±15 kV can be directed to ground and V_{CC} via the internal diode network. Once the voltages on the protected lines fall below the trigger voltage of the TPD2E001 (usually within 10s of nanoseconds) the device reverts back to a high impedance state.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TPD2E001 is a diode array type Transient Voltage Suppressor (TVS) which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level to the protected IC.

8.2 Typical Application

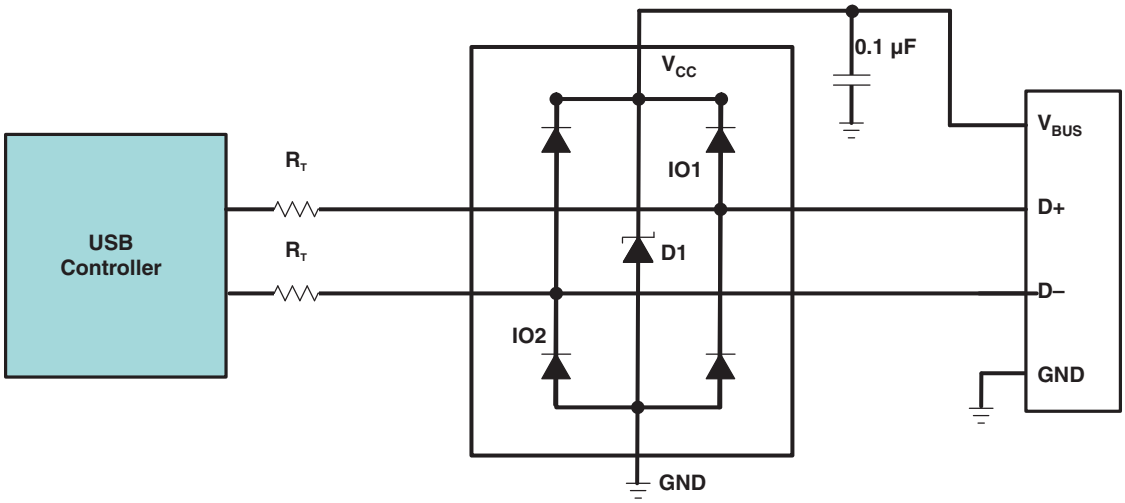

Figure 5. Typical USB Application Diagram

8.2.1 Design Requirements

For this design example, a single TPD2E001 is used to protect all pins of a USB 2.0 connector.

Given the USB application, Table 1 shows the Design Parameters:

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on IO1, and IO2	0 V to 5 V
Signal voltage range on V_{CC}	0 V to 5 V
Operating frequency	240 MHz

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal voltage range on all the protected lines
- Operating frequency

The V_{CC} pin can be connected in two different ways:

1. If the V_{CC} pin is connected to the system power supply, the TPD2E001 works as a transient suppressor for any signal swing above V_{CC} + V_F. A 0.1-µF capacitor on the device V_{CC} pin is recommended for ESD

bypass.

2. If the V_{CC} pin is not connected to the system power supply, the TPD2E001 can tolerate higher signal swing in the range up to 10 V. Please note that a 0.1-µF capacitor is still recommended at the V_{CC} pin for ESD bypass.

8.2.2.1 Signal Range on IO1 and IO2 and V_{CC} Pins

The TPD2E001 has 2 IO pins which support 0 to either 10 V or V_{CC} + $V_{forward}$ (depending on if the V_{CC} pin is connected to a V_{CC} line or has a 0.1 µF capacitor to ground).

9 Power Supply Recommendations

This device is a passive ESD protection device and there is no need to power it. Care should be taken to make sure that the maximum voltage specifications for each line are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

This application is typical of a differential data pair application, such a USB 2.0.

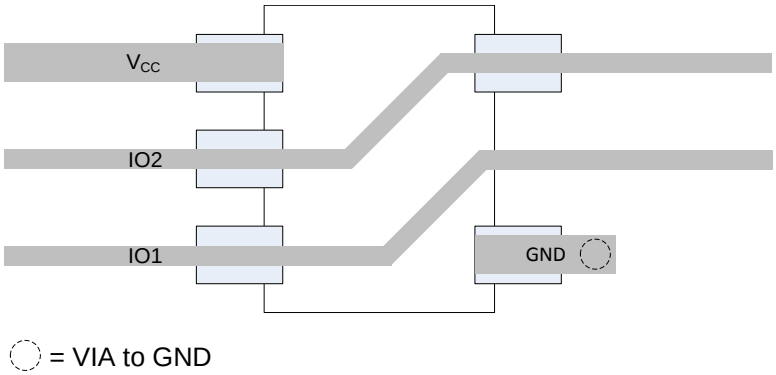

Figure 6. Routing With DRL Package

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11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
FireWire is a trademark of Apple Computer, Inc.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2E001DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(2AR, 2AZ) (2AH, 2AW)	Samples
TPD2E001DRLRG4	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(2AR, 2AZ) (2AH, 2AW)	Samples
TPD2E001DRSR	ACTIVE	SON	DRS	6	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWK	Samples
TPD2E001DRST-NM	ACTIVE	SON	DRS	6	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	ZWKNM	Samples
TPD2E001DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2A	Samples
TPD2E001DRYRG4	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2A	Samples
TPD2E001DZDR	ACTIVE	SOT-23	DZD	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFGO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPD2E001 :

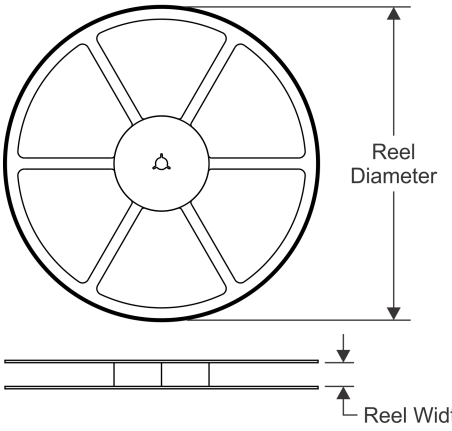
- Automotive: TPD2E001-Q1

NOTE: Qualified Version Definitions:

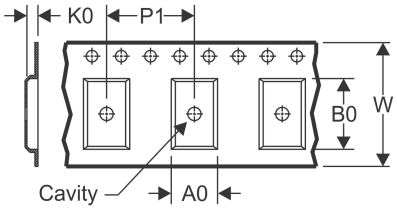
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

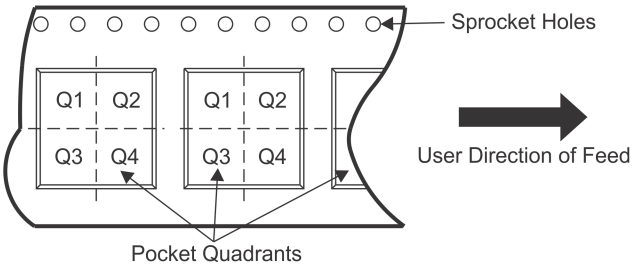


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

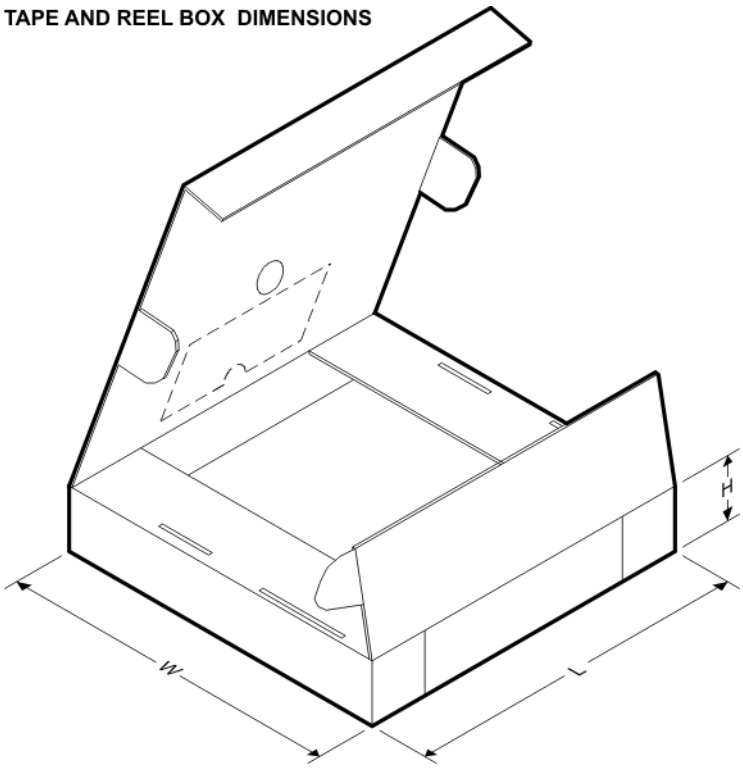
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

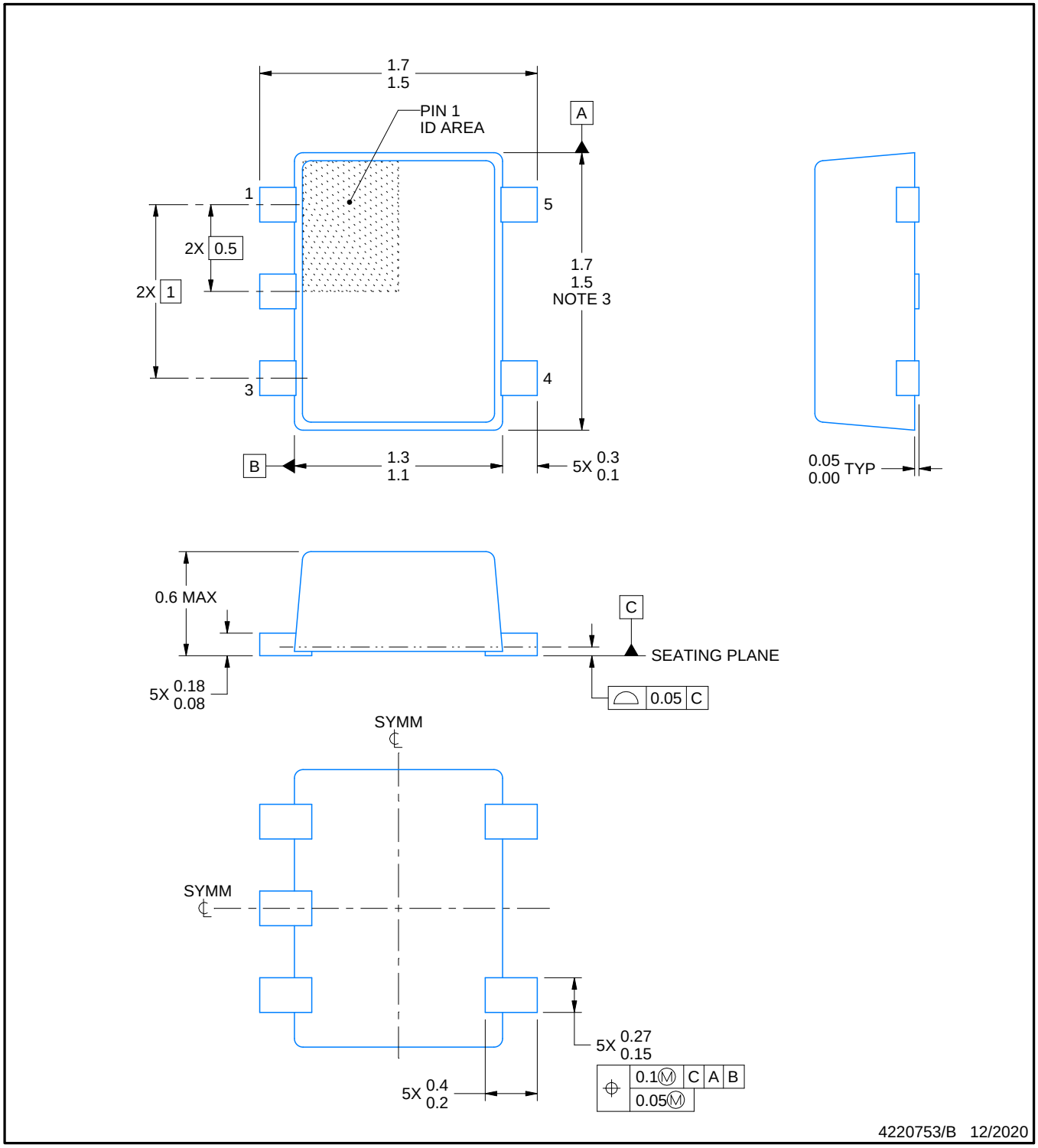
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E001DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TPD2E001DRSR	SON	DRS	6	1000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPD2E001DRST-NM	SON	DRS	6	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPD2E001DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
TPD2E001DZDR	SOT-23	DZD	4	3000	179.0	8.4	3.15	2.6	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



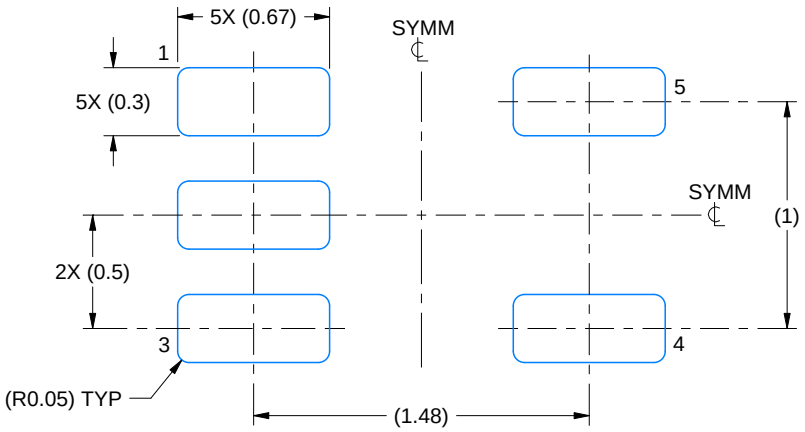
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E001DRLR	SOT-5X3	DRL	5	4000	183.0	183.0	20.0
TPD2E001DRSR	SON	DRS	6	1000	853.0	449.0	35.0
TPD2E001DRST-NM	SON	DRS	6	250	210.0	185.0	35.0
TPD2E001DRYR	SON	DRY	6	5000	189.0	185.0	36.0
TPD2E001DZDR	SOT-23	DZD	4	3000	200.0	183.0	25.0

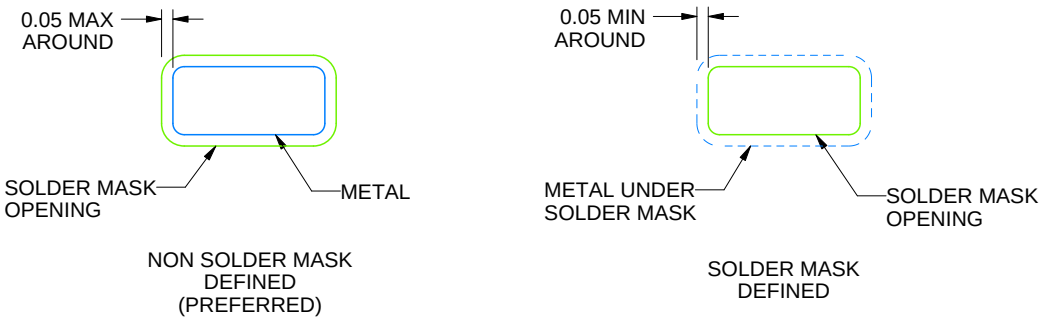


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X

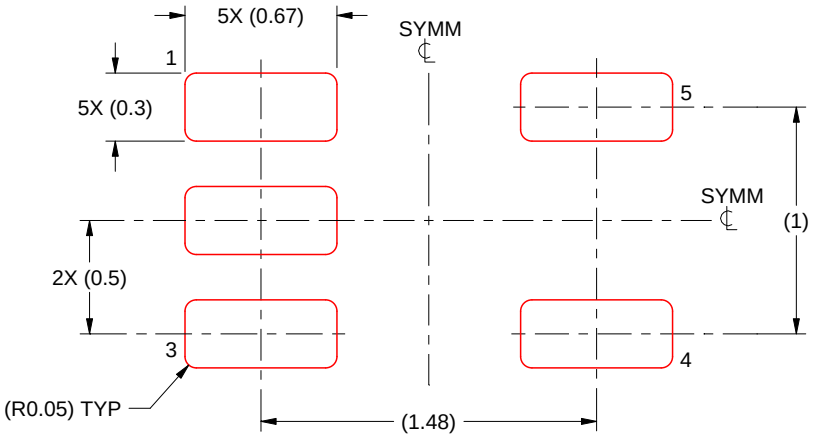


SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



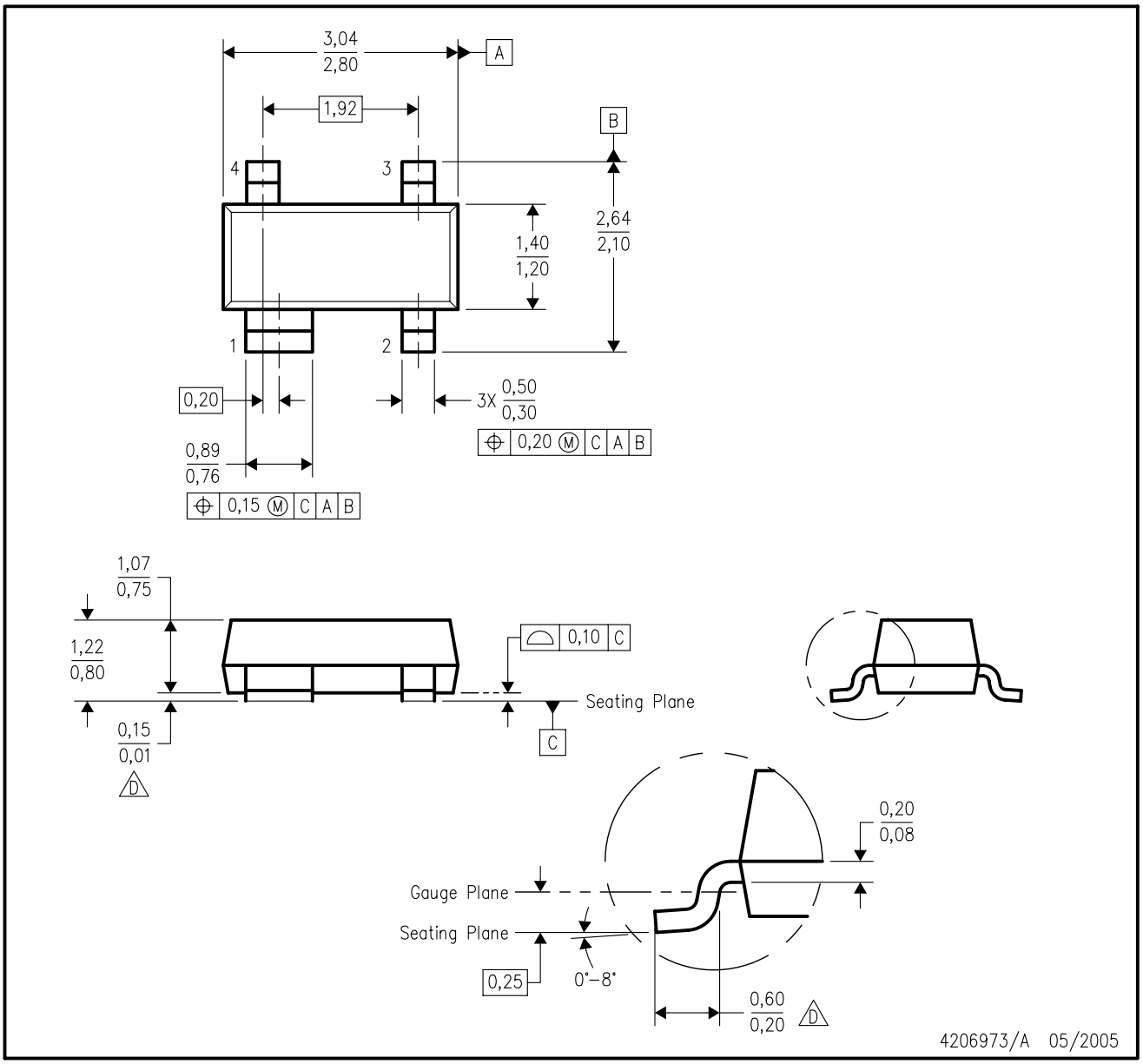
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/B 12/2020

NOTES: (continued)

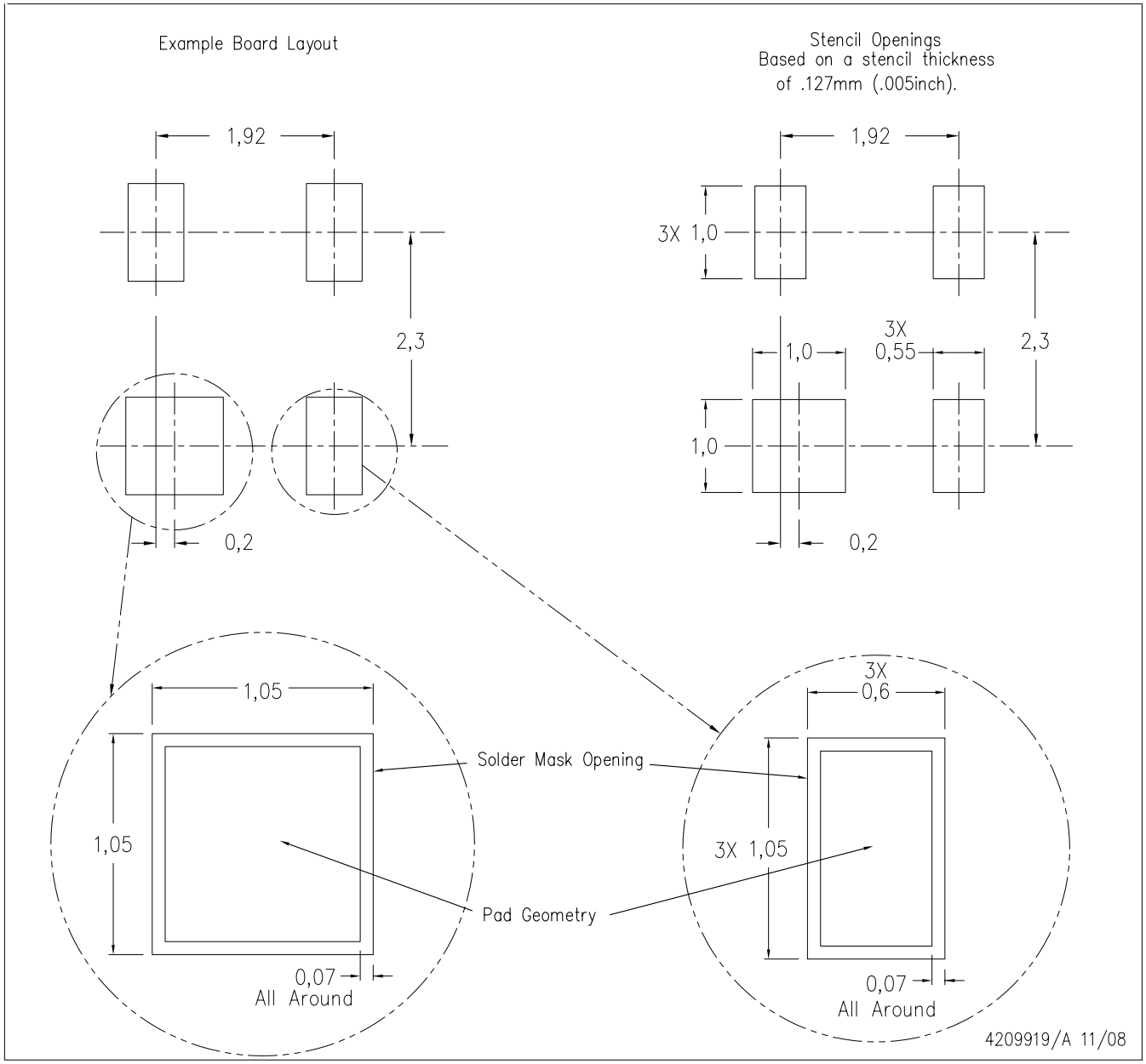
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DZD (R–PDSO–G4) PLASTIC SMALL–OUTLINE



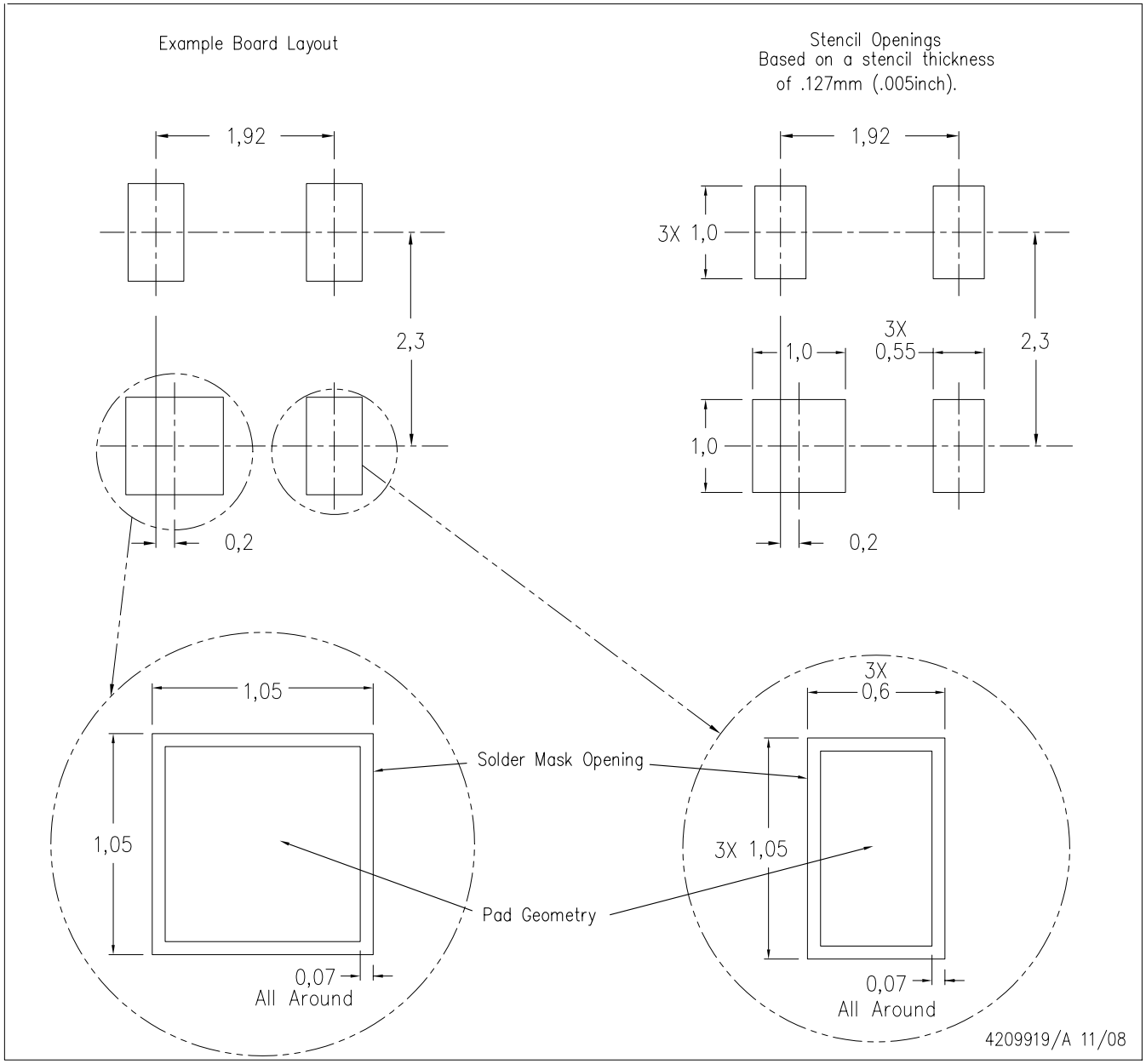
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.25 per side.
D. Falls within JEDEC TO–253 variation AA, except minimum foot length and minimum seating height.

DZD (R-PDSO-G4)



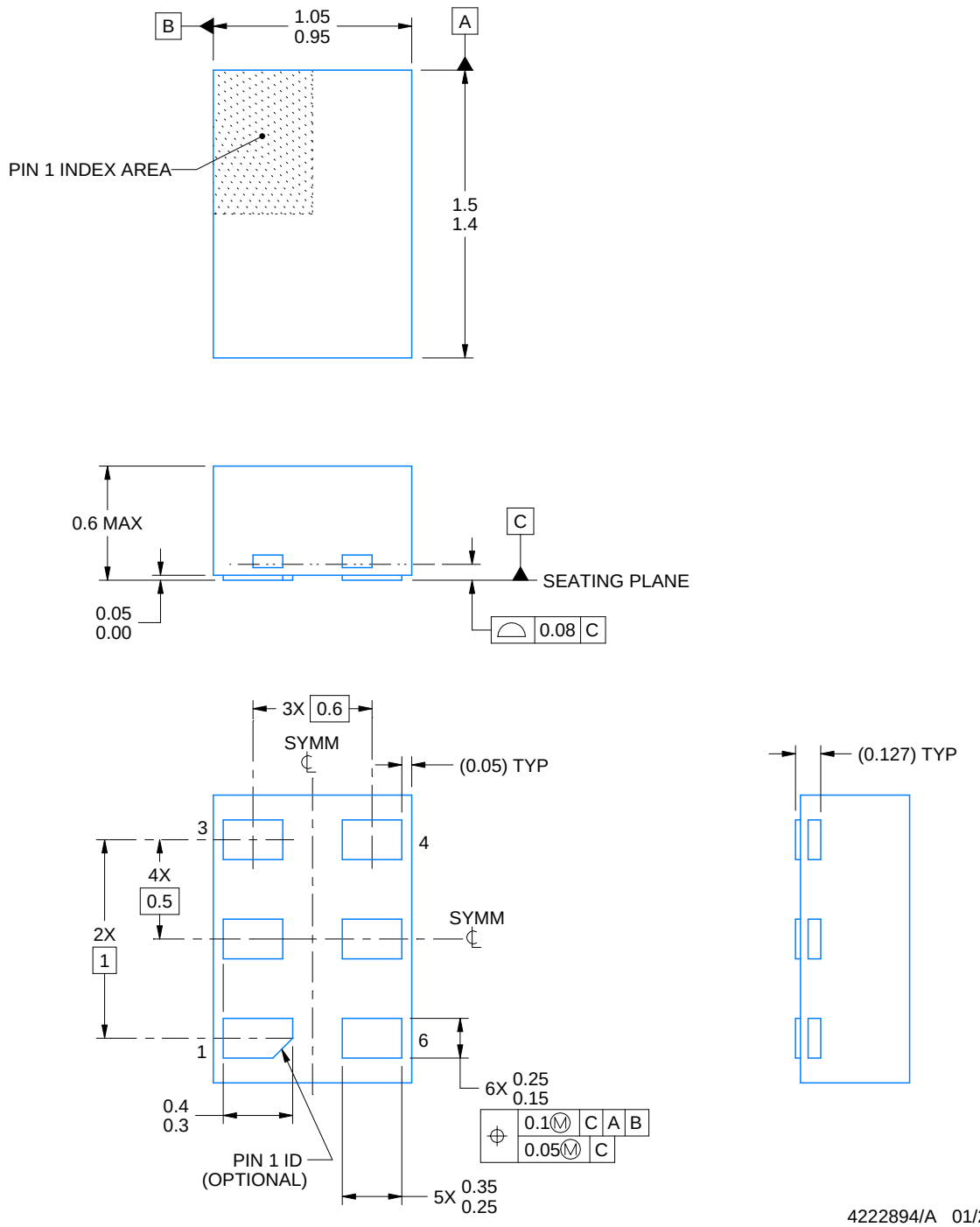
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.

DZD (R-PDSO-G4)



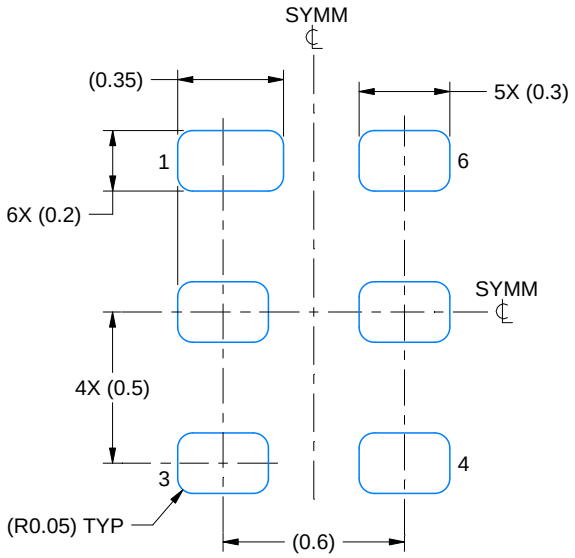
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

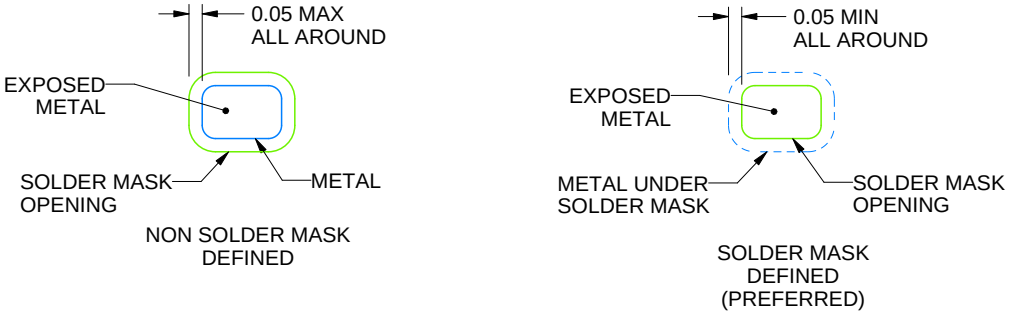


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X

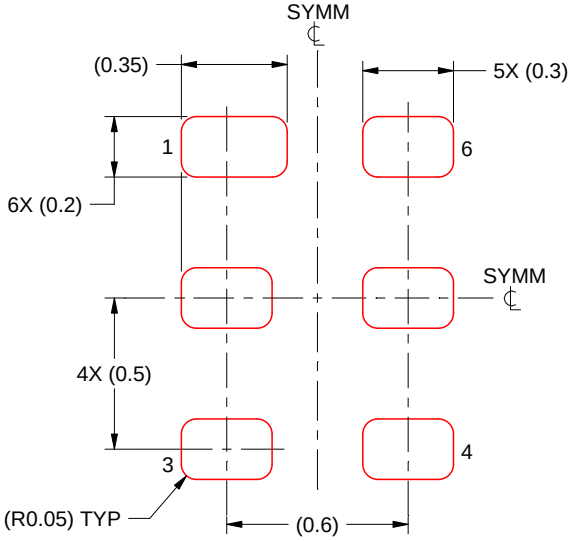


SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



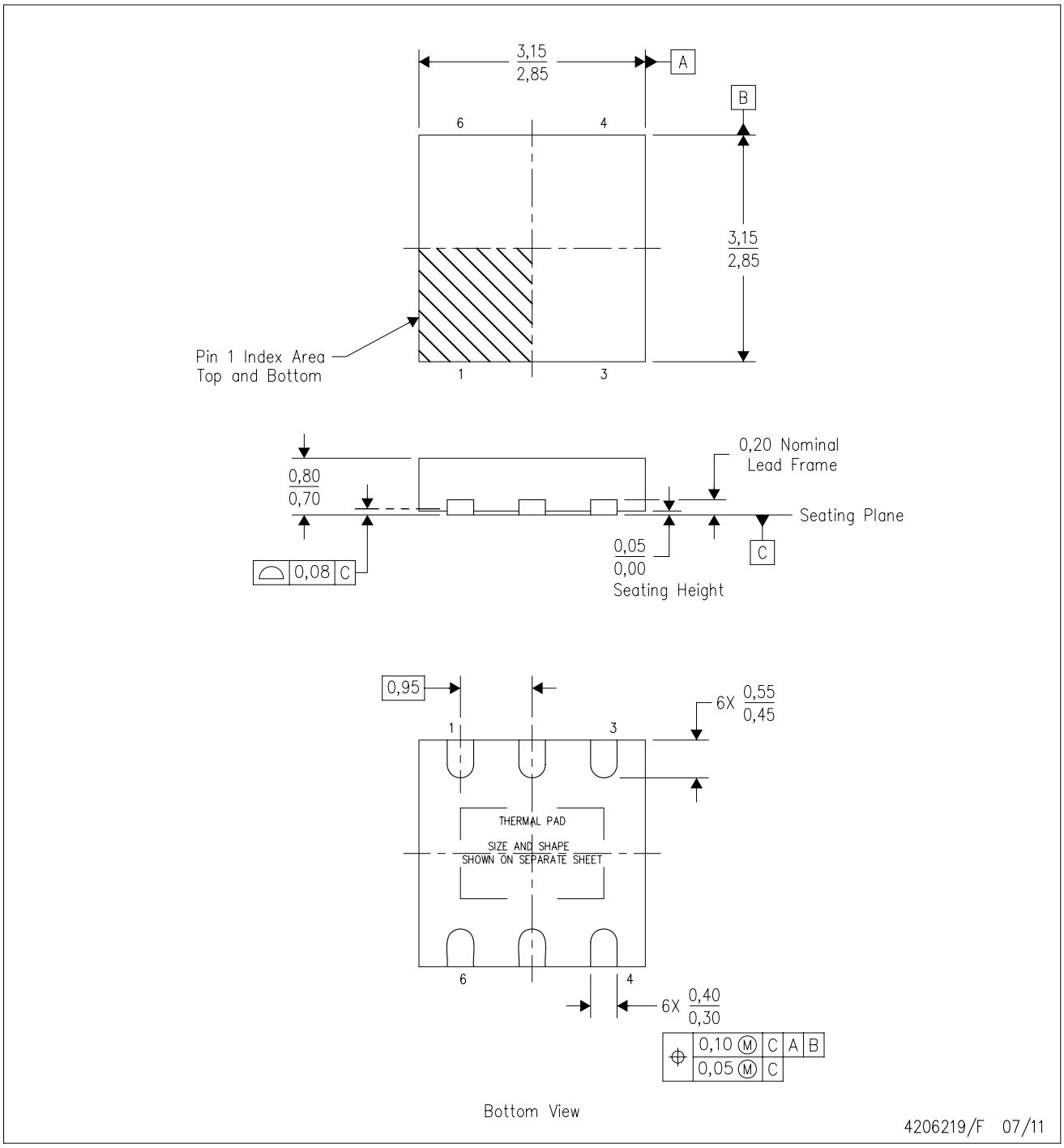
SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

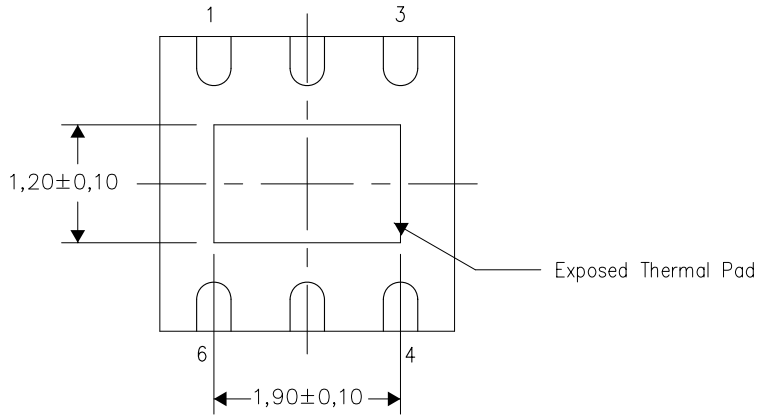
DRS (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



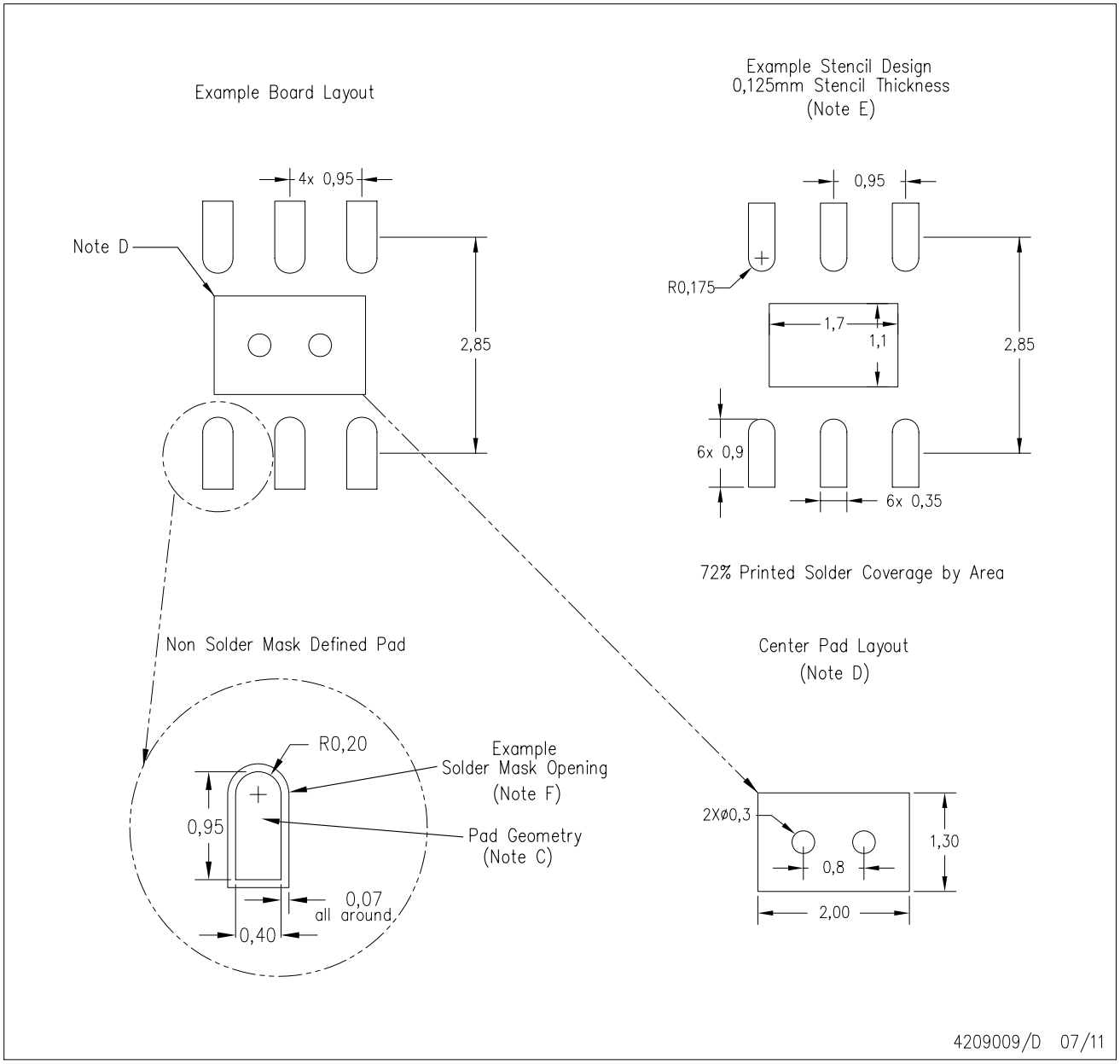
Bottom View

Exposed Thermal Pad Dimensions

4207663/E 07/11

NOTE: All linear dimensions are in millimeters

DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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