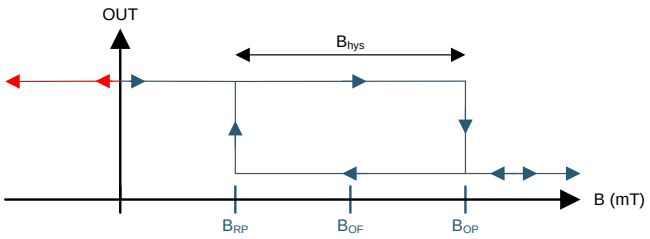
DRV5023 数字开关霍尔效应传感器

1 特性

- 数字单极性开关霍尔传感器
- 出色的温度稳定性
  - 温度范围内的灵敏度为 ±10%
- 多个灵敏度选项 (B_{OP}/B_{RP})：
  - 3.5/2mT（FA，请参见图 24）
  - 6.9/3.2mT（AJ，请参见 图 24）
  - 14.5/6mT（BI，请参见 图 24）
- 支持宽电压范围
  - 2.5V 至 38V
  - 无需外部稳压器
- 宽运行电压范围
  - T_A = -40 至 125°C（Q，请见 图 24）
- 开漏输出（30mA 灌电流）
- 35µs 快速上电时间
- 小型封装尺寸
  - 表面贴装 3 引脚小外形尺寸晶体管 (SOT)-23 (DBZ)
    - 2.92mm × 2.37mm
  - 插入式 3 引脚 TO-92 (LPG)
    - 4.00mm × 3.15mm
- 保护 特性
  - 反向电源保护（高达 -22V）
  - 支持高达 40V 抛负载
  - 输出短路保护
  - 输出电流限制

输出状态



2 应用

- 对接检测
- 门开关检测
- 接近感测
- 阀定位
- 脉冲计数

3 说明

DRV5023 器件是一款斩波稳定霍尔效应传感器，能够在整个温度范围内提供具有出色灵敏度稳定性和集成保护特性的磁场感测 解决方案。

当应用的磁通量密度超过 B_{OP} 阈值时，DRV5023 开漏输出变为低电平。输出将保持低电平，直到磁通量密度降至 B_{RP} 以下之后变为高阻抗。输出灌电流能力为 30mA。反向极性保护高达 -22V 的宽工作电压范围（2.5 至 38V）使得此器件广泛适用于各种工业 信号。

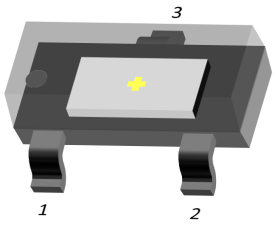
该器件提供针对反向电源情况、负载突降以及输出短路或过流故障的内部保护功能。

器件信息(1)

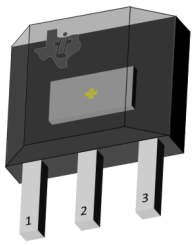
器件型号	封装	封装尺寸（标称值）
DRV5023	SOT-23 (3)	2.92mm × 1.30mm
	TO-92 (3)	4.00mm × 3.15mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

SOT-23



TO-92



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision F (May 2016) to Revision G — **Page**

- Changed the power-on time for the FA version in the *Electrical Characteristics* table ... 6
- Added the *Layout* section ... 19
- 已添加 *接收文档更新通知*部分 ... 21

Changes from Revision E (February 2016) to Revision F — **Page**

- Revised preliminary limits for the FA version ... 6

Changes from Revision D (December 2015) to Revision E — **Page**

- 已添加 FA 器件选项 ... 1
- Added the typical bandwidth value to the *Magnetic Characteristics* table ... 6

Changes from Revision C (May 2015) to Revision D — **Page**

- 已更正 SOT-23 封装体尺寸并将 SIP 封装名称更正为 TO-92 ... 1
- Added B_{MAX} to *Absolute Maximum Ratings* ... 5
- Removed table note from junction temperature ... 5
- 已更新封装卷带选项 M 和空白 ... 20
- 已添加 *社区资源* ... 21

Changes from Revision B (September 2014) to Revision C — **Page**

- 已将器件状态更新为量产数据 ... 1

Changes from Revision A (August 2014) to Revision B **Page**

- 已将“高灵敏度选项”更新为 +6.9/+3.2mT (AJ) 和 +14.5/+6mT (BI) 1
- Added typical rise and fall time and removed maximum value 6
- Updated the device values and typical values in *Magnetic Characteristics* 6
- Updated all *Typical Characteristics* graphs 7
- Updated Equation 4 17
- 已更新 图 24 20

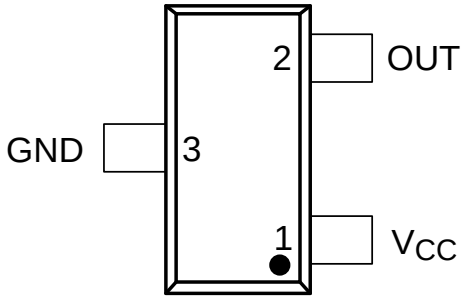
Changes from Original (May 2014) to Revision A **Page**

- 已更改 高灵敏度选项“+6.9/+2.3mT (AJ)”至“+6.9/+3.3mT (AJ)” 1
- Changed the maximum T_J value from 175°C to 150°C 5
- Changed MIN value for I_{OCP} from 20 to 15 6
- Changed Max value for I_{OCP} from 40 to 45 6
- Updated *Magnetic Characteristics* table. 6

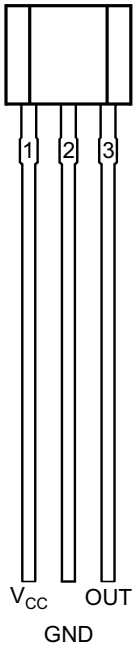
5 Pin Configuration and Functions

For additional configuration information, see *器件标记* and *机械、封装和可订购信息*.

DBZ Package
3-Pin SOT-23
Top View



LPG Package
3-Pin TO-92
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DBZ	LPG		
GND	3	2	GND	Ground pin
OUT	2	3	Output	Hall sensor open-drain output. The open drain requires a resistor pullup.
V_{CC}	1	1	Power	2.5 to 38 V power supply. Bypass this pin to the GND pin with a 0.01-μF (minimum) ceramic capacitor rated for V_{CC}.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply voltage	V_{CC}	–22(2)	40	V
	Voltage ramp rate (V_{CC}), V_{CC} < 5 V	Unlimited		V/µs
	Voltage ramp rate (V_{CC}), V_{CC} > 5 V	0	2	
Output pin voltage		–0.5	40	V
Output pin reverse current during reverse supply condition		0	100	mA
Magnetic flux density, B_{MAX}		Unlimited		
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Ensured by design. Only tested to –20 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Power supply voltage	2.5	38	V
V_O	Output pin voltage (OUT)	0	38	V
I_{SINK}	Output pin current sink (OUT)(1)	0	30	mA
T_A	Operating ambient temperature	–40	125	°C

(1) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC(1)		DRV5023		UNIT
		DBZ (SOT-23)	LPG (TO-92)	
		3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	333.2	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.9	98.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.9	154.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.9	40	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.2	154.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (V_{CC})						
V_{CC}	V_{CC} operating voltage		2.5		38	V
I_{CC}	Operating supply current	V_{CC} = 2.5 to 38 V, T_A = 25°C		2.7		mA
		V_{CC} = 2.5 to 38 V, T_A = 125°C		3	3.5	
t_{on}	Power-on time	AJ, BI versions		35	50	µs
		FA version		35	70	
OPEN DRAIN OUTPUT (OUT)						
$r_{DS(on)}$	FET on-resistance	V_{CC} = 3.3 V, I_O = 10 mA, T_A = 25°C		22		Ω
		V_{CC} = 3.3 V, I_O = 10 mA, T_A = 125°C		36	50	
$I_{lkg(off)}$	Off-state leakage current	Output Hi-Z			1	µA
PROTECTION CIRCUITS						
V_{CCR}	Reverse supply voltage		–22			V
I_{OCP}	Overcurrent protection level	OUT shorted V_{CC}	15	30	45	mA

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN DRAIN OUTPUT (OUT)						
t_d	Output delay time	B = B_{RP} – 10 mT to B_{OP} + 10 mT in 1 µs		13	25	µs
t_r	Output rise time (10% to 90%)	R1 = 1 kΩ, C_O = 50 pF, V_{CC} = 3.3 V		200		ns
t_f	Output fall time (90% to 10%)	R1 = 1 kΩ, C_O = 50 pF, V_{CC} = 3.3 V		31		ns

6.7 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT(1)
f_{BW}	Bandwidth(2)		20	30		kHz
DRV5023FA: 3.5 / 2 mT						
B_{OP}	Operate point (see Figure 12)	T_A = –40°C to 125°C	1.8	3.5	6.8	mT
B_{RP}	Release point (see Figure 12)		0.5	2	4.2	mT
B_{hys}	Hysteresis; B_{hys}= (B_{OP} – B_{RP})			1.5		mT
B_O	Magnetic offset, B_O = (B_{OP} + B_{RP}) / 2			2.8		mT
DRV5023AJ: 6.9 / 3.2 mT						
B_{OP}	Operate point (see Figure 12)	T_A = –40°C to 125°C	3	6.9	12	mT
B_{RP}	Release point (see Figure 12)		1	3.2	5	mT
B_{hys}	Hysteresis; B_{hys}= (B_{OP} – B_{RP})			3.7		mT
B_O	Magnetic offset, B_O = (B_{OP} + B_{RP}) / 2			5		mT
DRV5023BI: 14.5 / 6 mT						
B_{OP}	Operate point (see Figure 12)	T_A = –40°C to 125°C	6	14.5	24	mT
B_{RP}	Release point (see Figure 12)		3	6	9	mT
B_{hys}	Hysteresis; B_{hys} = (B_{OP} – B_{RP})(3)			8.5		mT
B_O	Magnetic offset, B_O = (B_{OP} + B_{RP}) / 2			10.3		mT

(1) 1 mT = 10 Gauss
(2) Bandwidth describes the fastest changing magnetic field that can be detected and translated to the output.
(3) $|B_{OP}|$ is always greater than $|B_{RP}|$.

6.8 Typical Characteristics

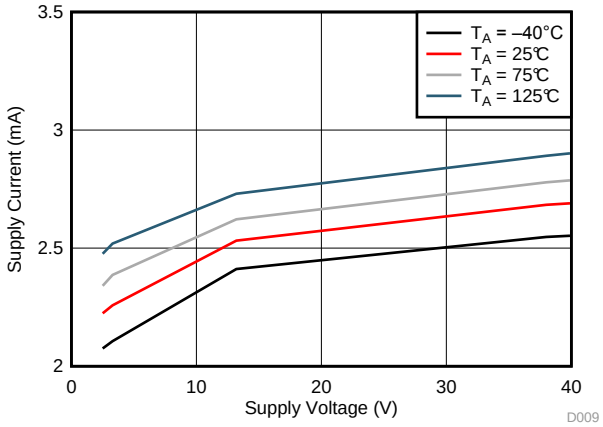


Figure 1. I_{CC} vs V_{CC}

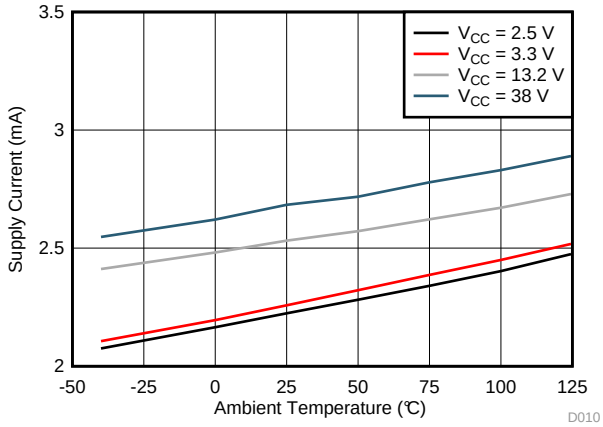


Figure 2. I_{CC} vs Temperature

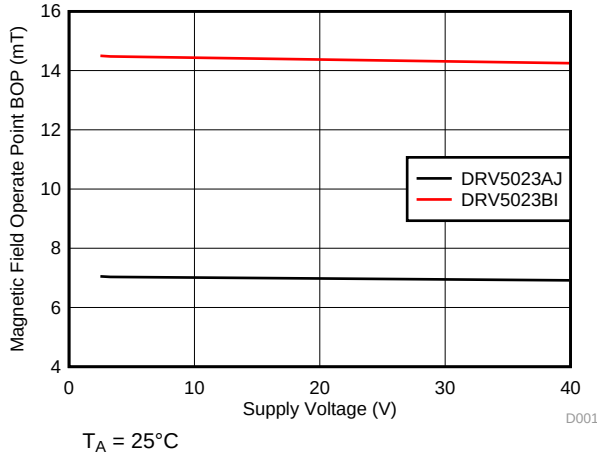


Figure 3. B_{OP} vs V_{CC}

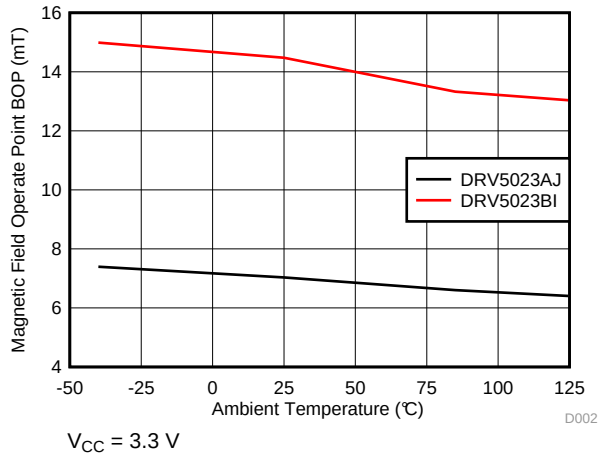


Figure 4. B_{OP} vs Temperature

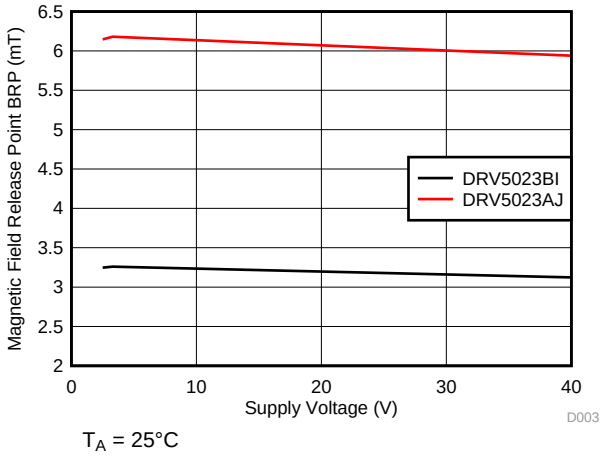


Figure 5. B_{RP} vs V_{CC}

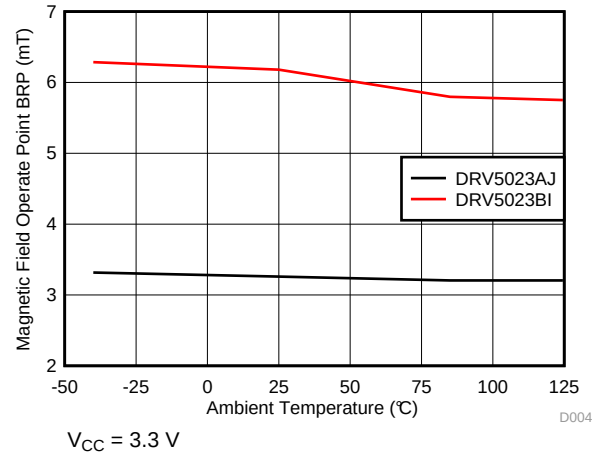
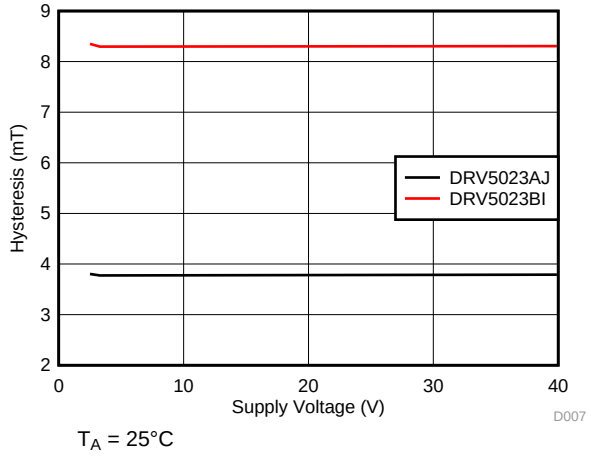


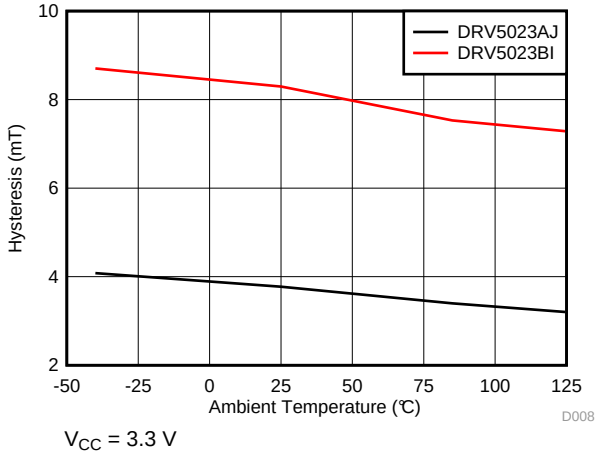
Figure 6. B_{RP} vs Temperature

Typical Characteristics (continued)



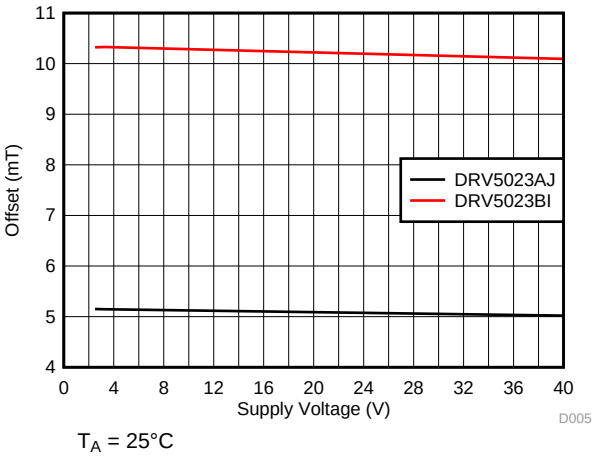
T_A = 25°C

Figure 7. Hysteresis vs V_{CC}



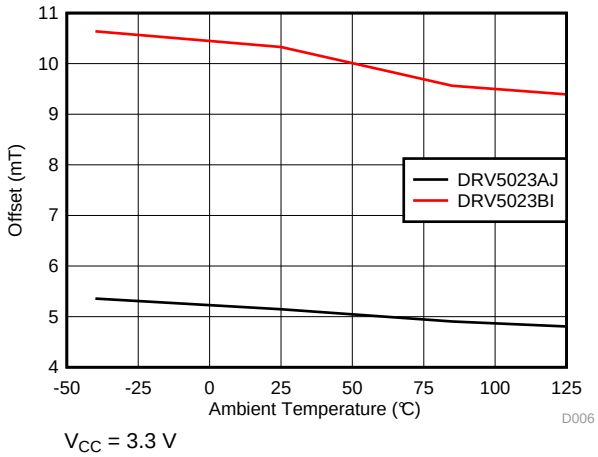
V_{CC} = 3.3 V

Figure 8. Hysteresis vs Temperature



T_A = 25°C

Figure 9. Offset vs V_{CC}



V_{CC} = 3.3 V

Figure 10. Offset vs Temperature

7 Detailed Description

7.1 Overview

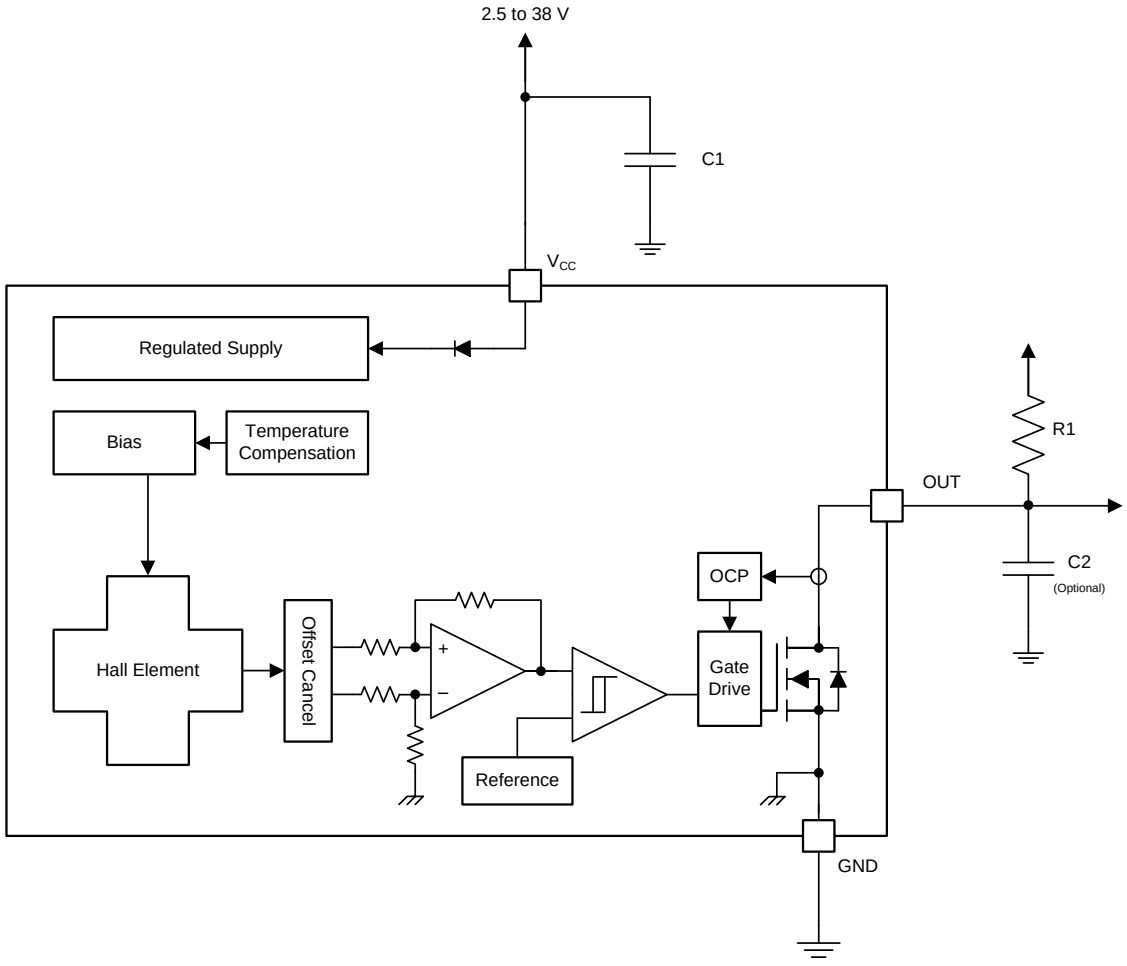
The DRV5023 device is a chopper-stabilized Hall sensor with a digital output for magnetic sensing applications. The DRV5023 device can be powered with a supply voltage between 2.5 and 38 V, and will survive –22 V reverse-battery conditions. The DRV5023 device does not operate when –22 to 2.4 V is applied to the V_{CC} pin (with respect to GND pin). In addition, the device can withstand supply voltages up to 40 V for transient durations.

The field polarity is defined as follows: a south pole near the marked side of the package is a positive magnetic field. A north pole near the marked side of the package is a negative magnetic field.

The output state is dependent on the magnetic field perpendicular to the package. A strong south pole near the marked side of the package causes the output to pull low (operate point, BOP), and a weak south pole causes the output to release (release point, BRP). Hysteresis is included in between the operate point and the release point therefore magnetic-field noise does not accidentally trip the output.

An external pullup resistor is required on the OUT pin. The OUT pin can be pulled up to V_{CC}, or to a different voltage supply. This allows for easier interfacing with controller circuits.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Field Direction Definition

A positive magnetic field is defined as a south pole near the marked side of the package as shown in Figure 11.

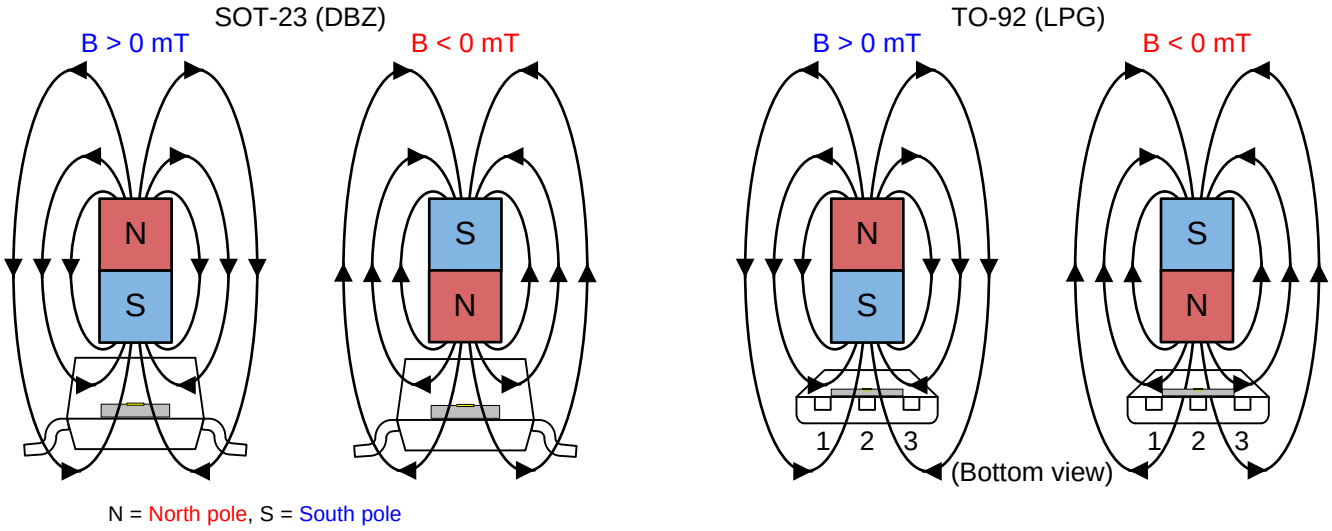


Figure 11. Field Direction Definition

7.3.2 Device Output

If the device is powered on with a magnetic field strength between B_{RP} and B_{OP}, then the device output is indeterminate and can either be Hi-Z or Low. For the FA, AJ, and BI device versions, if the field strength is greater than B_{OP}, then the output is pulled low; if the field strength is less than B_{RP}, then the output is released. For the FI device version, if the field strength is greater than B_{OP}, then the output is Hi-Z; if the field strength is less than B_{RP}, then the output is pulled Low.

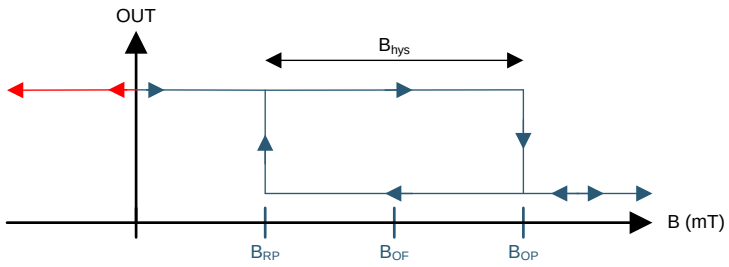


Figure 12. Output State

Feature Description (continued)

7.3.3 Power-On Time

After applying V_{CC} to the DRV5023 device, t_{on} must elapse before the OUT pin is valid. During the power-up sequence, the output is Hi-Z. A pulse as shown in Figure 13 and Figure 14 occurs at the end of t_{on}. This pulse can allow the host processor to determine when the DRV5023 output is valid after startup. In Case 1 (Figure 13) and Case 2 (Figure 14), the output is defined assuming a constant magnetic field B > B_{OP} and B < B_{RP}.

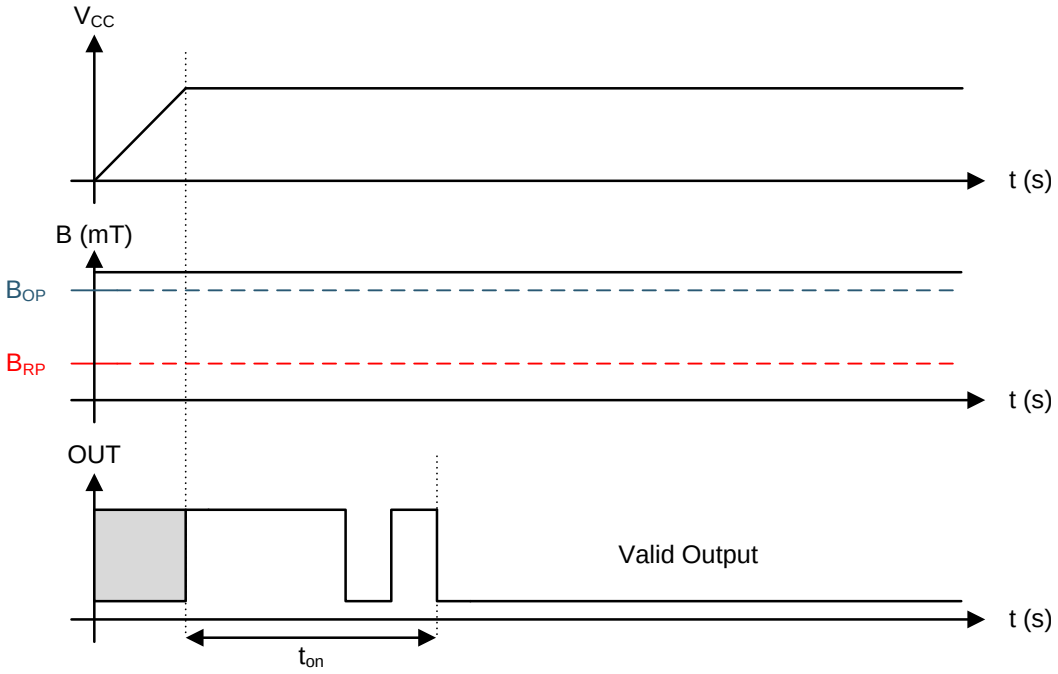


Figure 13. Case 1: Power On When B > B_{OP}

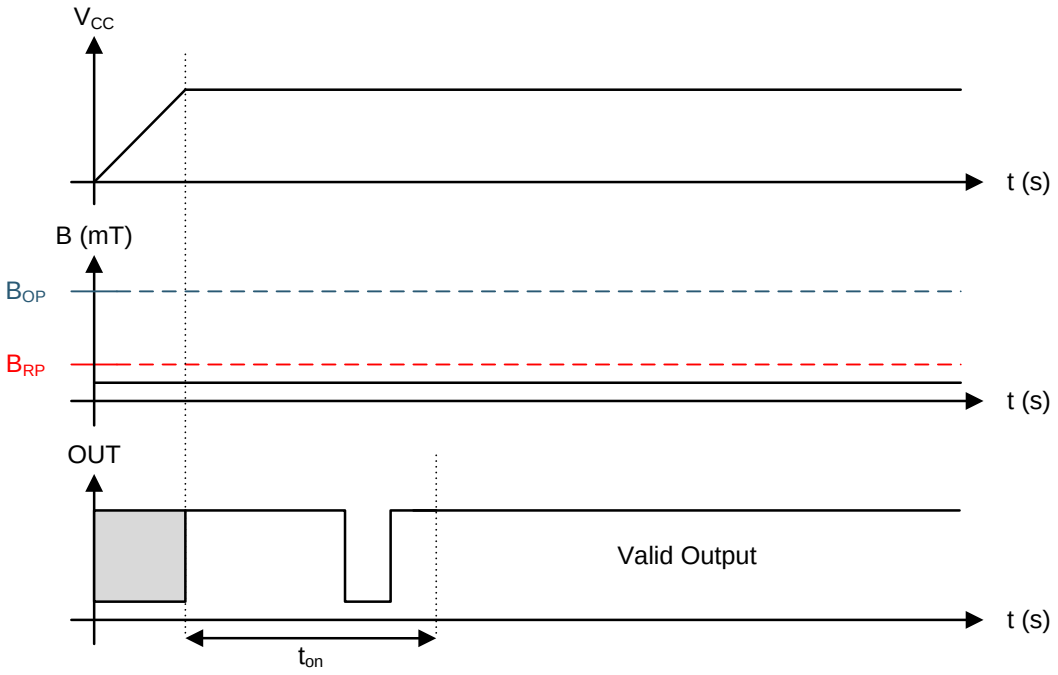


Figure 14. Case 2: Power On When B < B_{RP}

Feature Description (continued)

If the device is powered on with the magnetic field strength B_{RP} < B < B_{OP}, then the device output is indeterminate and can either be Hi-Z or pulled low. During the power-up sequence, the output is held Hi-Z until t_{on} has elapsed. At the end of t_{on}, a pulse is given on the OUT pin to indicate that t_{on} has elapsed. After t_{on}, if the magnetic field changes such that B_{OP} < B, the output is released. Case 3 (Figure 15) and Case 4 (Figure 16) show examples of this behavior.

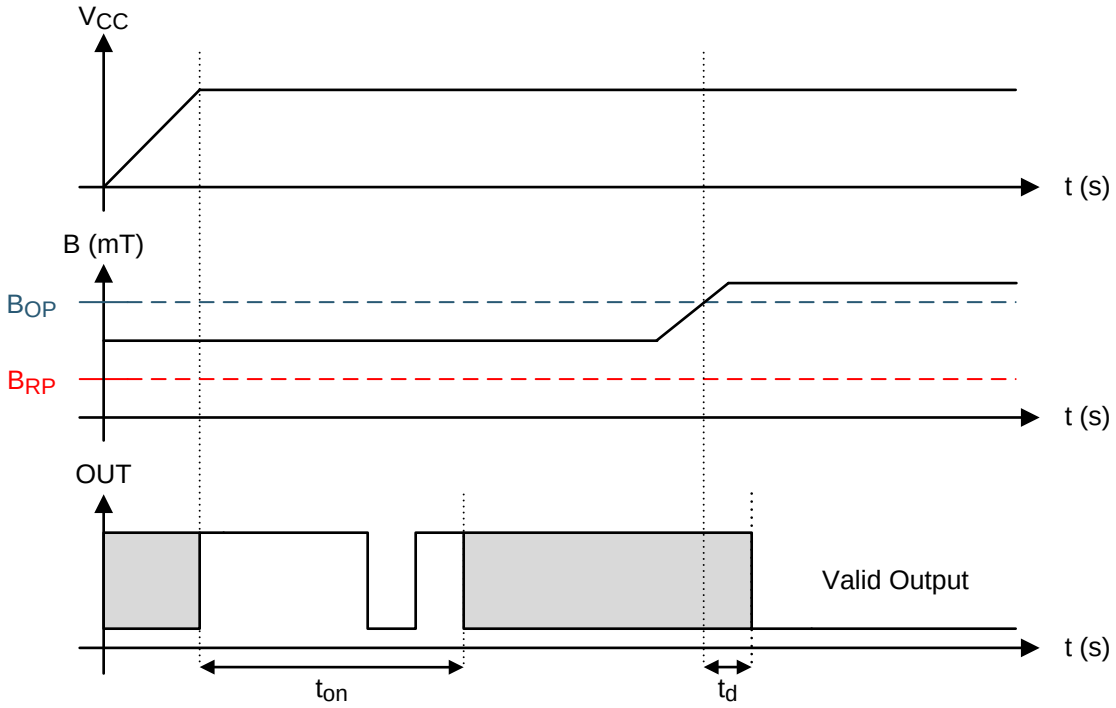


Figure 15. Case 3: Power On When B_{RP} < B < B_{OP}, Followed by B > B_{OP}

Feature Description (continued)

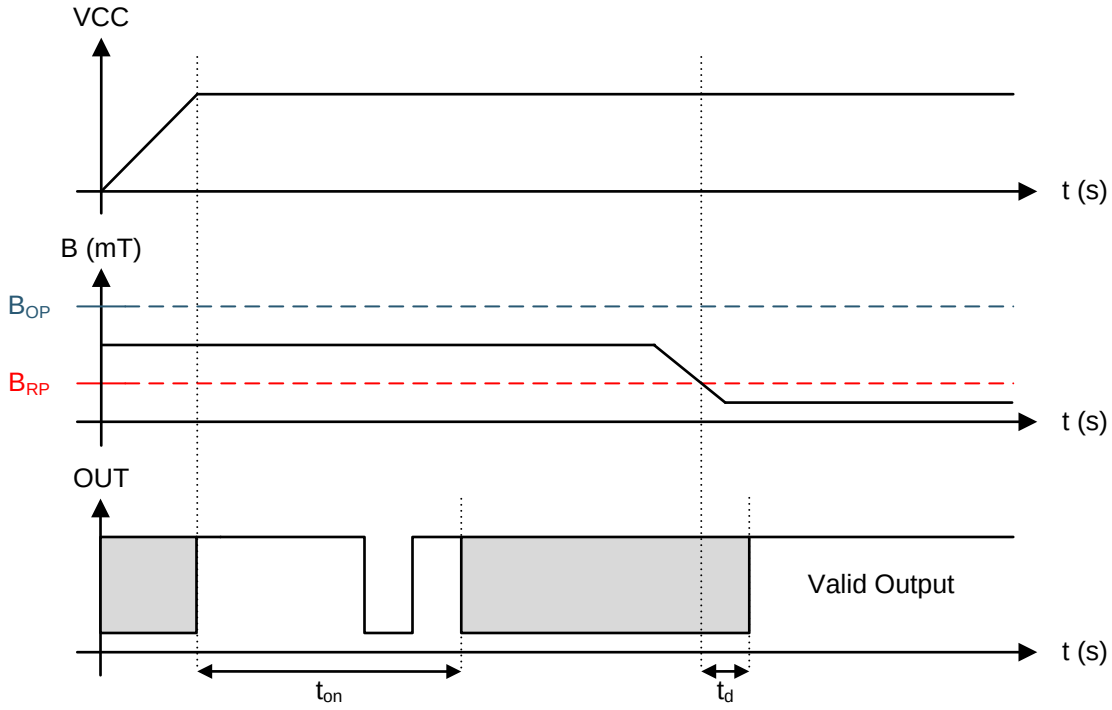


Figure 16. Case 4: Power On When B_{RP} < B < B_{OP}, Followed by B < B_{RP}

Feature Description (continued)

7.3.4 Output Stage

The DRV5023 output stage uses an open-drain NMOS, and it is rated to sink up to 30 mA of current. For proper operation, calculate the value of the pullup resistor R1 using Equation 1.

$$\frac{V_{ref}\,max}{30\ mA} \le R1 \le \frac{V_{ref}\,min}{100\ \mu A} \quad (1)$$

The size of R1 is a tradeoff between the OUT rise time and the current when OUT is pulled low. A lower current is generally better, however faster transitions and bandwidth require a smaller resistor for faster switching.

In addition, ensure that the value of R1 > 500 Ω to ensure the output driver can pull the OUT pin close to GND.

NOTE

V_{ref} is not restricted to V_{CC}. The allowable voltage range of this pin is specified in the *Absolute Maximum Ratings*.

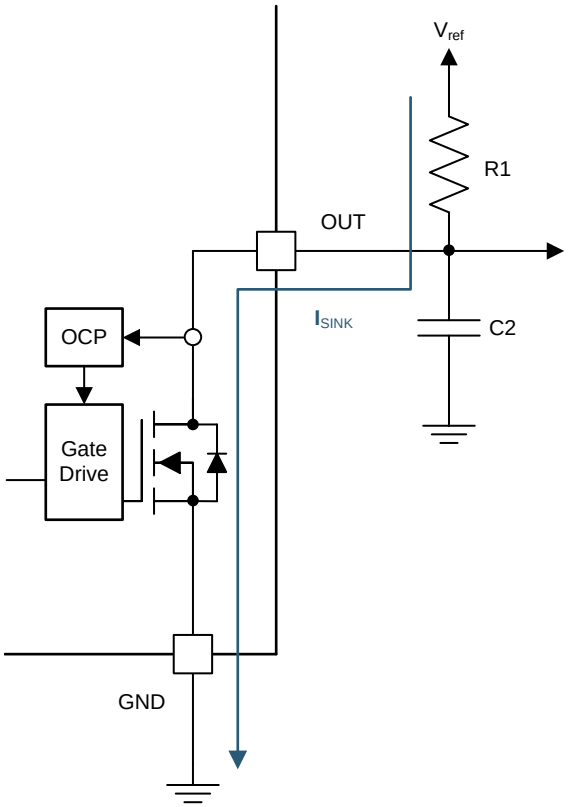


Figure 17.

Select a value for C2 based on the system bandwidth specifications as shown in Equation 2.

$$2 \times f_{BW}\ (Hz) < \frac{1}{2\pi \times R1 \times C2} \quad (2)$$

Most applications do no require this C2 filtering capacitor.

Feature Description (continued)

7.3.5 Protection Circuits

The DRV5023 device is fully protected against overcurrent and reverse-supply conditions.

7.3.5.1 Overcurrent Protection (OCP)

An analog current-limit circuit limits the current through the FET. The driver current is clamped to I_{OCP}. During this clamping, the $r_{DS(on)}$ of the output FET is increased from the nominal value.

7.3.5.2 Load Dump Protection

The DRV5023 device operates at DC V_{CC} conditions up to 38 V nominally, and can additionally withstand V_{CC} = 40 V. No current-limiting series resistor is required for this protection.

7.3.5.3 Reverse Supply Protection

The DRV5023 device is protected in the event that the V_{CC} pin and the GND pin are reversed (up to –22 V).

NOTE

In a reverse supply condition, the OUT pin reverse-current must not exceed the ratings specified in the *Absolute Maximum Ratings*.

Table 1.

FAULT	CONDITION	DEVICE	DESCRIPTION	RECOVERY
FET overload (OCP)	$I_{SINK} \geq I_{OCP}$	Operating	Output current is clamped to I_{OCP}	$I_O < I_{OCP}$
Load dump	38 V < V_{CC} < 40 V	Operating	Device will operate for a transient duration	$V_{CC} \leq$ 38 V
Reverse supply	–22 V < V_{CC} < 0 V	Disabled	Device will survive this condition	$V_{CC} \geq$ 2.5 V

7.4 Device Functional Modes

The DRV5023 device is active only when V_{CC} is between 2.5 and 38 V.

When a reverse supply condition exists, the device is inactive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV5023 device is used in magnetic-field sensing applications.

8.2 Typical Applications

8.2.1 Standard Circuit

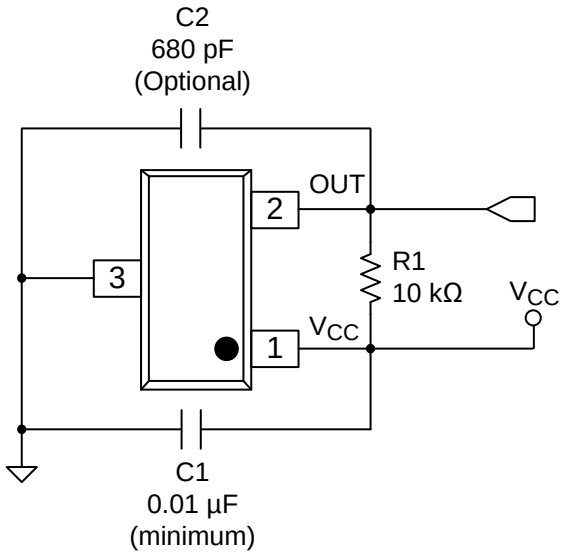


Figure 18. Typical Application Circuit

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	3.2 to 3.4 V
System bandwidth	f_{BW}	10 kHz

8.2.1.2 Detailed Design Procedure

Table 3. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C1	V_{CC}	GND	A 0.01-µF (minimum) ceramic capacitor rated for V_{CC}
C2	OUT	GND	**Optional**: Place a ceramic capacitor to GND
R1	OUT	REF(1)	Requires a resistor pullup

(1) REF is not a pin on the DRV5023 device, but a REF supply-voltage pullup is required for the OUT pin; the OUT pin may be pulled up to V_{CC}.

8.2.1.2.1 Configuration Example

In a 3.3-V system, 3.2 V ≤ V_{ref} ≤ 3.4 V. Use Equation 3 to calculate the allowable range for R1.

$$\frac{V_{ref}\,max}{30\ mA} \leq R1 \leq \frac{V_{ref}\,min}{100\ \mu A} \tag{3}$$

For this design example, use Equation 4 to calculate the allowable range of R1.

$$\frac{3.4\ V}{30\ mA} \leq R1 \leq \frac{3.2\ V}{100\ \mu A} \tag{4}$$

Therefore:

$$113\ \Omega \leq R1 \leq 32\ k\Omega \tag{5}$$

After finding the allowable range of R1 (Equation 5), select a value between 500 Ω and 32 kΩ for R1.

Assuming a system bandwidth of 10 kHz, use Equation 6 to calculate the value of C2.

$$2 \times f_{BW}\ (Hz) < \frac{1}{2\pi \times R1 \times C2} \tag{6}$$

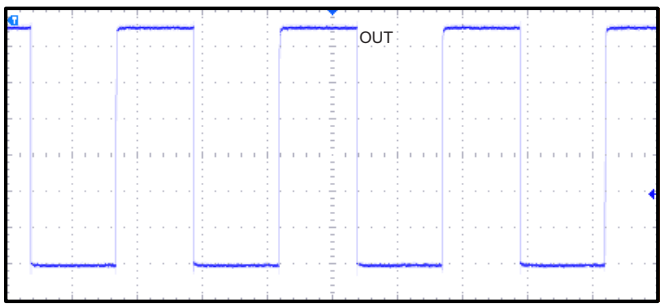
For this design example, use Equation 7 to calculate the value of C2.

$$2 \times 10\ kHz < \frac{1}{2\pi \times R1 \times C2} \tag{7}$$

An R1 value of 10 kΩ and a C2 value less than 820 pF satisfy the requirement for a 10-kHz system bandwidth.

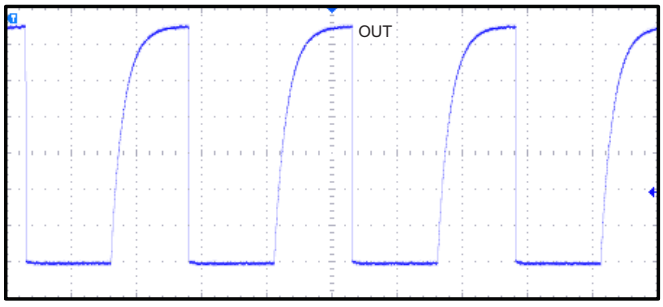
A selection of R1 = 10 kΩ and C2 = 680 pF would cause a low-pass filter with a corner frequency of 23.4 kHz.

8.2.1.3 Application Curves



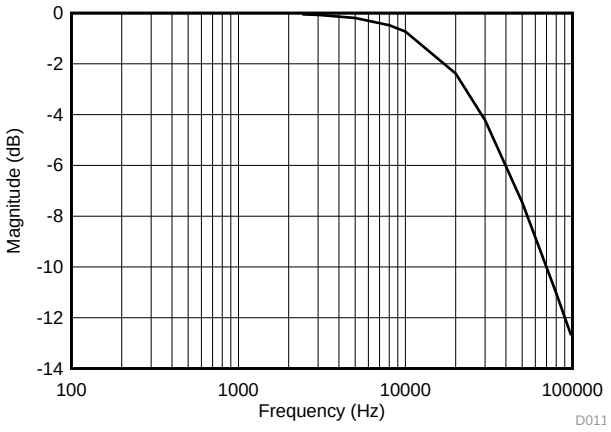
R1 = 10-kΩ pullup No C2

Figure 19. 10-kHz Switching Magnetic Field



R1 = 10-kΩ pullup C2 = 680 pF

Figure 20. 10-kHz Switching Magnetic Field



R1 = 10-kΩ pullup C2 = 680 pF

Figure 21. Low-Pass Filtering

8.2.2 Alternative Two-Wire Application

For systems that require minimal wire count, the device output can be connected to V_{CC} through a resistor, and the total supplied current can be sensed near the controller.

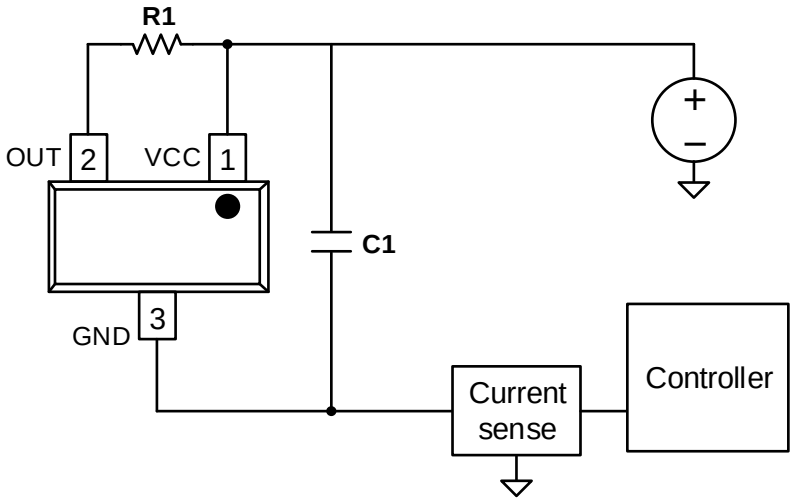


Figure 22. 2-Wire Application

Current can be sensed using a shunt resistor or other circuitry.

8.2.2.1 Design Requirements

Table 4 lists the related design parameters.

Table 4. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	12 V
OUT resistor	R1	1 kΩ
Bypass capacitor	C1	0.1 µF
Current when B < B_{RP}	$I_{RELEASE}$	About 3 mA
Current when B > B_{OP}	$I_{OPERATE}$	About 15 mA

8.2.2.2 Detailed Design Procedure

When the open-drain output of the device is high-impedance, current through the path equals the I_{CC} of the device (approximately 3 mA).

When the output pulls low, a parallel current path is added, equal to V_{CC} / (R1 + $r_{DS(on)}$). Using 12 V and 1 kΩ, the parallel current is approximately 12 mA, making the total current approximately 15 mA.

The local bypass capacitor C1 should be at least 0.1 µF, and a larger value if there is high inductance in the power line interconnect.

9 Power Supply Recommendations

The DRV5023 device is designed to operate from an input voltage supply (VM) range between 2.5 and 38 V. A 0.01-µF (minimum) ceramic capacitor rated for V_{CC} must be placed as close to the DRV5023 device as possible.

10 Layout

10.1 Layout Guidelines

The bypass capacitor should be placed near the DRV5023 device for efficient power delivery with minimal inductance. The external pullup resistor should be placed near the microcontroller input to provide the most stable voltage at the input; alternatively, an integrated pullup resistor within the GPIO of the microcontroller can be used.

Generally, using PCB copper planes underneath the DRV5023 device has no effect on magnetic flux, and does not interfere with device performance. This is because copper is not a ferromagnetic material. However, If nearby system components contain iron or nickel, they may redirect magnetic flux in unpredictable ways.

10.2 Layout Example

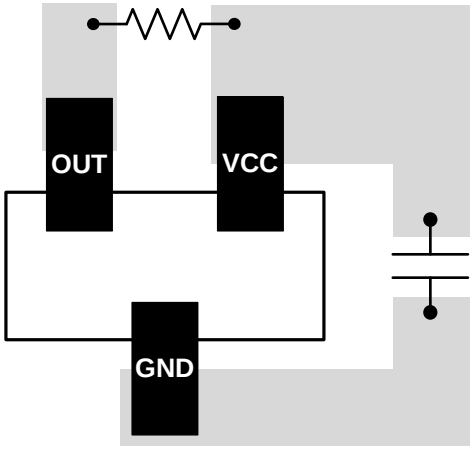


Figure 23. DRV5023 Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

图 24 显示了读取 DRV5023 器件完整器件名称的图例。

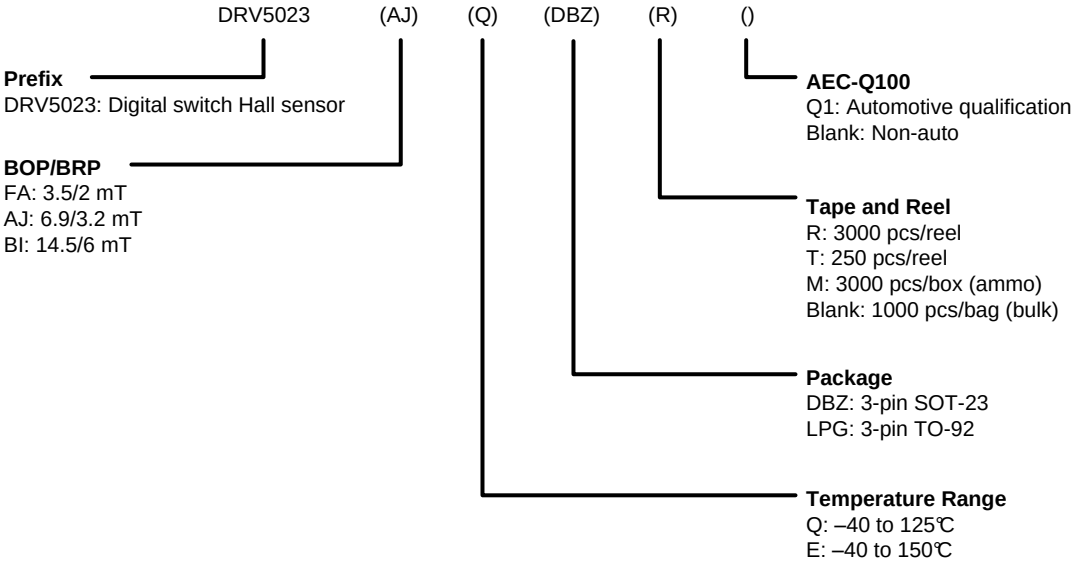


图 **24.** 器件命名规则

11.1.2 器件标记

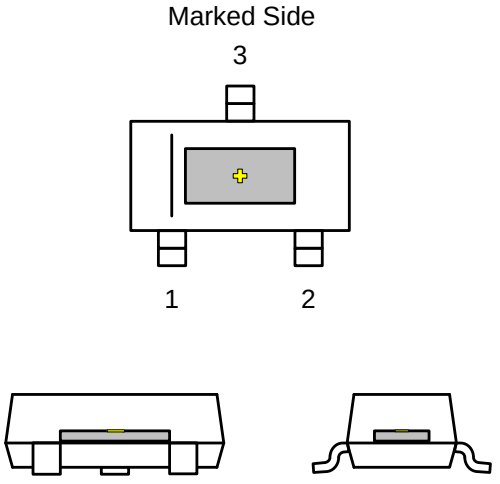


图 **25. SOT-23 (DBZ)** 封装

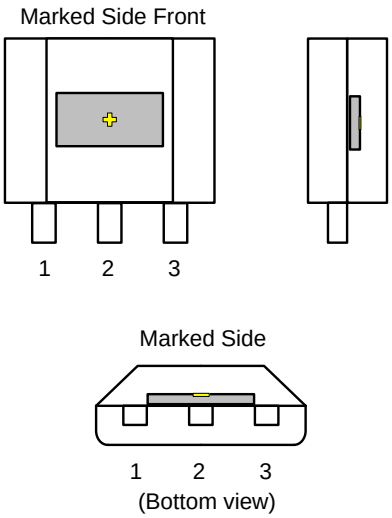


图 **26. TO-92 (LPG)** 封装

✚ 表示霍尔效应传感器（未按比例显示）。霍尔元件置于封装中央位置，容差为 ±100μm。在 DBZ 封装中，霍尔元件与封装底部的距离为 0.7mm ± 50μm；在 LPG 封装中，霍尔元件与封装底部的距离为 0.987mm ± 50μm。

11.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5023AJQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(+PLAJ, 1J22)	Samples
DRV5023AJQDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(+PLAJ, 1J22)	Samples
DRV5023AJQLPG	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+PLAJ	Samples
DRV5023AJQLPGM	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+PLAJ	Samples
DRV5023BIQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(+PLBI, 1J32)	Samples
DRV5023BIQDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(+PLBI, 1J32)	Samples
DRV5023BIQLPG	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+PLBI	Samples
DRV5023BIQLPGM	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+PLBI	Samples
DRV5023FAQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	(+PLFA, 1J42)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

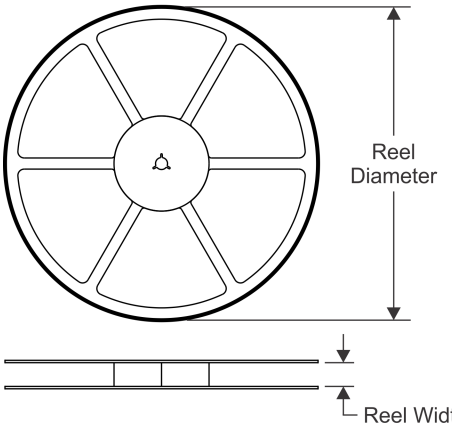
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

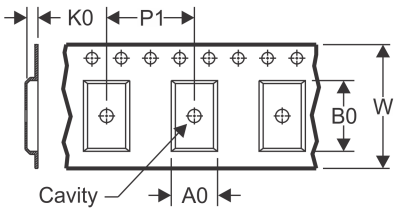
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

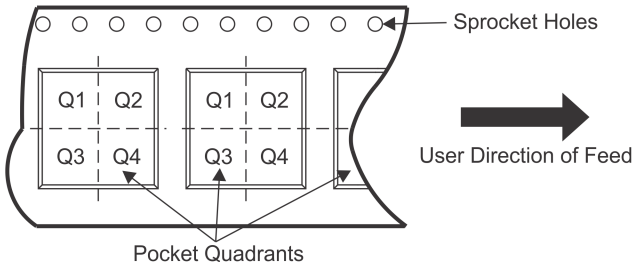


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

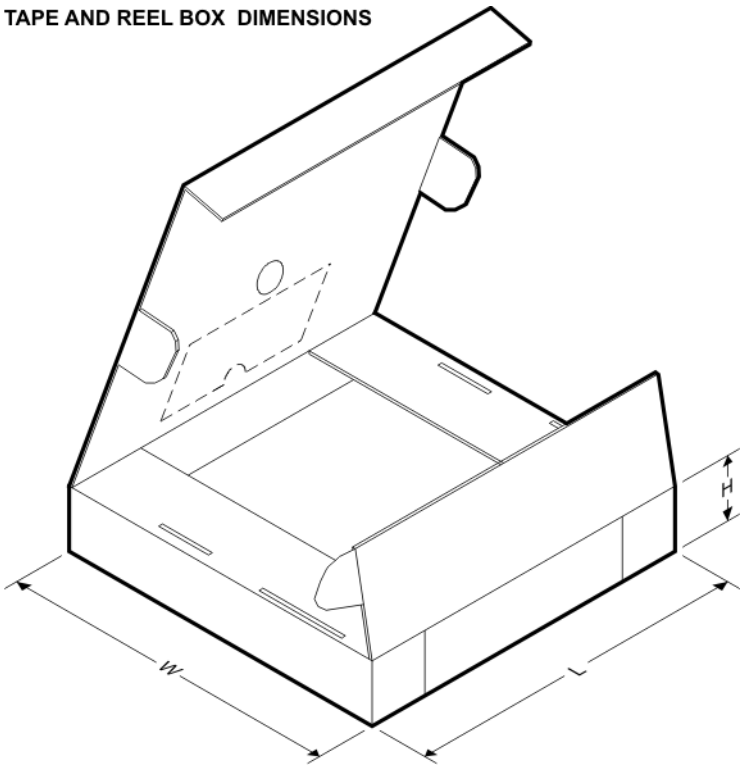
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV5023AJQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023AJQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023AJQDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023AJQDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023BIQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023BIQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023BIQDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023BIQDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023FAQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023FAQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



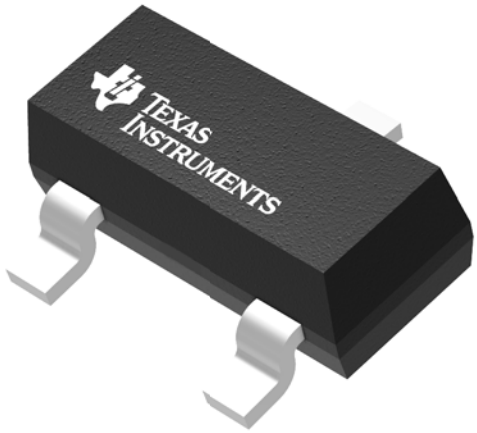
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV5023AJQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5023AJQDBZR	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5023AJQDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
DRV5023AJQDBZT	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5023BIQDBZR	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5023BIQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5023BIQDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
DRV5023BIQDBZT	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5023FAQDBZR	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5023FAQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0

GENERIC PACKAGE VIEW

DBZ 3 SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



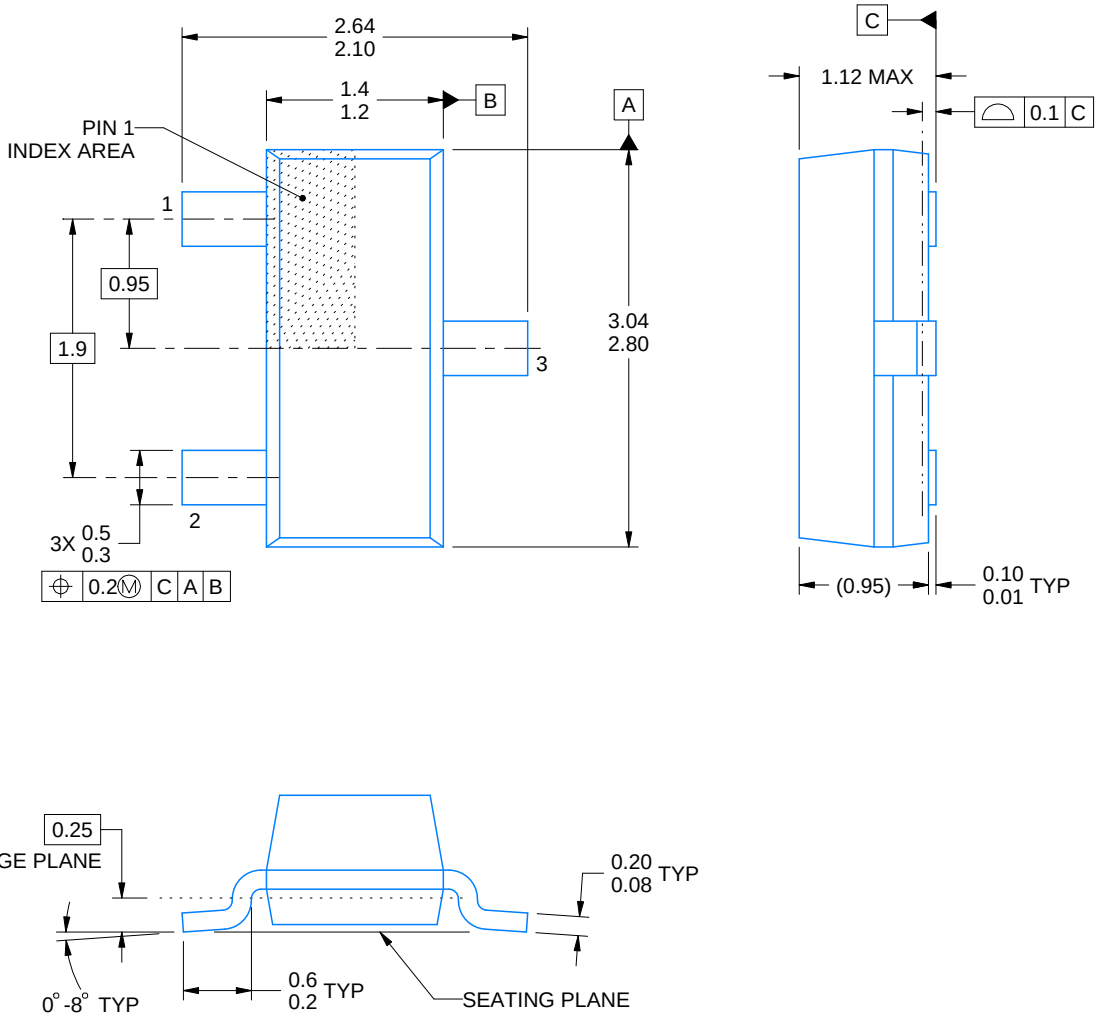
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

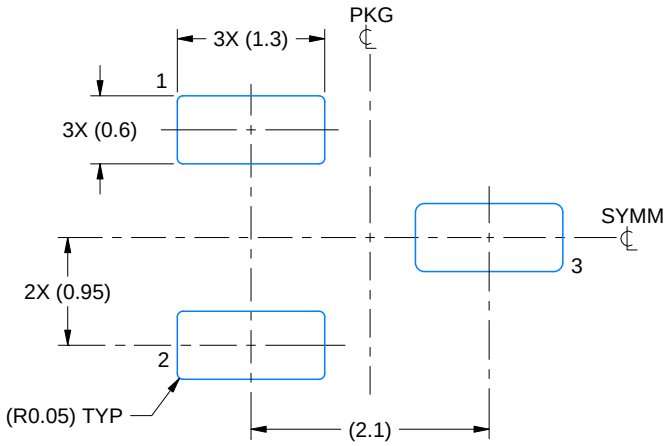
SMALL OUTLINE TRANSISTOR



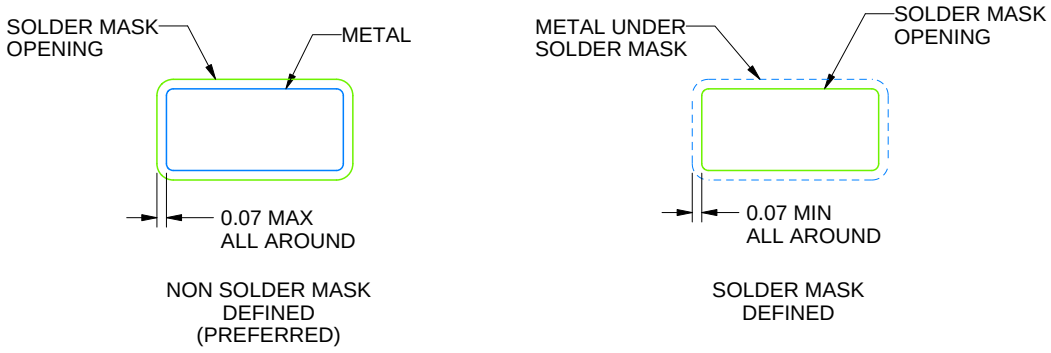
4214838/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.



LAND PATTERN EXAMPLE
SCALE:15X

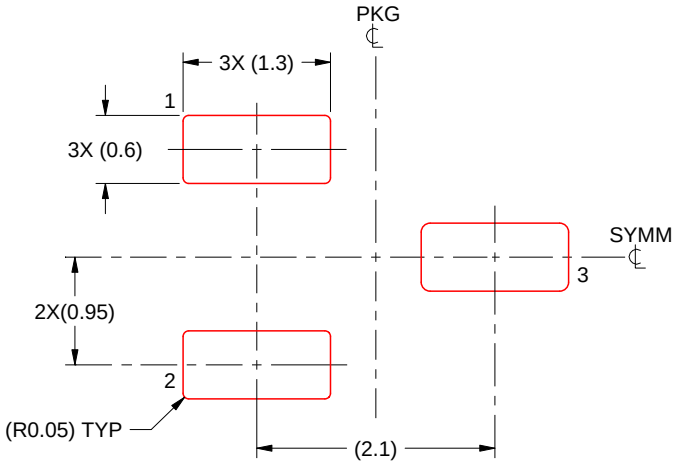


SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

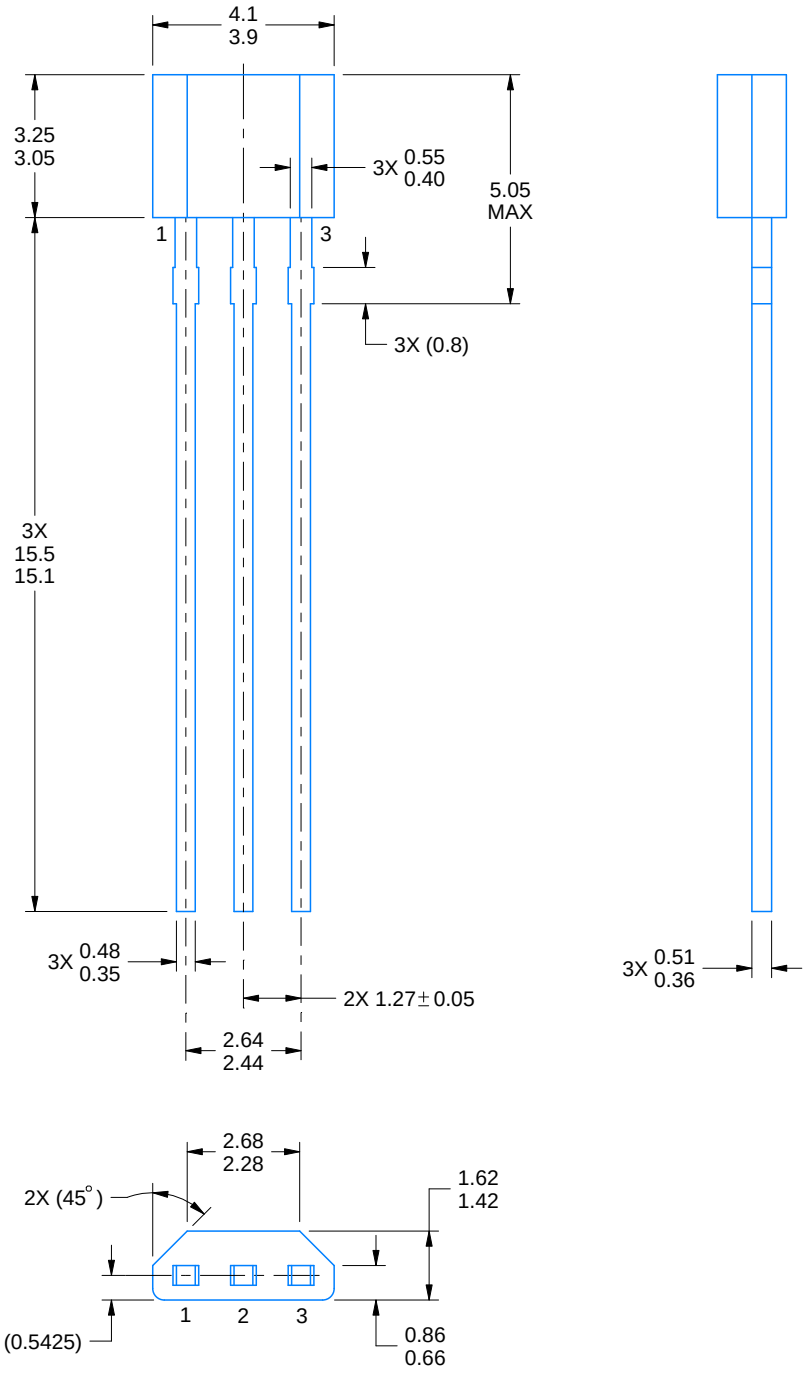
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

LPG0003A

TO-92 - 5.05 mm max height

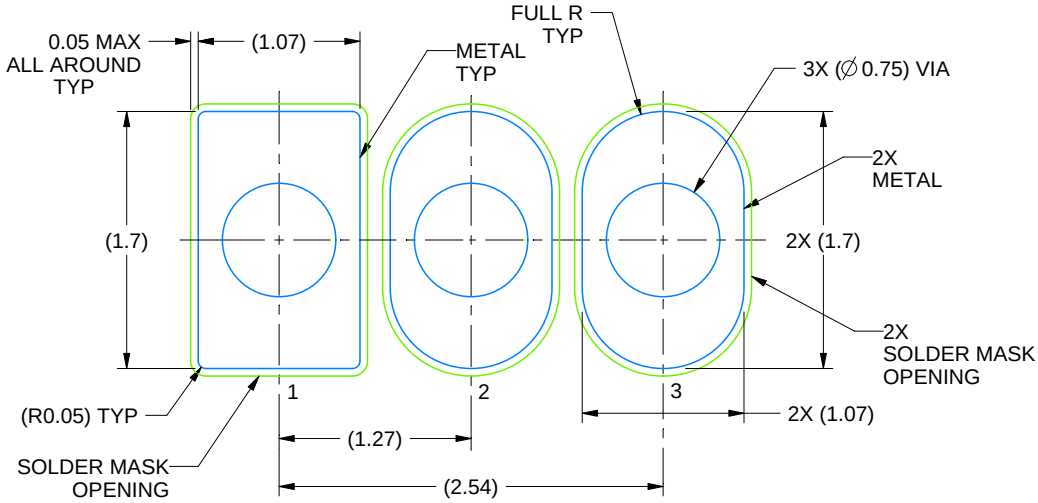
TRANSISTOR OUTLINE



4221343/C 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X

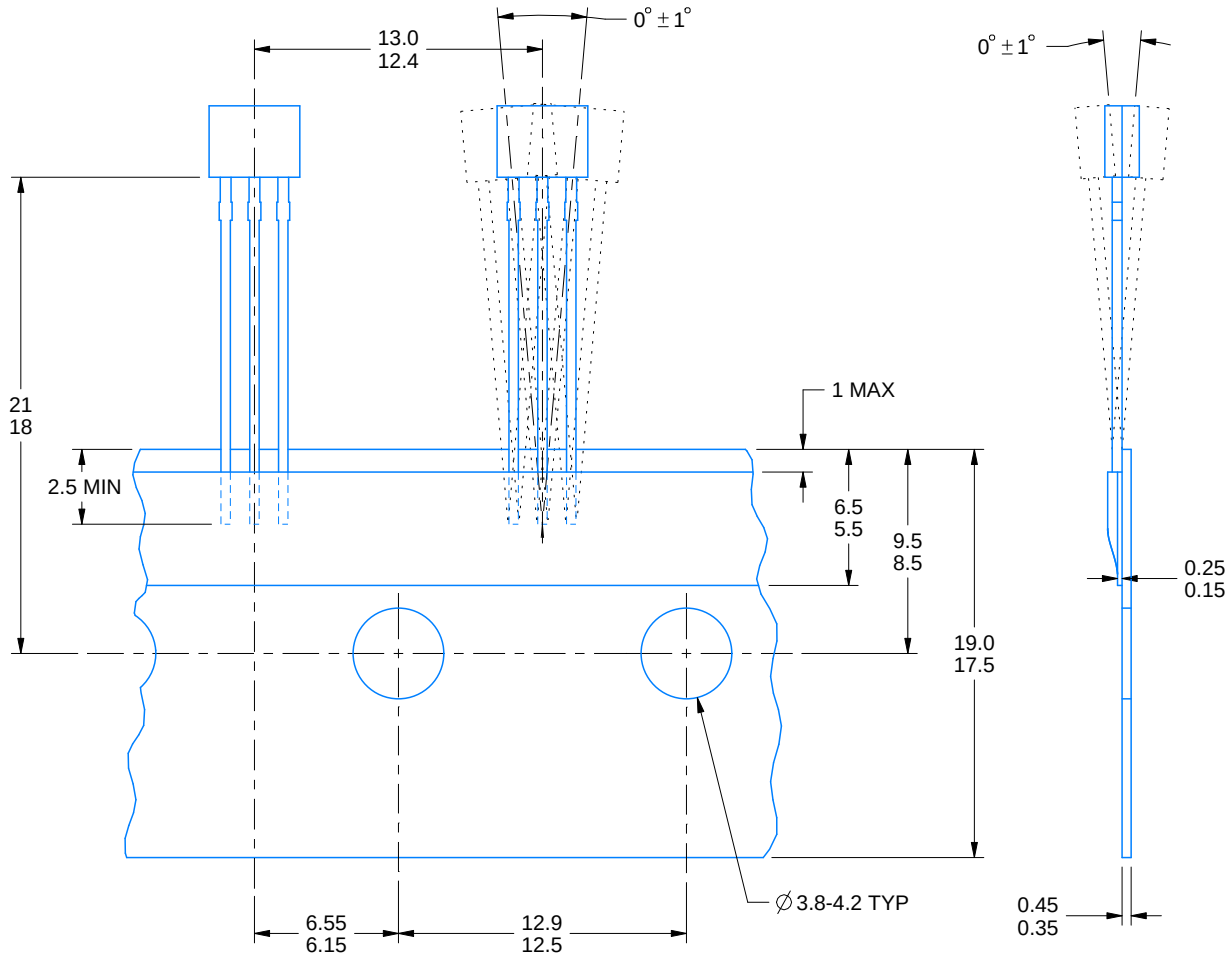
4221343/C 01/2018

TAPE SPECIFICATIONS

LPG0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



4221343/C 01/2018

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