Precision Voltage-to-Current Converter/Transmitter

Check for Samples: XTR111

FEATURES

- **EASY-TO-DESIGN INPUT/OUTPUT RANGES: 0mA–20mA, 4mA–20mA, 5mA–25mA AND VOLTAGE OUTPUTS**
- **NONLINEARITY: 0.002%**
- **LOW OFFSET DRIFT: 1µV/°C**
- **ACCURACY: 0.015%**
- **SINGLE-SUPPLY OPERATION**
- **WIDE SUPPLY RANGE: 7V to 44V**
- **OUTPUT ERROR FLAG ($\overline{EF}$)**
- **OUTPUT DISABLE (OD)**
- **ADJUSTABLE VOLTAGE REGULATOR: 3V to 15V**

APPLICATIONS

- **UNIVERSAL VOLTAGE-CONTROLLED CURRENT SOURCE**
- **CURRENT OR VOLTAGE OUTPUT FOR 3-WIRE SENSOR SYSTEMS**
- **PLC OUTPUT PROGRAMMABLE DRIVER**
- **CURRENT-MODE SENSOR EXCITATION**

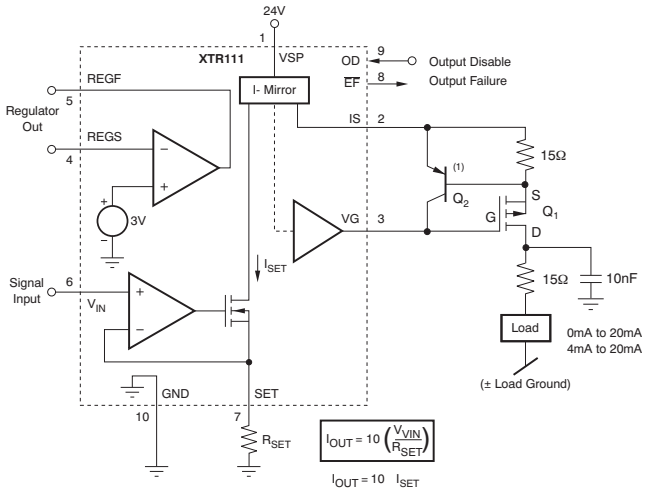
DESCRIPTION

The XTR111 is a precision voltage-to-current converter designed for the standard 0mA–20mA or 4mA–20mA analog signals, and can source up to 36mA. The ratio between input voltage and output current is set by the single resistor R_{SET}. The circuit can also be modified for voltage output.

An external P-MOSFET transistor ensures high output resistance and a broad compliance voltage range that extends from 2V below the supply voltage, V_{VSP}, to voltages well below GND.

The adjustable 3V to 15V sub-regulator output provides the supply voltage for additional circuitry.

The XTR111 is available in MSOP and DFN surface-mount packages.



NOTE: (1) See Application Information, External Current Limit Circuits for other options.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2006–2011, Texas Instruments Incorporated

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
XTR111	DFN-10	DRC	BSV
	MSOP-10	DGQ	CCM

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1) (2)

Over operating free-air temperature range (unless otherwise noted)

	XTR111	UNIT
Power Supply Voltage, V_{VSP}	+44	V
Voltage at SET(3)	–0.5 to +14	V
Voltage at IS(3) (4)	(V_{VSP}) – 5.5 to (V_{VSP}) + 0.5	V
Voltage at REGS, REGF, VIN, OD, $\overline{EF}$	–0.5 to (V_{VSP}) + 0.5	V
Voltage at REGF, VG	–0.5 to (V_{VSP}) + 0.5	V
Current into any pin(3) (4) (5)	±25	mA
Output Short-Circuit Duration(6):		
VG	Continous to common and V_{VSP}	
REGF	Continous to common and V_{VSP}	
Operating Temperature	–55 to +125	°C
Storage Temperature	–65 to +150	°C
Electrostatic Discharge Rating (HBM)	2000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Refer to the Package Option Addendum at the end of this document for lead temperature ratings.
(3) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited.
(4) The IS pin current absolute maximum rating is +25mA and –50mA.
(5) See the following sections Explanation of Pin Functions, External MOSFET, and Voltage Regulator in Application Information regarding safe voltage ranges and currents.
(6) See text in Application Information regarding safe voltage ranges and currents.

Copyright © 2006–2011, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range: **T_A = –40°C to +85°C.**
All specifications at T_A = +25°C, V_{VSP} = +24V, R_{SET} = 2.0kΩ, REGF connected to REGS; OD = Low, External FET connected, unless otherwise noted.

PARAMETER		CONDITIONS	XTR111 MIN	XTR111 TYP	XTR111 MAX	UNIT
TRANSMITTER						
Transfer Function				$I_{OUT} = 10 \times V_{VIN}/R_{SET}$		
Specified Output Current	I_{OUT}	Specified Performance(1)	0.1		25	mA
		Derated Performance(2)		0 to 36		mA
Current Limit for Output Current				42 ± 6		mA
Nonlinearity, I_{OUT}/I_{SET} (2) (3)		0.1mA to 25mA		0.002	0.02	% of Span
		0.1mA to 36mA		0.004		% of Span
Offset Current	I_{OS}	I_{OUT} = 4mA(1)		0.002	0.02	% of Span
vs Temperature				**0.0002**	**0.001**	**% of Span/°C**
vs Supply, V_{VSP}		8V to 40V Supply		0.0001	0.005	% of Span/V
Span Error, I_{OUT}/I_{SET} (2)		0.1mA to 25mA		0.015	0.1	% of Span
vs Temperature(1) (2)				**5**		**ppm/°C**
vs Supply(1)				0.0001		% of Span/V
Output Resistance		From Drain of Q_{EXT} (4)		> 1		GΩ
Output Leakage		OD = high		< 1		µA
Input Impedance (VIN)				2.4/30		GΩ/pF
Input Bias Current (VIN)	I_B			15	25	nA
Input Offset Voltage(2)	V_{OS}	V_{VIN} = 20mV		0.3	1.5	mV
vs Temperature				**1.5**		**µV/°C**
Input Voltage Range(5)	**V_{VIN}**			**0 to 12**		**V**
Noise, Referred to Input(2)		0.1Hz to 10Hz; I_{OUT} = 4mA		2.5		μV_{PP}
Dynamic Response				See Dynamic Performance Section		

(1) Includes input amplifier, but excludes R_{SET} tolerance. Offset current is the deviation from the current ratio of I_{SET} to I_{IS} (output current).
(2) See Typical Characteristics.
(3) Span is the change in output current resulting from a full-scale change in input voltage.
(4) Within compliance range limited by (+V_{VSP} – 2V) +V_{DS} required for linear operation of Q_{EXT}.
(5) See Application Information, *Input Voltage* section.

Copyright © 2006–2011, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

Boldface limits apply over the specified temperature range: **T_A = –40°C to +85°C.**
All specifications at T_A = +25°C, V_{VSP} = +24V, R_{SET} = 2.0kΩ, REGF connected to REGS; OD = Low, External FET connected, unless otherwise noted.

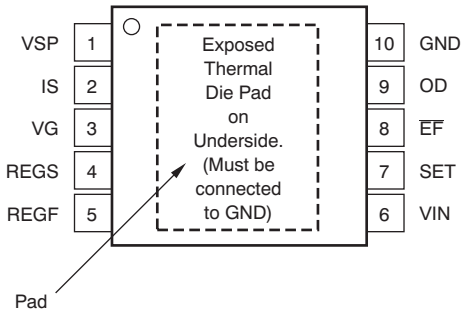
PARAMETER	CONDITIONS	XTR111 MIN	XTR111 TYP	XTR111 MAX	UNIT
V-Regulator Output (REGF)					
Voltage Reference(6)	R_{LOAD} = 5kΩ	2.85	3.0	3.15	V
vs Temperature(6)			**30**		**ppm/°C**
vs Supply(6)			0.1		mV/V
Bias Current into REGS(6)			0.8		µA
Load Regulation	0.6mA to 5mA		3	5	mV/mA
Supply Regulation(6)	R_{LOAD} = 5kΩ		0.01		mV/V
Output Current		5			mA
Short-Circuit Output Current			21		mA
DIGITAL INPUT (OD)					
V_{IL} Low-Level Threshold				**0.6**	**V**
V_{IH} High-Level Threshold		**1.8**			**V**
Internal Pull-Up Current	V_{OD} < 5.5V		4		µA
DIGITAL OUTPUT ($\overline{EF}$)					
I_{OH} Leakage Current (Open Drain)			1		µA
V_{OL} Low-Level Output Voltage	I_{EF} = 2.2mA			0.8	V
I_{OL} Current to 400mV Level	V_{EF} = 400mV		2		mA
POWER SUPPLY					
Specified Voltage Range		+8		+40	V
Operating Voltage			+7 to +44		V
Quiescent Current(6) I_Q	I_{OUT} = 0mA		450	550	µA
TEMPERATURE RANGE					
Specified Range		–40		+85	°C
Operating Range		–55		+125	°C
Package Thermal Impedance, θ_{JA}					
DFN			70		°C/W
MSOP			63		°C/W

(6) See Typical Characteristics.

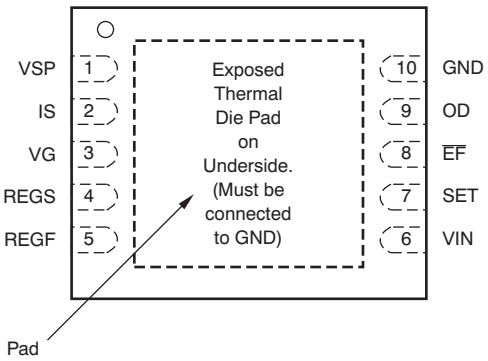
Copyright © 2006–2011, Texas Instruments Incorporated

PIN CONFIGURATIONS

DGQ PACKAGE
MSOP-10
TOP VIEW



DRC PACKAGE
DFN-10
TOP VIEW



PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	VSP	Positive Supply
2	IS	Source Connection
3	VG	Gate Drive
4	REGS	Regulator Sense
5	REGF	Regulator Force
6	VIN	Input Voltage
7	SET	Transconductance Set
8	$\overline{EF}$	Error Flag (Active Low)
9	OD	Output Disable (Active High)
10	GND	Negative Supply
Pad	Pad	Exposed Thermal Pad must be connected to GND

Copyright © 2006–2011, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS

At T_A = +25°C and V_{VSP} = +24V, unless otherwise noted.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

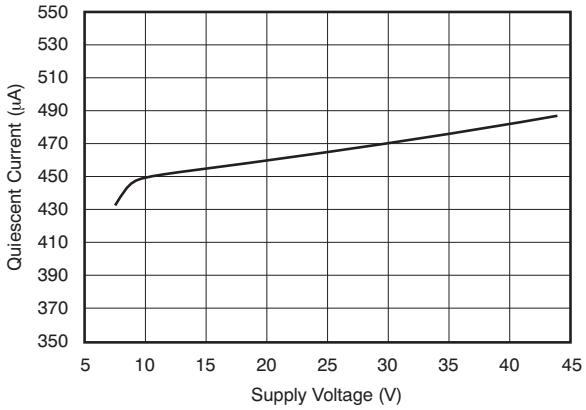


Figure 1.

QUIESCENT CURRENT vs TEMPERATURE

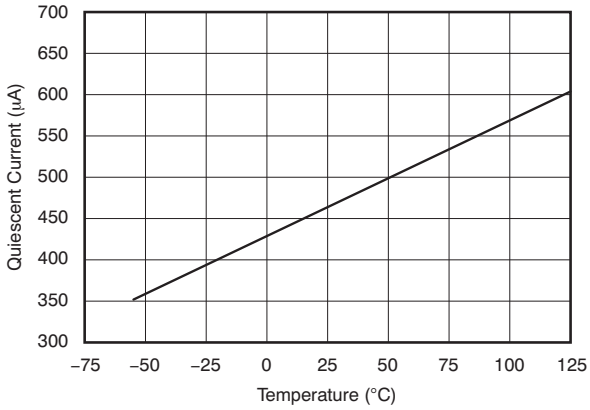


Figure 2.

GAIN vs FREQUENCY

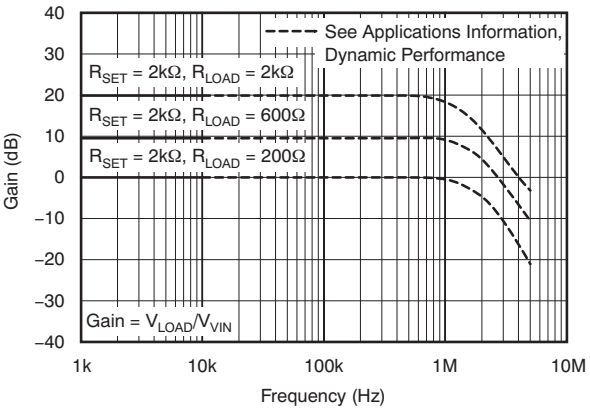


Figure 3.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

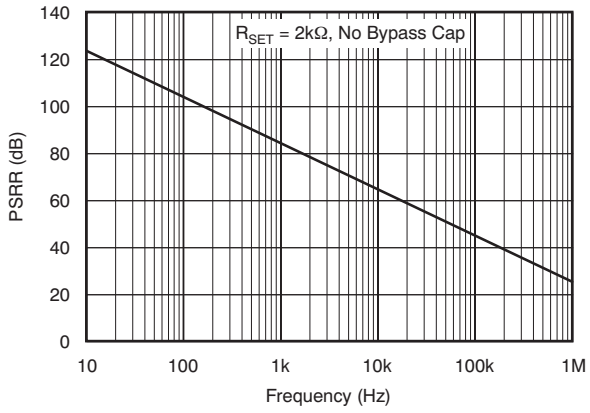


Figure 4.

0.1Hz to 10Hz NOISE, RTI

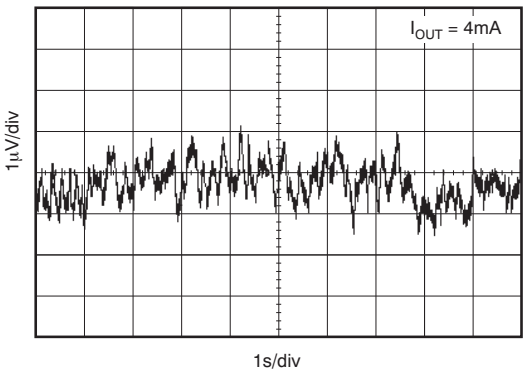


Figure 5.

INPUT-REFERRED NOISE SPECTRUM

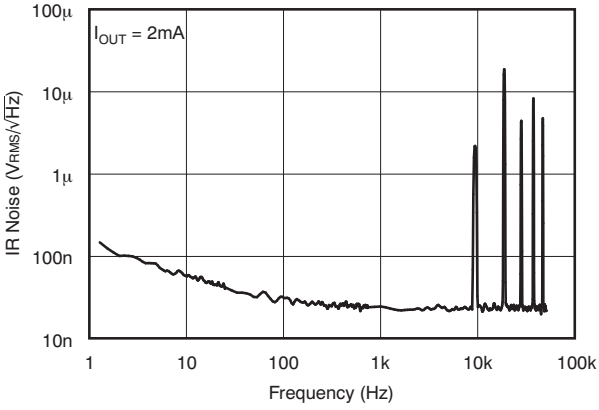


Figure 6.

Copyright © 2006–2011, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{VSP} = +24V, unless otherwise noted.

NONLINEARITY DISTRIBUTION

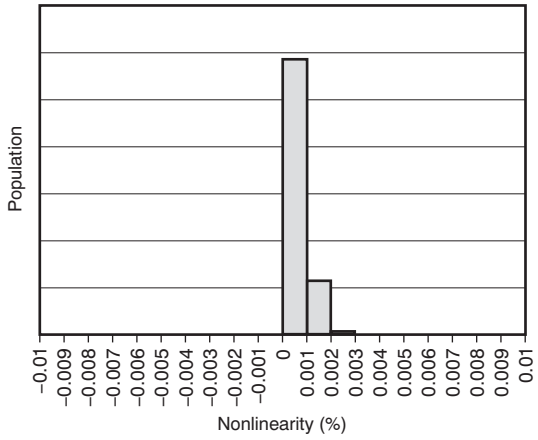


Figure 7.

GAIN ERROR DISTRIBUTION

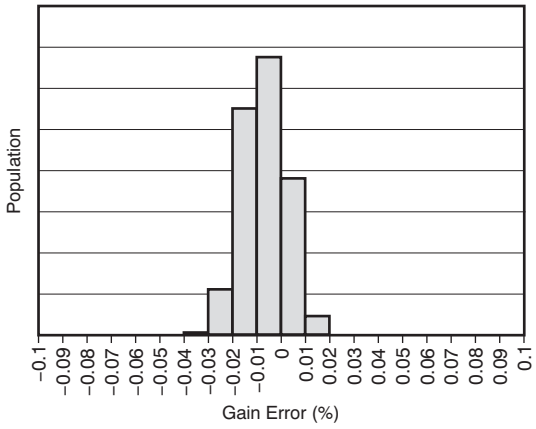


Figure 8.

NONLINEARITY vs TEMPERATURE

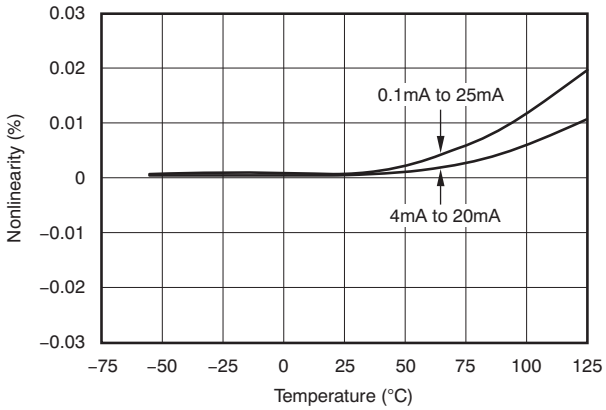


Figure 9.

NONLINEARITY DRIFT DISTRIBUTION
(I_{OUT} = 0.1mA to 25mA; T = –55°C to +125°C)

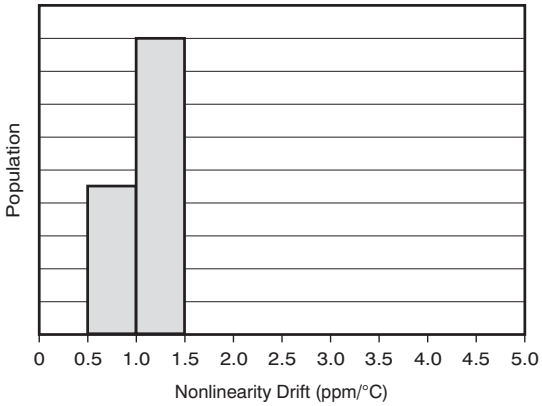


Figure 10.

GAIN ERROR vs TEMPERATURE

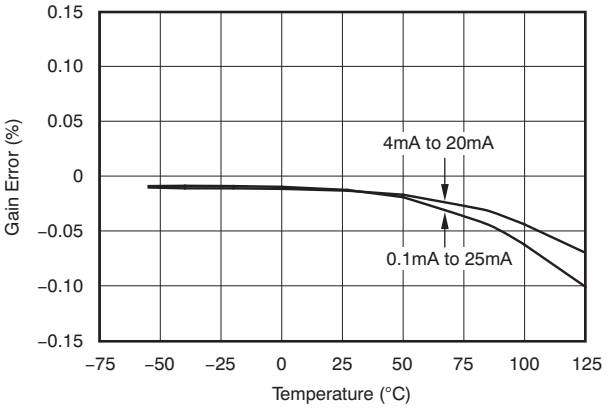


Figure 11.

GAIN ERROR DRIFT DISTRIBUTION
(I_{OUT} = 0.1mA to 25mA; T = –55°C to +125°C)

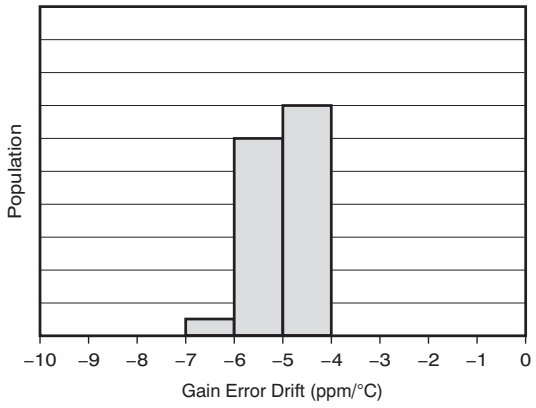


Figure 12.

Copyright © 2006–2011, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{VSP} = +24V, unless otherwise noted.

TYPICAL NONLINEARITY (2pt Calibration at 4mA and 20mA)

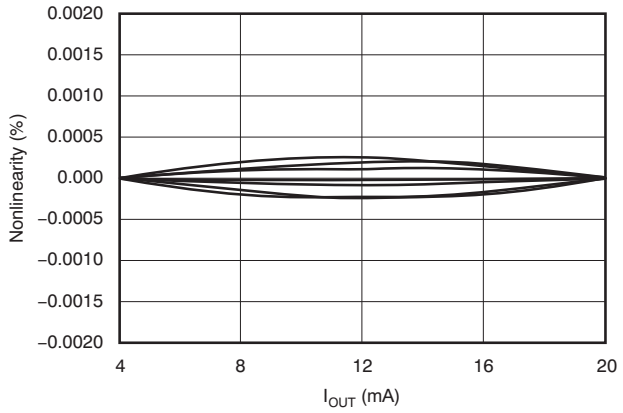


Figure 13.

TYPICAL NONLINEARITY (2pt Calibration at 0.1mA and 25mA)

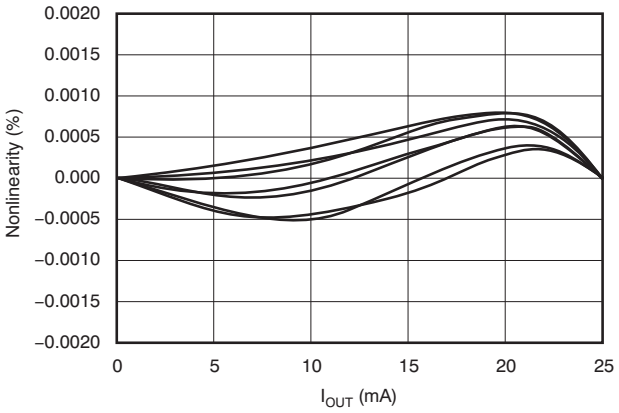


Figure 14.

TYPICAL NONLINEARITY (2pt Calibration at 0.1mA and 36mA)

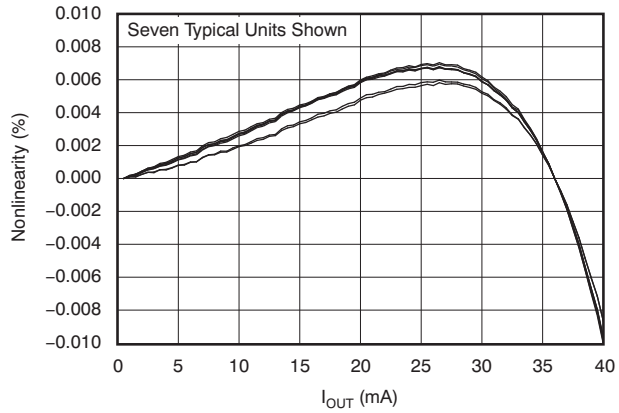


Figure 15.

INPUT VOLTAGE RANGE LIMIT TO THE POSITIVE SUPPLY vs TEMPERATURE

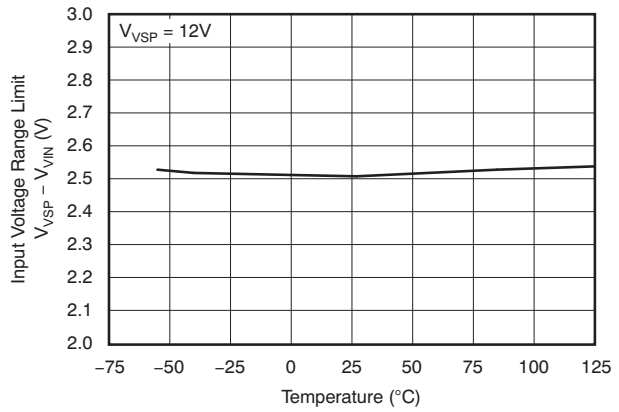


Figure 16.

OUTPUT SWING OF THE VOLTAGE ON IS PIN (V_{IS}) vs OUTPUT CURRENT

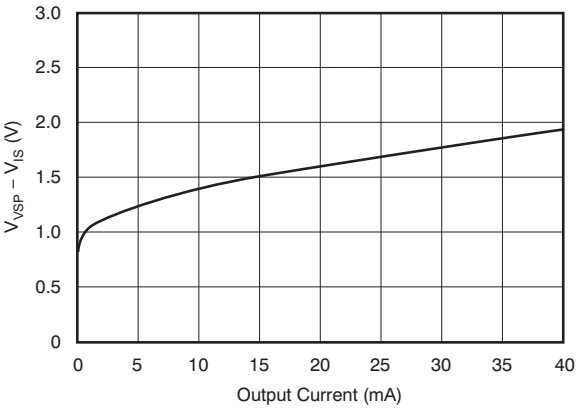


Figure 17.

OUTPUT SWING OF THE VOLTAGE ON IS PIN (V_{IS}) vs TEMPERATURE

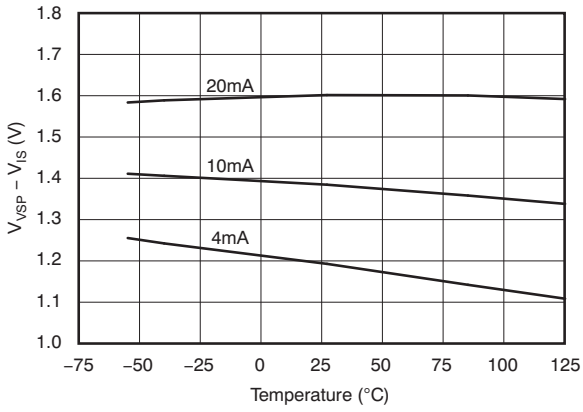


Figure 18.

Copyright © 2006–2011, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{VSP} = +24V, unless otherwise noted.

INPUT OFFSET VOLTAGE DISTRIBUTION

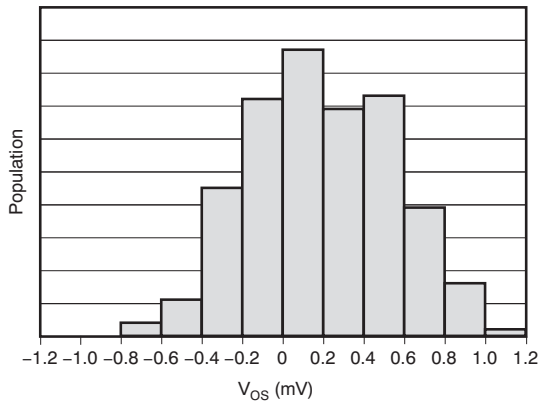


Figure 19.

INPUT OFFSET VOLTAGE DRIFT DISTRIBUTION

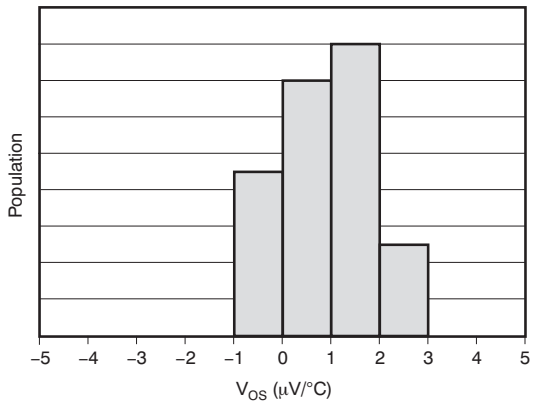


Figure 20.

INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE

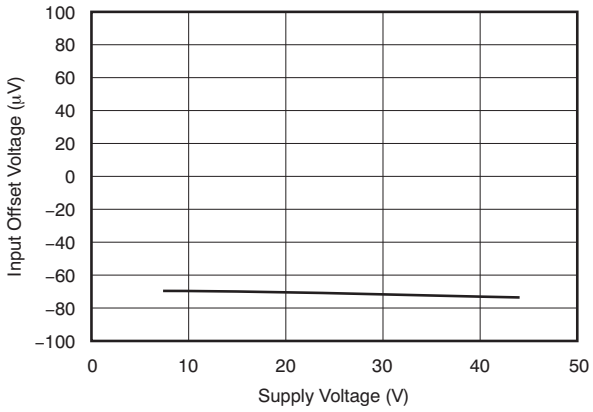


Figure 21.

AMPLIFIER INPUT BIAS CURRENT vs TEMPERATURE

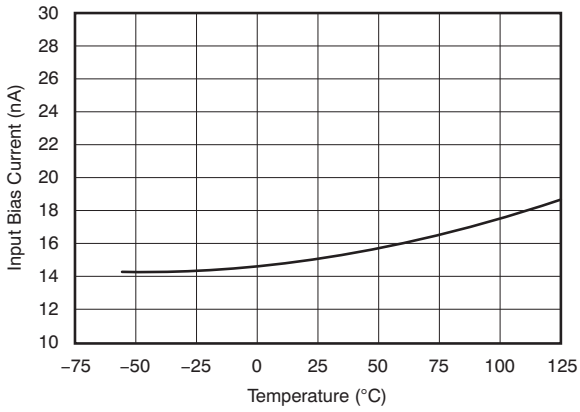


Figure 22.

OUTPUT CURRENT LIMIT DISTRIBUTION

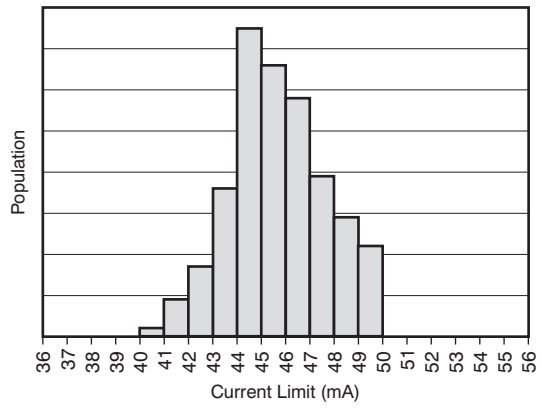


Figure 23.

OUTPUT CURRENT LIMIT vs TEMPERATURE

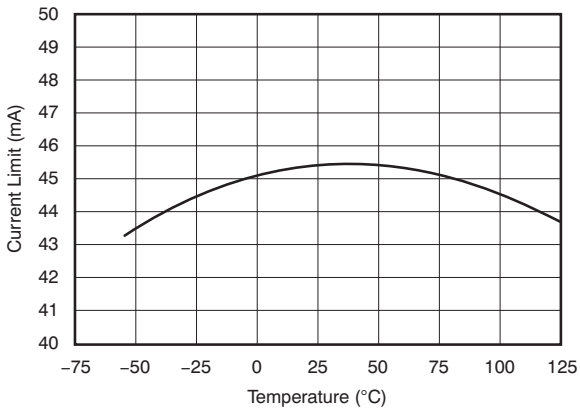


Figure 24.

Copyright © 2006–2011, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{VSP} = +24V, unless otherwise noted.

REGULATOR VOLTAGE DISTRIBUTION

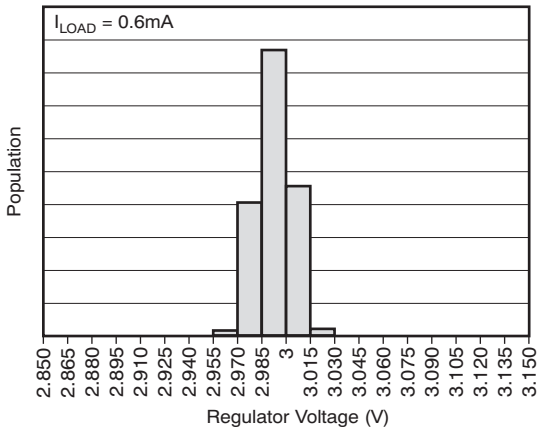


Figure 25.

REGULATOR VOLTAGE DRIFT DISTRIBUTION

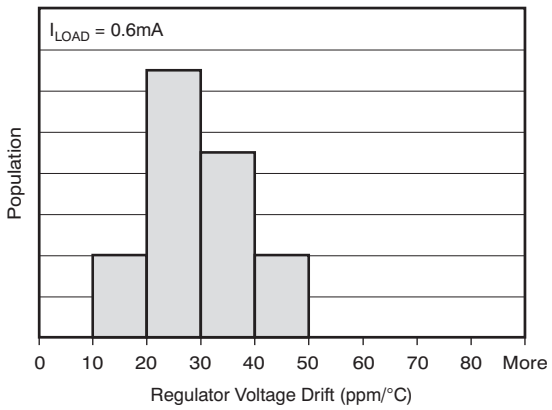


Figure 26.

REGULATOR INPUT BIAS CURRENT DISTRIBUTION (Current into REGS Pin)

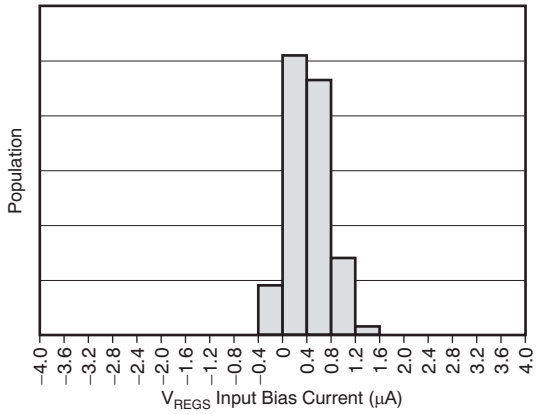


Figure 27.

REGULATOR INPUT BIAS CURRENT DRIFT DISTRIBUTION (Drift of Current into REGS Pin)

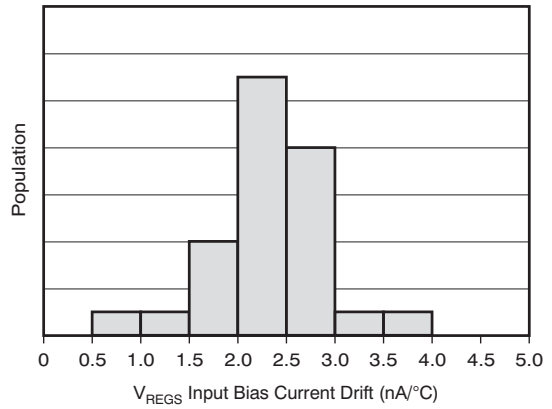


Figure 28.

REGULATOR VOLTAGE vs SUPPLY VOLTAGE

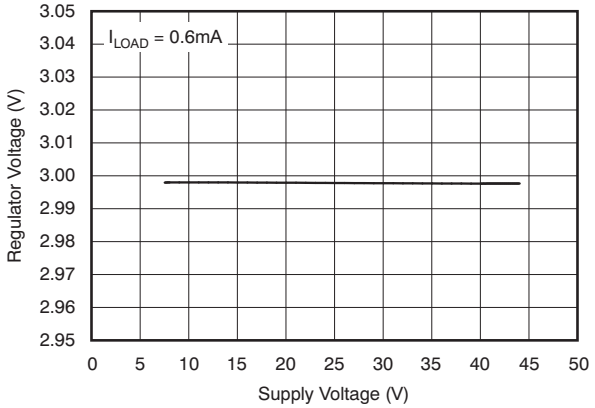


Figure 29.

REGULATOR VOLTAGE vs TEMPERATURE

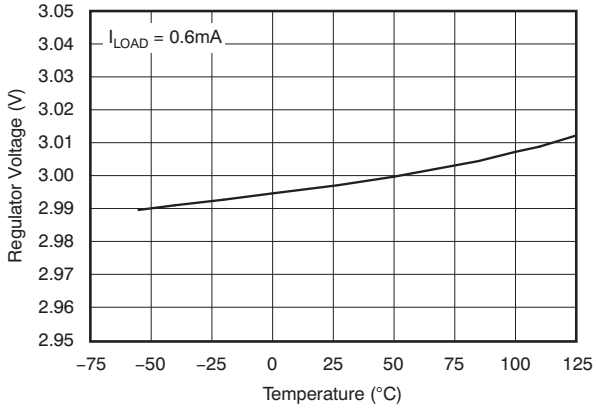


Figure 30.

Copyright © 2006–2011, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_{VSP} = +24V, unless otherwise noted.

STEP RESPONSE: V_{FS} = 4V, R_{SET} = 2kΩ, R_{LD} = 600Ω (Rising Edge Depends on C_{GATE} at VG Pin)

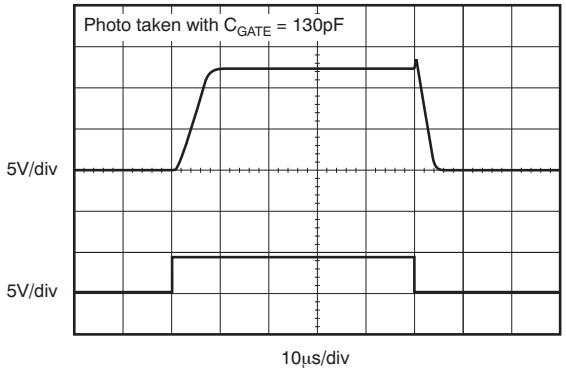


Figure 31.

STEP RESPONSE: V_{FS} = 2.5V, R_{SET} = 1.25kΩ, R_{LD} = 600Ω (Rising Edge Depends on C_{GATE} at VG Pin)

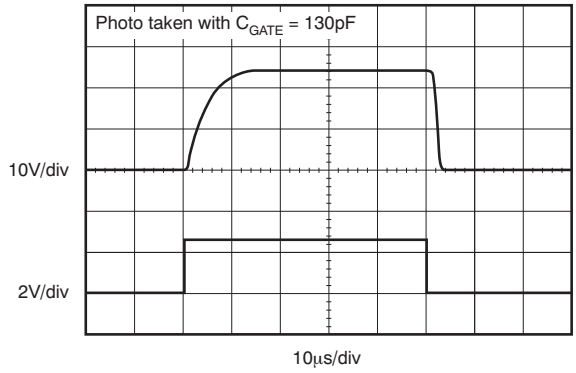


Figure 32.

REGULATOR LOAD TRANSIENT (V_{REG} Gain = 1V, V_{REGF} = 3V, C_L = 470nF, I_{LOAD} = 3mA ± 0.3mA)

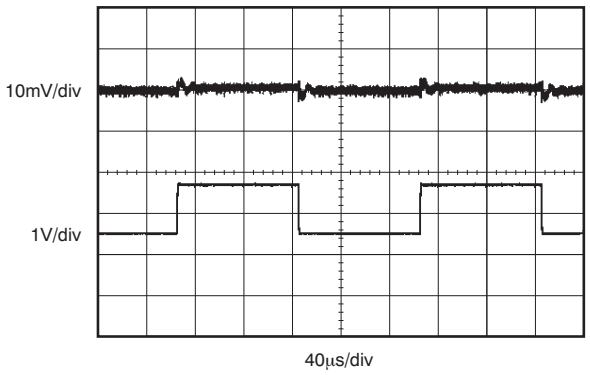


Figure 33.

REGULATOR LOAD TRANSIENT (V_{REG} Gain = 4V, V_{REGF} = 12V, C_L = 470nF, I_{LOAD} = 3mA ± 0.3mA)

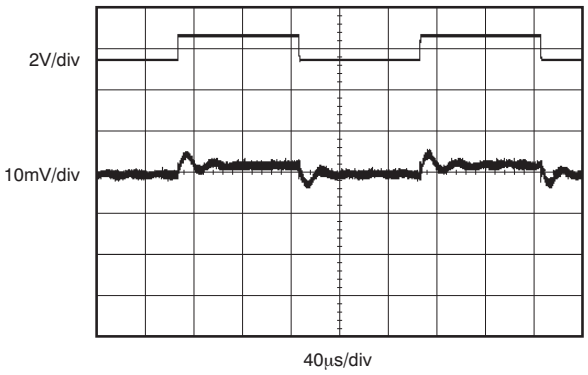


Figure 34.

MAXIMUM REGULATOR CURRENT vs TEMPERATURE

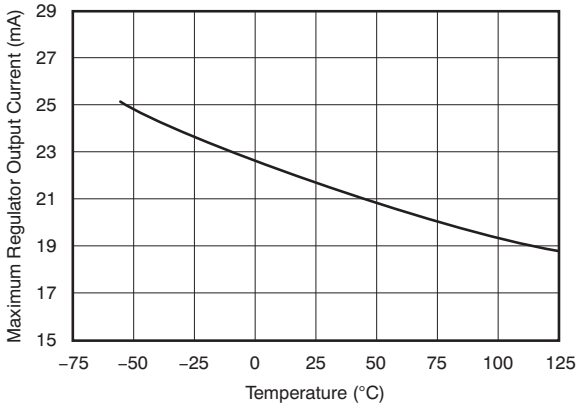


Figure 35.

Copyright © 2006–2011, Texas Instruments Incorporated

APPLICATION INFORMATION

The XTR111 is a voltage-controlled current source capable of delivering currents from 0mA to 36mA. The primary intent of the device is to source the commonly-used industrial current ranges of 0mA–20mA or 4mA–20mA. The performance is specified for a supply voltage of up to 40V. The maximum supply voltage is 44V. The voltage-to-current ratio is defined by an external resistor, R_{SET}; therefore, the input voltage range can be freely set in accordance with the application requirement. The output current is cascoded by an external P-Channel MOSFET transistor for large voltage compliance extending below ground, and for easy power dissipation. This arrangement ensures excellent suppression of typical interference signals from the industrial environment because of the extremely high output impedance and wide voltage compliance.

An error detection circuit activates a logic output (error flag) in case the output current cannot correctly flow. It indicates a wire break, high load resistor, or loss of headroom for the current output to the positive supply. The output disable (OD) provided can be used during power-on, multiplexing and other conditions where the output should present no current. It has an internal pull-up that causes the XTR111 to come up in output disable mode unless the OD pin is tied low.

The onboard voltage regulator can be adjusted between 3V to 15V and delivers up to 5mA load current. It is intended to supply signal conditioning and sensor excitation in 3-wire sensor systems. Voltages above 3V can be set by a resistive divider.

Figure 36 shows a basic connection for the XTR111. The input voltage V_{VIN} reappears across R_{SET} and controls 1/10 of the output current. The I-Mirror has a precise current gain of 10. This configuration leads to the transfer function:

$$I_{OUT} = 10 \bullet (V_{VIN}/R_{SET})$$

The output of the voltage regulator can be set over the range of 3V to 12V by selecting R_1 and R_2 using the following equation.

$$V_{REGF} = 3V \bullet (R_1 + R_2)/R_2 \quad (1)$$

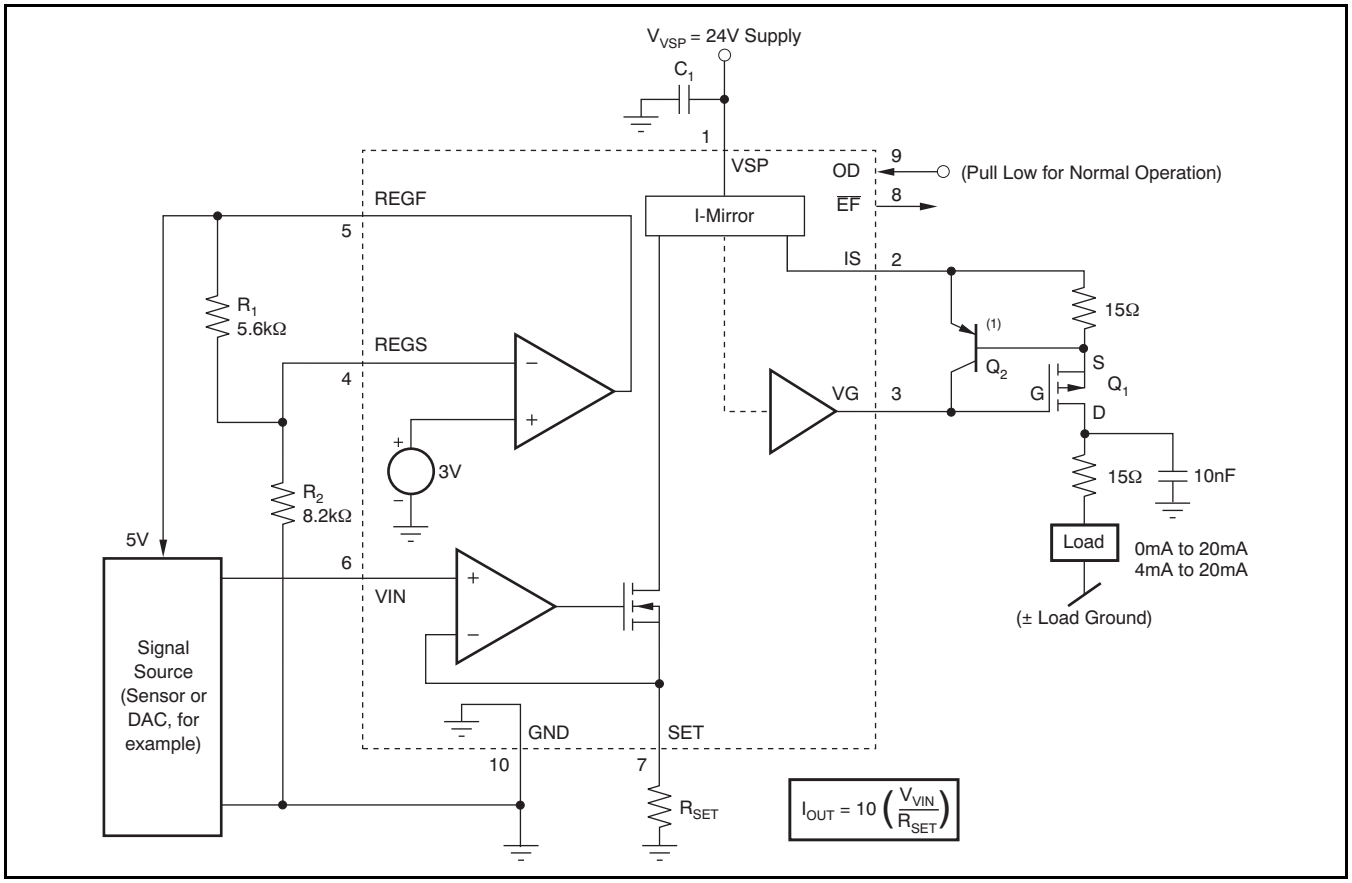


Figure 36. Basic Connection for 0mA to 20mA Related to 0V to 5V Signal Input. The Voltage Regulator is Set to 5V Output

Copyright © 2006–2011, Texas Instruments Incorporated

EXPLANATION OF PIN FUNCTIONS

VIN: This input is a conventional, noninverting, high-impedance input of the internal operational amplifier (OPA). The internal circuitry is protected by clamp diodes to supplies. An additional clamp connected to approximately 18V protects internal circuitry. Place a small resistor in series with the input to limit the current into the protection if voltage can be present without the XTR111 being powered. Consider a resistor value equal to R_{SET} for bias current cancellation.

SET: The total resistance connected between this pin and VIN reference sets the transconductance. Additional series resistance can degrade accuracy and drift. The voltage on this pin must not exceed 14V because this pin is not protected to voltages above this level.

IS: This output pin is connected to the transistor source of the external FET. The accuracy of the output current to IS is achieved by dynamic error correction in the current mirror. This pin should never be pulled more than 6.5V below the positive supply. An internal clamp is provided to protect the circuit; however, it must be externally current-limited to less than 50mA.

VG: The gate drive for the external FET is protected against shorts to the supply and GND. The circuit is clamped so that it will not drive more than 18V below the positive supply. The external FET should be protected if its gate could be externally pulled beyond its ratings.

REGF: The output of the regulator buffer can source up to 5mA current, but has very limited (less than 50µA) sinking capability. The maximum short-circuit current is in the range of 15mA to 25mA, changing over temperature.

REGS: This pin is the sense input of the voltage regulator. It is referenced to an internal 3V reference circuit. The input bias current can be up to 2µA. Avoid capacitive loading of REGS that may compromise the loop stability of the voltage regulator.

VSP: The supply voltage of up to a maximum of 44V allows operation in harsh industrial environment and provides headroom for easy protection against over-voltage. Use a large enough bypass capacitor (> 100nF) and eventually a damping inductor or a small resistor (5Ω) to decouple the XTR111 supply from the noise typically found on the 24V supplies.

$\overline{EF}$: The active low error flag (logic output) is intended for use with an external pull-up to logic-high for reliable operation when this output is used. However, it has a weak internal pull-up to 5V and can be left unconnected if not used.

OD: This control input has a 4µA internal pull-up disabling the output. A pull-down or short to GND is required to activate the output. Controlling OD reduces output glitches during power-on and power-off. This logic input controls the output. If not used, connect to GND.

The regulator is not affected by OD.

EXTERNAL CURRENT LIMIT

The XTR111 does not provide internal current limit for the case of when the external FET is forced to low impedance. The internal current source controls the current, but a high current from IS to GND forces an internal voltage clamp between VSP and IS to turn on. This results in a low resistance path and the current is only limited by the load impedance and the current capability of the external FET. A high current can destroy the IC. With the current loop interrupted (the load disconnected) the external MOSFET is fully turned on with large gate to source voltage stored in the gate capacitance. In the moment the loop is closed (the load connected) current flows into the load. But for the first few micro-seconds the MOSFET is still turned on and destructive current can flow, depending on the load impedance.

An external current limit is recommended to protect the XTR111 from this condition. Figure 37a shows an example of a current limit circuit. The current should be limited to 50mA. The 15Ω resistor (R_6) limits the current to approximately 37mA (33mA when hot). The PNP transistor should allow a peak current of several hundred mA. An example device is the (KST)2907. Power dissipation is not normally critical because the peak current duration is only a few micro-seconds. However, observe the leakage current through the transistor from IS to VG. The addition of this current limiting transistor and R_6 still require time to discharge the gate of the external MOSFET. R_7 and C_3 are added for this reason, as well as to limit the steepness of external distortion pulses. Additional EMI and over-voltage protection may be required according to the application.

Figure 37b is a universal and basic current limiter circuit, using PNP or NPN transistors that can be connected in the source (IS to S) or in the drain output (in series with the current path). This circuit does not contribute to leakage currents. Consider adding an output filter like R_7 and C_3 in this limiter circuit.

Copyright © 2006–2011, Texas Instruments Incorporated

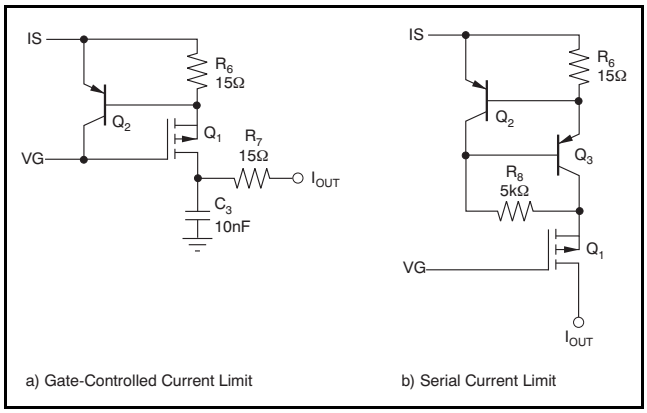


Figure 37. External Current Limit Circuits

EXTERNAL MOSFET

The XTR111 delivers the precise output current to the IS pin. The voltage at this pin is normally 1.4V below V_{VSP}.

This output requires an external transistor (Q_{EXT}) that forms a cascode for the current output. The transistor must be rated for the maximum possible voltage on V_{OUT} and must dissipate the power generated by the current and the voltage across it.

The gate drive (VG) can drive from close to the positive supply rail to 16V below the positive supply voltage (V_{VSP}). Most modern MOSFETs accept a maximum V_{GS} of 20V. A protection clamp is only required if a large drain gate capacitance can pulse the gate beyond the rating of the MOSFET. Pulling the OD pin high disables the gate driver and closes a switch connecting an internal 3kΩ resistor from the VSP pin to the VG pin. This resistor discharges the gate of the external FET and closes the channel; see Figure 38.

Table 1 lists some example devices in SO-compatible packages, but other devices can be used as well. Avoid external capacitance from IS. This capacitance could be compensated by adding additional capacitance from VG to IS; however, this compensation may slow the output down.

The drain-to-source breakdown voltage should be selected high enough for the application. Surge voltage protection might be required for negative over-voltages. For positive over-voltages, a clamp diode to the 24V supply is recommended, protecting the FET from reversing.

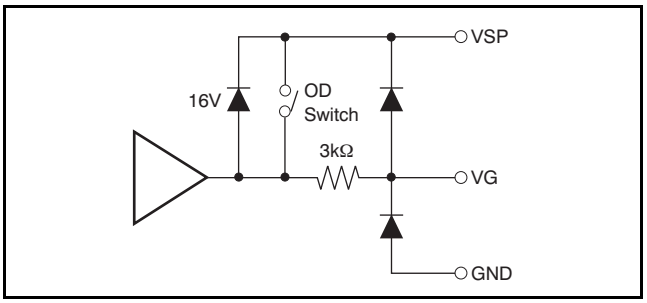


Figure 38. Equivalent Circuit for Gate Drive and Disable Switch

Table 1. P-Channel MOSFET (Examples)(1)

MANUFACTURER	PART NO.	BREAKDOWN VGS	PACKAGE	C-GATE
Infineon	BSP170P	–60V	SOT-223	328pF
NEC	2SJ326-Z	–60V	Spec.	320pF
ON Semiconductor	NTF2955	–60V	SOT-223	492pF
Supertex Inc.	TP2510	–100V	TO-243AA	80pF

(1) Data from published product data sheet; not ensured.

Copyright © 2006–2011, Texas Instruments Incorporated

DYNAMIC PERFORMANCE

The rise time of the output current is dominated by the gate capacitance of the external FET.

The accuracy of the current mirror relies on the dynamic matching of multiple individual current sources. Settling to full resolution may require a complete cycle lasting around 100µs. Figure 39 shows an example of the ripple generated from the individual current source values that average to the specified accuracy over the full cycle.

The output glitch magnitude depends on the mismatch of the internal current sources. It is approximately proportional to the output current level and scales directly with the load resistor value. It will differ slightly from part to part. The effects of filtering the output are shown in Figure 40 and Figure 41.

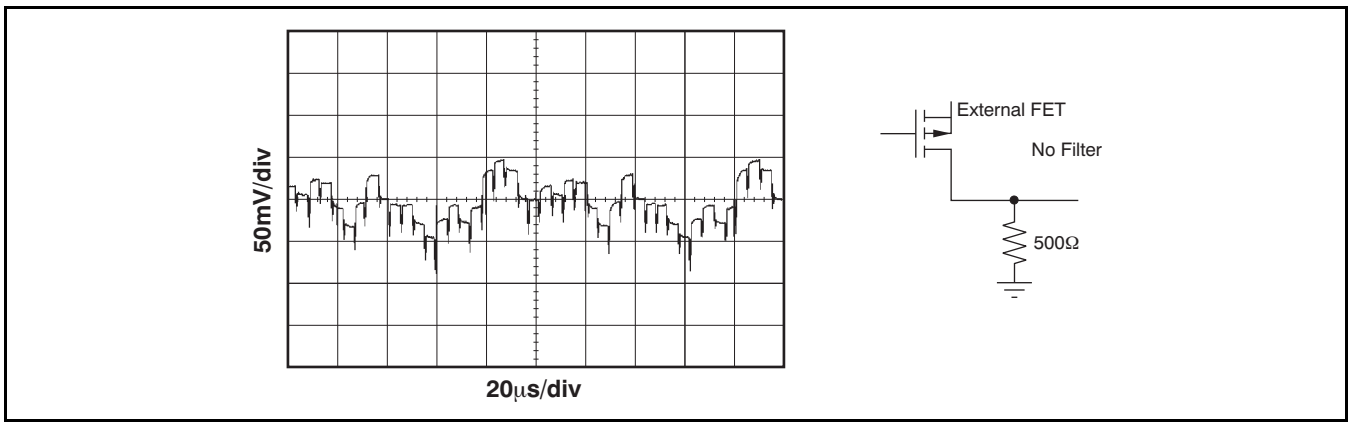


Figure 39. Output Noise without Filter into 500Ω

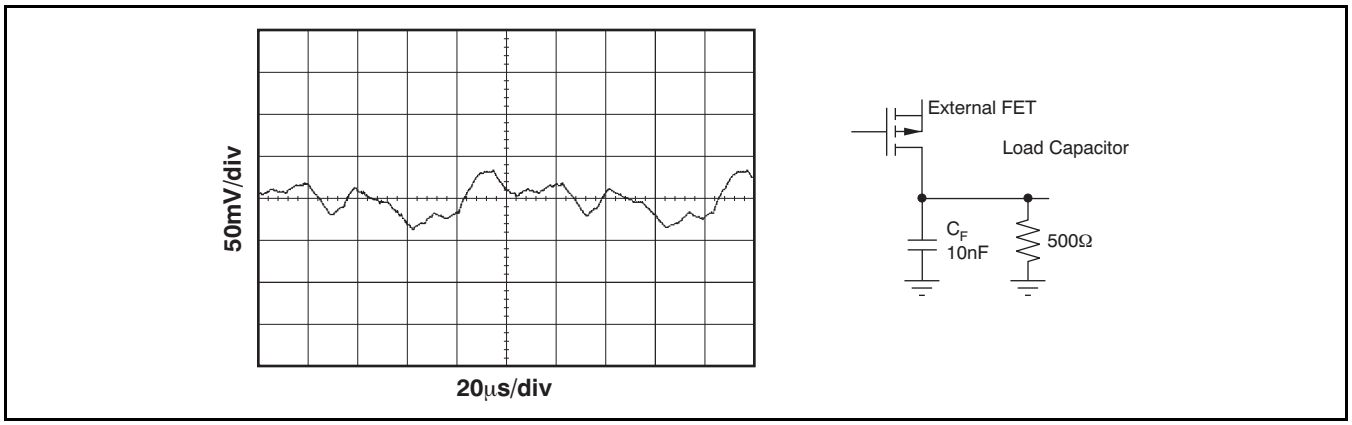


Figure 40. Output with 10nF Parallel to 500Ω

Copyright © 2006–2011, Texas Instruments Incorporated

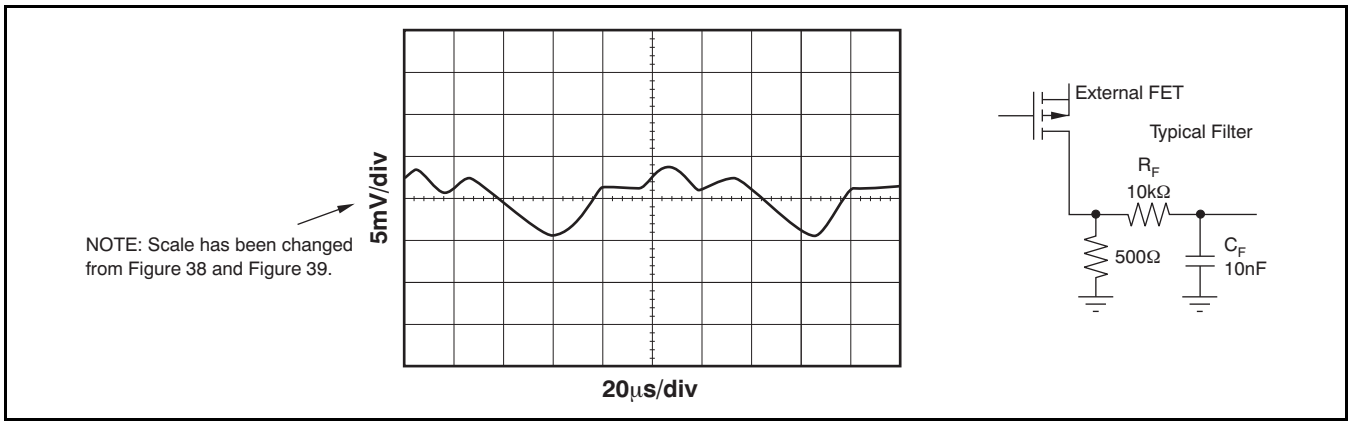


Figure 41. Output with Additional Filter

OUTPUT ERROR FLAG AND DISABLE INPUT

The XTR111 has additional internal circuitry to detect an error in the output current. In case the controlled output current cannot flow due to a wire break, high load resistance or the output voltage level approaching the positive supply, the error flag ($\overline{EF}$), an open drain logic output, pulls low. When used, this digital output requires external pull-up to logic high (the internal pull-up current is 2μA).

The output disable (OD) is a logic input with approximately 4μA of internal pull-up to 5V. The XTR111 comes up with the output disabled until the OD pin is pulled low. Logic high disables the output to zero output current. It can be used for calibration, power-on and power-off glitch reduction, and for output multiplexing with other outputs connected to the same terminal pin.

Power-on while the output is disabled (OD = high) cannot fully suppress output glitching. While the supply voltage passes through the range of 3V to 4V, internal circuits turn on. Additional capacitance between pins VG and IS can suppress the glitch. The smallest glitch energy appears with the OD pin left open; for practical use, however, this pin can be driven high through a 10kΩ resistor before the 24V supply is applied, if logic voltage is available earlier. Alternatively, an open drain driver can control this pin using the internal pull-up current. Pull-up to the internal regulator tends to increase the energy because of the delay of the regulator voltage increase, again depending on the supply voltage rise time for the first few volts.

INPUT VOLTAGE

The input voltage range for a given output current span is set by R_{SET} according to the transfer function. Select a precise and low drift resistor for best performance, because resistor drift directly converts into drift of the output current. Careful layout must also minimize any series resistance with R_{SET} and the VIN reference point.

The input voltage is referred to the grounding point of R_{SET}. Therefore, this point should not be distorted from other currents. Assuming a 5V full-scale input signal for a 20mA output current, R_{SET} is 2.5kΩ. A resistance uncertainty of just 2.5Ω already degrades the accuracy to below 0.1%.

The linear input voltage range extends from 0V to 12V, or 2.3V below the positive supply voltage (whichever is smaller). The lowest rated supply voltage accomodates an input voltage range of up to 5V. Potential clipping is not detected by an error signal; therefore, safe design guard banding is recommended.

Do not drive the input negative (referred to GND) more than 300mV. Higher negative voltages turn on the internal protection diodes. Insert a resistor in series with the input if negative signals can occur eventually during power-on or -off or during other transient conditions. Select a resistor value limiting the possible current to 0.3mA. Higher currents are non-destructive (see Absolute Maximum Ratings), but they can produce output current glitches unless in disable mode.

Copyright © 2006–2011, Texas Instruments Incorporated

More protection against negative input signals is provided using a standard diode and a 2.2kΩ resistor, as shown in Figure 42.

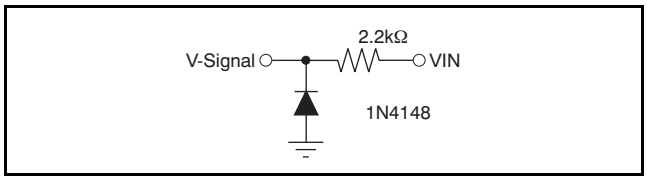


Figure 42. Enhanced Protection Against Negative Overload of V_{IN}

4mA–20mA OUTPUT

The XTR111 does not provide internal circuits to generate 4mA with 0V input signal. The most common way to shift the input signal is a two resistor network connected to a voltage reference and the signal source, as shown in Figure 43. This arrangement allows easy adjustment for over-and under-range. The example assumes a 5V reference (V_{REF}) that equals the full-scale signal voltage and a signal span of 0V to 5V for 4mA to 20mA (I_{MIN} to I_{MAX}) output.

The voltage regulator output or a more precise reference can be used as V_{REF}. Observe the potential drift added by the drift of the resistors and the voltage reference.

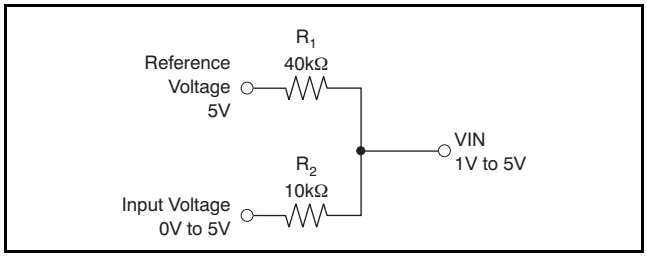


Figure 43. Resistive Divider for I_{MIN} to I_{MAX} Output (4mA to 20mA) with 0V to V_{FS} Signal Source

LEVEL SHIFT OF 0V INPUT AND TRANSCONDUCTANCE TRIM

The XTR111 offers low offset voltage error at the input, which normally does not require cancellation. If the signal source cannot deliver 0V in a single-supply circuit, an additional resistor from the SET pin to a positive reference voltage or the regulator output (Figure 44) can shift the zero level for the input (V_{IN}) to a positive voltage. Therefore, the signal source can drive this value within a positive voltage range. The example shows a +100mV (102.04mV) offset generated to the signal input. The larger this offset, however, the more influence of its drift and inaccuracy is seen in the output signal. The voltage at SET should not be larger than 12V for linear operation.

Transconductance (the input voltage to output current ratio) is set by R_{SET}. The desired resistor value may be found by choosing a combination of two resistors.

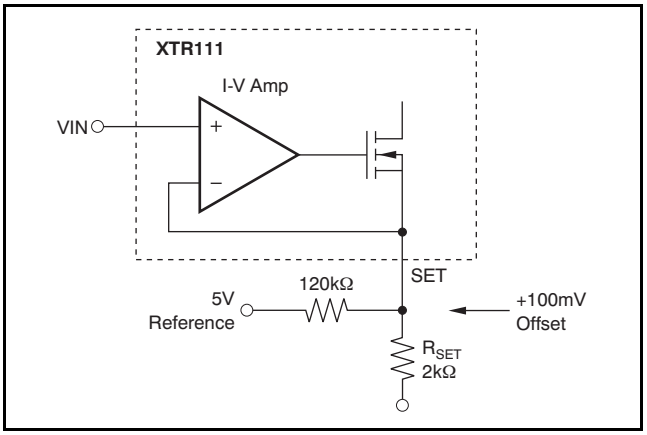


Figure 44. Input Voltage Level Shift for 0mA Output Current

Copyright © 2006–2011, Texas Instruments Incorporated

VOLTAGE REGULATOR

The externally adjustable voltage regulator provides up to 5mA of current. It offers drive (REGF) and sense (REGS) to allow external setting of the output voltage as shown in Figure 45. The sense input (REGS) is referenced to 3.0V representing the lowest adjustable voltage level. An external resistor divider sets V_{REGF}.

$$V_{REGF} = V_{REGS} \bullet (R_1 + R_2)/R_2$$

Table 2 provides example values for the regulator adjustment resistors.

Table 2. Examples for the Resistor Values Setting the Regulator Voltage

V_{REGF} (1)	R_1	R_2
3V	0	—
3.3V	3.3kΩ	33kΩ
5V	5.6kΩ	8.2kΩ
12.4V	27kΩ	8.6kΩ
(1) Values have been rounded.		

The voltage at REGF is limited by the supply voltage. If the supply voltage drops close to the set voltage, the driver output saturates and follows the supply with a voltage drop of less than 1V (depending on load current and temperature).

For good stability and transient response, use a load capacitance of 470nF or larger. The bias current into the sense input (REGS) is typically less than 1µA. This current should be considered when selecting high resistance values for the voltage setting because it lowers the voltage and produces additional temperature dependence.

The REGF output cannot sink current. In case of supply voltage loss, the output is protected against the discharge currents from load capacitors by internal protection diodes; the peak current should not exceed 25mA.

If the voltage regulator output is not used, connect REGF to REGS (the 3V mode) loaded with a 2.2nF capacitor. Alternatively, overdrive the loop pulling REGS high (see Figure 45d).

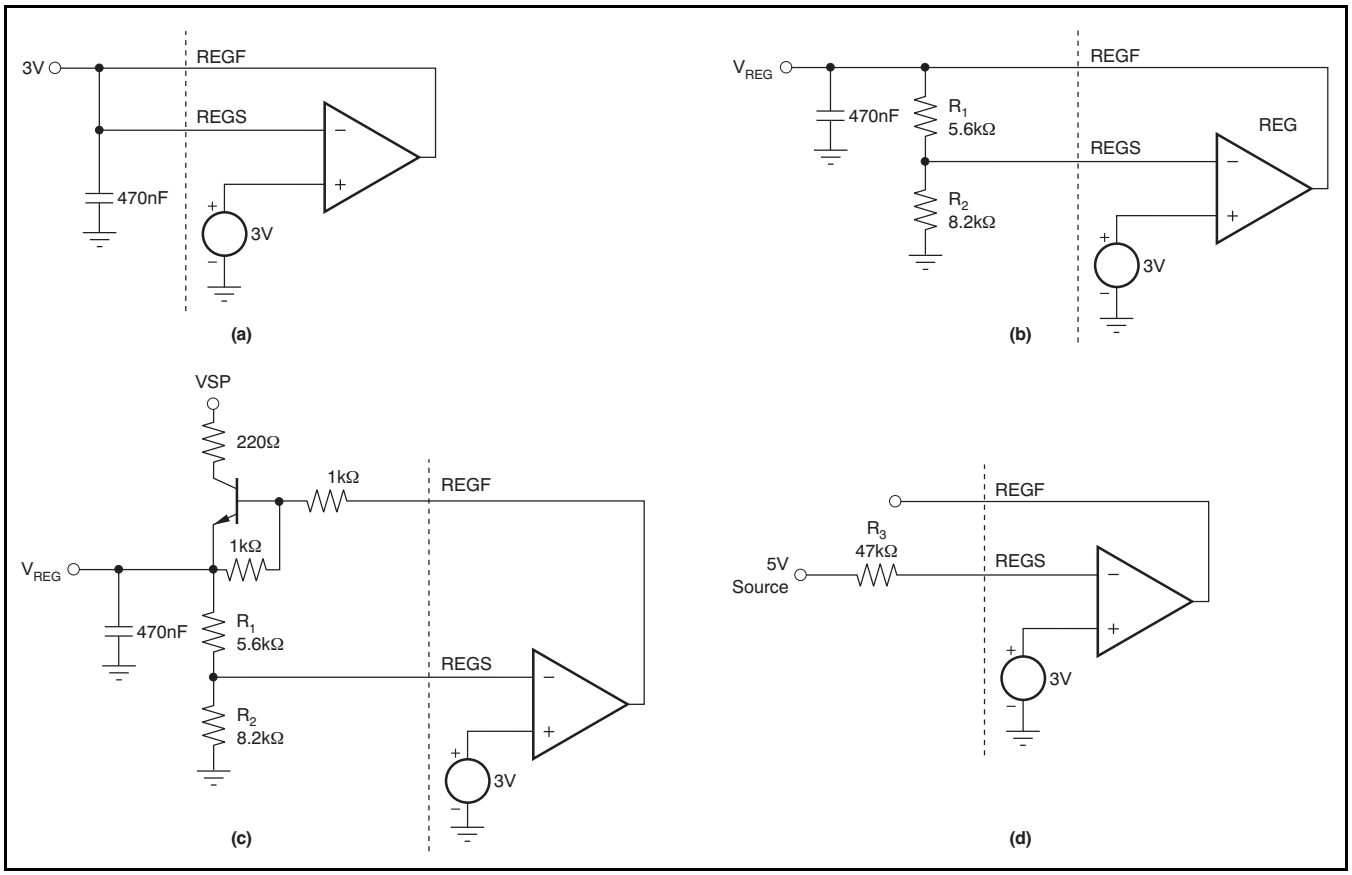


Figure 45. Basic Connections of the Voltage Regulator

Copyright © 2006–2011, Texas Instruments Incorporated

APPLICATION BLOCK DIAGRAMS

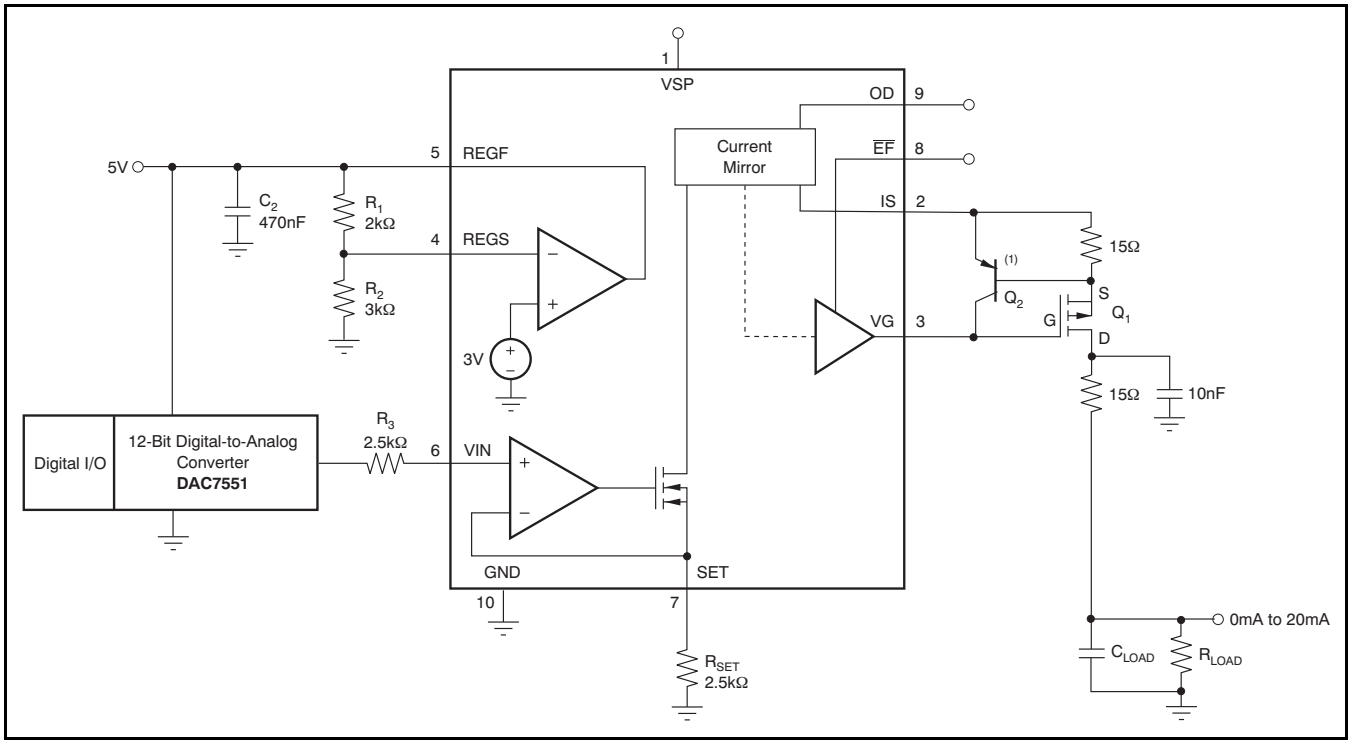


Figure 46. Current Using 0V to 5V Input from a 12-Bit Digital-to-Analog Converter DAC7551

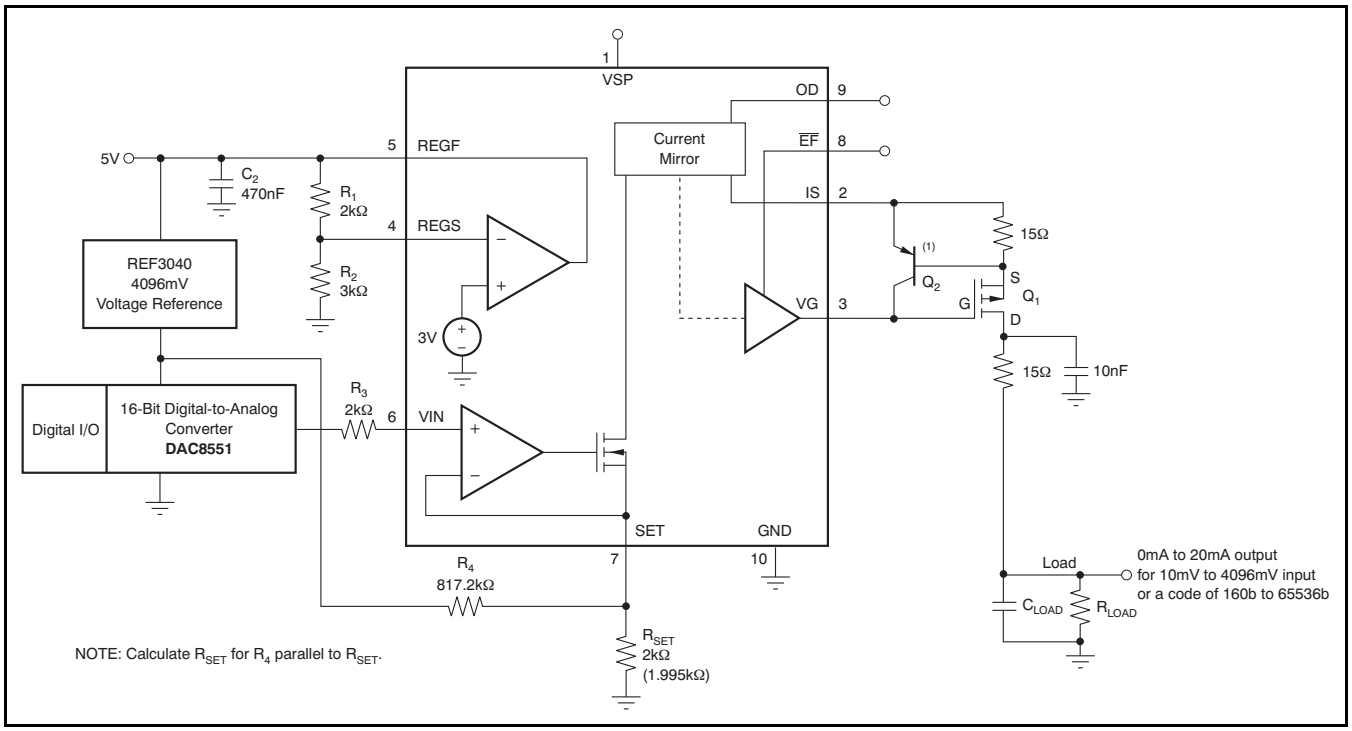


Figure 47. Precision Current Output with Signal from 16-Bit DAC. Input Offset Shifted (R4) by 10mV for Zero Adjustment Range

Copyright © 2006–2011, Texas Instruments Incorporated

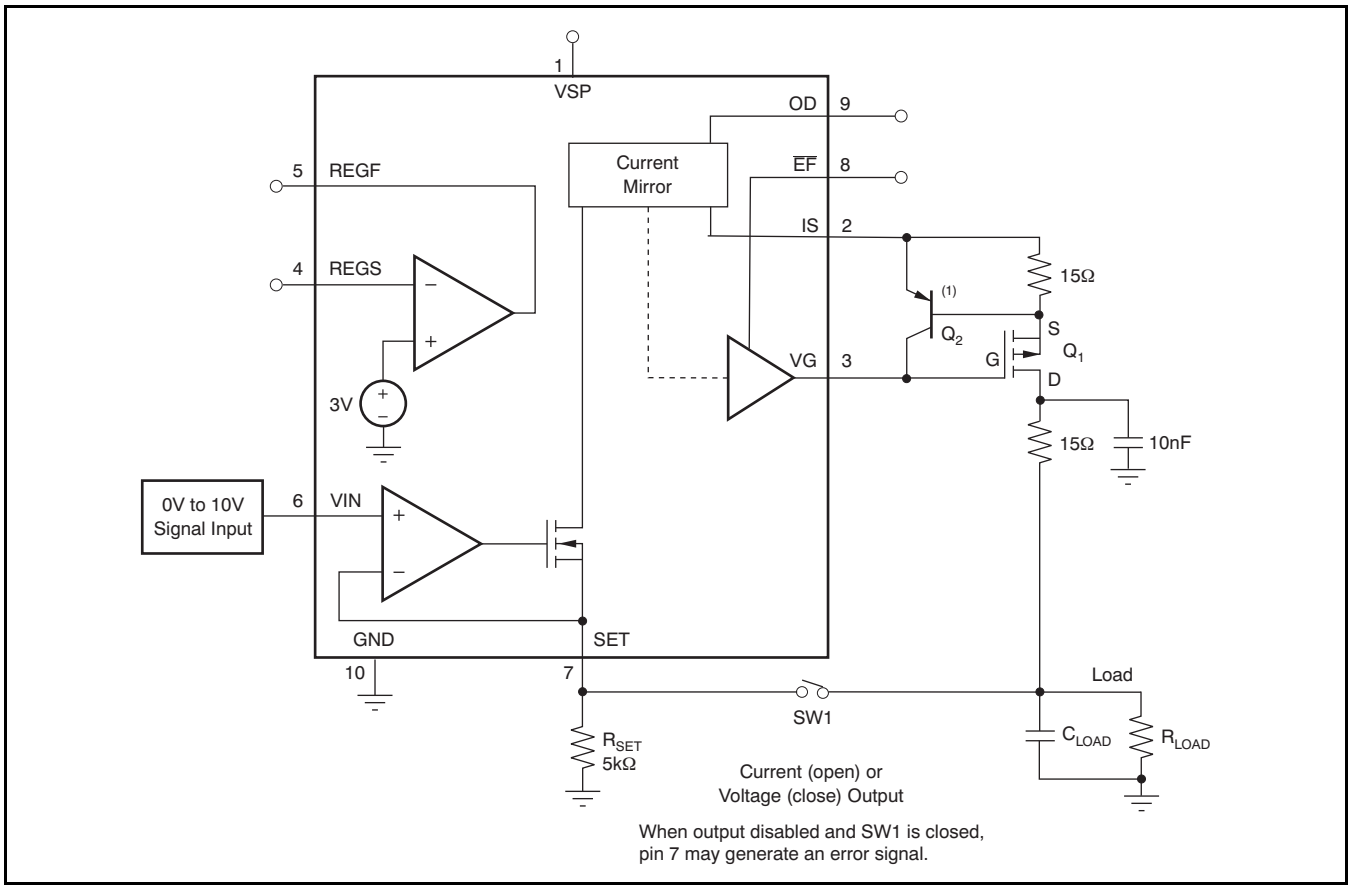


Figure 48. 0V to 10V or 0mA to 20mA Output Selected by Jumper (SW1)

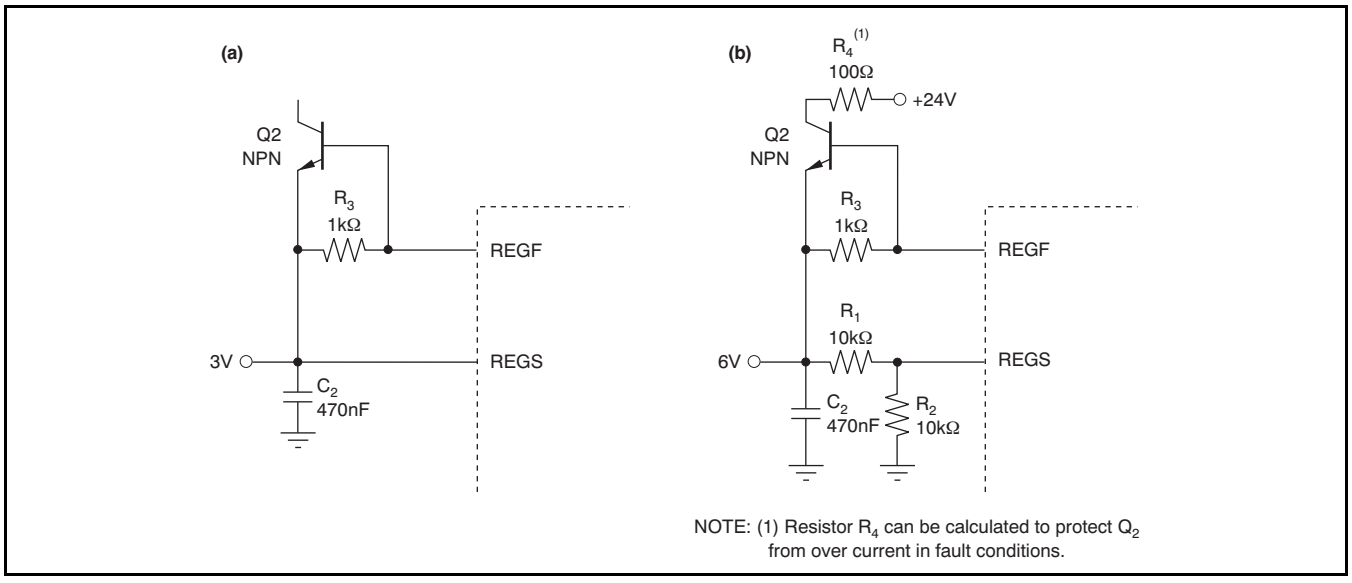


Figure 49. Voltage Regulator Current Boost Using a Standard NPN Transistor

Copyright © 2006–2011, Texas Instruments Incorporated

PACKAGE AND HEAT SINKING

The dominant portion of power dissipation for the current output is in the external FET.

The XTR111 only generates heat from the supply voltage with the quiescent current, the internal signal current that is 1/10 of the output current, and the current and internal voltage drop of the regulator.

The exposed thermal pad on the bottom of the XTR111 package allows excellent heat dissipation of the device into the printed circuit board (PCB).

THERMAL PAD

The thermal pad must be connected to the same voltage potential as the device GND pin.

Packages with an exposed thermal pad are specifically designed to provide excellent power dissipation, but board layout greatly influences overall heat dissipation. The thermal resistance from junction-to-ambient (T_{JA}) is specified for the packages with the exposed thermal pad soldered to a normalized PCB, as described in Technical Brief SLMA002, PowerPAD Thermally-Enhanced Package. See also EIA/JEDEC Specifications JESD51-0 to 7, QFN/SON PCB Attachment (SLUA271), and Quad Flatpack No-Lead Logic Packages (SCBA017). These documents are available for download at www.ti.com.

NOTE: All thermal models have an accuracy variation of 20%.

Component population, layout of traces, layers, and air flow strongly influence heat dissipation. Worst-case load conditions should be tested in the real environment to ensure proper thermal conditions. Minimize thermal stress for proper long-term operation with a junction temperature well below +125°C.

LAYOUT GUIDELINES

The leadframe die pad should be soldered to a thermal pad on the PCB. A mechanical data sheet showing an example layout is attached at the end of this data sheet. Refinements to this layout may be required based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June, 2010) to Revision C — **Page**

- Corrected wiring error in Figure 46 19

Changes from Revision A (August, 2007) to Revision B — **Page**

- Corrected errors in Figure 37 14

Copyright © 2006–2011, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTR111AIDGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CCM	Samples
XTR111AIDGQRG4	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CCM	Samples
XTR111AIDGQT	ACTIVE	HVSSOP	DGQ	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CCM	Samples
XTR111AIDGQTG4	ACTIVE	HVSSOP	DGQ	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CCM	Samples
XTR111AIDRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BSV	Samples
XTR111AIDRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BSV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

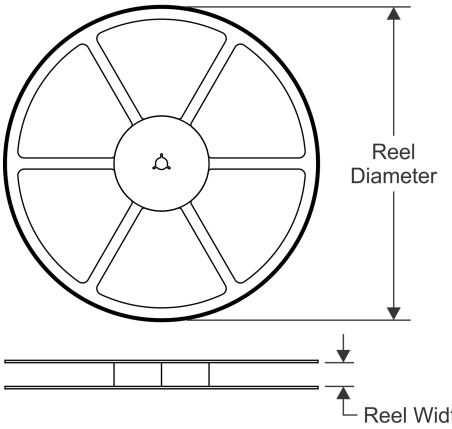
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

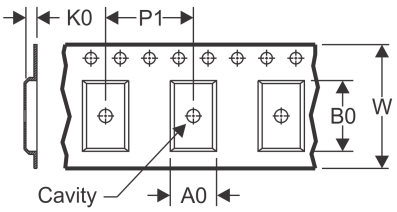
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

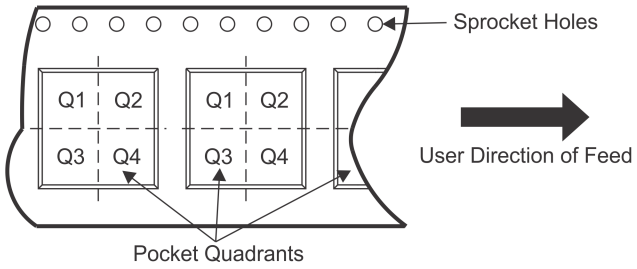


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

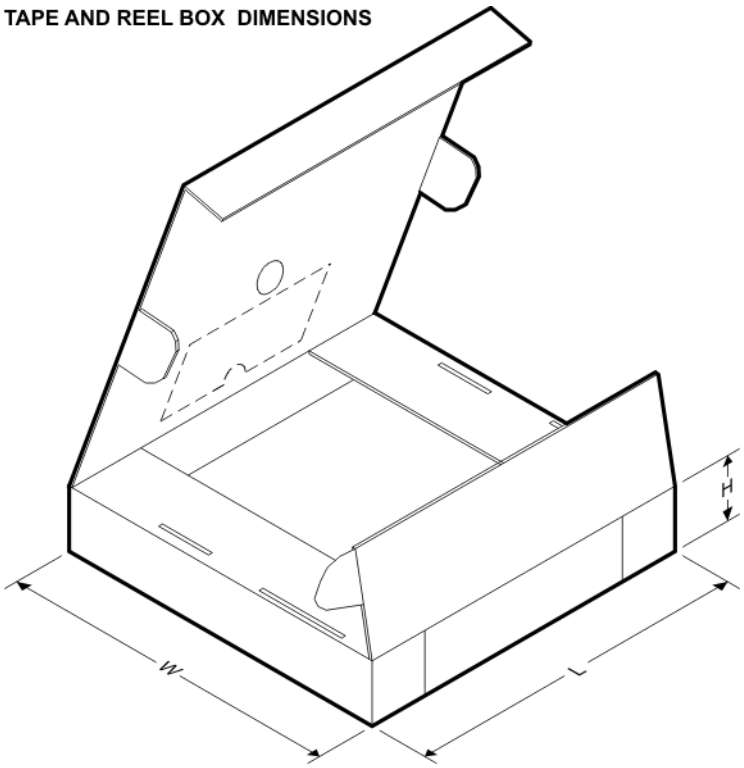
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR111AIDGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
XTR111AIDGQT	HVSSOP	DGQ	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
XTR111AIDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
XTR111AIDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR111AIDGQR	HVSSOP	DGQ	10	2500	367.0	367.0	38.0
XTR111AIDGQT	HVSSOP	DGQ	10	250	213.0	191.0	35.0
XTR111AIDRCR	VSON	DRC	10	3000	853.0	449.0	35.0
XTR111AIDRCT	VSON	DRC	10	250	210.0	185.0	35.0

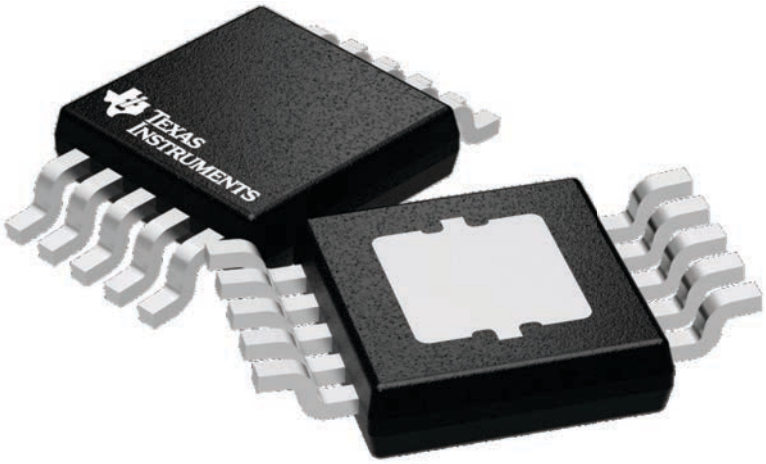
GENERIC PACKAGE VIEW

DGQ 10

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

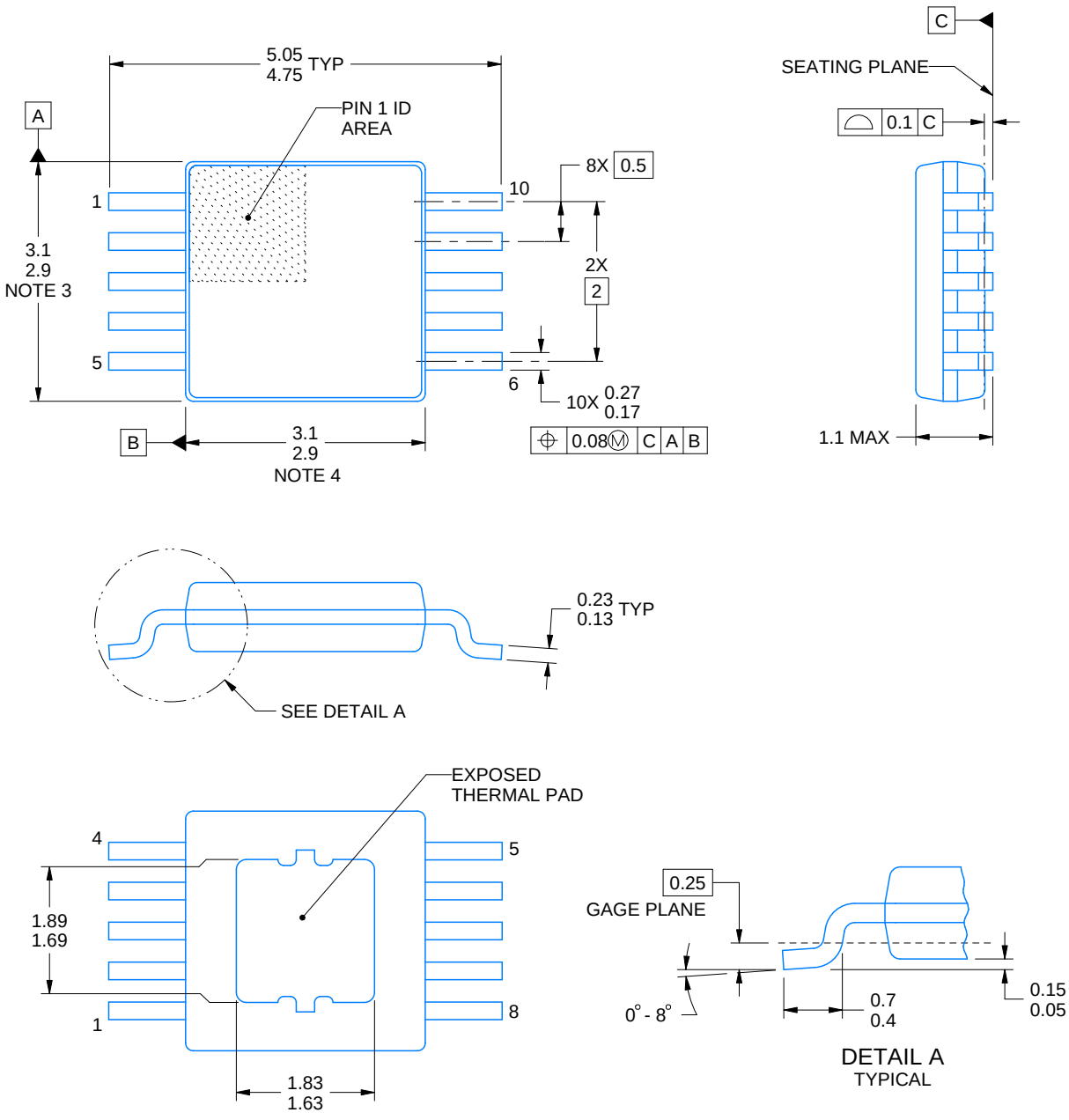
4224775/A

PACKAGE OUTLINE

DGQ0010D

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE

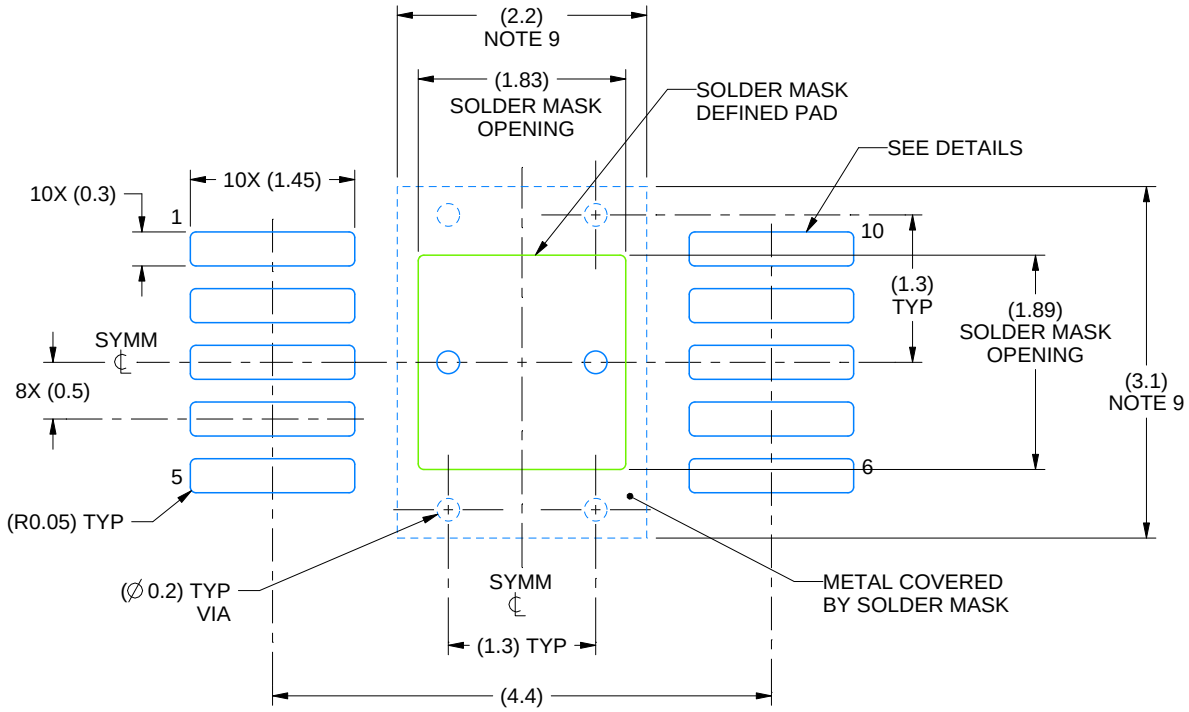


4218842/A 01/2019

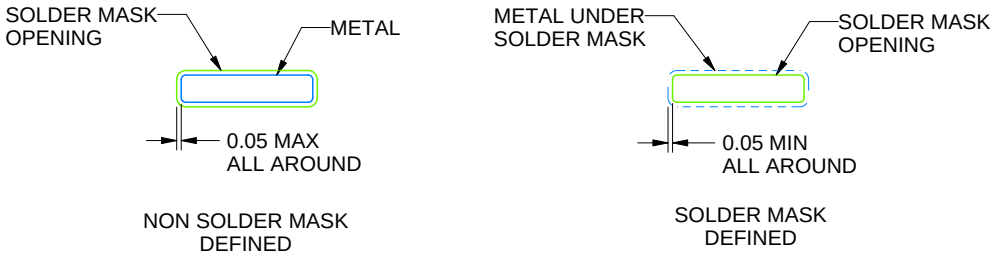
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE
SCALE:15X

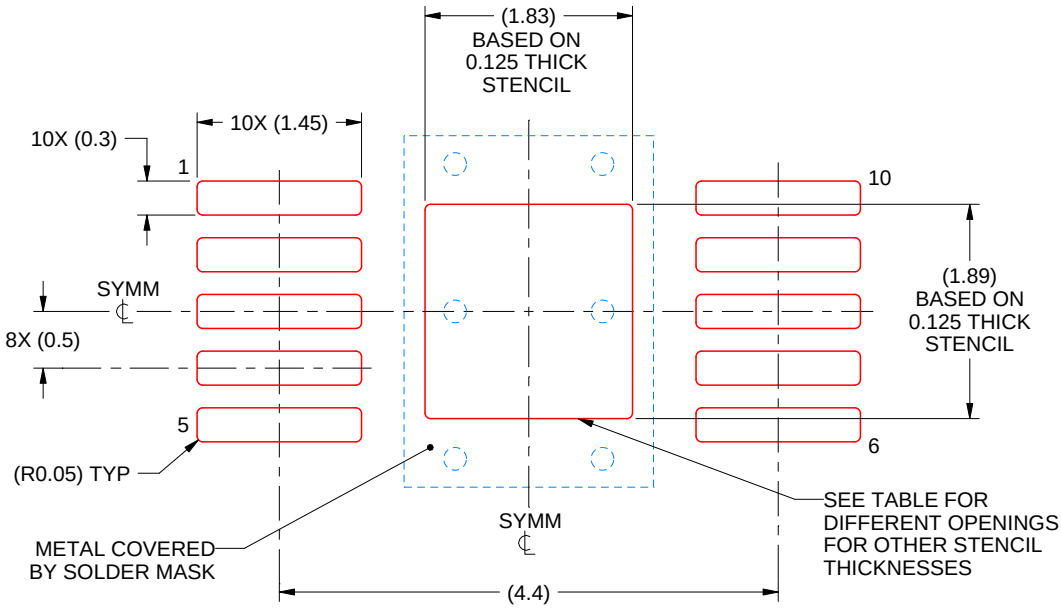


SOLDER MASK DETAILS

4218842/A 01/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.11
0.125	1.83 X 1.89 (SHOWN)
0.150	1.67 X 1.73
0.175	1.55 X 1.60

4218842/A 01/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

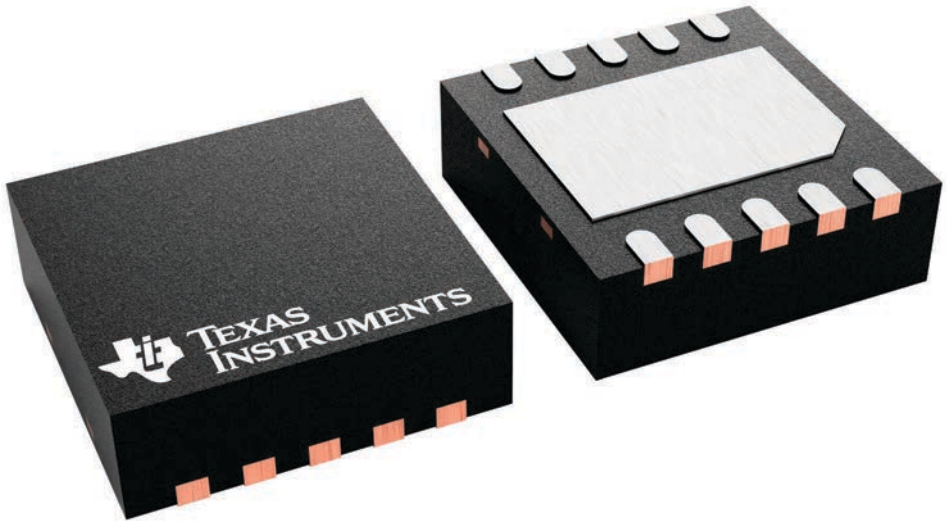
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



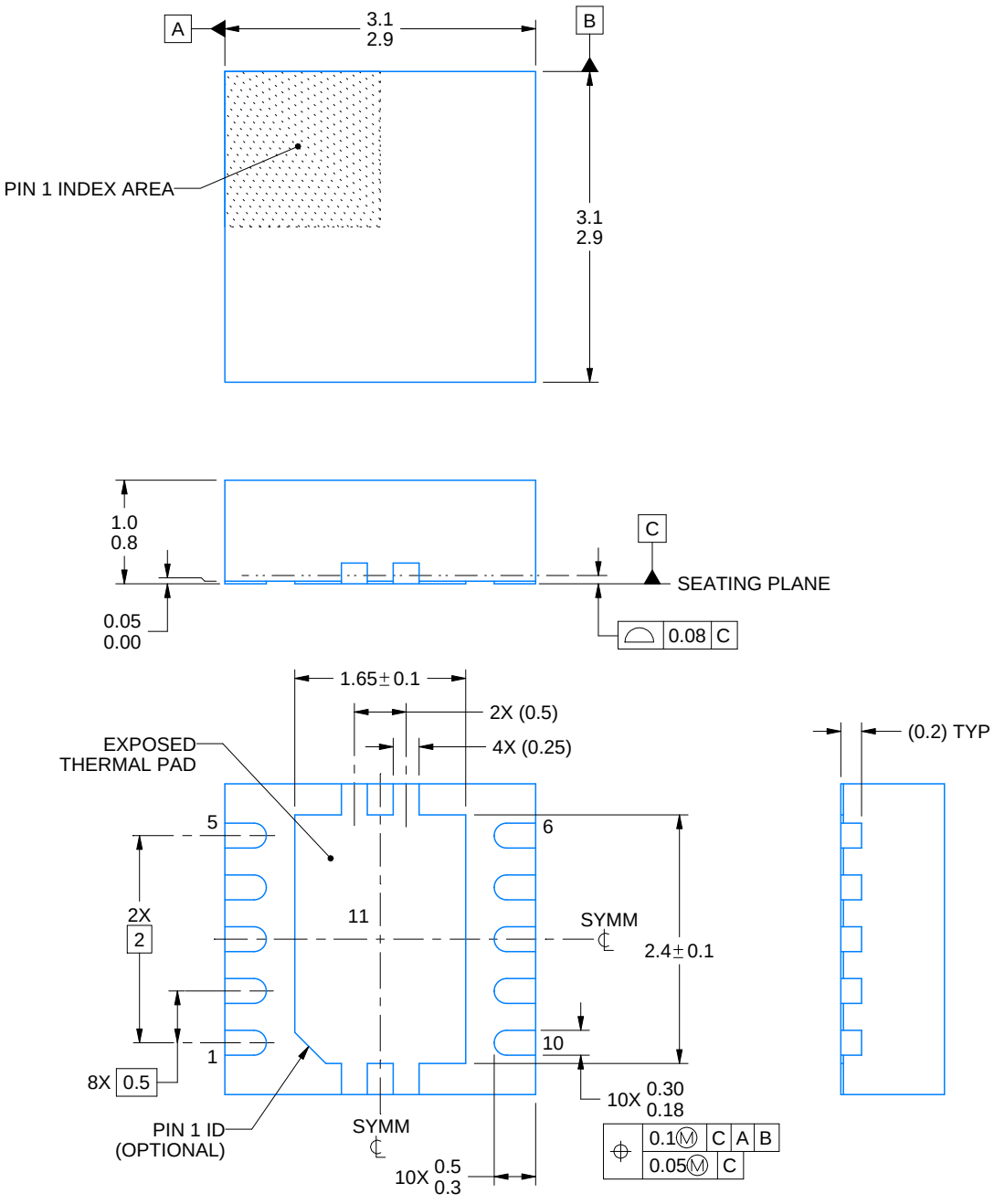
4226193/A

DRC0010J

PACKAGE OUTLINE

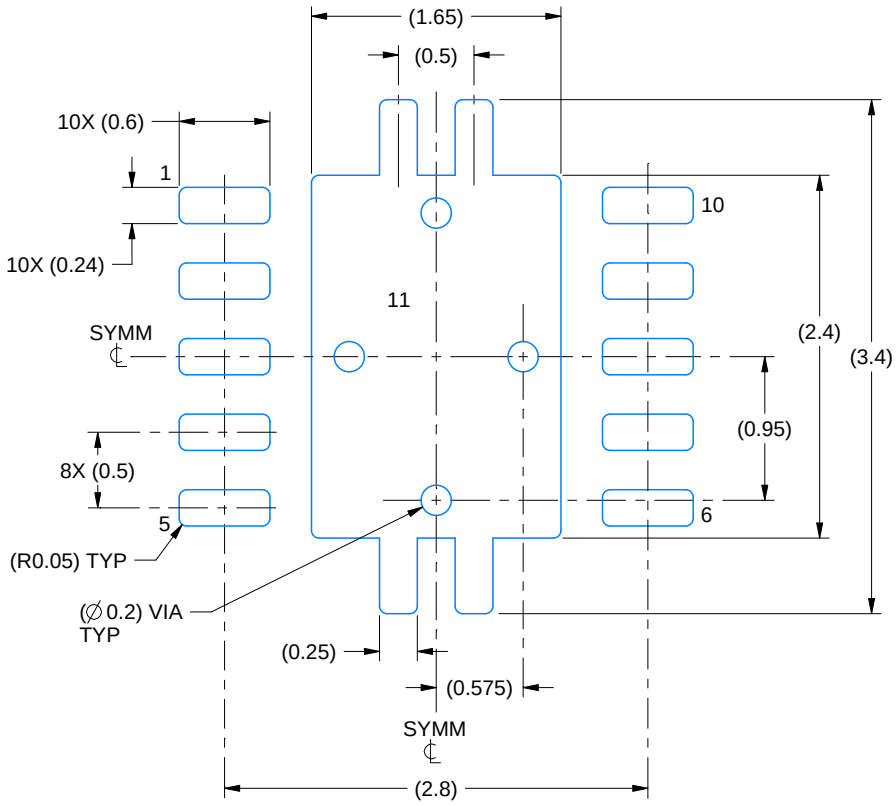
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

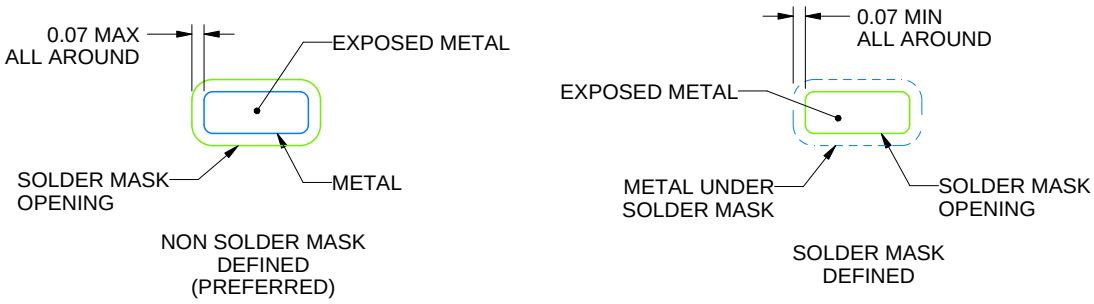


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

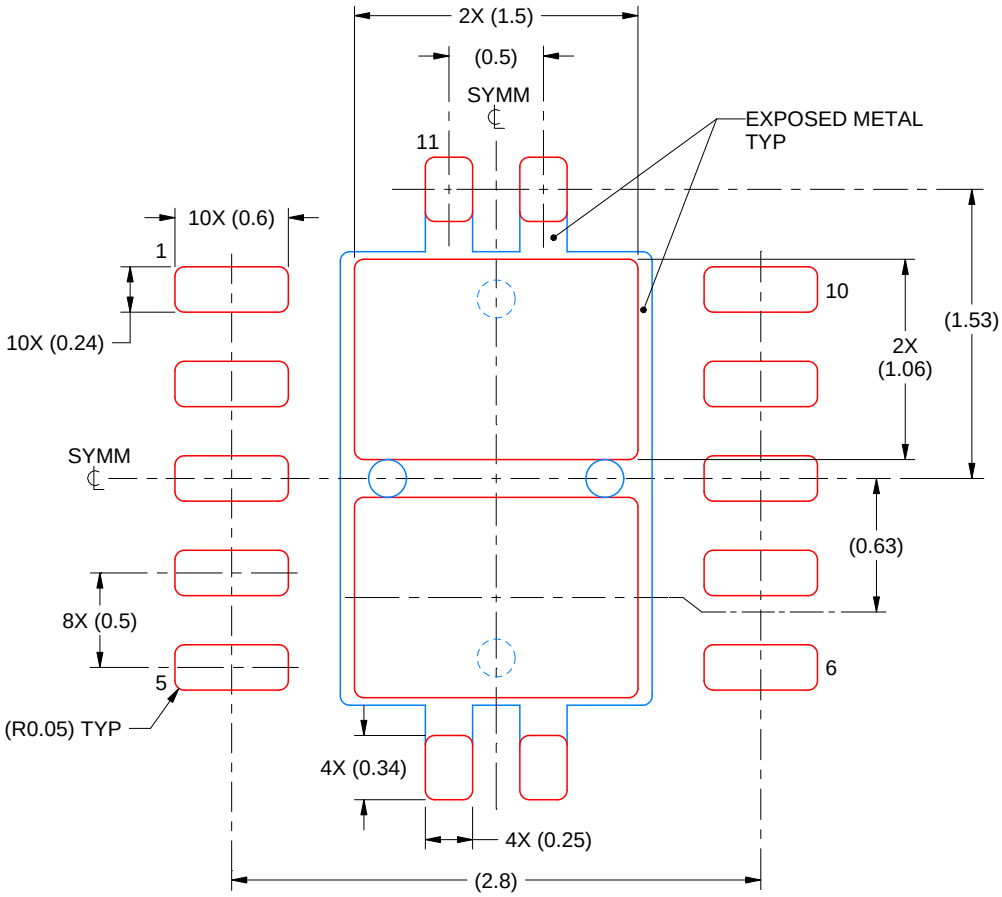
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated