TEXAS INSTRUMENTS

TPS62160, TPS62161, TPS62162, TPS62163

ZHCS504E – NOVEMBER 2011 – REVISED MAY 2017

具有 DCS-Control™ 的 TPS6216x 3V 至 17V 1A 降压转换器

1 特性

- DCS-Control™拓扑技术
- 输入电压范围为 3V 至 17V
- 输出电流高达 1A
- 可调节输出电压范围为 0.9V 至 6V
- 固定输出电压版本
- 无缝省电模式转换
- 静态电流典型值为 17μA
- 电源正常输出
- 100% 占空比模式
- 短路保护
- 过热保护
- 与 TPS62170 和 TPS62125 引脚兼容
- 采用 3.00mm x 3.00mm 8 引脚超薄小外形尺寸 (VSSOP) 和 2.00mm × 2.0 mm 8 引脚晶圆级小外形无引线 (WSON) 封装
- 结合使用 TPS62160 和 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 标准 12V 导轨式电源
- 单个或者多个锂离子电池供电的负载点 (POL) 电源
- 低压降稳压器 (LDO) 替代产品
- 嵌入式系统
- 数码相机、数码摄像机
- 移动电脑、平板电脑、调制解调器

3 说明

TPS6216x 系列是一款简单易用的同步降压 DC-DC 转换器，针对 高功率密度的应用 进行了优化。该系列器件的开关频率典型值高达 2.25MHz，允许使用小型电感器，通过利用 DCS-Control™ 拓扑技术提供快速瞬态响应并实现高精度的输出电压。

该器件的宽运行电压范围为 3V 至 17V，非常适用于由锂离子或其他电池以及 12V 中间电源轨供电的系统。该器件的输出电压为 0.9V 至 6V，支持高达 1A 的持续输出电流（使用 100% 占空比模式）。

此外，还可以通过配置使能引脚和开漏电源正常状态引脚实现电源排序。

在节能模式下，器件可根据输入电压 (VIN) 生成约 17μA 的静态电流。负载较小时可自动且无缝进入节能模式，同时该模式可保持整个负载范围内的高效率。该器件在关断模式下处于关断状态，期间的流耗低于 2μA。

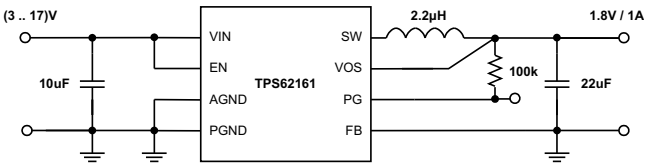
此器件具有可调节输出电压和固定输出电压版本，采用 2.00mm x 2.00mm 8 引脚 WSON 封装 (DSG) 或 3.00mm x 3.00mm 8 引脚 VSSOP 封装 (DGK)。

器件信息(1)

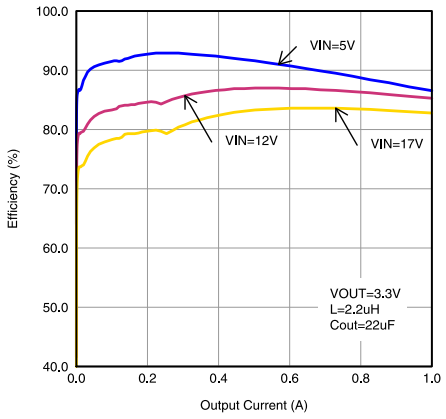
器件型号	封装	封装尺寸（标称值）
TPS6216x	WSON (8)	2.00mm x 2.00mm
TPS62160	VSSOP (8)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路原理图



效率与输出电流间的关系



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

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- Added "SW (AC), less than 10ns" specification to Absolute Maximum Ratings table ... 5
- Changed T_J MAX spec from "125" to "150" ... 5
- Added I_Q and I_{SD} specifications ... 6
- Added 125°C plot line in Figure 1 and Figure 4 Typical Characteristics graphic entities. ... 7

Changes from Revision C (September 2013) to Revision D — **Page**

- 已添加*器件信息表*，*ESD 额定值表*，*特性 说明* 部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分。 ... 1

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- Changed 50mV/μs to 50mV/s in *Enable / Shutdown (EN)* section ... 9

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- Added note to Terminal Functions ... 4
- Changed Equation 13 ... 25
- Added diode to Figure 41 ... 25

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- 已更改 数据表状态“混合状态”至“量产数据” ... 1
- 已添加 “VSSOP-8 封装”至 特性 ... 1
- 已添加 “8 引脚 VSSOP 封装”至 说明 ... 1

- Added DGK package pinout 4
- Added DGK package to Thermal Information 5
- Changed Table 2 14

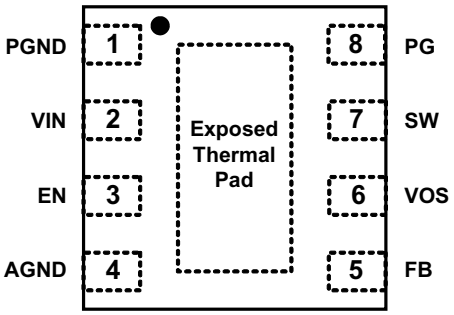
5 Device Voltage Options

OUTPUT VOLTAGE(1)	PART NUMBER	PACKAGE
adjustable	TPS62160	WSON (8)
1.8 V	TPS62161	
3.3 V	TPS62162	
5.0 V	TPS62163	
adjustable	TPS62160	VSSOP (8)

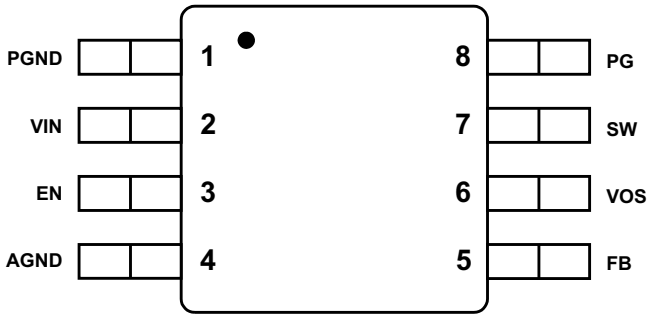
(1) Contact the factory to check availability of other fixed output voltage versions.

6 Pin Configuration and Functions

DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View



DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN(1)		I/O	DESCRIPTION
NAME	NO.		
PGND	1	—	Power ground
VIN	2	I	Supply voltage
EN	3	I	Enable input (High = enabled, Low = disabled)
AGND	4	—	Analog ground
FB	5	I	Voltage feedback of adjustable version. Connect resistive voltage divider to this pin. It is recommended to connect FB to AGND on fixed output voltage versions for improved thermal performance.
VOS	6	I	Output voltage sense pin and connection for the control loop circuitry.
SW	7	O	Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.
PG	8	O	Output power good (High = VOUT ready, Low = VOUT below nominal regulation); open drain (requires pull-up resistor; goes high impedance, when device is switched off)
Exposed Thermal Pad(2)		—	Must be connected to AGND. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see *Detailed Description* and *Application Information* sections.
(2) The exposed thermal pad is available with the DSG package only, not with DGK package.

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Pin voltage range(2)	VIN	–0.3	20	V
	EN, SW (DC)	–0.3	V_{IN} + 0.3	V
	SW (AC), less than 10ns(3)	–2	24.5	
	FB, PG, VOS	–0.3	7	V
Power good sink current	PG		10	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) While switching.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply Voltage, V_{IN}	3		17	V
Output Voltage, V_{OUT}	0.9		6	V
Operating junction temperature, T_J	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6216X		UNIT
		DSG (WSON)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.8	184.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.3	74.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.5	105.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	13.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.4	104.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.6	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Over junction temperature range (T_J = –40°C to +125°C), typical values at V_{IN} = 12 V and T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range(1)			3		17	V
I_Q	Operating quiescent current	EN = High, I_{OUT} = 0 mA, device not switching			17	30	µA
			T_J = -40°C to +85°C		17	25	
I_{SD}	Shutdown current(2)	EN = Low			1.5	25	µA
			T_J = -40°C to +85°C		1.5	4	
V_{UVLO}	Undervoltage lockout threshold	Falling input voltage		2.6	2.7	2.82	V
		Hysteresis			180		mV
T_{SD}	Thermal shutdown temperature	Rising temperature			160		°C
	Thermal shutdown hysteresis	Falling temperature			20		
CONTROL (EN, PG)							
V_{EN_H}	High level input threshold voltage (EN)			0.9	0.6		V
V_{EN_L}	Low level input threshold voltage (EN)				0.56	0.3	V
I_{LKG_EN}	Input leakage current (EN)	EN = V_{IN} or GND			0.01	1	µA
V_{TH_PG}	Power good threshold voltage	Rising (%V_{OUT})		92%	95%	98%	
		Falling (%V_{OUT})		87%	90%	93%	
V_{OL_PG}	Power good output low voltage	I_{PG} = –2 mA			0.07	0.3	V
I_{LKG_PG}	Input leakage current (PG)	V_{PG} = 1.8 V			1	400	nA
POWER SWITCH							
$R_{DS(ON)}$	High-side MOSFET ON-resistance	V_{IN} ≥ 6 V			300	600	mΩ
		V_{IN} = 3 V			430		
	Low-side MOSFET ON-resistance	V_{IN} ≥ 6 V			120	200	mΩ
		V_{IN} = 3 V			165		
I_{LIMF}	High-side MOSFET forward current limit(3)	V_{IN} = 12 V, T_J = 25°C		1.45	1.95	2.45	A
OUTPUT							
V_{REF}	Internal reference voltage(4)				0.8		V
I_{LKG_FB}	Pin leakage current (FB)	TPS62160, V_{FB} = 1.2 V			5	400	nA
V_{OUT}	Output voltage range (TPS62160)	V_{IN} ≥ V_{OUT}		0.9		6.0	V
	Initial output voltage accuracy(5)	PWM mode operation, V_{IN} ≥ V_{OUT} + 1 V		–3%		3%	
		Power save mode operation, C_{OUT} = 22 µF		–3.5%		4%	
	DC output voltage load regulation(6)	V_{IN} = 12 V, V_{OUT} = 3.3 V, PWM mode operation			0.05		%/A
	DC output voltage line regulation (6)	3 V ≤ V_{IN} ≤ 17 V, V_{OUT} = 3.3 V, I_{OUT} = 0.5 A, PWM mode operation			0.02		%/V

(1) The device is still functional down to under voltage lockout (see parameter V_{UVLO}).
(2) Current into VIN pin.
(3) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see *Current Limit and Short Circuit Protection* section).
(4) This is the voltage regulated at the FB pin.
(5) This is the accuracy provided by the device itself (line and load regulation effects are not included). For fixed voltage versions, the (internal) resistive feedback divider is included.
(6) Line and load regulation are depending on external component selection and layout (see Figure 18 and Figure 19).

7.6 Typical Characteristics

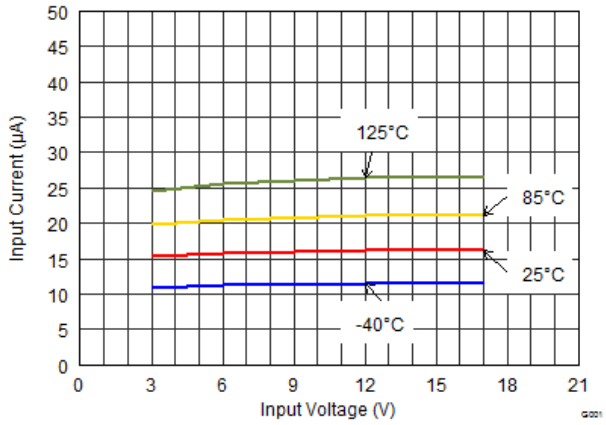


Figure 1. Quiescent Current

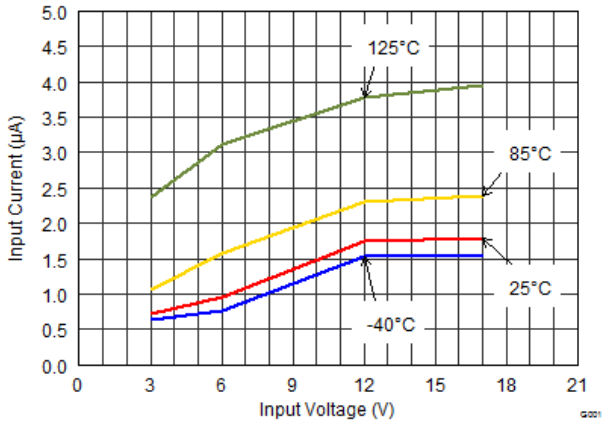


Figure 2. Shutdown Current

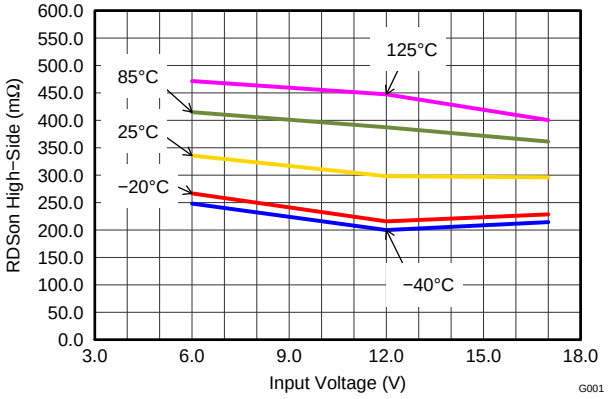


Figure 3. High-Side Switch

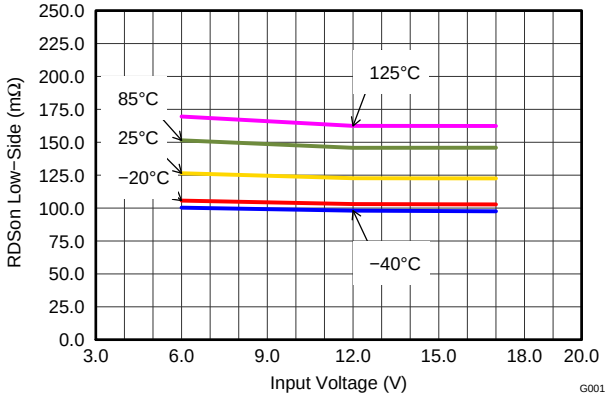


Figure 4. Low-Side Switch

8 Detailed Description

8.1 Overview

The TPS6216x synchronous step-down DC/DC converters are based on DCS-Control™ (**D**irect **C**ontrol with **S**eamless transition into power save mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports pulse width modulation (PWM) mode for medium and heavy load conditions and a power save mode at light loads. During PWM mode, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.25 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters power save mode to sustain high efficiency down to very light loads. In power save mode, the switching frequency decreases linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to power save mode is seamless without effects on the output voltage.

Fixed output voltage versions provide smallest solution size and lowest current consumption, requiring only 3 external components. An internal current limit supports nominal output currents of up to 1 A.

The TPS6216x family offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

8.2 Functional Block Diagrams

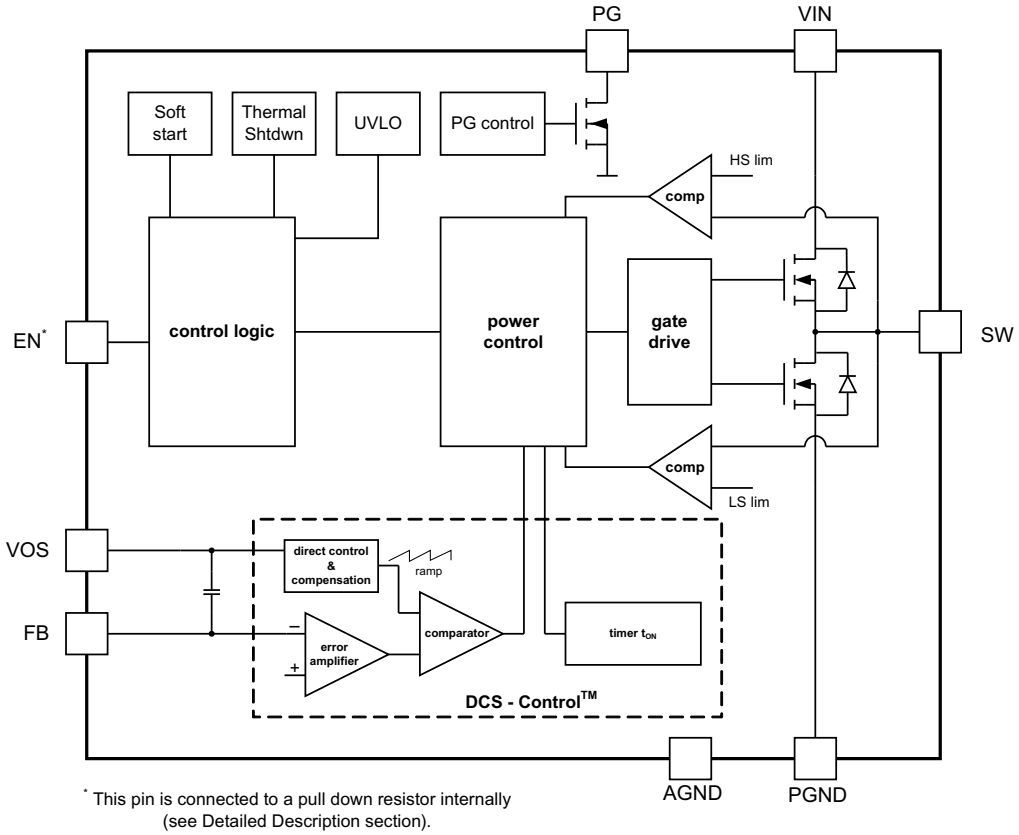


Figure 5. TPS62160 (Adjustable Output Voltage)

Functional Block Diagrams (continued)

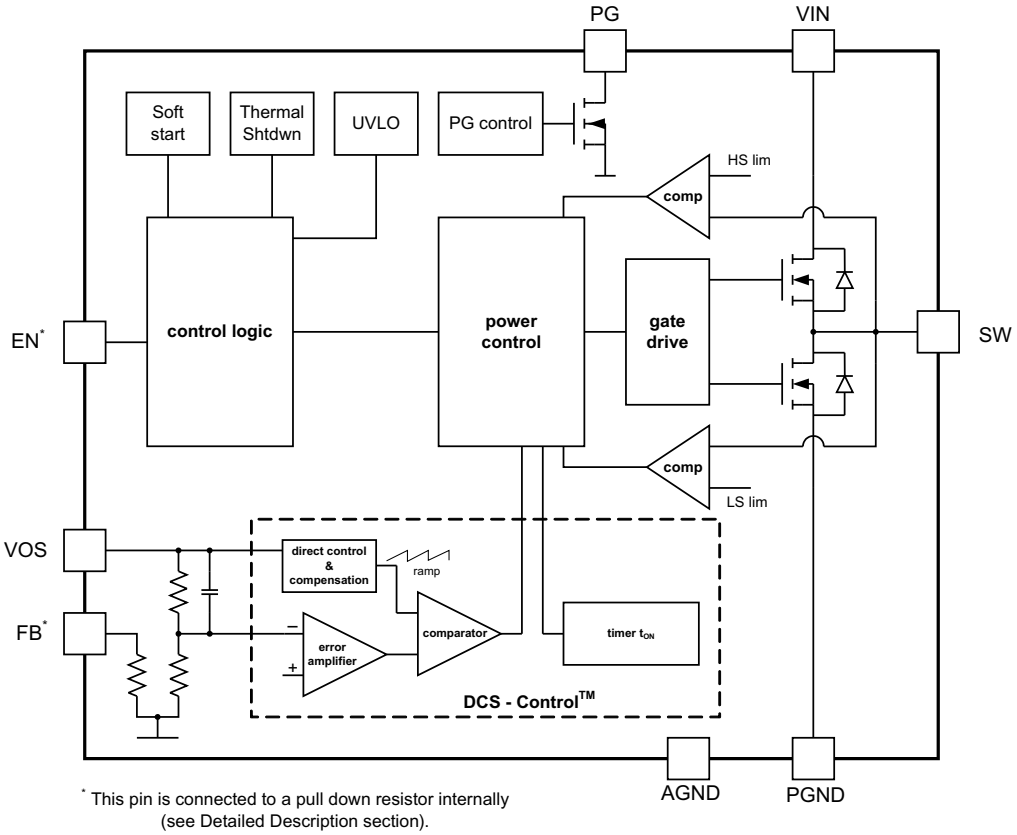


Figure 6. TPS62161/TPS62162/TPS62163 (Fixed Output Voltage)

8.3 Feature Description

8.3.1 Enable and Shutdown (EN)

When enable (EN) is set high, the device starts operation.

Shutdown is forced if EN is pulled low with a shutdown current of typically 1.5 µA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. If the EN pin is low, an internal pull-down resistor of about 400 kΩ is connected and keeps it low, to avoid bouncing.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

8.3.2 Current Limit and Short Circuit Protection

The TPS6216x devices are protected against heavy load and short circuit events. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET is turned off. Avoiding shoot through current, the low-side FET is switched on to allow the inductor current to decrease. The high-side FET turns on again, only if the current in the low-side FET decreases below the low-side current limit threshold of typically 1.2 A.

The output current of the device is limited by the current limit (see *Electrical Characteristics*). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit is calculated as follows:

Feature Description (continued)

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD}$$

where

- I_{LIMF} is the static current limit, specified in *Electrical Characteristics*
- L is the inductor value
- V_L is the voltage across the inductor
- t_{PD} is the internal propagation delay (1)

The dynamic high-side switch peak current is calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{(V_{IN} - V_{OUT})}{L} \cdot 30ns \quad (2)$$

Take care with the current limit, if the input voltage is high and very small inductances are used.

8.3.3 Power Good (PG)

The TPS6216x has a built in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor (to any voltage below 7 V). It can sink 2 mA of current and maintain its specified logic low level. It is high impedance when the device is turned off due to EN, UVLO or thermal shutdown. If not used, the PG pin should be connected to GND but may be left floating.

Table 1. Power Good Pin Logic Table

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	$V_{FB} \geq V_{TH\_PG}$	√	
	$V_{FB} \leq V_{TH\_PG}$		√
Shutdown (EN=Low)		√	
UVLO	$0.7\ V < V_{IN} < V_{UVLO}$	√	
Thermal Shutdown	$T_J > T_{SD}$	√	
Power Supply Removal	$V_{IN} < 0.7\ V$	√	

8.3.4 Undervoltage Lockout (UVLO)

If the input voltage drops, the under voltage lockout prevents misoperation of the device by switching off both the power FETs. The under voltage lockout threshold is set typically to 2.7 V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 180 mV.

8.3.5 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 160°C (typical), the device goes into thermal shut down. Both the high-side and low-side power FETs are turned off and PG goes high impedance. When T_J decreases below the hysteresis amount, the converter resumes normal operation, beginning with soft start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shut down temperature.

8.4 Device Functional Modes

8.4.1 Soft Start

The internal soft start circuitry controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50 µs and V_{OUT} rises with a slope of about 25 mV/µs. See Figure 30 and Figure 31 for typical startup operation.

The TPS6216x can start into a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to turn on until the device's internal ramp sets an output voltage above the pre-bias voltage.

8.4.2 Pulse Width Modulation (PWM) Operation

The TPS6216x operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of about 2.25 MHz. The frequency variation in PWM is controlled and depends on V_{IN}, V_{OUT} and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters power save mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor's ripple current.

8.4.3 Power Save Mode Operation

The TPS6216x's built in power save mode is entered seamlessly, if the load current decreases. This secures a high efficiency in light load operation. The device remains in power save mode as long as the inductor current is discontinuous.

In power save mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of power save mode happens within the entire regulation scheme and is seamless in both directions.

The TPS6216x includes a fixed on-time circuitry. This on-time, in steady-state operation, is estimated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 420ns \tag{3}$$

For very small output voltages, the on-time increases beyond the result of Equation 3, to stay above an absolute minimum on-time, $t_{ON(min)}$, which is around 80 ns, to limit switching losses. The peak inductor current in PSM is approximated by:

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \cdot t_{ON} \tag{4}$$

When V_{IN} decreases to typically 15% above V_{OUT}, the TPS6216x does not enter power save mode, regardless of the load current. The device maintains output regulation in PWM mode.

8.4.4 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by $D = V_{OUT}/V_{IN}$ and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal setpoint. This allows the conversion of small input to output voltage differences, such as for longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, is calculated as:

Device Functional Modes (continued)

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left(R_{DS(on)} + R_L\right) \quad (5)$$

where

- I_{OUT} is the output current
- $R_{DS(on)}$ is the $R_{DS(on)}$ of the high-side FET
- R_L is the DC resistance of the inductor used

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6216x device family are easy to use synchronous step-down DC/DC converters optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response as well as high output voltage accuracy by utilization of the DCS-Control™ topology. With its wide operating input voltage range of 3 V to 17 V, the devices are ideally suited for systems powered from either a Li-Ion or other battery as well as from 12-V intermediate power rails. It supports up to 1-A continuous output current at output voltages between 0.9 V and 6 V (with 100% duty cycle mode).

9.2 Typical Application

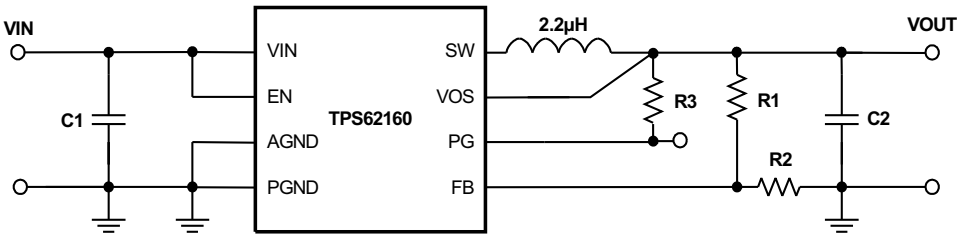


Figure 7. TPS62160 Adjustable Power Supply

9.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the *Recommended Operating Conditions*.

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS62160 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

Typical Application (continued)

9.2.2.2 Programming the Output Voltage

While the output voltage of the TPS62160 is adjustable, the TPS62161/TPS62162/TPS62163 are programmed to fixed output voltages. For fixed output versions, the FB pin is pulled down internally and may be left floating. It is recommended to connect it to AGND to improve thermal resistance. The adjustable version can be programmed for output voltages from 0.9 V to 6 V by using a resistive divider from VOUT to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from Equation 6. It is recommended to choose resistor values which allow a current of at least 2 µA, meaning the value of R2 should not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design. For applications requiring lowest current consumption, the use of fixed output voltage versions is recommended.

$$R_1 = R_2\left(\frac{V_{OUT}}{0.8V} - 1\right) \quad (6)$$

If the FB pin becomes open, the device clamps the output voltage at the VOS pin to about 7.4 V.

9.2.2.3 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS6216x is optimized to work within a range of external components. The LC output filter's inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter (see *Output Filter and Loop Stability* section). Table 2 can be used to simplify the output filter component selection. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

Table 2. Recommended LC Output Filter Combinations(1)

	4.7µF	10µF	22µF	47µF	100µF	200µF	400µF
1µH							
2.2µH		√	√(2)	√	√	√	
3.3µH		√	√	√	√		
4.7µH							

(1) The values in the table are nominal values. Variations of typically ±20% due to tolerance, saturation and DC bias are assumed.
(2) This LC combination is the standard value and recommended for most applications.

More detailed information on further LC combinations can be found in SLVA463.

9.2.2.4 Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions.

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \quad (7)$$

$$\Delta I_{L(\max)} = V_{OUT} \cdot \left(\frac{1 - \frac{V_{OUT}}{V_{IN(\max)}}}{L_{(\min)} \cdot f_{SW}} \right)$$

where

- I_L(max) is the maximum inductor current
- ΔI_L is the peak-to-peak inductor ripple current
- L(min) is the minimum effective inductor value
- f_{SW} is the actual PWM switching frequency

(8)

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS6216x and are recommended for use:

Table 3. List of Inductors(1)

Type	Inductance [µH]	Current [A](2)	Dimensions [L x B x H] mm	Manufacturer
VLF3012ST-2R2M1R4	2.2 µH, ±20%	1.9 A	3.0 x 2.8 x 1.2	TDK
VLF302512MT-2R2M	2.2 µH, ±20%	1.9 A	3.0 x 2.5 x 1.2	TDK
VLS252012T-2R2M1R3	2.2 uH, ±20%	1.3 A	2.5 x 2.0 x 1.2	TDK
XFL3012-222MEC	2.2 µH, ±20%	1.9 A	3.0 x 3.0 x 1.2	Coilcraft
XFL3012-332MEC	3.3 µH, ±20%	1.6 A	3.0 x 3.0 x 1.2	Coilcraft
LPS3015-332ML_	3.3 uH, ±20%	1.4 A	3.0 x 3.0 x 1.4	Coilcraft
NR3015T-2R2M	2.2 uH, ±20%	1.5 A	3.0 x 3.0 x 1.5	Taiyo Yuden
744025003	3.3 uH, ±20%	1.5 A	2.8 x 2.8 x 2.8	Wuerth
PSI25201B-2R2MS	2.2 uH, ±20%	1.3 A	2.0 x 2.5 x 1.2	Cyntec

(1) See the *Third-Party Products Disclaimer*.
(2) I_{RMS} at 40°C rise or I_{SAT} at 30% drop.

The TPS6216x can operate with an inductor as low as 2.2 µH. However, for applications with low input voltages, 3.3 µH is recommended to allow the full output current. The inductor value also determines the load current at which Power Save Mode is entered:

$$I_{load(PSM)} = \frac{1}{2} \Delta I_L$$

(9)

Using Equation 8, this current level is adjusted by changing the inductor value.

9.2.2.5 Capacitor Selection

9.2.2.5.1 Output Capacitor

The recommended value for the output capacitor is 22 uF. The architecture of the TPS6216x allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use an X7R or X5R dielectric. Using a higher value can have some advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode (see SLVA463).

Note: In power save mode, the output voltage ripple depends on the output capacitance, its ESR and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

9.2.2.5.2 Input Capacitor

For most applications, 10 µF is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between VIN and PGND as close as possible to those pins.

NOTE

DC bias effect: High capacitance ceramic capacitors have a DC bias effect, which has a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

9.2.2.6 Output Filter and Loop Stability

The devices of the TPS6216x family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency calculated with Equation 10:

$$f_{LC} = \frac{1}{2\pi \sqrt{L \cdot C}} \tag{10}$$

Proven nominal values for inductance and ceramic capacitance are given in Table 2 and are recommended for use. Different values may work, but care has to be taken on the loop stability which is affected. More information including a detailed L-C stability matrix is found in SLVA463.

The TPS6216X devices, both fixed and adjustable versions, include an internal 25 pF feed forward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per Equation 11 and Equation 12:

$$f_{zero} = \frac{1}{2\pi \cdot R_1 \cdot 25pF} \tag{11}$$

$$f_{pole} = \frac{1}{2\pi \cdot 25pF} \cdot \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \tag{12}$$

Though the TPS6216x devices are stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in power save mode and/or improved transient response. An external feed-forward capacitor can also be added. A more detailed discussion on the optimization for stability versus transient response can be found in SLVA289 and SLVA466.

If using ceramic capacitors, the DC bias effect has to be considered. The DC bias effect results in a drop in effective capacitance as the voltage across the capacitor increases (see **NOTE** in *Input Capacitor* section).

9.2.2.7 TPS6216x Components List

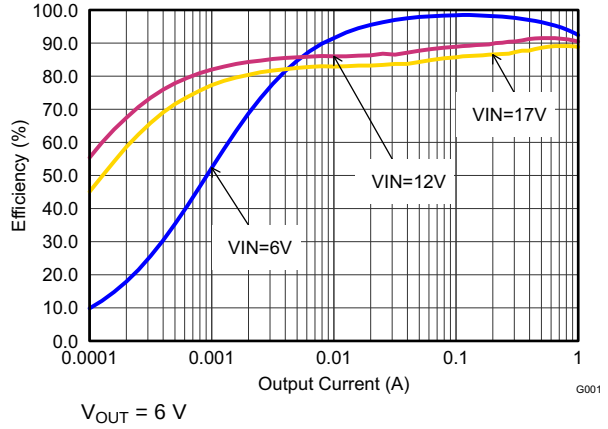
Table 4 shows the list of components for the *Application Curves*.

Table 4. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
IC	17 V, 1 A Step-Down Converter, WSON	TPS62160DSG, Texas Instruments
L1	2.2 µH, 1.4 A, 3 mm x 2.8 mm x 1.2 mm	VLF3012ST-2R2M1R4, TDK
C1	10 µF, 25 V, Ceramic, 0805	Standard
C2	22 µF, 6.3 V, Ceramic, 0805	Standard
R1	depending on V_{OUT}	
R2	depending on V_{OUT}	
R3	100 kΩ, Chip, 0603, 1/16 W, 1%	Standard

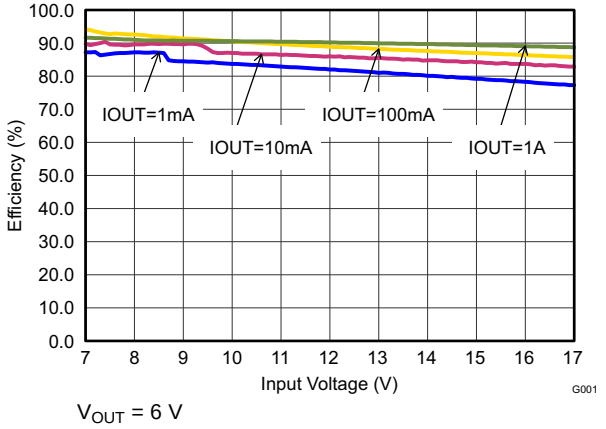
9.2.3 Application Curves

V_{IN}=12 V, V_{OUT}=3.3 V, T_A=25°C, (unless otherwise noted)



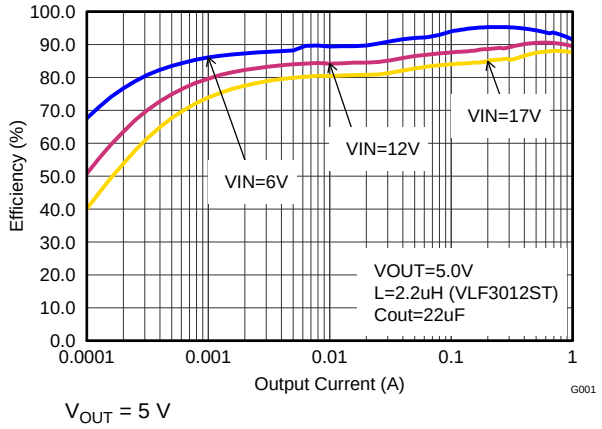
V_{OUT} = 6 V

Figure 8. Efficiency vs Output Current



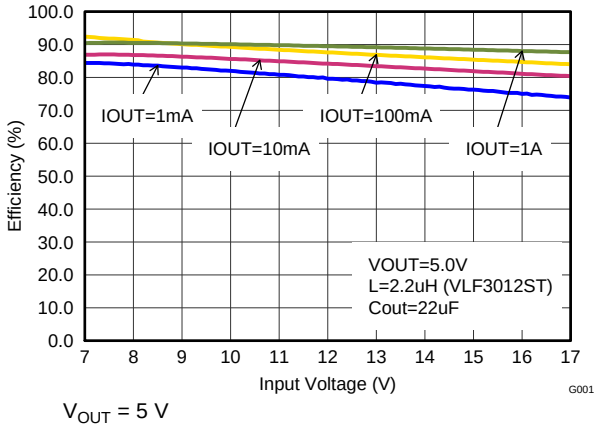
V_{OUT} = 6 V

Figure 9. Efficiency vs Input Voltage



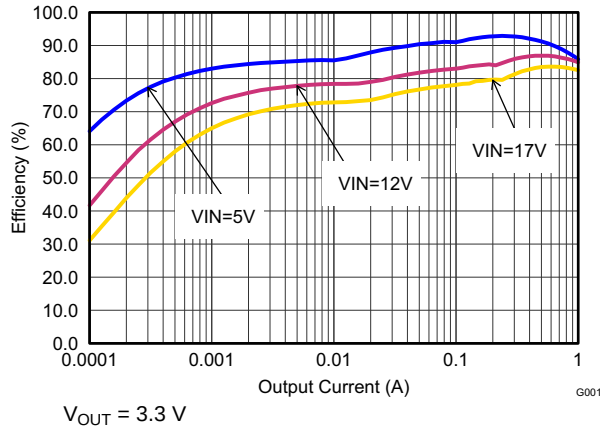
V_{OUT} = 5 V

Figure 10. Efficiency vs Output Current



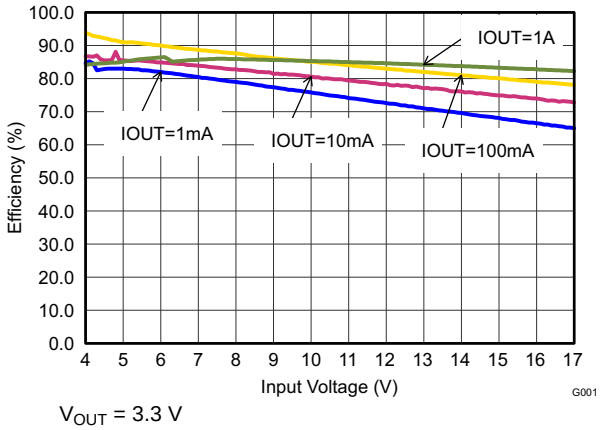
V_{OUT} = 5 V

Figure 11. Efficiency vs Input Voltage



V_{OUT} = 3.3 V

Figure 12. Efficiency vs Output Current



V_{OUT} = 3.3 V

Figure 13. Efficiency vs Input Voltage

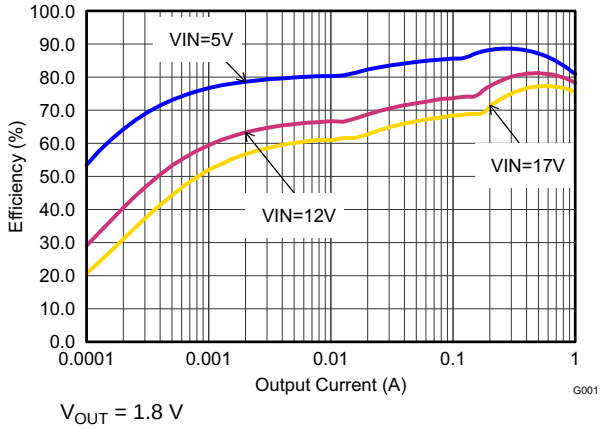


Figure 14. Efficiency vs Output Current

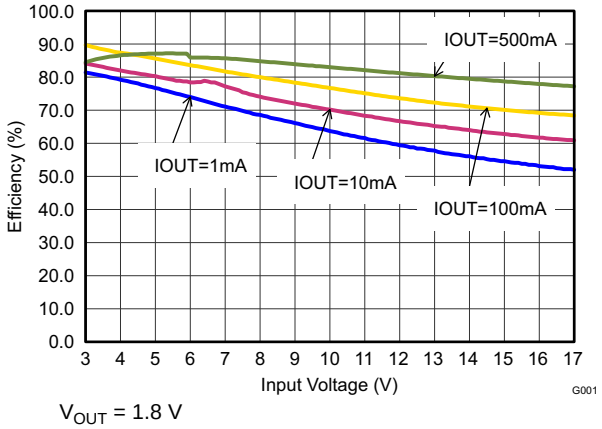


Figure 15. Efficiency vs Input Voltage

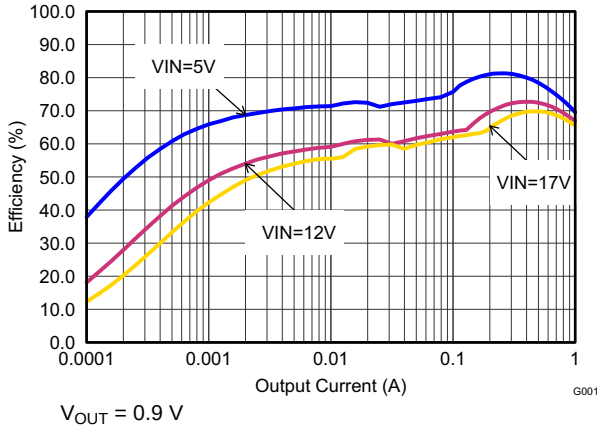


Figure 16. Efficiency vs Output Current

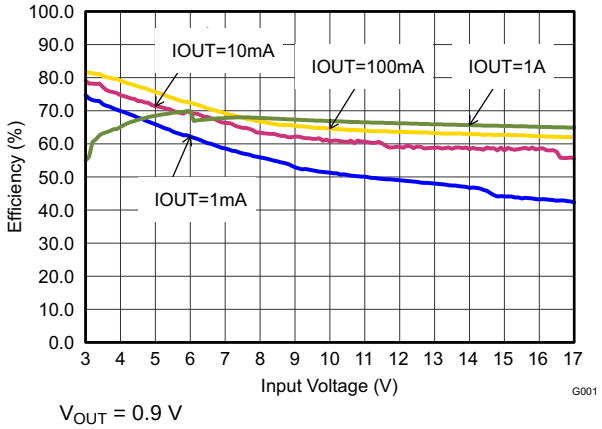


Figure 17. Efficiency vs Input Voltage

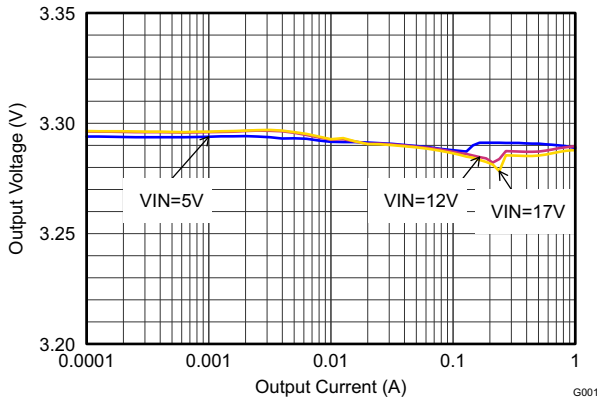


Figure 18. Output Voltage Accuracy (Load Regulation)

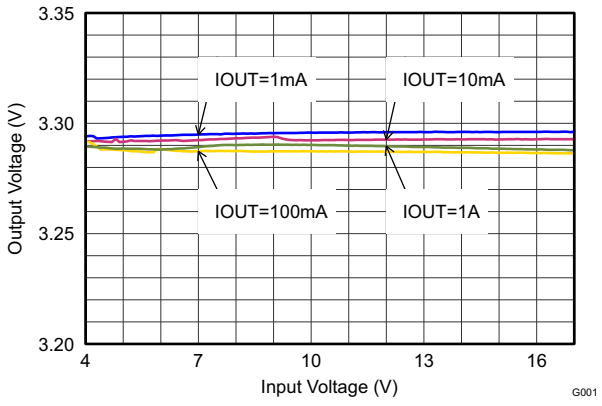


Figure 19. Output Voltage Accuracy (Line Regulation)

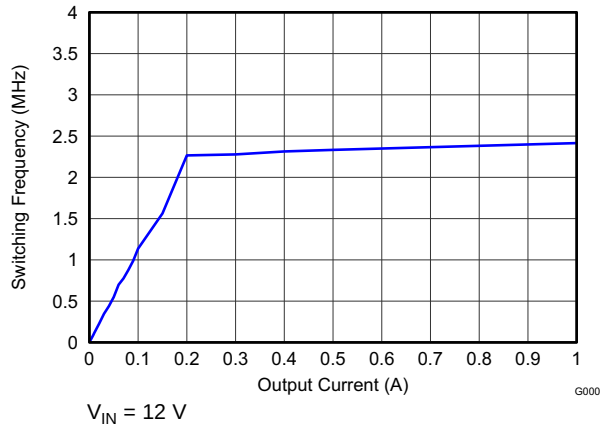


Figure 20. Switching Frequency

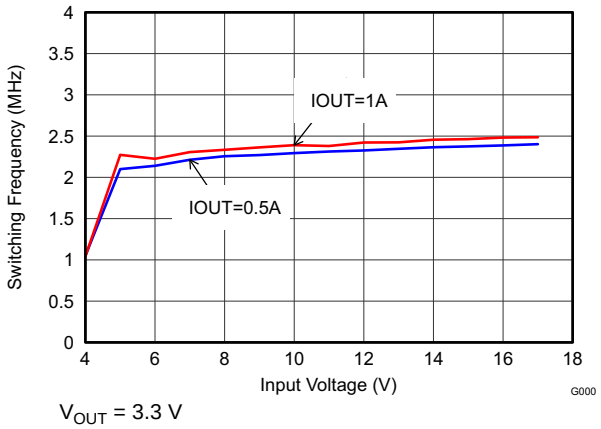


Figure 21. Switching Frequency

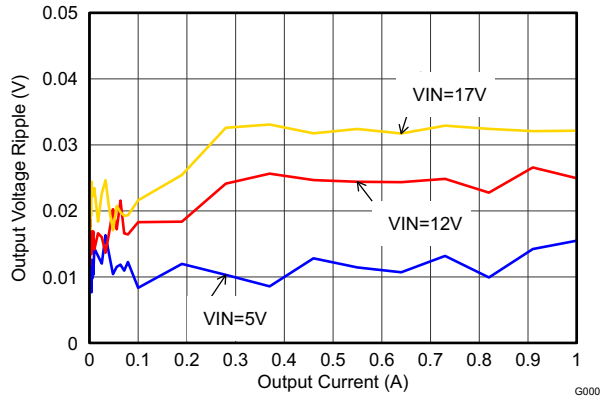


Figure 22. Output Voltage Ripple

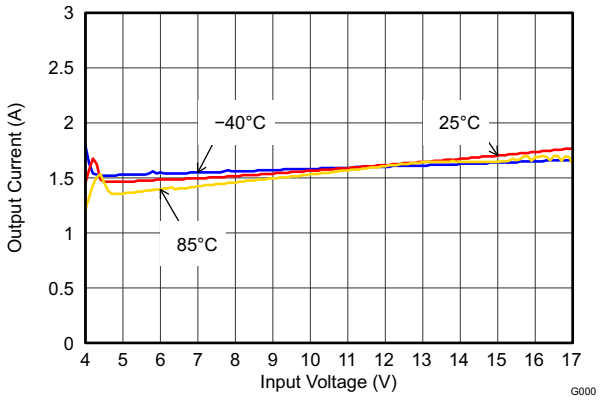


Figure 23. Maximum Output Current

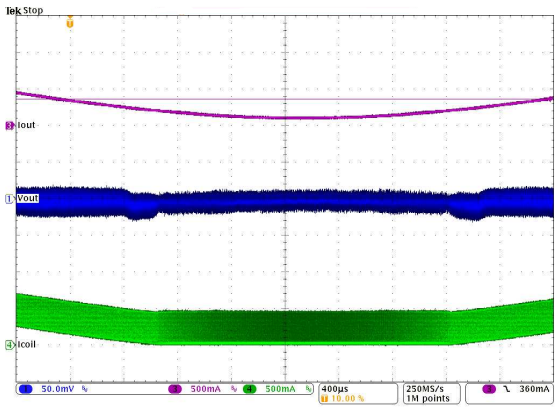


Figure 24. PWM to PSM Mode Transition

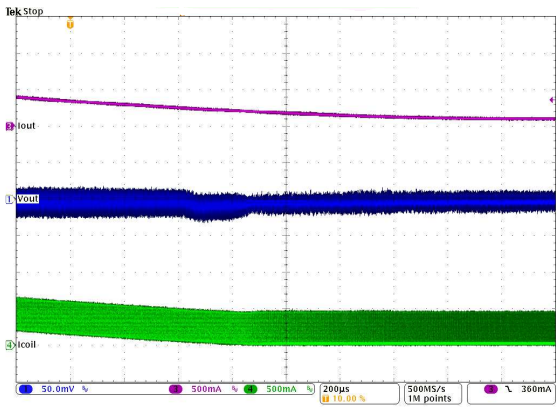


Figure 25. PSM to PWM Mode Transition

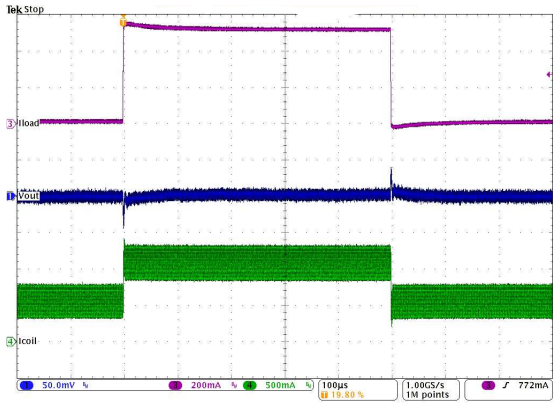


Figure 26. Load Transient Response in PWM Mode (500 mA to 1 A)

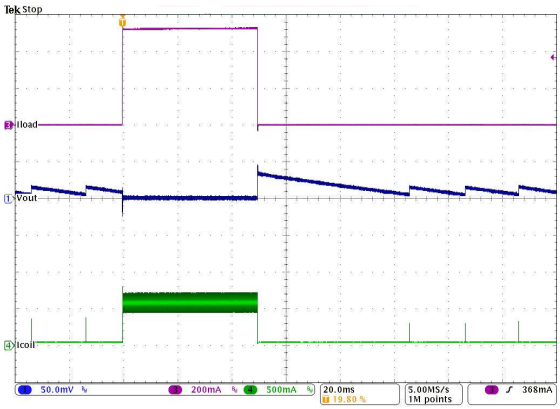


Figure 27. Load Transient Response from Power Save Mode (100 mA to 500 mA)

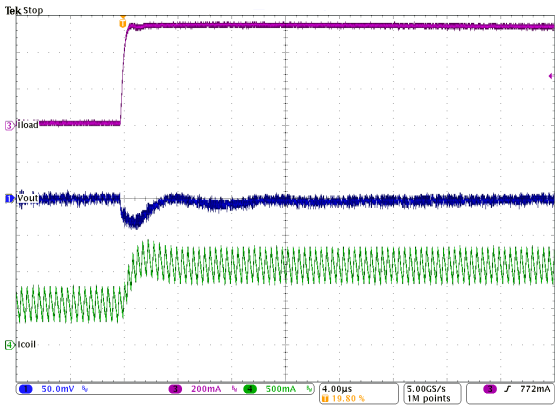


Figure 28. Load Transient Response in PWM Mode (500 mA to 1 A), Rising Edge

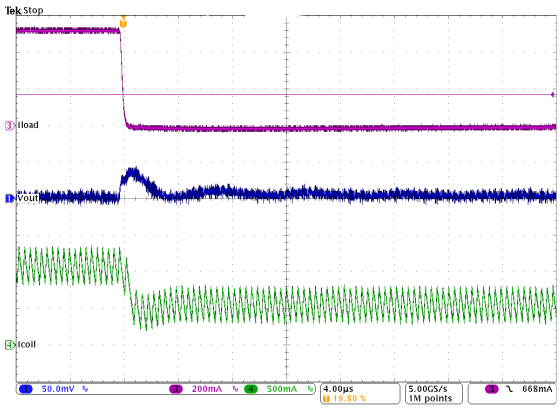


Figure 29. Load Transient Response in PWM Mode (500 mA to 1 A), Falling Edge

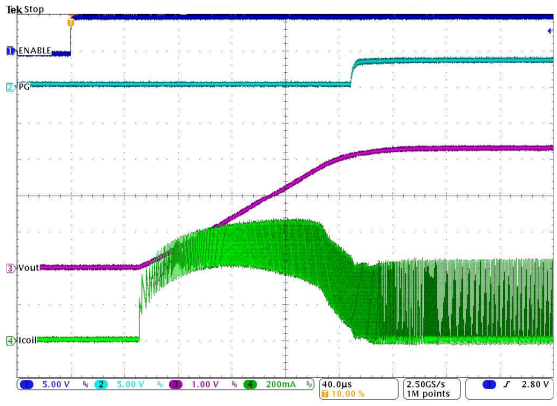


Figure 30. Startup with I_{OUT} = 100 mA

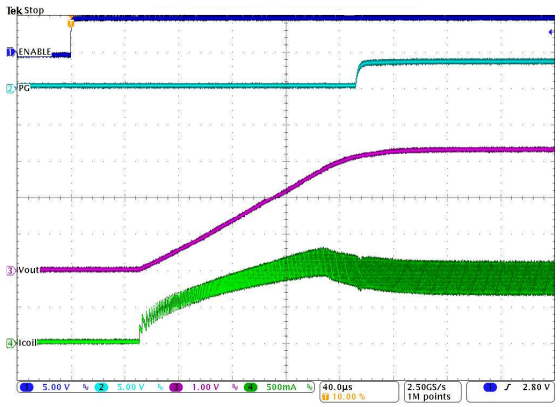
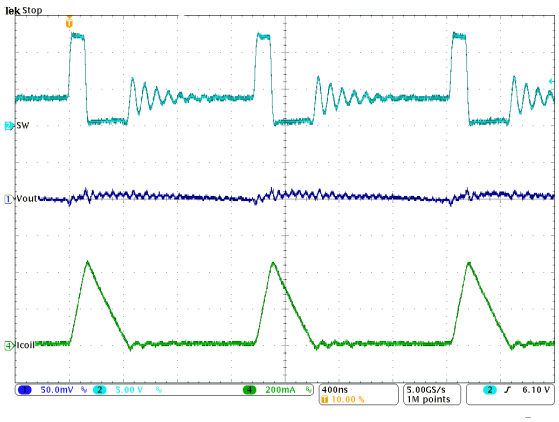
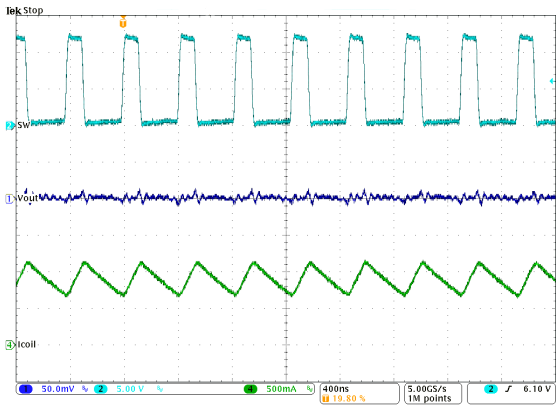


Figure 31. Startup with I_{OUT} = 1 A



I_{OUT} = 66 mA

Figure 32. Typical Operation in Power Save Mode



I_{OUT} = 1 A

Figure 33. Typical Operation in PWM Mode

9.3 System Examples

9.3.1 1-A Power Supply

The following example circuits show various TPS6216x devices and input voltages that provide a 1-A power supply with output voltage options.

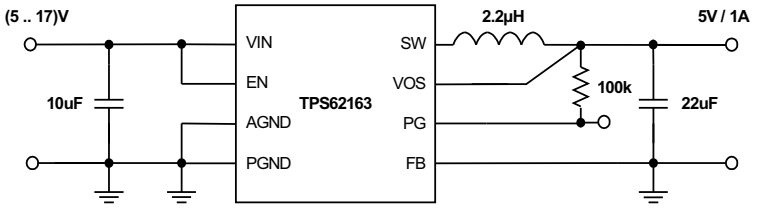


Figure 34. 5 V / 1 A Power Supply

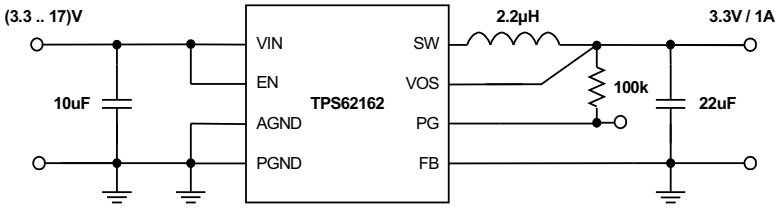


Figure 35. 3.3 V / 1 A Power Supply

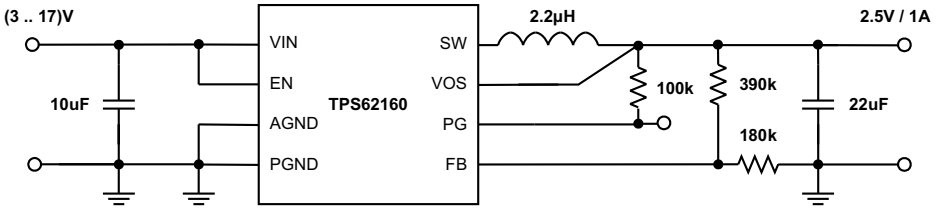


Figure 36. 2.5 V / 1 A Power Supply

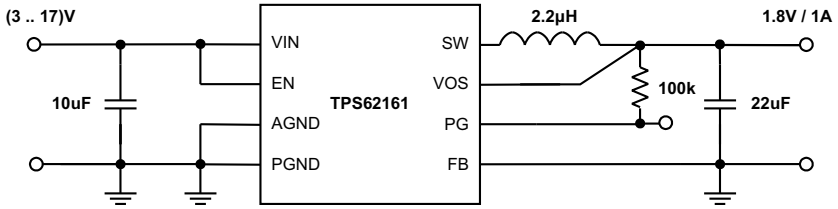


Figure 37. 1.8 V / 1 A Power Supply

System Examples (continued)

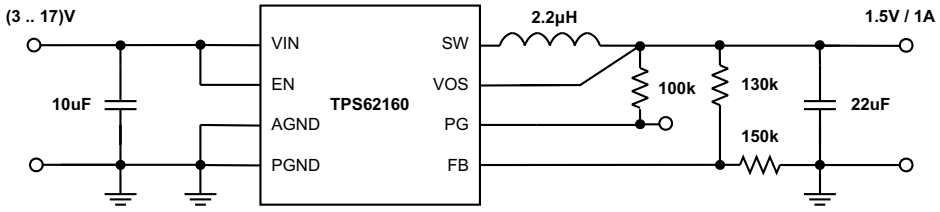


Figure 38. 1.5 V / 1 A Power Supply

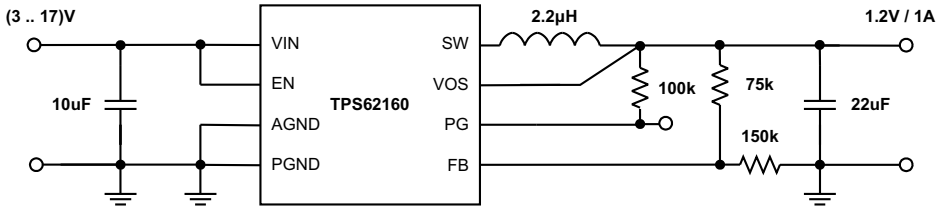


Figure 39. 1.2 V / 1 A Power Supply

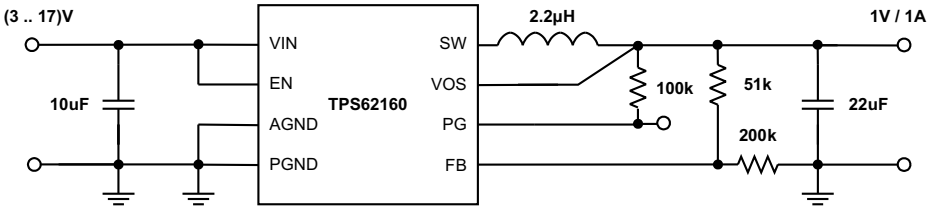


Figure 40. 1 V / 1 A Power Supply

System Examples (continued)

9.3.2 Inverting Power Supply

The TPS6216x can be used as inverting power supply by rearranging external circuitry as shown in Figure 41. As the former GND node now represents a voltage level below system ground, the voltage difference between V_{IN} and V_{OUT} has to be limited for operation to the maximum supply voltage of 17 V (see Equation 13).

$$V_{IN} + \left|V_{OUT}\right| \le V_{IN\,max} \tag{13}$$

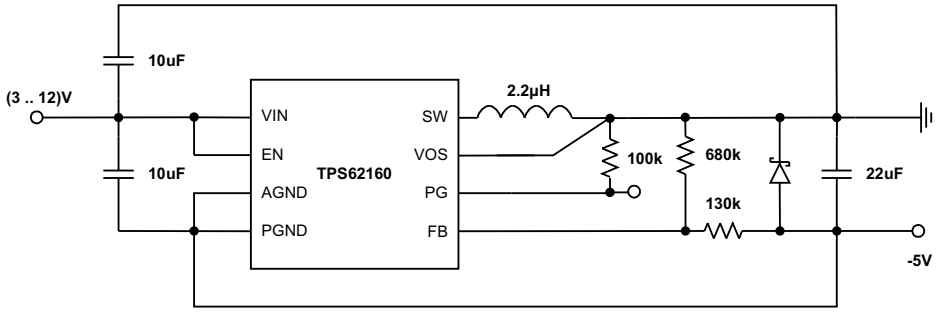


Figure 41. –5 V Inverting Power Supply

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a right half plane zero additionally. The loop stability has to be adapted and an output capacitance of at least 22 µF is recommended. A detailed design example is given in SLVA469.

10 Power Supply Recommendations

The TPS6216x device family has no special requirements for its input power supply. The input power supply' s output current needs to be rated according to the supply voltage, output voltage, and output current of the TPS6216x.

11 Layout

11.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TPS6216x demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation, and noise sensitivity.

Provide low inductive and resistive paths to ground for loops with high di/dt. Therefore paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths, with respect to all other nodes, for wires with high dv/dt. Therefore the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Also sensitive nodes like FB and VOS should be connected with short wires, not nearby high dv/dt signals, such as SW. As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). Signals not assigned to power transmission, such as the feedback divider, should refer to the signal ground (AGND) and always be separated from the power ground (PGND).

In summary, the input capacitor should be placed as close as possible to the VIN and PGND pin of the IC. This connections should be done with wide and short traces. The output capacitor should be placed such that its ground is as close as possible to the IC's PGND pins - avoiding additional voltage drop in traces. This connection should also be made short and wide. The inductor should be placed close to the SW pin and connect directly to the output capacitor - minimizing the loop area between the SW pin, inductor, output capacitor and PGND pin. The feedback resistors, R_1 and R_2, should be placed close to the IC and connect directly to the AGND and FB pins. Those connections (including VOUT) to the resistors and especially to the VOS pin should stay away from noise sources, such as the inductor. The VOS pin should connect in the shortest way to VOUT at the output capacitor, while the VOUT connection to the feedback divider can connect at the load.

A single point grounding scheme should be implemented with all grounds (AGND, PGND and the thermal pad) connecting at the IC's exposed thermal pad. See Figure 42 for the recommended layout of the TPS6216x. More detailed information can be found in the EVM Users Guide, SLVU483.

The exposed thermal pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation. Although the exposed thermal pad can be connected to a floating circuit board trace, the device has better thermal performance if it is connected to a larger ground plane. The exposed thermal pad is electrically connected to AGND.

11.2 Layout Example

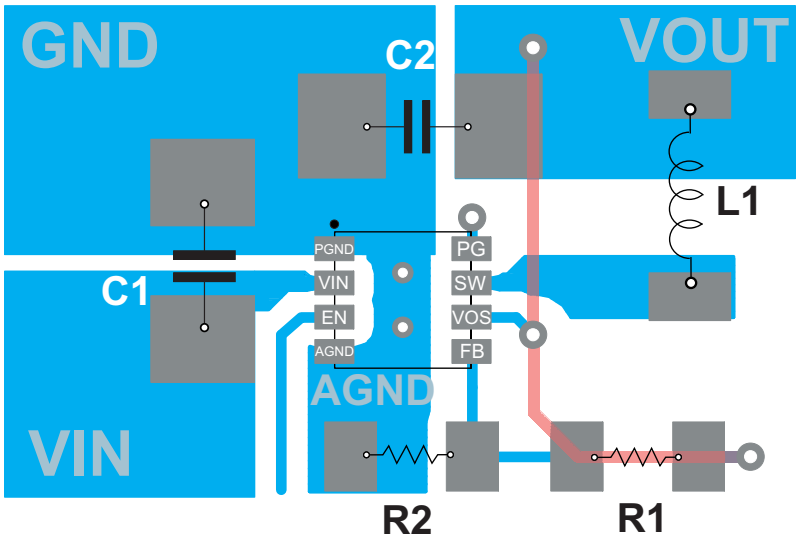


Figure 42. TPS6216x Board Layout

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the exposed thermal pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application reports *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs,* SZZA017 and *Semiconductor and IC Package Thermal Metrics,* SPRA953.

The TPS6216x is designed for a maximum operating junction temperature (T_J) of 125°C. Therefore the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. If the thermal resistance of the package is given, the size of the surrounding copper area and a proper thermal connection of the IC can reduce the thermal resistance. To get an improved thermal behavior, TI recommends to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.1.2 开发支持

12.1.2.1 使用 WEBENCH® 工具定制设计方案

请单击此处，结合使用 TPS62160 器件和 WEBENCH® 电源设计器创建定制设计方案。

1. 在开始阶段键入输出电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键设计参数，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- *《优化 TPS62130/40/50/60/70 输出滤波器》*，SLVA463
- *《采用前馈电容优化内部补偿 DC-DC 转换器的瞬态响应》*，SLVA289
- *《采用前馈电容提升 TPS62130/40/50/60/70 的稳定性和带宽》*，SLVA466
- *《采用 JEDEC PCB 设计的线性和逻辑封装散热特性》*，SZZA017

12.3 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **5.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
TPS62160	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62161	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62162	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62163	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

社区资源 **(**接下页**)**

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.5 商标

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All other trademarks are the property of their respective owners.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62160DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	62160	Samples
TPS62160DGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	62160	Samples
TPS62160DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTV	Samples
TPS62160DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTV	Samples
TPS62161DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUB	Samples
TPS62161DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUB	Samples
TPS62162DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUC	Samples
TPS62162DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUC	Samples
TPS62163DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUD	Samples
TPS62163DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

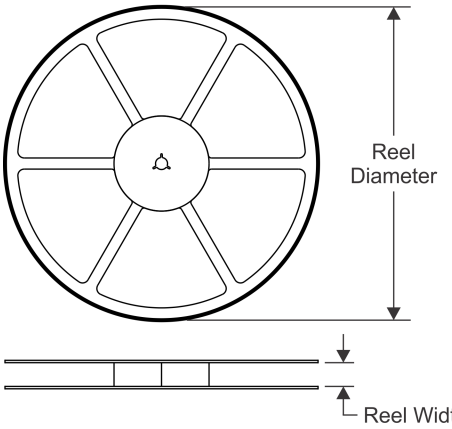
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

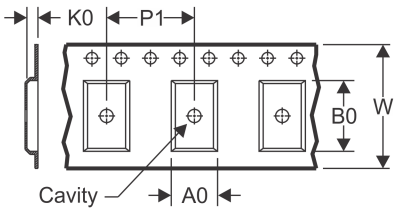
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

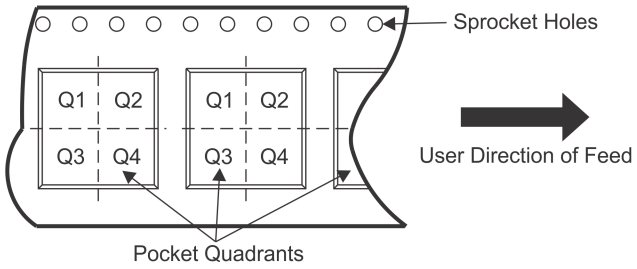


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

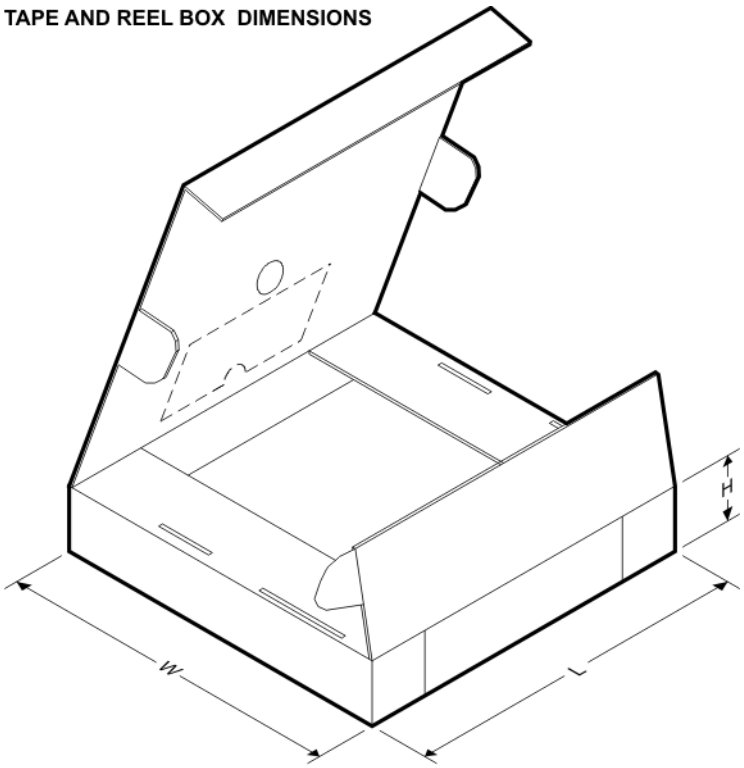
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62160DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62160DGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62160DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62160DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62160DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62161DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62161DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62162DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62162DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62162DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62163DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62163DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

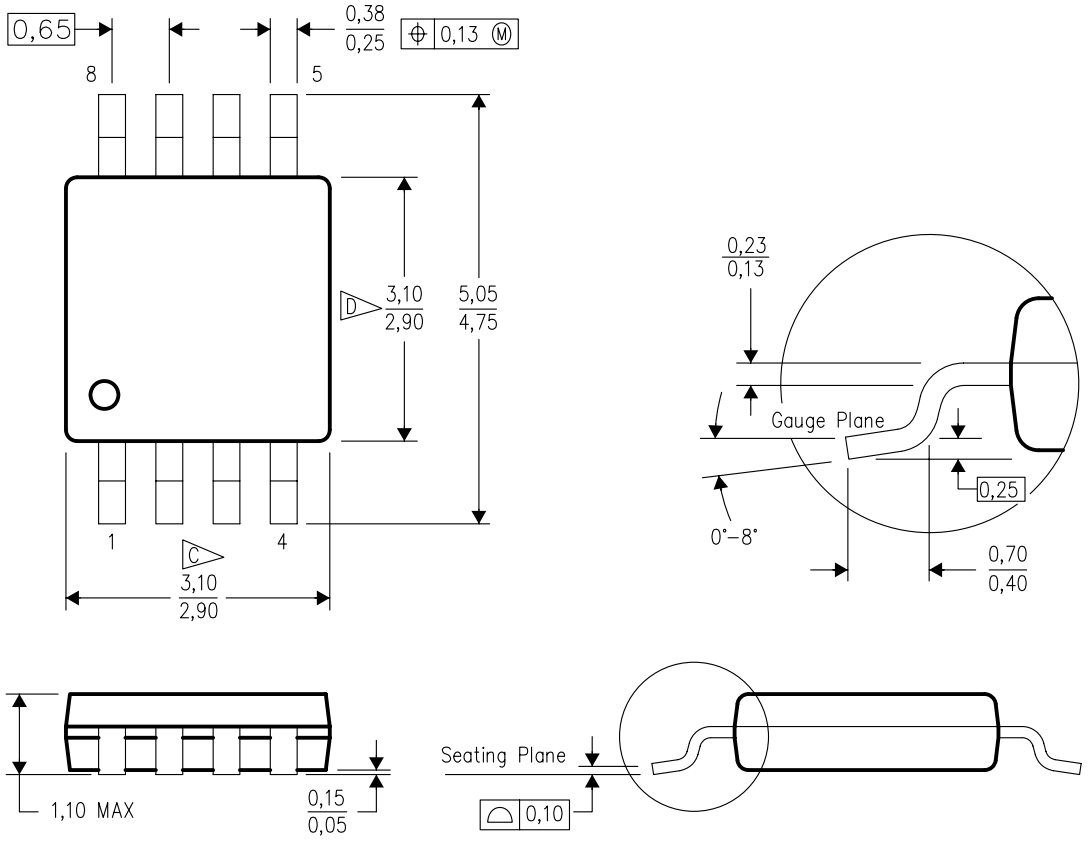
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62160DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TPS62160DGKT	VSSOP	DGK	8	250	364.0	364.0	27.0
TPS62160DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62160DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62160DSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS62161DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62161DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS62162DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62162DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62162DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS62163DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62163DSGT	WSON	DSG	8	250	210.0	185.0	35.0

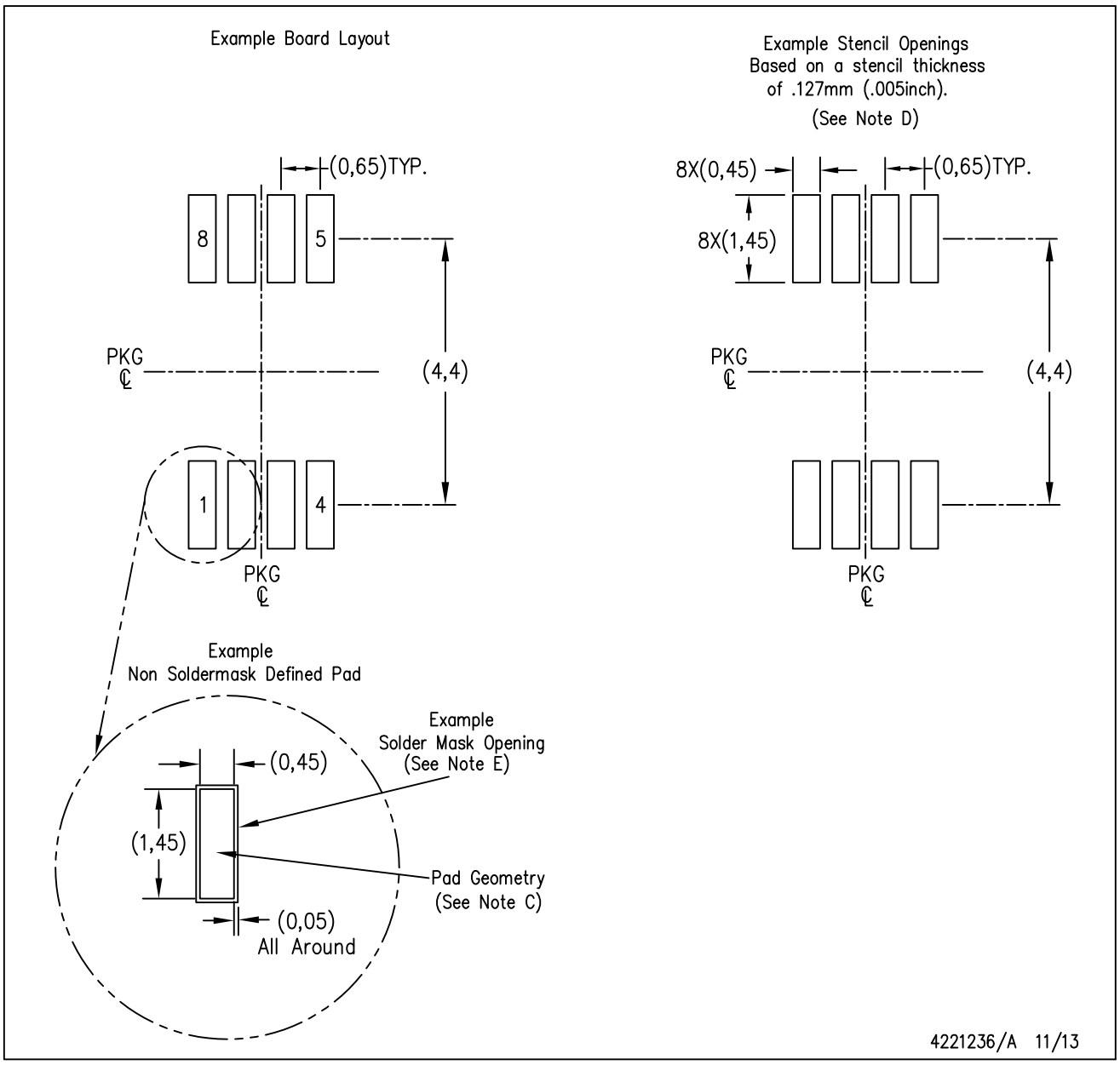
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

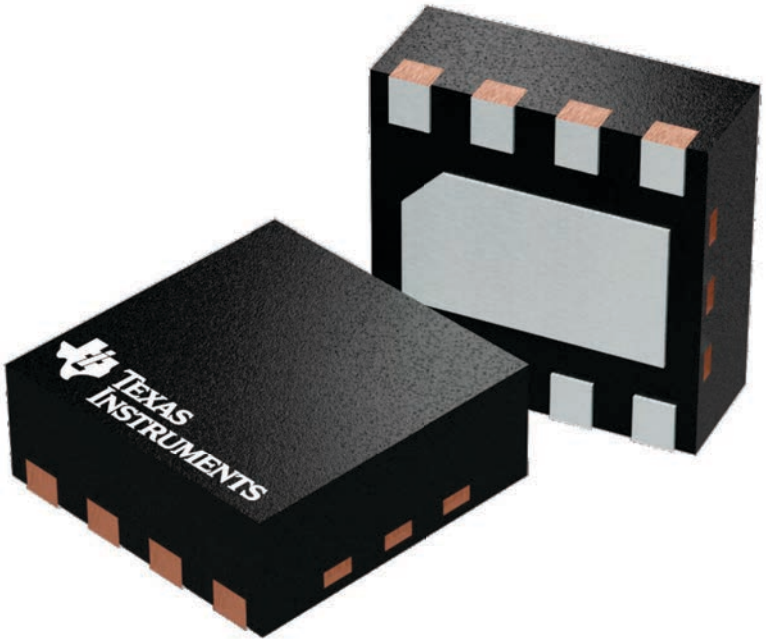
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



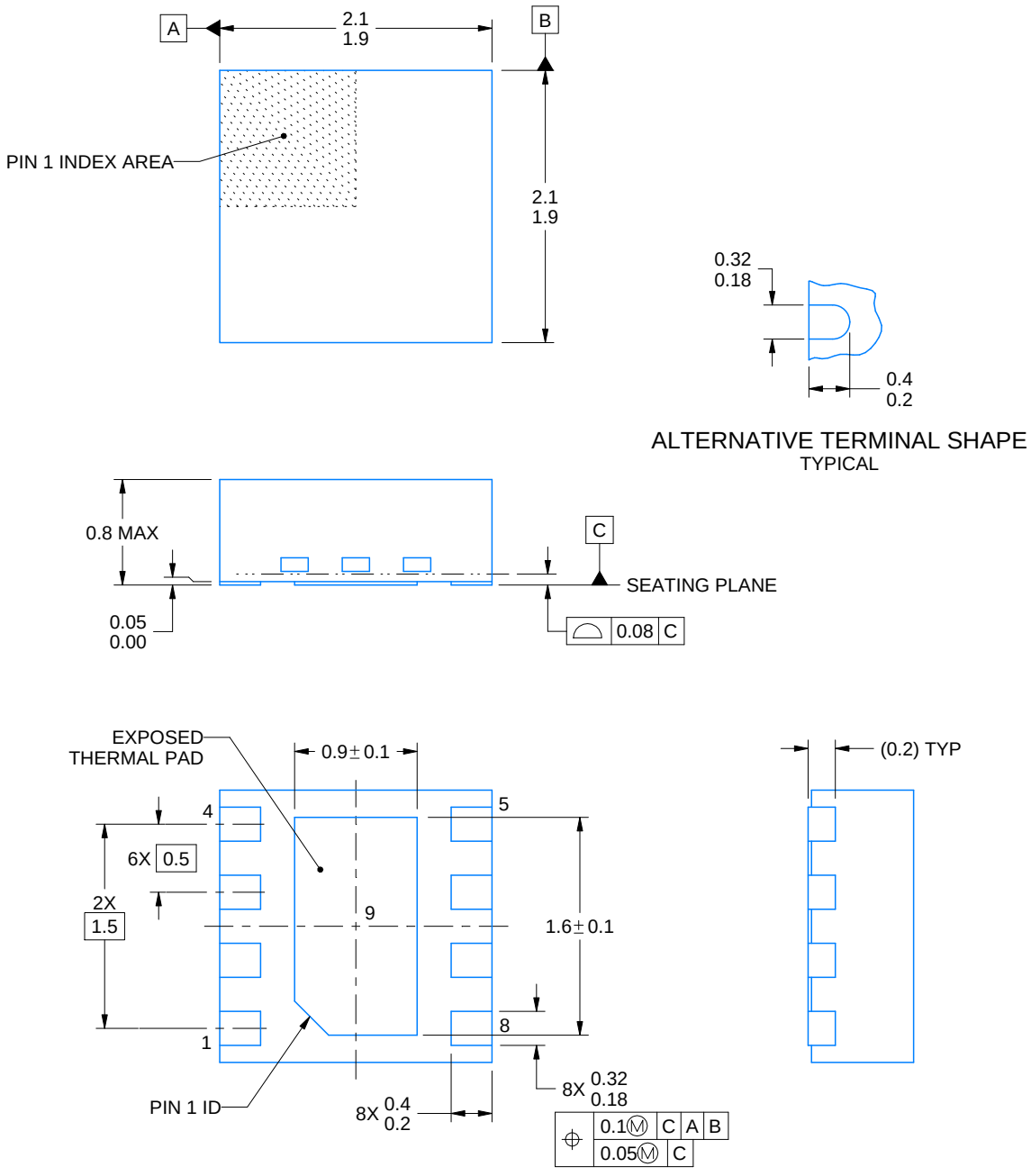
4224783/A

PACKAGE OUTLINE

DSG0008A

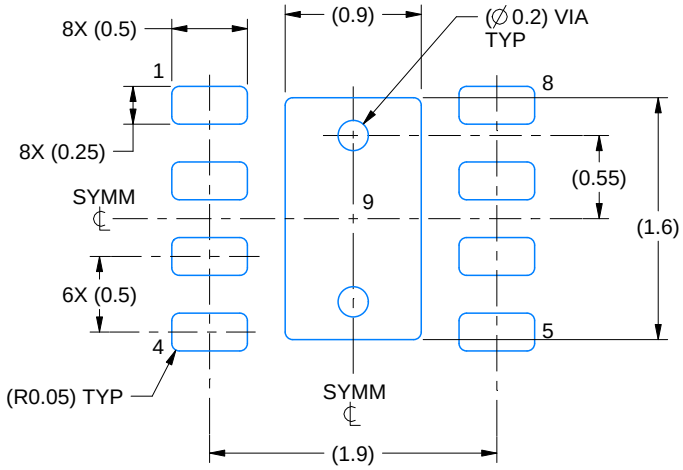
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

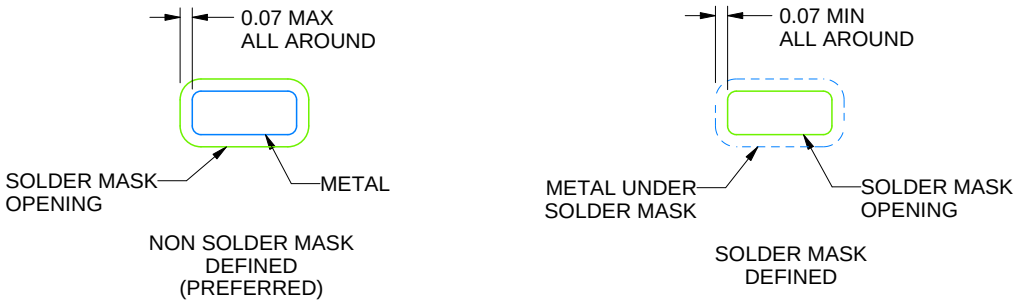


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/D 04/2020

NOTES: (continued)

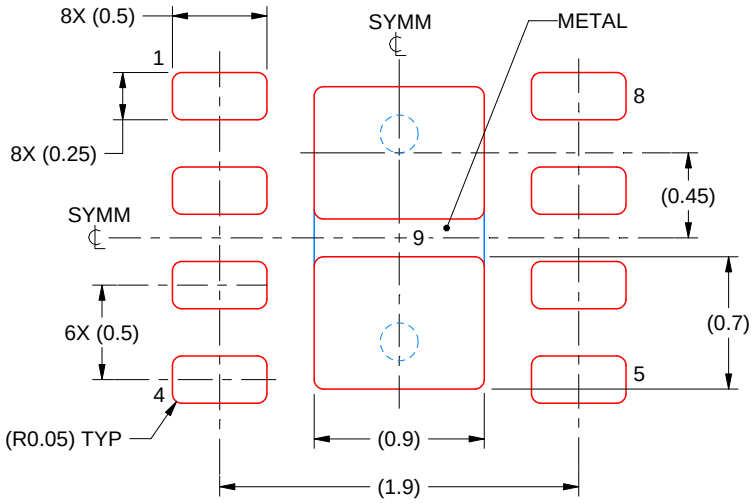
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/D 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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