



具有杂音抑制功能的 25mW DIRECTPATH™ 立体声头戴式耳机放大器

查询样品: [TPA6136A2](#)

特性

- 专利 **DirectPath™** 技术免除了增设隔直流电容器的需要
 - 输出被偏置于 **0 V**
 - 卓越的低频保真度
- 喀嗒/噼啪噪声抑制活动
- 高阻抗输出模式允许共用输出插孔
- 电源电流通常为 **2.1mA**
- 全差分输入降低了系统噪声
 - 也可配置为单端输入
- **SGND** 引脚可减少接地环路噪声
- **2.3V 至 5.5V** 电源提供恒定最大输出功率
 - 简化了设计以防声震
- 可兼容 **Microsoft™ Windows Vista™**
- **100dB** 电源噪声抑制
- 宽电源范围: **2.3V 至 5.5V**
- 增益设定值: **0 dB 和 6 dB**
- 短路和过热保护
- **±8kV HBM ESD** 保护输出
- 提供小封装
 - **16 焊球、1.6mm x 1.6mm、0.4mm 间距 W CSP**

应用

- 智能电话/手机
- 便携式媒体 / **MP3** 播放器
- 笔记本电脑
- 便携式游戏设备

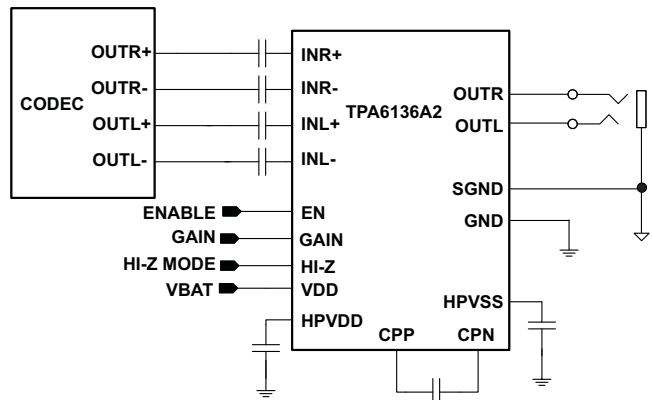
说明

TPA6136A2 (有时被称为 TPA6136) 是一款 DirectPath™ 立体声头戴式耳机放大器, 该器件免除了增设外部隔直流输出电容器的需要。差动立体声输入和内置电阻设置器件增益, 进一步减少了外部组件数。可选增益为 0 dB 或 6 dB。该放大器可从 2.3V 单电源为 16Ω 扬声器输送 25mW 的驱动功率。TPA6136A2 (TPA6136) 提供了一个与电源电压无关的恒定最大输出功率, 因而可简化防声震设计。

TPA6136A2 (TPA6136) 具有全差分输入和一个集成型低通滤波器, 旨在减少音源与头戴式耳机放大器之间的系统噪声拾拾, 并降低 DAC 带外噪声。高电源噪声抑制性能和差分架构提升了射频 (RF) 噪声免疫力。对于单端输入信号, 请将 INL+ 和 INR+ 接地。

该器件具有内置杂音抑制电路, 可以完全消除开启和关闭期间的噼啪噪声干扰。放大器输出具有短路和热过载保护以及 ±8 kV HBM ESD 保护能力, 从而可使终端设备更加容易地与 IEC 61000-4-2 ESD 标准的要求相符。

TPA6136A2 (TPA6136) 采用 2.3V 至 5.5V 单工作电源, 典型电源电流为 2.1mA。停机模式可将电源电流减小至 1μA 以下。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DirectPath is a trademark of Texas Instruments.

Windows Vista is a trademark of Microsoft Corporation.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TPA6136A2

ZHCS458A – JULY 2009 – REVISED AUGUST 2009

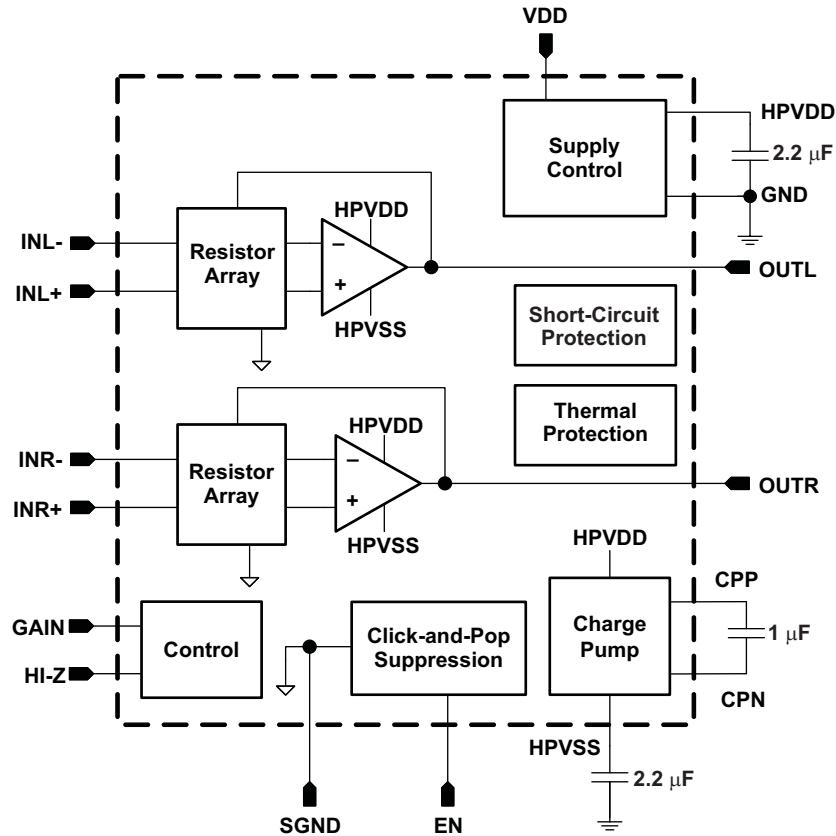
www.ti.com.cn



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

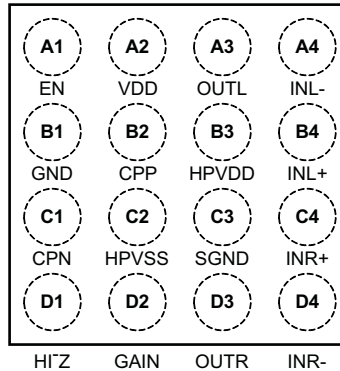
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



DEVICE PINOUT

WCSP PACKAGE (TOP VIEW)



PIN FUNCTIONS

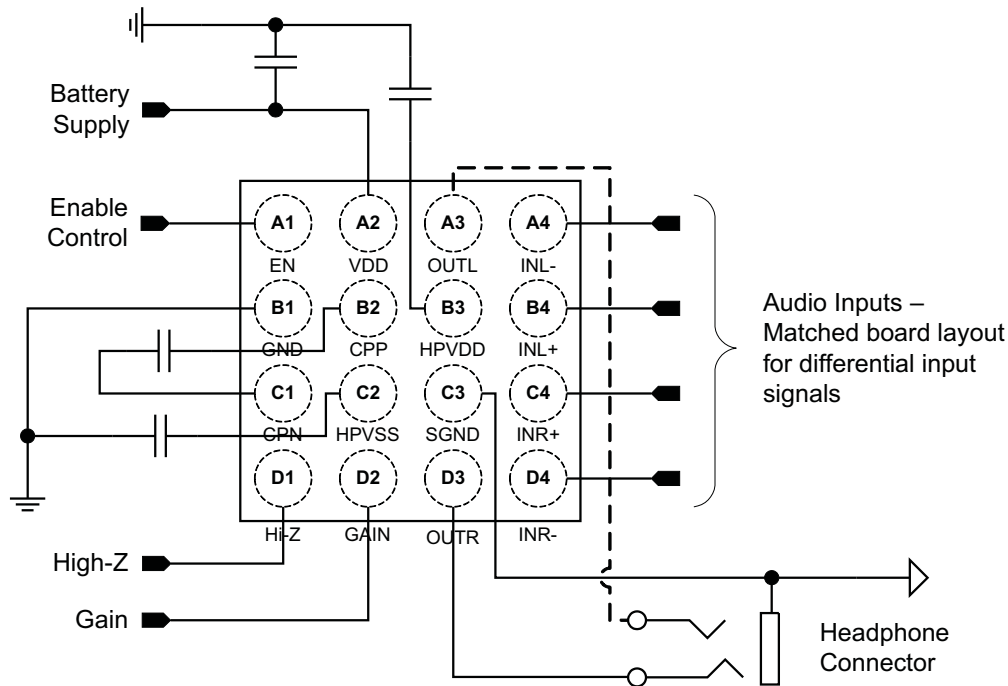
PIN		I/O/P	PIN DESCRIPTION
NAME	WCSP		
INL-	A4	I	Inverting left input for differential signals; left input for single-ended signals
INL+	B4	I	Non-inverting left input for differential signals. Connect to ground for single-ended input applications
INR+	C4	I	Non-inverting right input for differential signals. Connect to ground for single-ended input applications
INR-	D4	I	Inverting right input for differential signals; right input for single-ended signals
OUTR	D3	O	Right headphone amplifier output. Connect to right terminal of headphone jack
HI-Z	D1	I	Output impedance select. Set to logic LOW for normal operation and to logic HIGH for high output impedance
GAIN	D2	I	Gain select. Set to logic LOW for a gain of 0dB and to logic HIGH for a gain of 6dB
HPVSS	C2	P	Charge pump output and negative power supply for output amplifiers; connect 1µF capacitor to GND
CPN	C1	P	Charge pump negative flying cap. Connect to negative side of 1µF capacitor between CPP and CPN
GND	B1	P	Ground
CPP	B2	P	Charge pump positive flying cap. Connect to positive side of 1µF capacitor between CPP and CPN
HPVDD	B3	P	Positive power supply for headphone amplifiers. Connect to a 2.2µF capacitor. Do not connect to VDD
EN	A1	I	Amplifier enable. Connect to logic low to shutdown; connect to logic high to activate
VDD	A2	P	Positive power supply for TPA6136A2
SGND	C3	I	Amplifier reference voltage. Connect to ground terminal of headphone jack
OUTL	A3	O	Left headphone amplifier output. Connect to left terminal of headphone jack

TPA6136A2

ZHCS458A – JULY 2009 – REVISED AUGUST 2009

www.ti.com.cn

BOARD LAYOUT CONCEPT



ABSOLUTE MAXIMUM RATINGS

 over operating free-air temperature range, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

		VALUE / UNIT
	Supply voltage, VDD	-0.3 V to 6.0 V
	Headphone amplifier supply voltage, HPVDD (do not connect to external supply)	-0.3 V to 1.9 V
V_I	Input voltage (INR+, INR-, INL+, INL-)	1.4 V_{RMS}
	Output continuous total power dissipation	See Dissipation Rating Table
T_A	Operating free-air temperature range	-40°C to 85°C
T_J	Operating junction temperature range	-40°C to 150°C
T_{stg}	Storage temperature range	-65°C to 150°C
ESD Protection – HBM	OUTL, OUTR	8 kV
	All Other Pins	2 kV

ORDERING GUIDE

T_A	PACKAGED DEVICES ⁽¹⁾	PART NUMBER ⁽²⁾	SYMBOL
-40°C to 85°C	16-ball, 1.6 mm × 1.6 mm WCSP	TPA6136A2YFFR	AOWI
		TPA6136A2YFFT	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) The YFF packages is only available taped and reeled. The suffix "R" indicates a reel of 3000, the suffix "T" indicates a reel of 250

DISSIPATION RATINGS TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ⁽¹⁾	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
YFF (WCSP)	1250 mW	10 mW/°C	800 mW	650 mW

(1) See JEDEC Standard 51-3 for Low-K board, JEDEC Standard 51-7 for High-K board, and JEDEC Standard 51-12 for using package thermal information. See JEDEC document page for downloadable copies: <http://www.jedec.org/download/default.cfm>.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Supply voltage, VDD	2.3	5.5	V
V _{IH} High-level input voltage; EN, GAIN, HI-Z	1.3		V
V _{IL} Low-level input voltage; EN, GAIN, HI-Z		0.6	V
Voltage applied to Output; OUTR, OUTL (when EN = 0 V)	-0.3	3.6	V
Voltage applied to Output; OUTR, OUTL (when EN ≥ 1.3 V and HI-Z ≥ 1.3 V)	-1.8	1.8	V
T _A Operating free-air temperature	-40	85	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output offset voltage		-0.5		0.5	mV
Power supply rejection ratio	V _{DD} = 2.3 V to 5.5 V		100		dB
High-level output current (EN, GAIN, HI-Z)				1	μA
Low-level output current (EN, GAIN, HI-Z)				1	μA
Supply Current	V _{DD} = 2.3 V, No load, EN = V _{DD}		2.1	2.8	mA
	V _{DD} = 3.6 V, No load, EN = V _{DD}		2.1	2.8	
	V _{DD} = 5.5 V, No load, EN = V _{DD}		2.2	2.9	
	V _{DD} = 2.3 V to 5.5 V, No load, EN = HI-Z = V,		0.7	1.2	
Shutdown Supply Current	EN = 0 V, V _{DD} = 2.3 V to 5.5 V		0.7	1.2	μA

TPA6136A2

ZHCS458A – JULY 2009 – REVISED AUGUST 2009

www.ti.com.cn

OPERATING CHARACTERISTICS

 $V_{DD} = 3.6\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 16\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P _O	Output power ⁽¹⁾ (Outputs in phase)	THD = 1%, f = 1 kHz		25		mW
		THD = 1%, f = 1 kHz, R _L = 32 Ω		22		
V _O	Output voltage ⁽¹⁾ (Outputs in phase)	THD = 1%, V _{DD} = 3.6 V, f = 1 kHz, R _L = 100 Ω		1.1		V _{RMS}
A _V	Closed-loop voltage gain (OUT / IN–)	GAIN = 0 V, (0 dB)	–0.95	–1.0	–1.05	V/V
		GAIN \geq 1.3 V (6 dB)	–1.95	–2.0	–2.05	
ΔA_V	Gain matching	Between Left and Right channels		1%		
R _{IN}	Input impedance (per input pin)	GAIN = 0 V (0 dB)		19.8		k Ω
		GAIN \geq 1.3 V (6 dB)		13.2		
	Input impedance in shutdown (per input pin)	EN = 0 V		10		
V _{CM}	Input common-mode voltage range		–0.5		1.5	V
	Output Impedance	EN = HI-Z \geq 1.3 V, f = 10 kHz		40		k Ω
		EN = HI-Z \geq 1.3 V, f = 1 MHz		4.5		
		EN = HI-Z \geq 1.3 V, f = 10 MHz		0.75		
		EN = 0 V (shutdown mode)		25		Ω
	Input-to-output attenuation in shutdown	EN = 0 V		80		dB
AC PSRR	AC-power supply rejection ratio	200 mV _{pp} ripple, f = 217 Hz	–80	–100		dB
		200 mV _{pp} ripple, f = 10 kHz		–90		
THD+N	Total harmonic distortion plus noise ⁽²⁾	P _O = 20 mW, f = 1 kHz		0.02%		
		P _O = 25 mW into 32 Ω , V _{DD} = 5.5 V, f = 1 kHz		0.01%		
SNR	Signal-to-noise ratio	P _O = 20 mW; GAIN = 0 V, (A _V = 0 dB)		100		dB
E _n	Noise output voltage	A-weighted		5.5		μV_{RMS}
f _{osc}	Charge pump switching frequency		1200	1275	1350	kHz
t _{ON}	Start-up time from shutdown			5		ms
	Crosstalk	P _O = 20 mW, f = 1 kHz		–80		dB
	Thermal shutdown	Threshold		150		$^\circ\text{C}$
		Hysteresis		20		$^\circ\text{C}$

(1) Per output channel

(2) A-weighted

TYPICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.6\text{ V}$, Gain = 0 dB, EN = 3.6 V, $C_{HPVDD} = C_{HPVSS} = 2.2\ \mu\text{F}$, $C_{INPUT} = C_{FLYING} = 1\ \mu\text{F}$, Outputs in Phase

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

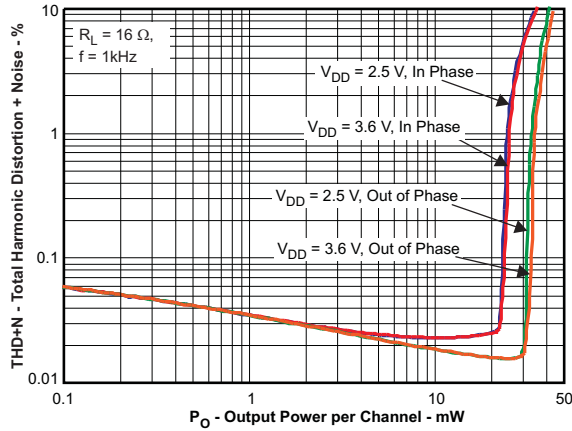


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

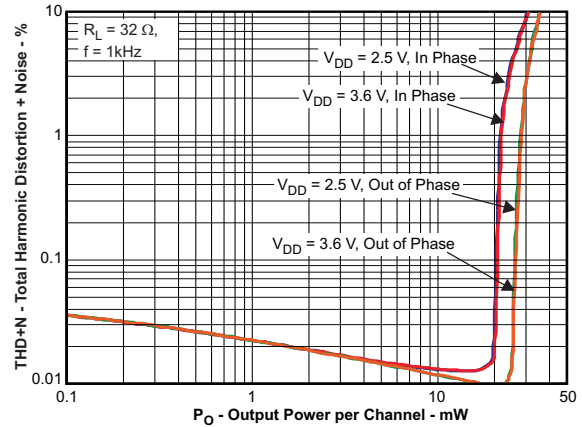


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

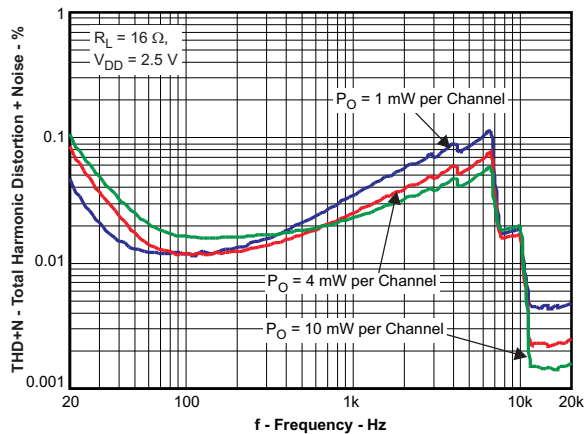


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

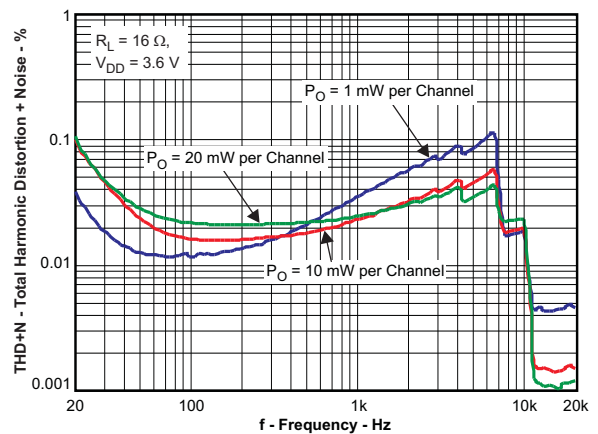


Figure 4.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

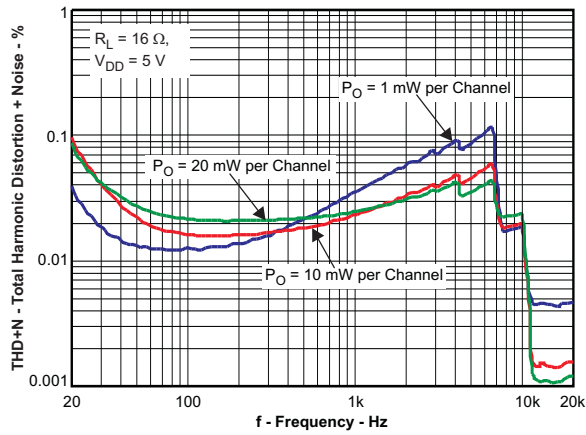


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

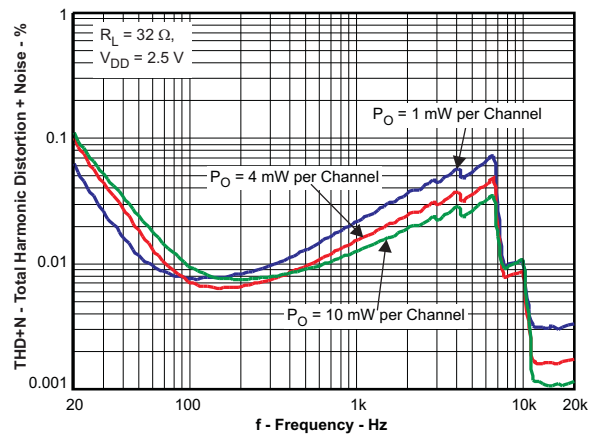


Figure 6.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

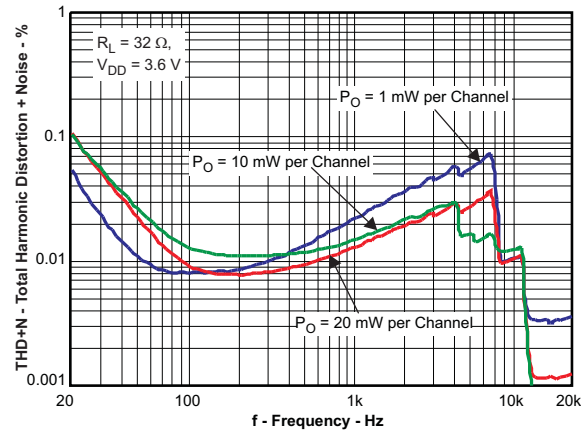


Figure 7.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

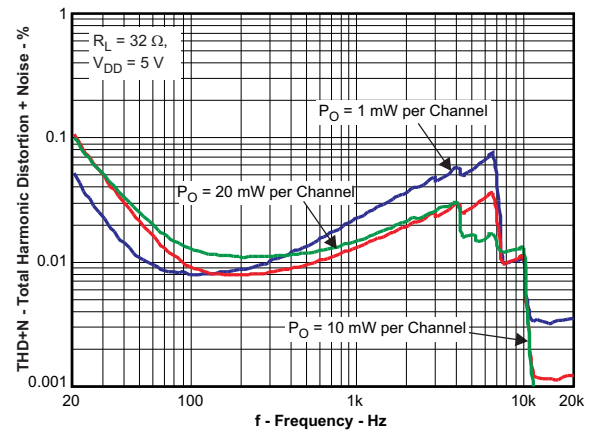


Figure 8.

OUTPUT POWER vs SUPPLY VOLTAGE

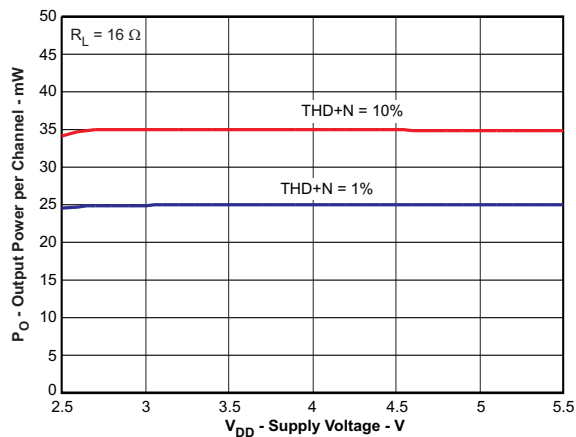


Figure 9.

OUTPUT POWER vs SUPPLY VOLTAGE

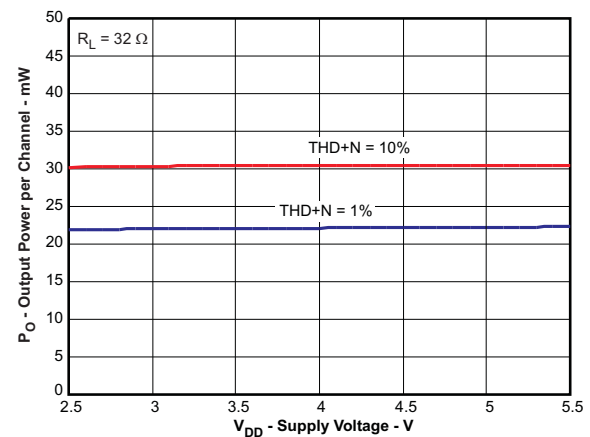


Figure 10.

TYPICAL CHARACTERISTICS (continued)

OUTPUT POWER vs LOAD RESISTANCE

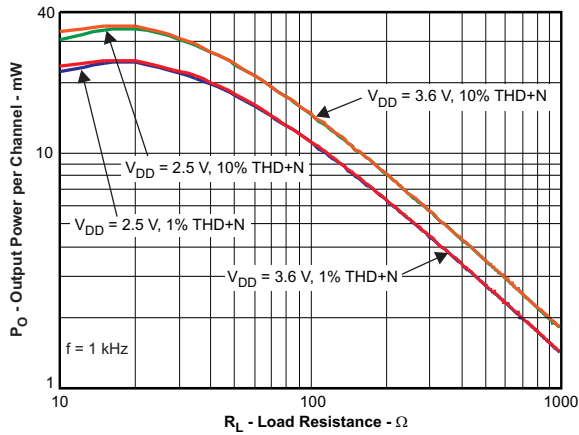


Figure 11.

OUTPUT POWER vs LOAD RESISTANCE

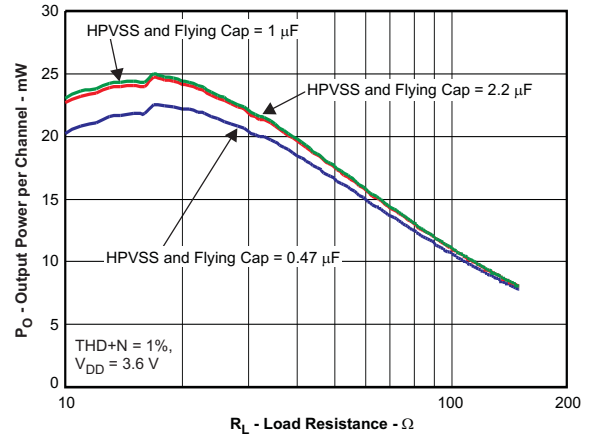


Figure 12.

OUTPUT VOLTAGE vs SUPPLY VOLTAGE

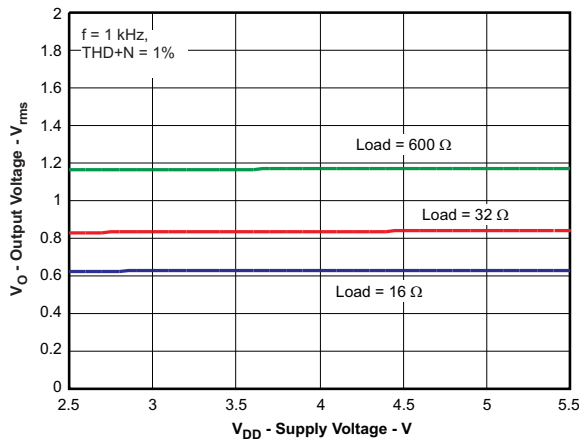


Figure 13.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

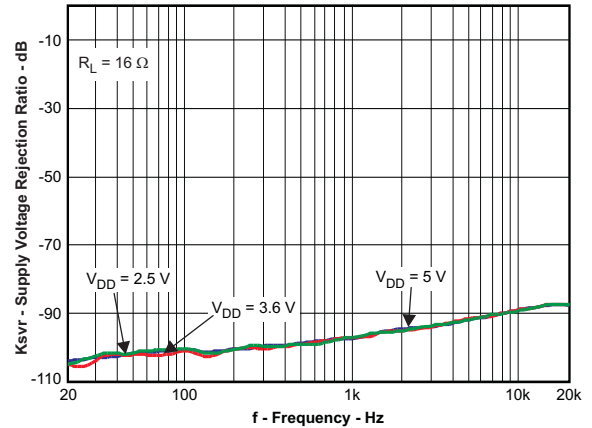


Figure 14.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

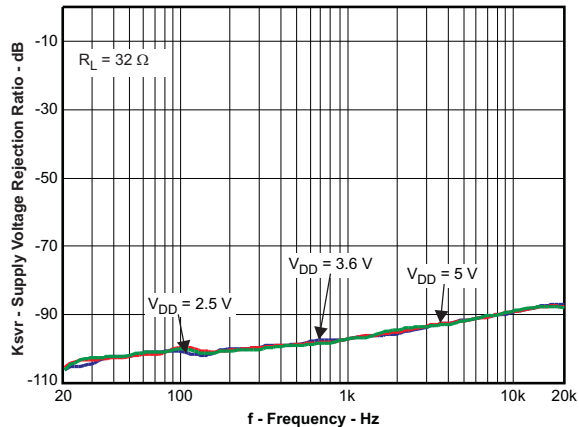


Figure 15.

QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

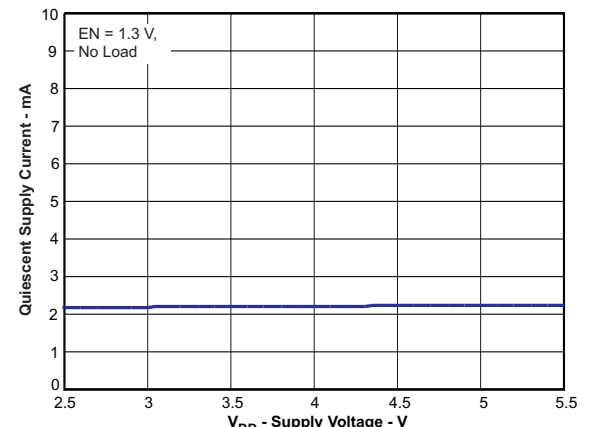


Figure 16.

TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT vs TOTAL OUTPUT POWER

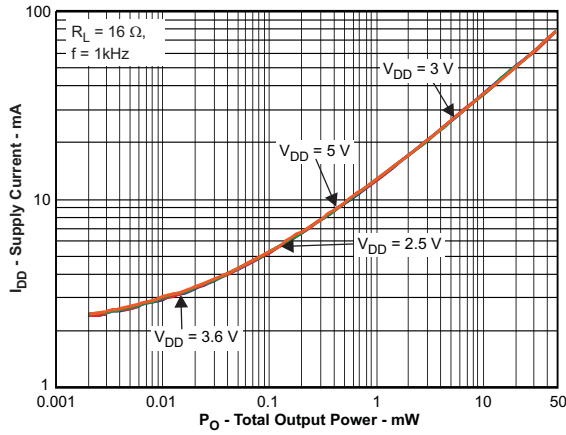


Figure 17.

SUPPLY CURRENT vs TOTAL OUTPUT POWER

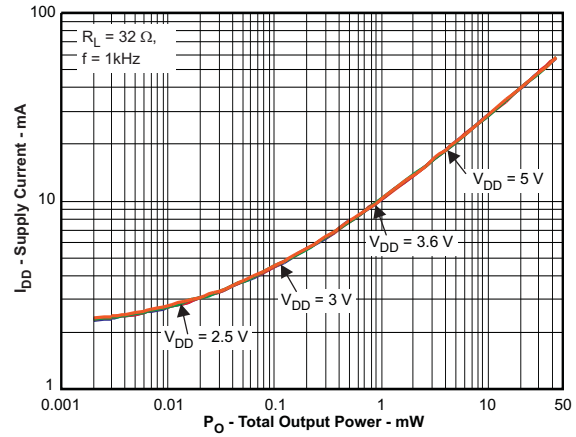


Figure 18.

CROSSTALK vs FREQUENCY

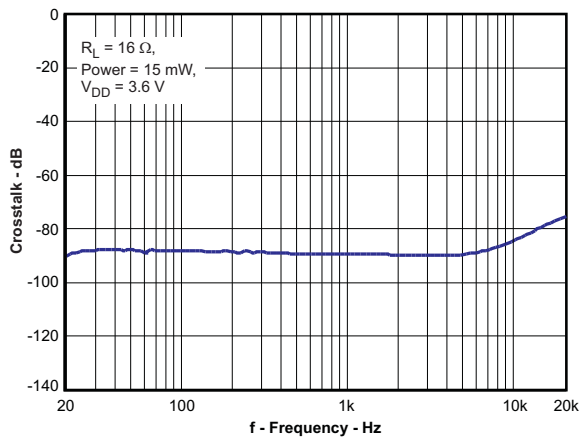


Figure 19.

OUTPUT SPECTRUM vs FREQUENCY

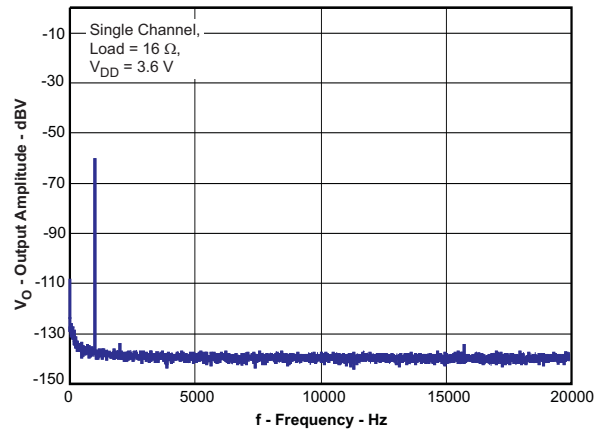


Figure 20.

HI-Z OUTPUT IMPEDANCE vs FREQUENCY

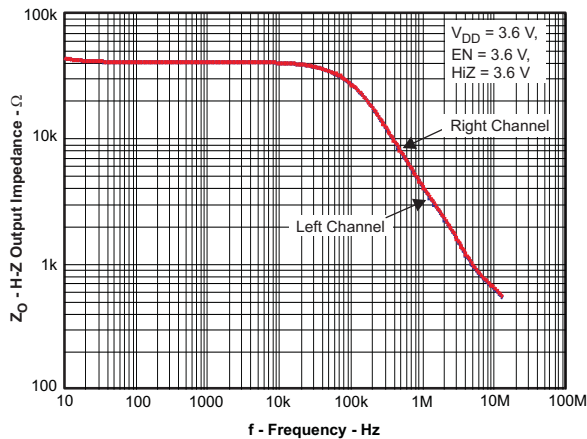


Figure 21.

STARTUP WAVEFORMS vs TIME

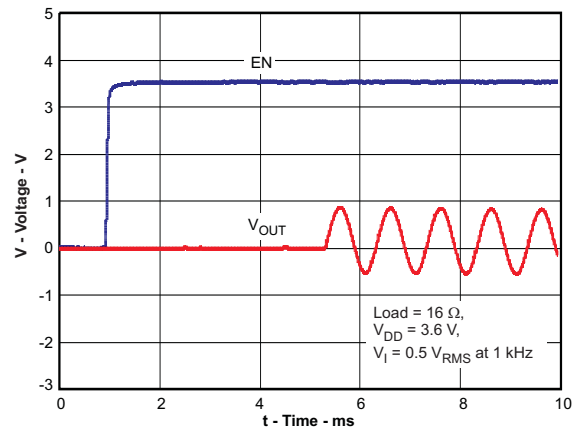


Figure 22.

TYPICAL CHARACTERISTICS (continued)
SHUTDOWN WAVEFORMS vs
TIME

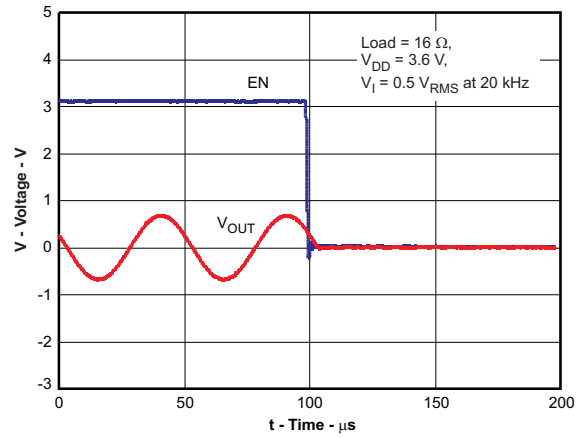


Figure 23.

APPLICATION INFORMATION

APPLICATION CIRCUIT

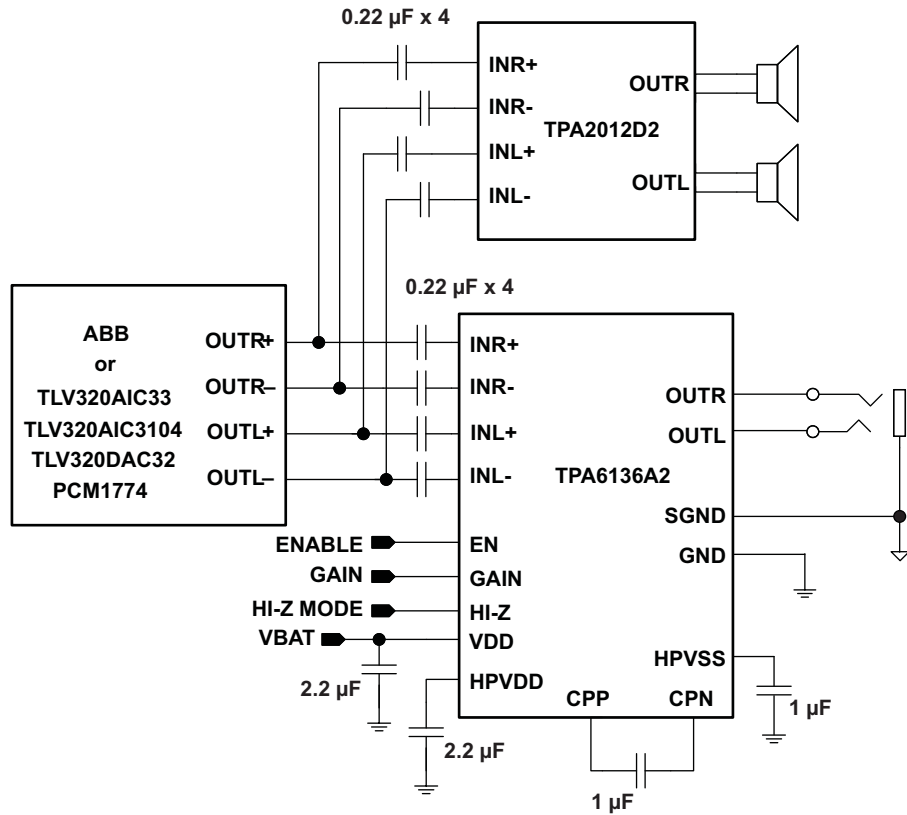


Figure 24. Typical Application Configuration with Differential Input Signals

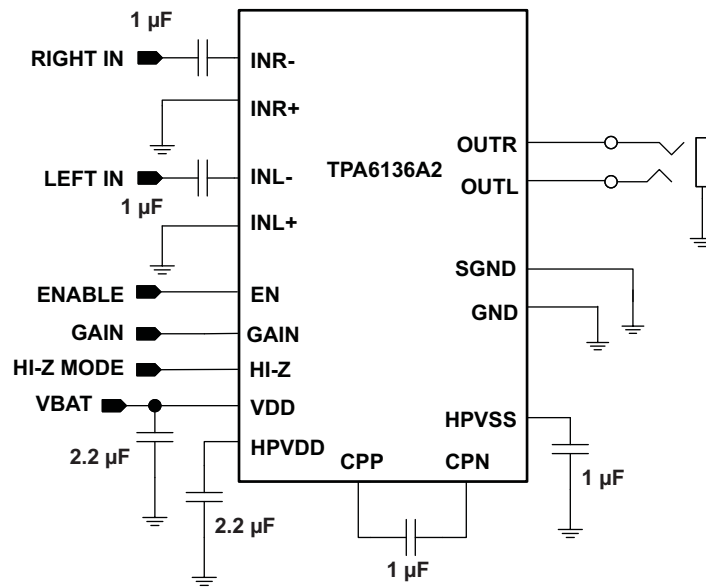


Figure 25. Typical Application Configuration with Single-Ended Input Signals

GAIN CONTROL

The TPA6136A2 has two gain settings which are controlled with the GAIN pin. The following table gives an overview of the gain function.

GAIN VOLTAGE	AMPLIFIER GAIN
≤ 0.6 V	0 dB
≥ 1.3 V	6 dB

Table 1. Windows Vista™ Premium Mobile Mode Specifications

Device Type	Requirement	Windows Premium Mobile Vista Specifications	TPA6136A2 Typical Performance
Analog Speaker Line Jack [$R_L = 10$ k Ω , FS = 0.707 Vrms]	THD+N	≤ -65 dB FS [20 Hz, 20 kHz]	-75 dB FS [20 Hz, 20 kHz]
	Dynamic Range with Signal Present	≤ -80 dB FS A-Weight	-100 dB FS A-Weight
	Line Output Crosstalk	≤ -60 dB [20 Hz, 20 kHz]	-90 dB [20 Hz, 20 kHz]
Analog Headphone Out Jack [$R_L = 32\Omega$, FS = 0.300 Vrms]	THD+N	≤ -45 dB FS [20 Hz, 20 kHz]	-65 dB FS [20 Hz, 20 kHz]
	Dynamic Range with Signal Present	≤ -80 dB FS A-Weight	-94 dB FS A-Weight
	Headphone Output Crosstalk	≤ -60 dB [20 Hz, 20 kHz]	-90 dB [20 Hz, 20 kHz]

HIGH OUTPUT IMPEDANCE

The TPA6136A2 has a HI-Z control pin that increases output impedance while muting the amplifier. Apply a voltage greater than 1.3 V to the HI-Z and EN pin to activate the HI-Z mode. This feature allows the headphone output jack to be shared for other functions besides audio. For example, sharing of a headphone jack between audio and video as shown in Figure 26. The TPA6136A2 output impedance is high enough to prevent attenuating the video signal.

Enable Voltage	HI-Z Voltage	Output Impedance	Maximum External Voltage Applied to the Output Pins	Comments
≤ 0.6 V	≤ 0.6 V	20 Ω – 30 Ω	-0.3 V to 3.3 V ⁽¹⁾	Shutdown Mode
≤ 0.6 V	≥ 1.3 V	20 Ω – 30 Ω		
≥ 1.3 V	≤ 0.6 V	≤ 1 Ω	-	Active Mode
≥ 1.3 V	≥ 1.3 V	40 k Ω @ 10 kHz	-1.8 V to 1.8 V	HI-Z Mode
		4.5 k Ω @ 1 MHz		
		750 Ω @ 10 MHz		

(1) If V_{DD} is < 3.3 V, then maximum allowed external voltage applied is V_{DD} in this mode

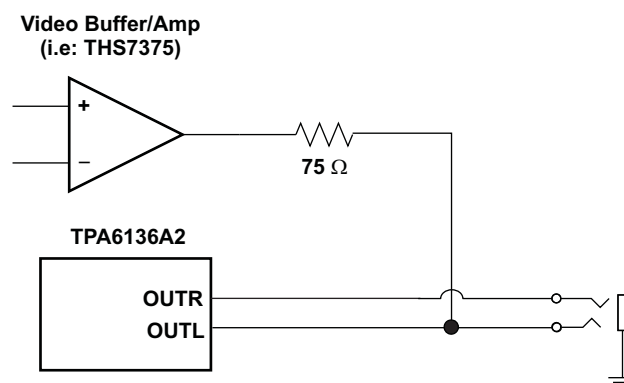


Figure 26. Sharing One Connector Between Audio and Video Signals Example

GROUND SENSE FUNCTION

The ground sense pin, SGND, reduces ground-loop noise when the audio output jack is connected to a different ground reference than codec and amplifier ground. Always connect the SGND pin to the headphone jack. This reduces output offset voltage and eliminates turn-on pop. Figure 27 shows how to connect SGND when an FM radio antenna function is implemented on the headphone wire. The nH coil and capacitor separate the RF signal from the audio GND signal. In this case, SGND is used to eliminate the offset voltage that is generated from the audio signal current and the RF coil low-frequency impedance.

The voltage difference between SGND and AGND cannot be greater than ± 300 mV. The amplifier performance degrades if the voltage difference between SGND and AGND is greater than ± 300 mV.

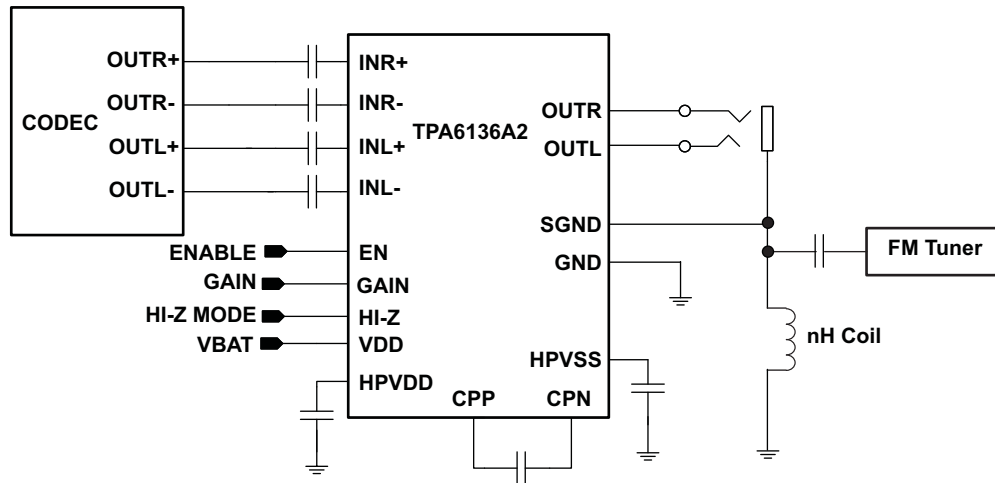


Figure 27. Typical Application Circuit Using Ground Sense Function

HEADPHONE AMPLIFIERS

Single-supply headphone amplifiers typically require dc-blocking capacitors to remove dc bias from their output voltage. The top drawing in Figure 28 illustrates this connection. If dc bias is not removed, large dc current will flow through the headphones which wastes power, clips the output signal, and potentially damages the headphones.

These dc-blocking capacitors are often large in value and size. Headphone speakers have a typical resistance between 16Ω and 32Ω . This combination creates a high-pass filter with a cutoff frequency as shown in Equation 1, where R_L is the load impedance, C_O is the dc-block capacitor, and f_C is the cutoff frequency.

$$f_C = \frac{1}{2\pi R_L C_O} \quad (1)$$

For a given high-pass cutoff frequency and load impedance, the required dc-blocking capacitor is found as:

$$C_O = \frac{1}{2\pi f_C R_L} \quad (2)$$

Reducing f_C improves low frequency fidelity and requires a larger dc-blocking capacitor. To achieve a 20 Hz cutoff with 16Ω headphones, C_O must be at least $500 \mu\text{F}$. Large capacitor values require large packages, consuming PCB area, increasing height, and increasing cost of assembly. During start-up or shutdown the dc-blocking capacitor has to be charged or discharged. This causes an audible pop on start-up and power-down. Large dc-blocking capacitors also reduce audio output signal fidelity.

Two different headphone amplifier architectures are available to eliminate the need for dc-blocking capacitors. The Capless amplifier architecture provides a reference voltage to the headphone connector shield pin as shown in the middle drawing of Figure 28. The audio output signals are centered around this reference voltage, which is typically half of the supply voltage to allow symmetrical output voltage swing.

When using a Capless amplifier do not connect the headphone jack shield to any ground reference or large currents will result. This makes Capless amplifiers ineffective for plugging non-headphone accessories into the headphone connector. Capless amplifiers are useful only with floating GND headphones.

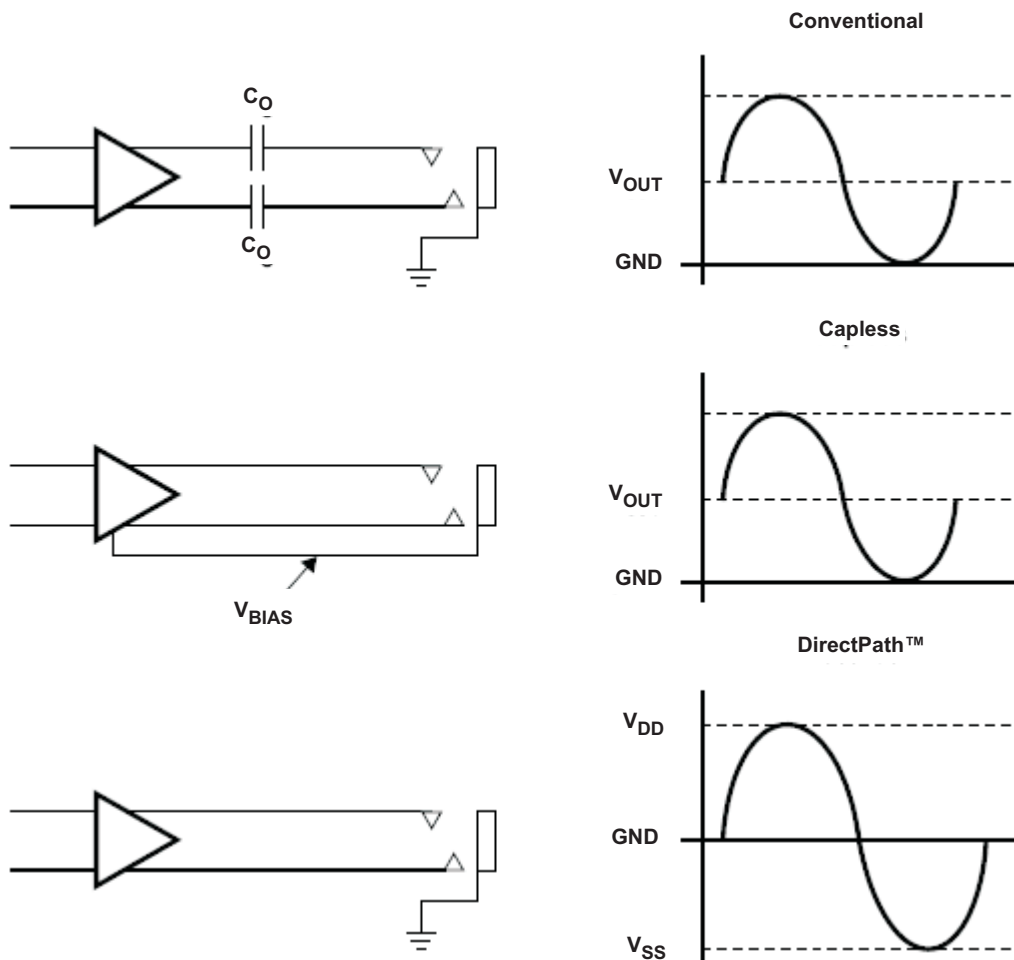


Figure 28. Amplifier Applications

The DirectPath™ amplifier architecture operates from a single supply voltage and uses an internal charge pump to generate a negative supply rail for the headphone amplifier. The output voltages are centered around 0 V and are capable of positive and negative voltage swings as shown in the bottom drawing of Figure 28. DirectPath amplifiers require no output dc-blocking capacitors. The headphone connector shield pin connects to ground and will interface with headphones and non-headphone accessories. The TPA6136A2 is a DirectPath amplifier.

ELIMINATING TURN-ON POP AND POWER SUPPLY SEQUENCING

The TPA6136A2 has excellent noise and turn-on / turn-off pop performance. It uses an integrated click-and-pop suppression circuit to allow fast start-up and shutdown without generating any voltage transients at the output pins. Typical start-up time from shutdown is 5 ms.

DirectPath technology keeps the output dc voltage at 0 V even when the amplifier is powered up. The DirectPath technology together with the active pop-and-click suppression circuit eliminates audible transients during start up and shutdown.

Use input coupling capacitors to ensure inaudible turn-on pop. Activate the TPA6136A2 after all audio sources have been activated and their output voltages have settled. On power-down, deactivate the TPA6136A2 before deactivating the audio input source. The EN pin controls device shutdown: Set to 0.6 V or lower to deactivate the TPA6136A2; set to 1.3 V or higher to activate.

RF AND POWER SUPPLY NOISE IMMUNITY

The TPA6136A2 employs a new differential amplifier architecture to achieve high power supply noise rejection. Power supply noise is common in modern electronics. Although power supply noise frequencies are much higher than the 20 kHz audio band, signal modulation often falls in-band. This, in turn, modulates the supply voltage, allowing a coupling path into the audio amplifier. A common example is the 217 Hz GSM frame-rate buzz often heard from an active speaker when a cell phone is placed nearby during a phone call.

The TPA6136A2 has excellent rejection of power supply noise, preventing audio signal degradation.

CONSTANT MAXIMUM OUTPUT POWER AND ACOUSTIC SHOCK PREVENTION

Typically the output power increases with increasing supply voltage on an unregulated headphone amplifier. The TPA6136A2 maintains a constant output power independent of the supply voltage. Thus the design for prevention of acoustic shock (hearing damage due to exposure to a loud sound) is simplified since the output power will remain constant, independent of the supply voltage. This feature allows maximizing the audio signal at the lowest supply voltage.

INPUT COUPLING CAPACITORS

Input coupling capacitors block any dc bias from the audio source and ensure maximum dynamic range. Input coupling capacitors also minimize TPA6136A2 turn-on pop to an inaudible level.

The input capacitors are in series with TPA6136A2 internal input resistors, creating a high-pass filter. [Equation 3](#) calculates the high-pass filter corner frequency. The input impedance, R_{IN} , is dependent on device gain. Larger input capacitors decrease the corner frequency. See the Operating Characteristics table for input impedance values.

$$f_C = \frac{1}{2\pi R_{IN} C_{IN}} \quad (3)$$

For a given high-pass cutoff frequency, the minimum input coupling capacitor is found as:

$$C_{IN} = \frac{1}{2\pi f_C R_{IN}} \quad (4)$$

Example: Design for a 20 Hz corner frequency with a TPA6136A2 gain of +6 dB. The Operating Characteristics table gives R_{IN} as 13.2 k Ω . [Equation 4](#) shows the input coupling capacitors must be at least 0.6 μ F to achieve a 20 Hz high-pass corner frequency. Choose a 0.68 μ F standard value capacitor for each TPA6136A2 input (X5R material or better is required for best performance).

Input capacitors can be removed provided the TPA6136A2 inputs are driven differentially with less than $\pm 1 V_{RMS}$ and the common-mode voltage is within the input common-mode range of the amplifier. Without input capacitors turn-on pop performance may be degraded and should be evaluated in the system.

CHARGE PUMP FLYING CAPACITOR AND HPVSS CAPACITOR

The TPA6136A2 uses a built-in charge pump to generate a negative voltage supply for the headphone amplifiers. The charge pump flying capacitor connects between CPP and CPN. It transfers charge to generate the negative supply voltage. The HPVSS capacitor must be at least equal in value to the flying capacitor to allow maximum charge transfer. Use low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance) to maximize charge pump efficiency. Typical values are 1 μ F to 2.2 μ F for the HPVSS and flying capacitors. Although values down to 0.47 μ F can be used, total harmonic distortion (THD) will increase.

OPERATION WITH DACs AND CODECs AND INPUT RF NOISE REJECTION

When using amplifiers with CODECs and DACs, sometimes there is an increase in the output noise floor from the audio amplifier. This occurs when the output out-of-band noise of the CODEC/DAC folds back into the audio frequency due to the limited gain bandwidth product of the audio amplifier. Single-ended RF noise can also fold back into the audio band thus degrading the audio signal even further.

The TPA6136A2 has a built-in low-pass filter to reduce CODEC/DAC out-of-band noise and RF noise, that could fold back into the audio frequency.

POWER SUPPLY AND HPVDD DECOUPLING CAPACITORS AND CONNECTIONS

The TPA6136A2 DirectPath headphone amplifier requires adequate power supply decoupling to ensure that output noise and total harmonic distortion (THD) remain low. Use good low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance). Place a 2.2 μF capacitor within 5 mm of the VDD pin. Reducing the distance between the decoupling capacitor and VDD minimizes parasitic inductance and resistance, improving TPA6136A2 supply rejection performance. Use 0402 or smaller size capacitors if possible. Ensure that the ground connection of each of the capacitors has a minimum length return path to the device. Failure to properly decouple the TPA6136A2 may degrade audio or EMC performance.

For additional supply rejection, connect an additional 10 μF or higher value capacitor between VDD and ground. This will help filter lower frequency power supply noise. The high power supply rejection ratio (PSRR) of the TPA6136A2 makes the 10 μF capacitor unnecessary in most applications.

Connect a 2.2 μF capacitor between HPVDD and ground. This ensures the amplifier internal bias supply remains stable and maximizes headphone amplifier performance.

WARNING

DO NOT connect HPVDD directly to VDD or an external supply voltage. The voltage at HPVDD is generated internally. Connecting HPVDD to an external voltage can damage the device.

LAYOUT RECOMMENDATIONS

GND CONNECTIONS

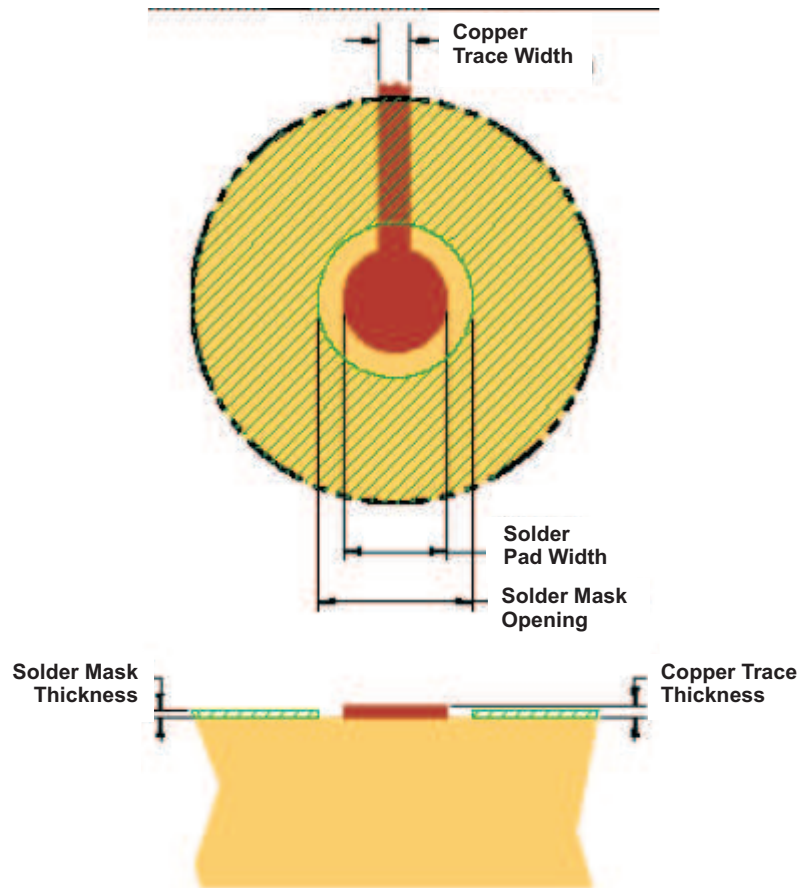
The SGND pin is an input reference and must be connected to the headphone ground connector pin. This ensures no turn-on pop and minimizes output offset voltage. Do not connect more than ± 0.3 V to SGND.

GND is a power ground. Connect supply decoupling capacitors for VDD, HPVDD, and HPVSS to GND.

BOARD LAYOUT

In making the pad size for the WCSP balls, it is recommended that the layout use non-solder-mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. [Figure 29](#) and [Table 2](#) shows the appropriate diameters for a WCSP layout.

For improved RF immunity it is recommended that all signal traces are routed in the middle layers of the multi-layer PCB. The top and bottom layers are used for the supply voltage plane and the GND plane.


Figure 29. Land Pattern Dimensions
Table 2. Land Pattern Dimensions^{(1) (2) (3) (4)}

SOLDER PAD DEFINITIONS	COPPER PAD	SOLDER MASK ⁽⁵⁾ OPENING	COPPER THICKNESS	STENCIL ^{(6) (7)} OPENING	STENCIL THICKNESS
Non-solder-mask defined (NSMD)	230 μm (+0.0, -25 μm)	310 μm (+0.0, -25 μm)	1 oz max (32 μm)	275 μm \times 275 μm Sq. (rounded corners)	100 μm thick

- (1) Circuit traces from NSMD defined PWB lands should be 75 μm to 100 μm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.
- (2) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application
- (3) Recommend solder paste is Type 3 or Type 4.
- (4) For a PWB using a Ni/Au surface finish, the gold thickness should be less 0,5 mm to avoid a reduction in thermal fatigue performance.
- (5) Solder mask thickness should be less than 20 μm on top of the copper circuit pattern
- (6) Best solder stencil performance is achieved using laser cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control.
- (7) Trace routing away from WCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

TRACE WIDTH

Recommended trace width at the solder balls is 75 μm to 100 μm to prevent solder wicking onto wider PCB traces. For high current pins (VDD, HPVDD, HPVSS, CPP, CPN, OUTL, and OUTR) of the TPA6136A2, use 100 μm trace widths at the solder balls and at least 500 μm PCB traces to ensure proper performance and output power for the device. For the remaining signals of the TPA6136A2, use 75 μm to 100 μm trace widths at the solder balls. The audio input pins (INL-, INL+, INR- and INR+) must run side-by-side to maximize common-mode noise cancellation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA6136A2YFFR	ACTIVE	DSBGA	YFF	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AOW1	Samples
TPA6136A2YFFT	ACTIVE	DSBGA	YFF	16	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AOW1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

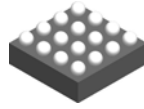
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6136A2YFFR	DSBGA	YFF	16	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1
TPA6136A2YFFT	DSBGA	YFF	16	250	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6136A2YFFR	DSBGA	YFF	16	3000	210.0	185.0	35.0
TPA6136A2YFFT	DSBGA	YFF	16	250	182.0	182.0	20.0

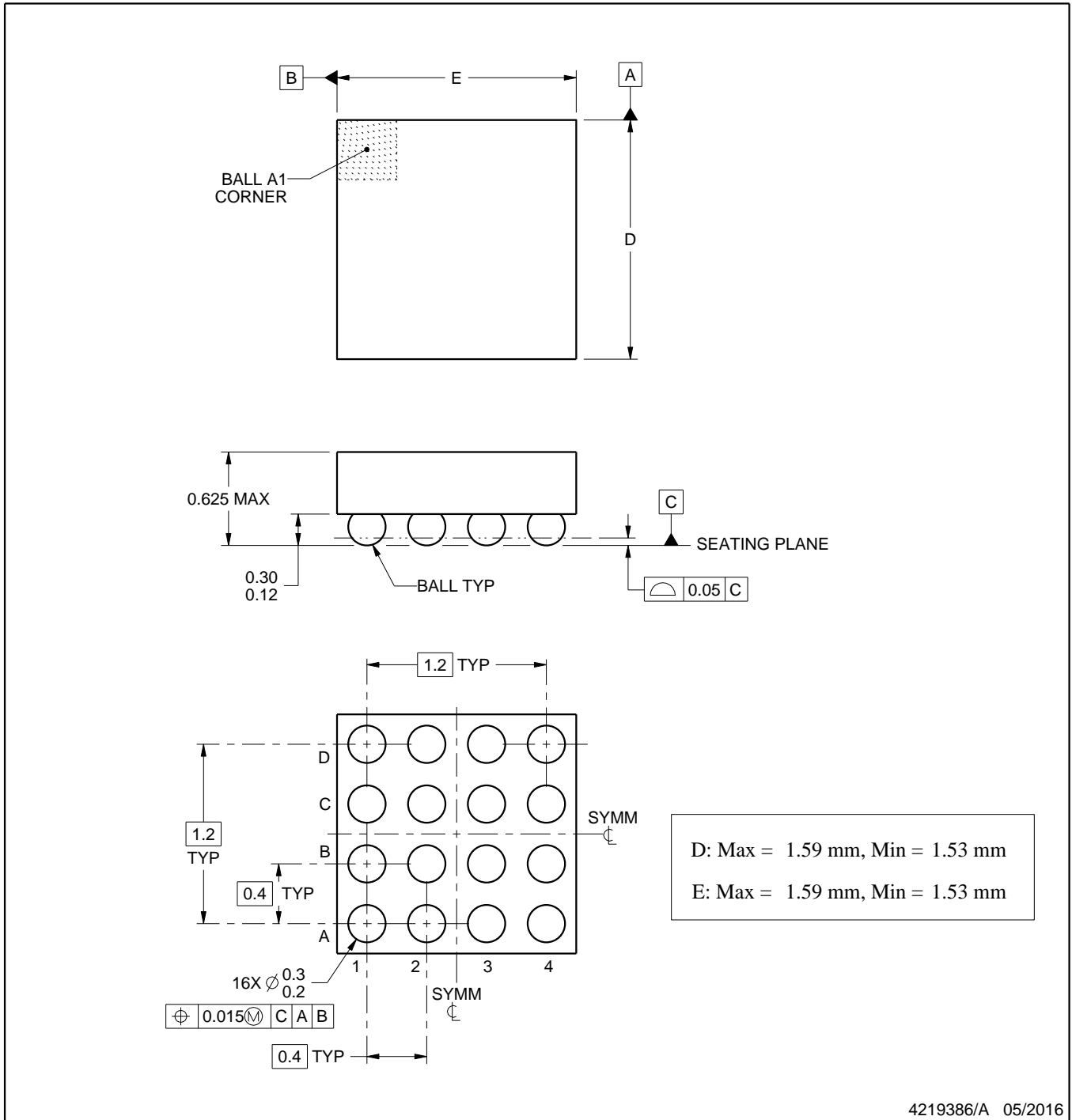
YFF0016



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



4219386/A 05/2016

NOTES:

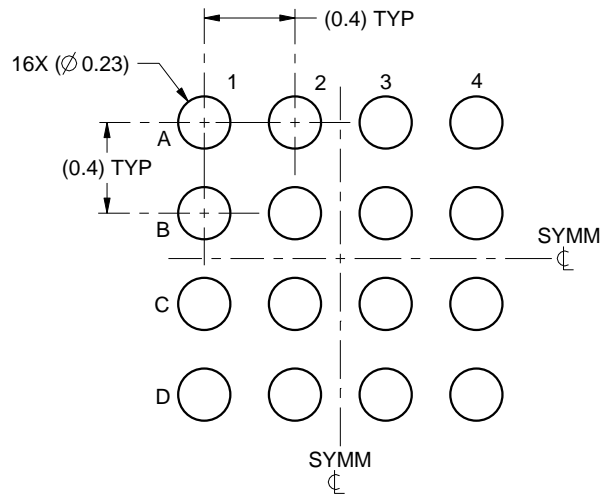
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

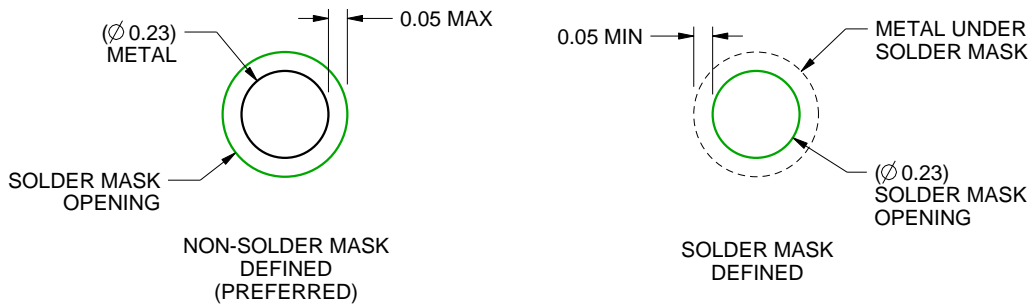
YFF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4219386/A 05/2016

NOTES: (continued)

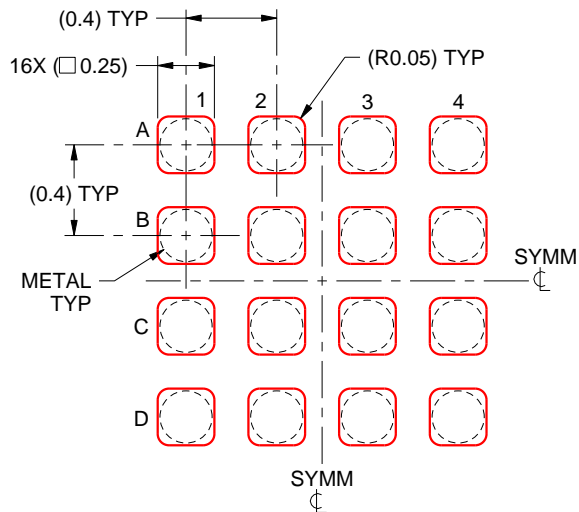
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219386/A 05/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2022，德州仪器 (TI) 公司