具有 VBUS LDO 稳压器的TPS6612x集成灌电流

1 特性

- 集成 22mΩ（典型值），32V 耐压 NFET 4V 至 22V 灌电流路径，高达 5A
- 内置软启动可限制浪涌电流
- 集成高电压 VBUS LDO 稳压器（每种器件类型为 3.3V 或 5.0V）
- 通过引脚配置的可选 VBUS 过压保护。
- 系统电源和 VBUS 欠压保护
- 过热保护
- 反向电流保护
- 具有抗尖峰脉冲故障报告功能的故障引脚
- 小型 WCSP 封装，无需 HDI。

2 应用

- 台式计算机/主板
- 标准笔记本电脑
- Chromebook 和 WOA
- 集线站
- 端口/线缆适配器和加密狗

3 说明

TPS6612x 包含一个集成 4V 至 22V 灌电流电源路径。该电源路径都支持过热保护和反向电流保护。VBUS 具有过压保护，其电平由可选的外部电阻分压器设置。如果不需要过压保护，可以通过接地 OVP 终端来禁用。TPS6612x 支持显示过热事件的故障引脚。

TPS6612x 系列还支持高电压 VBUS LDO 稳压器（每种器件类型为 3.3V 或 5V），可用于在电池电量耗尽的情况下为设备和其他系统组件供电。将 TPS66120 调节至 3.3V，将 TPS66121 调节至 5V。

器件信息(1)

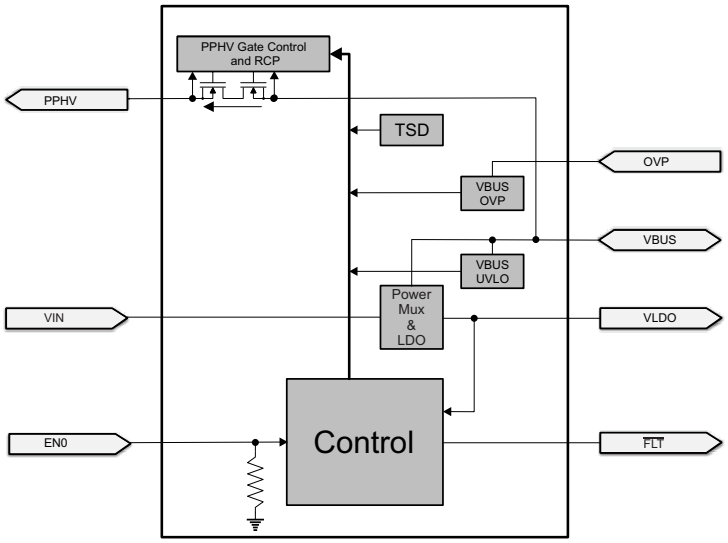
器件型号	封装	封装尺寸（标称值）
TPS66120	WCSP (28)	1.606mm x 2.806mm
TPS66121		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

功能表

EN0	器件状态
0	灌电流路径禁用
1	灌电流路径启用

TPS6612x 方框图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

Changes from Revision A (September 2019) to Revision B **Page**

- 将“预告信息”更改为“生产数据” ... 1

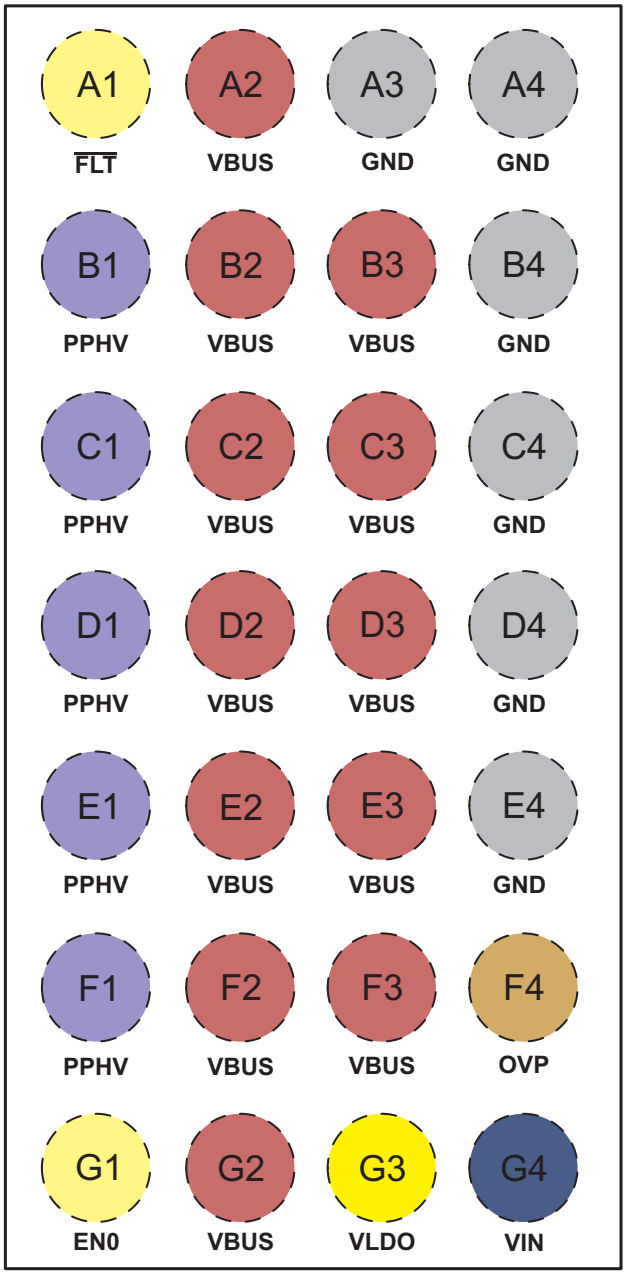
Changes from Original (August 2019) to Revision A **Page**

- 更新了附带链接的应用部分 ... 1
- 已添加 Typical Characteristics section ... 9
- 已添加 Application Curves section ... 22

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5 Pin Configuration and Functions

TPS6612x YBG Package
28-Pin WCSP
Top View



Pin Functions

Pin		I/O	Reset State	Description
Name	No.			
PPHV	B1, C1, D1, E1, F1	Power	Off	HV System Supply from VBUS. Bypass with capacitance CPPHV to GND.
VBUS	A2, B2, B3, C2, C3, D2, D3, E2, E3, F2, F3, G2	Power	-	4V to 20V nominal input supply to PPHV. Bypass with capacitance CVBUS to GND.

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Pin Functions (continued)

Pin		I/O	Reset State	Description
Name	No.			
VIN	G4	Power	-	Device input supply. Bypass with capacitance CVIN to GND.
VLDO	G3	Power	-	VIN supply or VBUS LDO regulated supply output from power multipexer. Bypass with capacitance CVLDO to GND.
GND	A3, A4, B4, C4, D4, E4	Ground	-	Ground. Connect all pins to ground plane.
OVP	F4	Analog	-	Selects VBUS OVP. Tie pin to VBUS resistor divider output to set desired VBUS OVP level. Tie pin to GND to remove VBUS OVP function.
EN0	G1	Digital Input	Pull-down	Enable PPHV sink path. Internal pull-down.
$\overline{FLT}$	A1	Digital OUtput	Hi-Z	Fault Output Indicator. Active low. This pin is a true open-drain (no PMOS). Float pin when unused.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Terminal voltage range (2)	EN0(3), $\overline{FLT}$, VIN, VLDO	–0.3	6.2	V
Terminal voltage range (2)	OVP	–0.3	VBUS	V
Terminal voltage range (2)	VBUS, power path disabled (stand off voltage)	–0.5	32	V
Terminal voltage range (2)	VBUS, power path enabled(4)	–0.5	26	V
Terminal voltage range (2)	PPHV	–0.3	26	V
Terminal positive source current	VLDO sourced from VBUS VLDO		Internally limited	mA
	VLDO sourced from VIN		50	mA
Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.
(3) EN0 has an internal voltage clamp and may be driven above the absolute maximium voltage rating up to EN_CLAMP maximum specification if current is limited to less than 100µA.
(4) For VBUS, a TVS protection with a break down voltage falling between the Recommended and Absolute maximum ratings is recommended, such as the TVS2200.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{VIN}	Input voltage range (1)	VIN, TPS66120 only.	2.85	3.6	V
		VIN, TPS66121 only.	4.5	5.5	V
V_{PPHV}	Output voltage range (1)	PPHV	0	22	V
V_{VBUS}	Input voltage range (1)	VBUS when sinking	4	22	V
V_{EN}	Input voltage range (1)	EN0	0	5.5	V
$V_{\overline{FLT}}$	Output voltage range (1)	$\overline{FLT}$	0	5.5	V

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the ground plane of the board.

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Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
I_{O_PPHV}	Continuous current from VBUS to PPHV	T_J = 105℃		4	A
		T_J = 100℃		5	A
I_{O_VLDO}	Output current from VBUS LDO			30	mA
R_{IREF}	External resistor current limit reference	75kΩ ±1% overall tolerance	74.25	75.75	kΩ
T_J	Operating junction temperature		–10	125	°C
RR_PPHV	Maximum ramp rate on PPHV input supply		–2	2	V/µs
RR_VBUS	Maximum ramp rate on VBUS input supply		–2	2	V/µs
RR_VIN	Maximum ramp rate on VIN input supply			30	mV/µs

6.4 Recommended Supply Load Capacitance

over operating free-air temperature range (unless otherwise noted)

PARAMETER(1)		MIN	TYP	MAX	UNIT
CVIN	Capacitance on VIN	1			µF
CVLDO	Capacitance on VLDO	2.5	4.7	10	µF
CVBUS	Capacitance on VBUS	1		10	µF
CPPHV	Capacitance present on PPHV(2)	1	47	100	µF

(1) Capacitance values do not include any derating factors. For example, if 5.0 µF is required and the external capacitor value reduces by 50% at the required operating voltage, then the required external capacitor value would be 10 µF.
(2) This capacitance represents the system side load capacitance that may be seen by the device e.g. from a typical battery charging system. Discrete capacitance is not required for proper operation.

6.5 Thermal Information

THERMAL METRIC(1)		TPS6612x YBG (WCSP) 28 PINS	UNIT
$R_{\theta JA,EFF}$	Effective Junction-to-ambient thermal resistance(2)	44.3	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.7	°C/W
$\psi_{JB,EFF}$	Effective Junction-to-board characterization parameter(2)	14.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Models based on typical application layout.

6.6 PPHV Power Switch Characteristics

Operating under these conditions unless otherwise noted: -10 ℃ ≤ T_J ≤ 125 ℃, 2.85V ≤ V_{VIN} ≤ 5.5V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PPHV}	Resistance from PPHV to VBUS	I_{LOAD} = 1 A, T_J = 25 ℃, SNK state.		22	26	mΩ
		I_{LOAD} = 1 A, -10 ℃ ≤ T_J ≤ 125 ℃, SNK state.		22	45	mΩ
V_{PPHV_RCP}	Maximum voltage due to reverse current during RCP response.	SNK state, V_{VBUS} = 5.5V, ramp V_{PPHV} from 5.5V to 21V at 100 V/ms, C_{VBUS} = 10µF, measure V_{VBUS}			5.8	V
V_{PPHV_OVP}	Maximum voltage rise due to reverse current during VBUS OVP response.	SNK state, V_{VBUS} = 5.5V, set V_{OVP} = 6V, ramp V_{VBUS} from 5.5V to 21V at 100 V/ms, C_{PPHV} = 4.7µF, measure V_{PPHV}			6.2	V

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PPHV Power Switch Characteristics (continued)

Operating under these conditions unless otherwise noted: -10 ℃ ≤ T_J ≤ 125 ℃, 2.85V ≤ V_{VIN} ≤ 5.5V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{RCP_THRES_PPHV}$	Reverse current blocking voltage threshold for PPHV switch		2	6	10	mV
SS	Soft-start slew rate	Transition from DISABLED state to SNK state, V_{VBUS} = 5V, C_{PPHV} = 100µF. Measure slew rate on PPHV.	0.2		0.6	V/ms
t_{ON_PPHV}	PPHV enable time including Soft-start.	R_{PPHV} = 100Ω, V_{VBUS} = 5V, C_{PPHV} = 100 µF. Transition from DISABLED state to SNK state, V_{PPHV} at 90% of final value.	9	15	29	ms
t_{OFF_PPHV}	PPHV disable time.	R_{PPHV} = 100Ω, V_{VBUS} = 5V, C_{PPHV} = 4.7 µF. Transition from SNK state to DISABLED state, V_{PPHV} falls to 4.5V.	0.9	2.2	4.3	ms

6.7 Power Path Supervisory

Operating under these conditions unless otherwise noted: -10 ℃ ≤ T_J ≤ 125 ℃, 2.85V ≤ V_{VIN} ≤ 5.5V, R_{IREF} = 75 kΩ ±1% overall tolerance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UV_VIN_R	Undervoltage threshold for VIN. VBUS LDO disables when threshold reached.	VIN rising, TPS66120 only.	2.45		2.75	V
		VIN rising, TPS66121 only.	3.89		4.40	V
UV_VIN_F	Undervoltage threshold for VIN. Device resets.	VIN falling, TPS66120 only.	2.35		2.65	V
		VIN falling, TPS66121 only.	3.79		4.30	V
UVH_VIN	Undervoltage hysteresis for VIN.			100		mV
UV_VBUS_R	Undervoltage threshold for VBUS. PPHV switch disabled unitl threshold reached.	VBUS rising	3.35		3.75	V
UV_VBUS_F	Undervoltage threshold for VBUS. PPHV switch disables when threshold reached.	VBUS falling	3.15		3.55	V
UVH_VBUS	Undervoltage hysteresis for VBUS			200		mV
OVP_REF	OVP reference voltage.		0.93	1	1.07	V
VFWD_DROP_VIN	Forward voltage drop across VIN to VLDO switch	I_{VLDO} = 35 mA			90	mV
t_{VIN_STABLE}	When VIN is above UV_VIN_R for this duration, VIN is considered valid. If device is being powered by VBUS LDO, it will then switch to VIN supply and VBUS LDO will be disabled.		5		15	ms

6.8 VBUS LDO Characteristics

Operating under these conditions unless otherwise noted: -10 ℃ ≤ T_J ≤ 125 ℃, 2.85V ≤ V_{VIN} ≤ 5.5V, R_{IREF} = 75 kΩ ±1% overall tolerance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_VBUS_LDO_3V	Output voltage of VBUS LDO	For TPS66120: VIN = 0V, VBUS ≥ 3.8V, 0 ≤ I_VBUS_LDO ≤ 30mA	3.07	3.3	3.53	V
V_VBUS_LDO_5V	Output voltage of VBUS LDO	For TPS66121: VIN = 0V, VBUS ≥ 5.5V, 0 ≤ I_VBUS_LDO ≤ 30mA	4.65	5.0	5.35	V
VDO_VBUS_LDO_3V	Drop out voltage of VDD LDO	For TPS66120: VIN = 0V, VBUS = 3.135 V, I_VBUS_LDO = 30 mA			0.5	V
VDO_VBUS_LDO_5V	Drop out voltage of VDD LDO	For TPS66121: VIN= 0V, VBUS = 4.75V, I_VBUS_LDO = 30 mA			0.5	V
ILIMIT_VBUS_LDO	Current limit VBUS LDO.	VBUS = 5.5V, VIN= 0V, VLDO = 0V	50		100	mA

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VBUS LDO Characteristics (continued)

Operating under these conditions unless otherwise noted: -10 ℃ ≤ T_J ≤ 125 ℃, 2.85V ≤ V_{VIN} ≤ 5.5V, R_{IREF} = 75 kΩ ±1% overall tolerance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{EN_VBUS_LDO}$	Turn-on time of VBUS LDO.	For TPS66120: I_VBUS_LDO = 30mA, CVLDO = 4.7 µF, VIN = 0V. Ramp V_{VBUS} from 0 to 5V at ≥50V/ms. Measure from VBUS = 4.5V to VLDO = 3V.			1.2	ms
		For TPS66121: I_VBUS_LDO = 30mA, CVLDO = 4.7 µF, VIN = 0V. Ramp V_{VBUS} from 0 to 7.5V at ≥50V/ms. Measure from VBUS = 7V to VLDO = 4.5V.			1.2	ms

6.9 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TSD_PPHV_R	Thermal Shutdown Temperature of the PPHV power path.	Temperature rising	128	150	172	°C
TSD_PPHV_F	Thermal Shutdown Temperature of the PPHV power path.	Temperature falling	115	140	165	°C
TSDH_PPHV	Thermal Shutdown hysteresis of the PPHV power path.			10		°C
TSD_MAIN_R	Thermal Shutdown Temperature of the entire device.	Temperature rising	140	160	178	°C
TSD_MAIN_F	Thermal Shutdown Temperature of the entire device.	Temperature falling	120	140	160	°C
TSDH_MAIN	Thermal Shutdown hysteresis of the entire device.			20		°C

6.10 Input-output (I/O) Characteristics

Operating under these conditions unless otherwise noted: -10 ℃ ≤ T_J ≤ 125 ℃, 2.85 V ≤ V_{VIN} ≤ 5.5V, R_{IREF} = 75 kΩ ±1% overall tolerance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN_Vt+	Positive going input-threshold voltage, % of VLDO	VLDO = 2.85 - 5.5V	40		70	%
EN_Vt-	Negative going input-threshold voltage, % of VLDO	VLDO = 2.85 - 5.5V	30		60	%
EN_HYS	Input hysteresis voltage, % of VLDO	VLDO = 2.85 - 5.5V		10		%
EN_RPD	Pull-down resistance EN pin.	Measured with pin voltage V_{EN} = 3.3V	500	650	800	kΩ
EN_CLAMP	Voltage clamp on EN pin.	I_{EN} = 100 µA		6	7.1	V
FLT_VOL	Output Low Voltage, $\overline{FLT}$ pin	I_{OL} = 2mA, $\overline{FLT}$ driven low.			0.4	V
FLT_ILKG	Leakage Current, $\overline{FLT}$ pin	$\overline{FLT}$ not driven low.	–1		1	µA
t_{H_FLT}	Time $\overline{FLT}$ pin remains asserted low.		4	10	16	ms
t_{DG_EN}	Enable deglitch filter. Pulses on EN0 < $t_{DG_EN(MIN)}$ are not propagated to the control logic. Pulses on EN0 > $t_{DG_EN(MAX)}$ are propagated to the control logic. Pulses on EN0 ≥ $t_{DG_EN(MIN)}$ and ≤ $t_{DG_EN(MAX)}$ may or may not propagate to the control logic.		78		242	µs

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6.11 Power Consumption Characteristics

Operating under these conditions unless otherwise noted: -10 ℃ ≤ T_J ≤ 85 ℃, 2.85V ≤ V_{VIN} ≤ 5.5V, R_{IREF} = 75 kΩ ±1% overall tolerance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{VIN_DISABLE}$	Current consumed by VIN(1)	VIN = 3.3V, VBUS = 0V, PPHV = 0V, DISABLED state. Measure I_{VIN}. TPS66120 only.			19	27	µA
		VIN = 5V, VBUS = 0V, PPHV = 0V, DISABLED state. Measure I_{VIN}. TPS66121 only.			25	36	µA
I_{VIN_SNK}	Current consumed by VIN(1)	VIN = 3.3V, SNK state. Measure I_{VIN}. TPS66120 only.	VBUS = 5.5V/22V		130		µA
		VIN = 5V, SNK state. Measure I_{VIN}. TPS66121 only.	VBUS = 5.5V/22V		215		µA
I_{SD_VBUS}	Current consumed by VBUS(1)	VIN = 3.3V, PPHV= 0V, DISABLED state. Measure I_{VBUS}. TPS66120 only.	VBUS = 5.5V		12	26	µA
			VBUS = 22V		34		µA
		VIN = 5V, PPHV= 0V, DISABLED state. Measure I_{VBUS}. TPS66121 only.	VBUS = 5.5V		8		µA
			VBUS = 22V		30		µA
$I_{SD_VBUS_LDO}$	Current consumed by VBUS(1)	VIN = 0V, PPHV= 0V, DISABLED state. Measure $I_{VBUS.}$	VBUS = 5.5V		45		µA
			VBUS = 22V		68		µA
$I_{SD_VBUS_LDO}$	Current consumed by VBUS(1)	VIN = 0V, PPHV= 0V, DISABLED state. Measure $I_{VBUS.}$	VBUS = 5.5V		45		µA
			VBUS = 22V		69		µA
I_{ACT_VBUS}	Current consumed by VBUS(1)	VIN = 3.3V, SNK state. Measure I_{VBUS}. TPS66120 only.	VBUS = 5.5V		325		µA
			VBUS = 22V		360		µA
		VIN = 5V, SNK state. Measure I_{VBUS}. TPS66121 only.	VBUS = 5.5V		342		µA
			VBUS = 22V		377		µA
V_{OC_VBUS}	Open circuit voltage, VBUS	PPHV = 22V, DISABLED state, no DC loading on VBUS. Measure V_{VBUS} under steady state conditions.				0.8	V
V_{OC_PPHV}	Open circuit voltage, PPHV	VBUS = 22V, DISABLED state, no DC loading on PPHV. Measure V_{PPHV} under steady state conditions.				0.8	V

(1) Measured with EN0 set to GND or VLDO levels as required for the respective state.

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6.12 Typical Characteristics

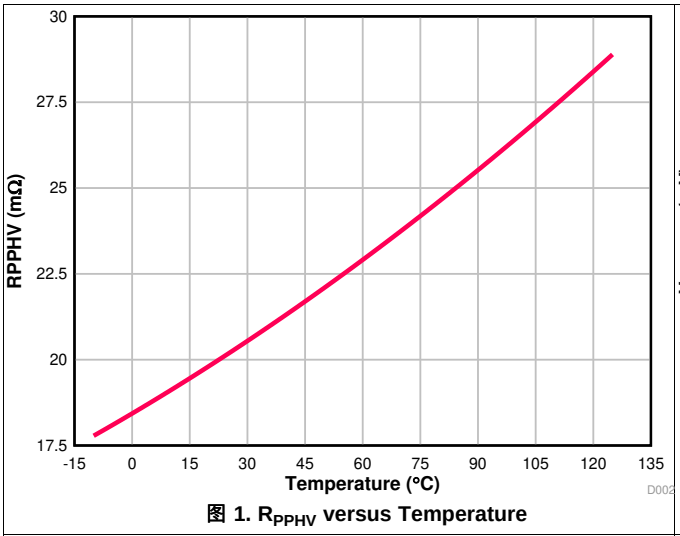


图 1. R_{PPHV} versus Temperature

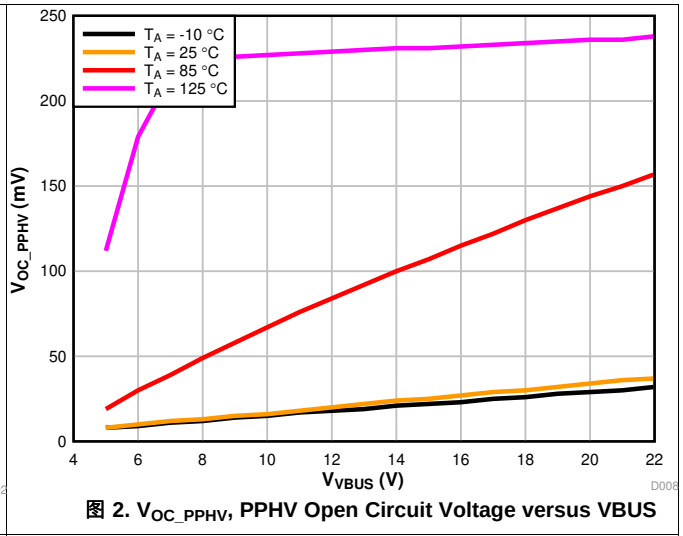


图 2. V_{OC_PPHV}, PPHV Open Circuit Voltage versus VBUS

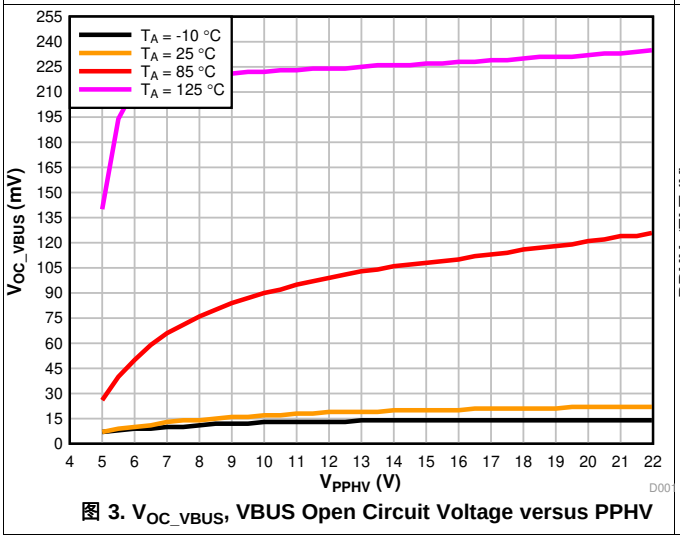


图 3. V_{OC_VBUS}, VBUS Open Circuit Voltage versus PPHV

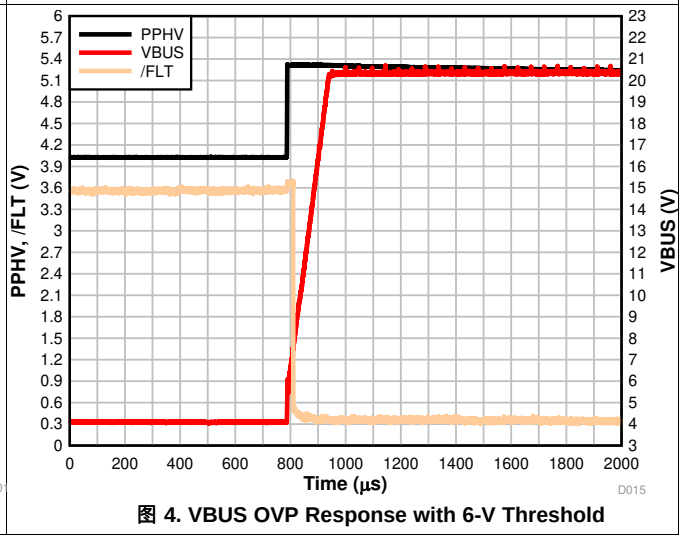


图 4. VBUS OVP Response with 6-V Threshold

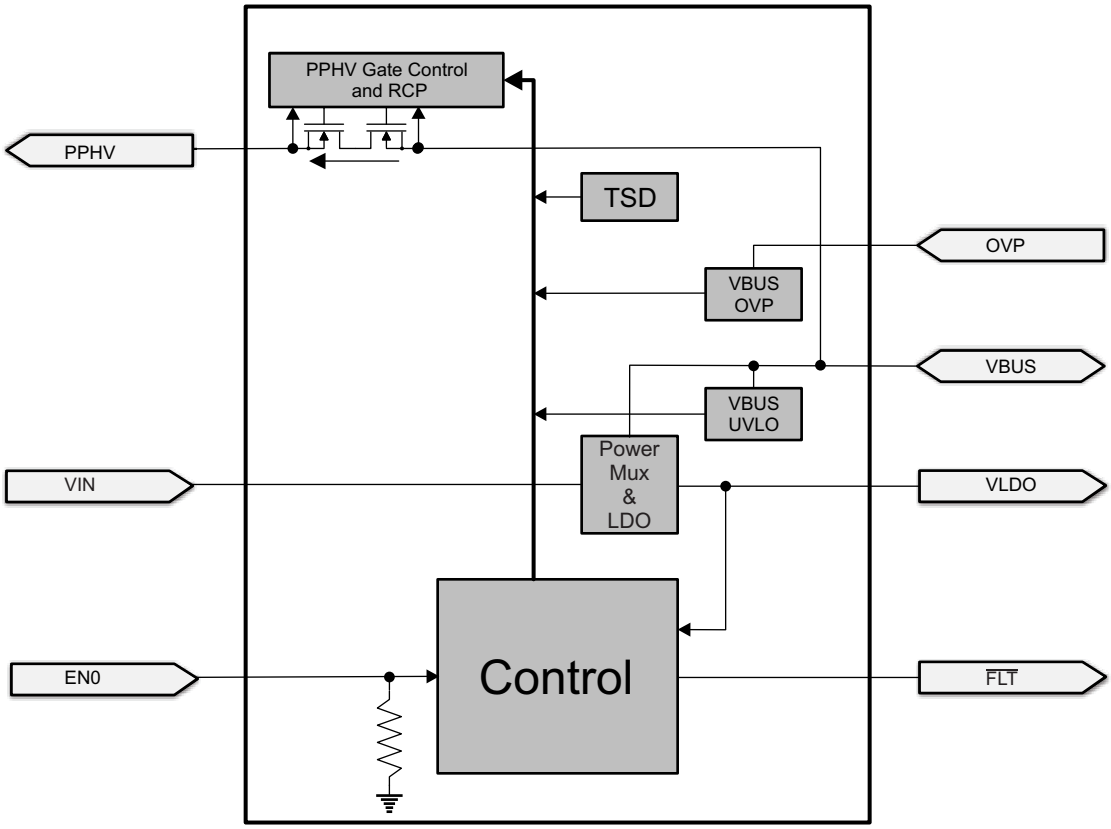
7 Detailed Description

7.1 Overview

The TPS6612x is a fully featured integrated Sink power path with a high voltage VBUS LDO voltage regulator. The Sink power path can support up to 5 A at 20 V controlled by a general-purpose I/O. The Sink power path includes soft-start to minimize in-rush currents, overtemperature protection, reverse-current protection, undervoltage protection, and an optional overvoltage protection configured in the application. See the *20-V Sink (PPHV Power Path)* section.

The VBUS low dropout voltage regulator may be used in systems that require power during dead battery conditions and can provide up to 30 mA to the system via the VLDO pin. Once VIN power is available, VLDO pin power is switched from the VBUS LDO regulator to the VIN pin. The TPS66120 devices VBUS LDO regulator nominally supplies 3.3 V where the TPS66121 device VBUS LDO regulator nominally supplies 5 V. See the *Power Management and Supervisory* section.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 20-V Sink (PPHV Power Path)

The PPHV path is a Sink only path, providing power from the VBUS terminal to the PPHV terminal when enabled. The PPHV power path uses two back-to-back N-channel MOSFETs, and blocks current in both directions when the power path is disabled.

7.3.1.1 PPHV Soft Start

The TPS6612x PPHV power path has soft start circuitry to control in-rush current when the PPHV power path is enabled. DC loading should be minimized during soft start since the PPHV path may experience high power dissipation especially at higher VBUS voltages. This may lead to a PPHV overtemperature protection event.

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Feature Description (接下页)

7.3.1.2 PPHV Reverse Current Protection (RCP)

When the PPHV power path is enabled, the RCP circuitry monitors the voltage across the path. If the RCP monitor detects V_{PPHV} - V_{VBUS} ≥ $V_{RCP_THRES_PPHV}$, the PPHV path will be disabled preventing additional current flow from PPHV to VBUS. The power path will be completely disabled and remain disabled as long as the RCP condition persists. After the RCP event, the PPHV path will automatically re-enable. $\overline{FLT}$ is not asserted when a reverse current protection event occurs on the PPHV path.

7.3.2 Overtemperature Protection

The PPHV power path has an integrated temperature sensor to protect it from excessive heating. When the sensor in the path detects an overtemperature condition, the PPHV path will be automatically disabled (if enabled) and cannot be enabled until the overtemperature condition has been removed. $\overline{FLT}$ is asserted when an overtemperature event occurs.

In addition, the device has an integrated main temperature sensor. When the sensor detects an overtemperature condition, the PPHV power pathand the VBUS LDO of the device are completely disabled until the overtemperature condition has been removed.

7.3.3 VBUS Overvoltage Protection (OVP)

TPS6612x supports overvoltage protection on the VBUS terminal. When the voltage detected on OVP exceeds a set level, the PPHV power path will automatically be disabled (if enabled), and will remain disabled until the OVP event is removed. $\overline{FLT}$ is asserted when an overvoltage event occurs. The VBUS OVP threshold may be set using a resistor divider from VBUS to GND, whose divider output is connected to the OVP terminal as shown in 图 5. 表 1 shows resistor divider settings for common USB Power Delivery fixed voltage supply contracts along with the resulting nominal OVP thresholds. These thresholds may be adjusted based on desired margins for a given application. If VBUS OVP is not required or needs to be disabled, the OVP terminal may be tied or driven to GND as shown in 图 6. Lastly, as one example implementation, the OVP threshold may be controlled dynamically using outputs from a PD controller or microcontroller as shown in 图 7. By selecting each output, different VBUS OVP threshold settings are possible.

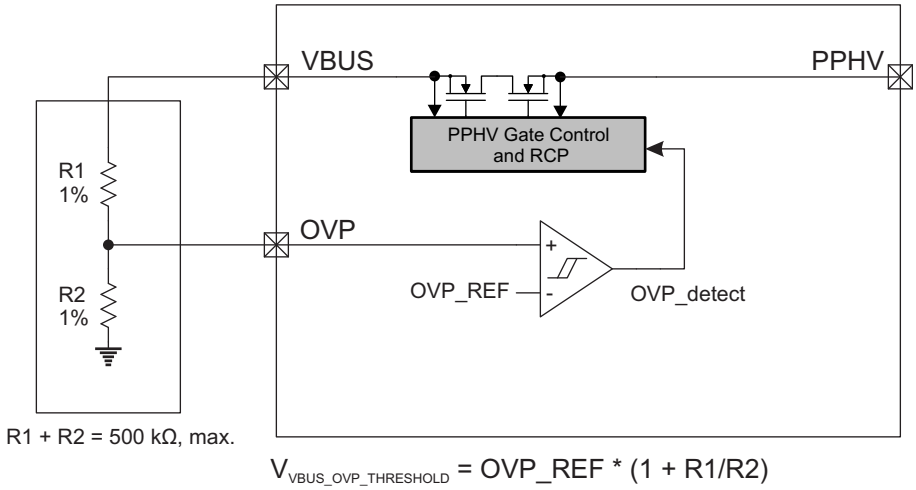


图 5. VBUS OVP Threshold Set by External Resistor Divider

表 1. Typical External Resistor Divider Settings

PD Fixed Contract	R1, kΩ	R2, kΩ	Nominal VBUS OVP Threshold, V
5 V	102	20	6.1
9 V	182	20	10.1
15 V	309	20	16.5
20 V	432	20	22.6

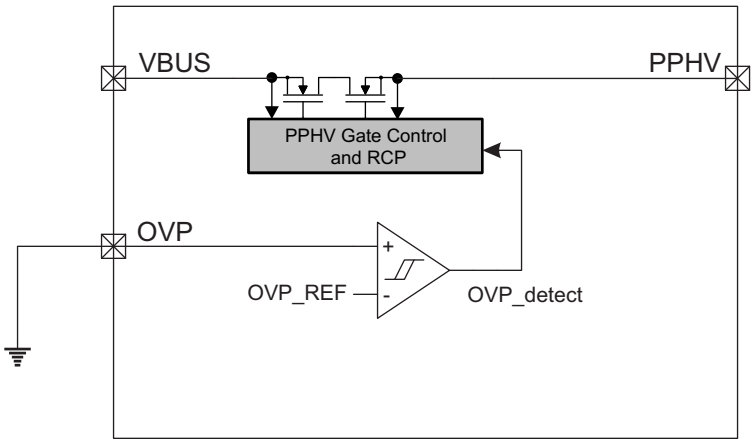


图 6. VBUS OVP Disabled

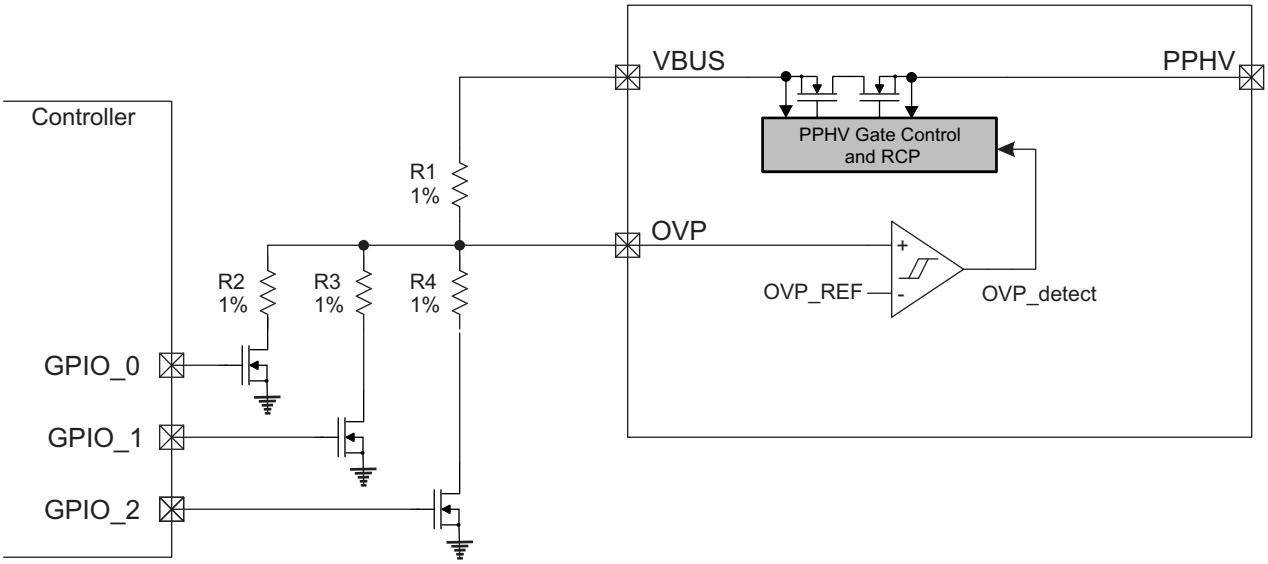


图 7. Selectable VBUS OVP Thresholds

7.3.4 Power Management and Supervisory

The TPS6612x Power Management block receives power from VIN or VBUS and generates voltages to provide power to the TPS6612x internal circuitry, as well as, provides power to VLDO. The power supply management and supervisory block is shown in 图 8.

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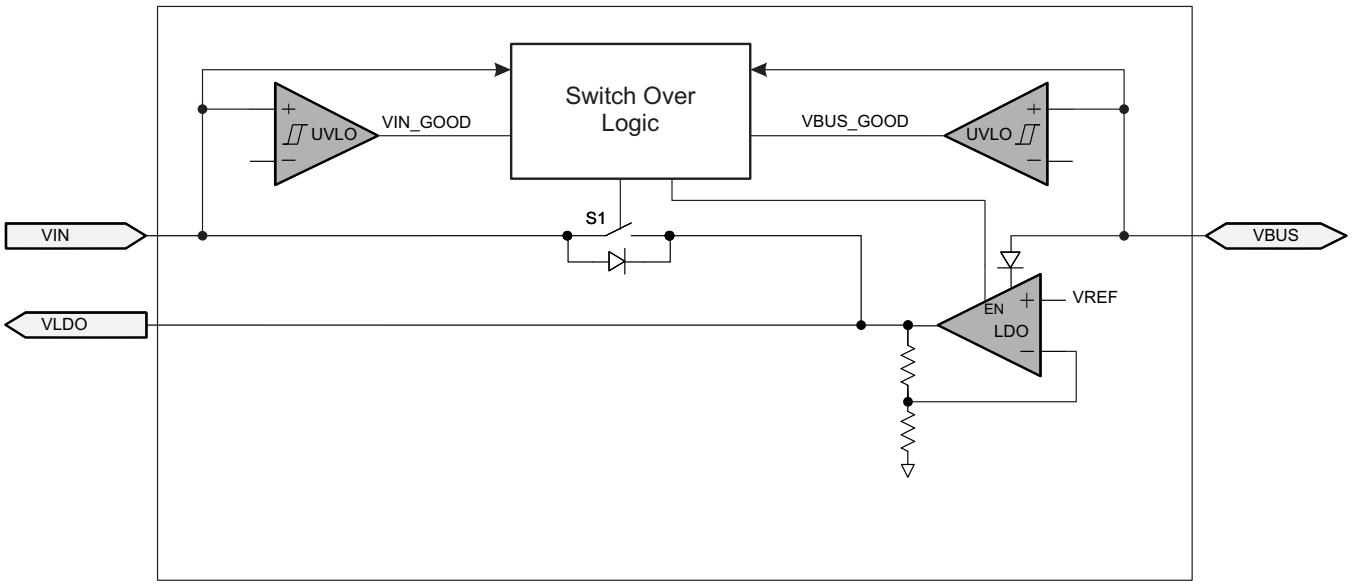


图 8. Power Management and Supervisory

The VLDO terminal may be powered from either VIN or VBUS. The normal power supply input is VIN. When VIN is present, S1 is closed and current flows from VIN to VLDO and the VBUS LDO is disabled. When VIN power is unavailable, as in a dead battery condition, the VBUS LDO will be automatically enabled when VBUS is present, and the VLDO terminal is powered by the VBUS LDO. The Switch Over Logic provides the decision making capability to choose VIN or VBUS power, depending on the state of these voltages (based on their respective UVLO comparators) and their relative levels to each other.

7.3.4.1 Supply Connections

图 9 shows the TPS66120 VIN being supplied from a 3.3-V supply. The VLDO output may or may not be used to supply other circuitry in the application, for example a PD Controller. During dead battery, the internal 3.3-V VBUS LDO provides power to the TPS66120 and the VLDO output. Once VIN input supply becomes available, the VBUS LDO is disabled and VIN provides power to the VLDO output.

图 10 shows the TPS66121 VIN being supplied from a 5-V supply. The VLDO output may or may not be used to supply power to external circuitry. During dead battery, the internal 5-V VBUS LDO provides power to the TPS66121 and the VLDO output. Once VIN input supply becomes available, the VBUS LDO is disabled and VIN provides power to the VLDO output.

Another option is to power the TPS66120 from the VBUS LDO only as shown in 图 11. Since VIN is tied to GND, power to the TPS66120 is provided by the 3.3-V VBUS LDO when VBUS power is present. The VLDO output may be used optionally to supply power to external circuitry.

Similarly, 图 12 shows the TPS66121 being powered from the VBUS LDO only. Since VIN is tied to GND, power to the TPS66121 is provided by the 5-V VBUS LDO when VBUS power is present. The VLDO output may be used optionally to supply power to external circuitry.

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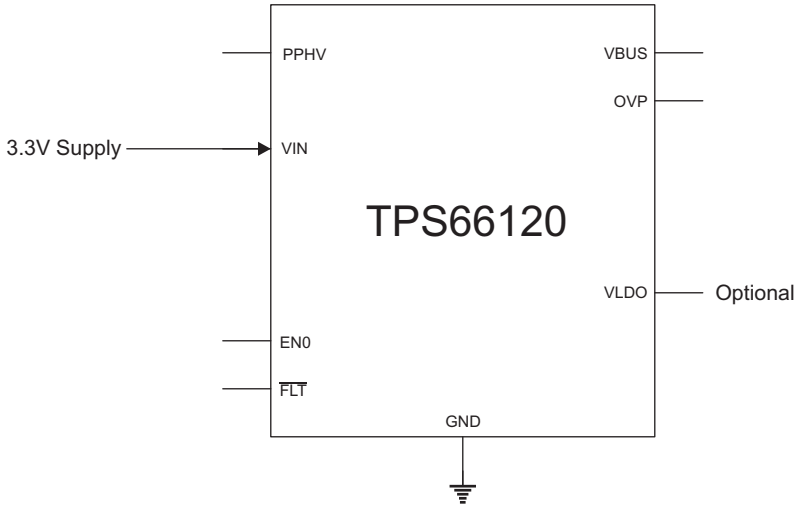


图 9. TPS66120 VIN 3.3-V Supply

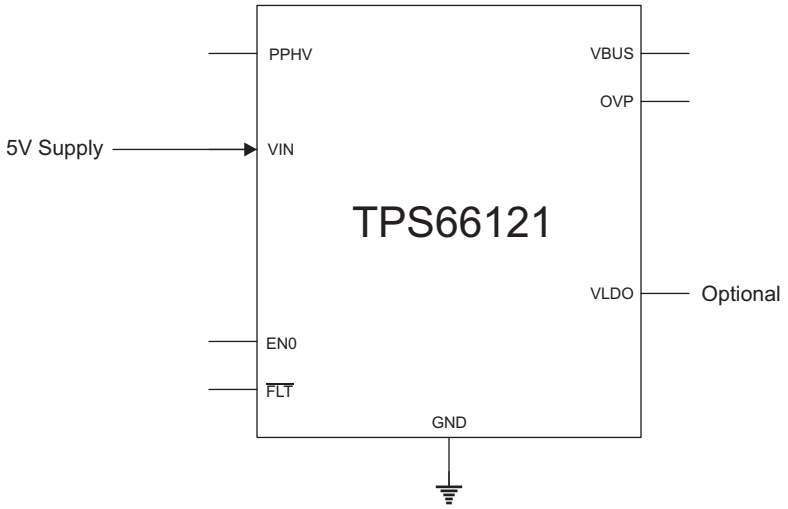


图 10. TPS66121 VIN 5-V Supply

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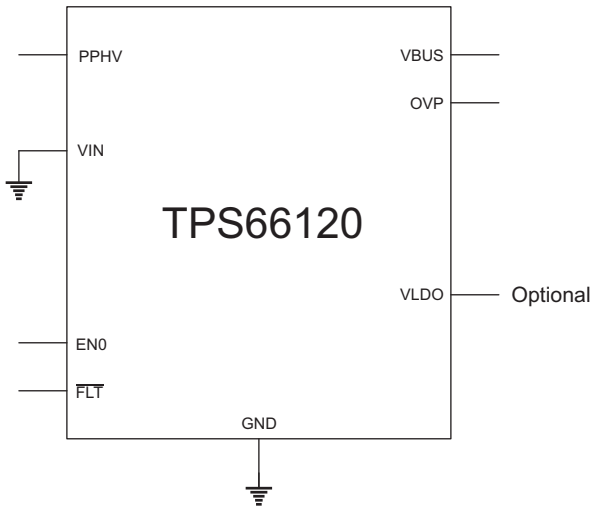


图 11. TPS66120 VBUS Powered

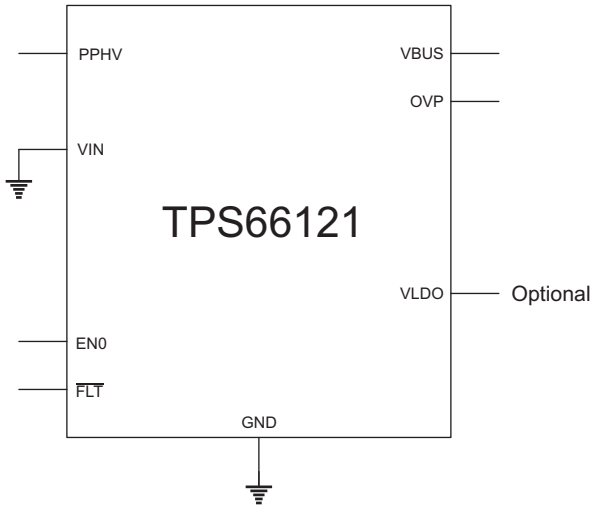
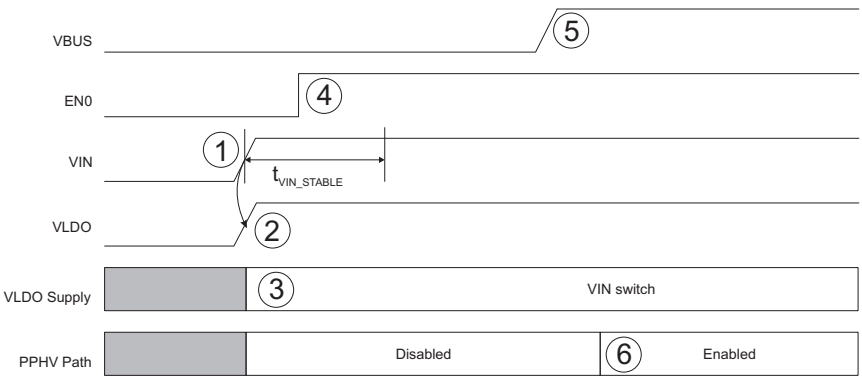


图 12. TPS66121 VBUS Powered

7.3.4.2 Power Up Sequences

7.3.4.2.1 Normal Power Up

图 13 shows a typical power up sequence. During normal power up, VIN supplies power to the TPS6612x. In this case, VBUS remains powered down. It is assumed a PD Controller is controlling the TPS6612x, and Sink operation is being requested.



1. Both the VBUS and VIN supplies are powered down. VIN supply begins to rise.

2. VLDO terminal begins to rise.

3. VLDO supplied by VIN via switch S1. VBUS LDO remains disabled.

4. PD Controller requests Sink path to be enabled. Since VIN supply has not been above its UVLO threshold for t_{VIN_STABLE}, Sink path remains disabled. In addtion, VBUS is not above its UVLO switch threshold, which also keeps the Sink path disabled.

5. VBUS rises.

6. VIN supply remained above its UVLO threshold for t_{VIN_STABLE} and VBUS is above its UVLO threshold. The Sink path enables. VBUS LDO remains disabled since VIN supply is available

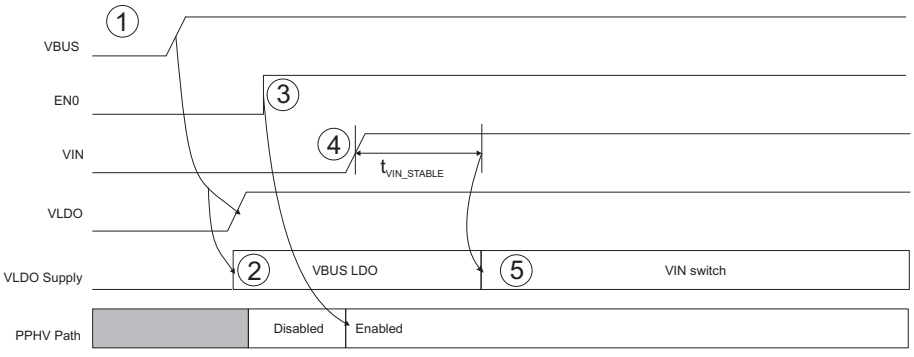
图 13. Normal Power Up Sequence

7.3.4.2.2 Dead Battery Operation

图 14 shows the typical power up sequence during a dead battery condition. During a dead battery condition, the TPS6612x is internally powered by the VBUS LDO. The VBUS LDO may be used to supply a limited amount of current for use in the system during dead battery, such as supplying power to a PD controller. In this case, it is assumed the VLDO terminal is providing power to a PD controller that is controlling the TPS6612x. Once VIN is stable, the VLDO terminal switches from being supplied by the VBUS LDO to being supplied by the VIN terminal, and the VBUS LDO is automatically disabled. The switch over process is completely seamless.

注

Switching from VBUS LDO operation to VIN operation is seamless and no device reset will occur. When switching from VIN power to VBUS LDO operation, the switch over circuitry will attempt to switch over to the VBUS LDO, however it is not assured that the VLDO level will be maintained above the VLDO UVLO threshold. In this case, a device reset may or may not occur.



1. Device is in dead battery condition. PD controller advertises as a Sink. Upon connection to a Source, VBUS begins to rise.

2. VBUS LDO is selected by the power management logic and VLDO begins to rise.

3. PD Controller negotiates a contract (may be 5V or higher) and asserts EN0 to turn on the PPHV Sink path in order to charge the system.

4. System begins to charge and VIN begins to rise. VIN passes its UVLO threshold.

5. If VIN supply remains above its UVLO threshold for t_{VIN_STABLE}, VBUS LDO is disabled and VLDO is switched over to be supplied by VIN via switch S1.

图 14. Dead Battery Power Up Sequence

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7.4 Device Functional Modes

7.4.1 State Transitions

EN0 is used by the application to control the state of the device. 图 15 shows the supported state transitions.

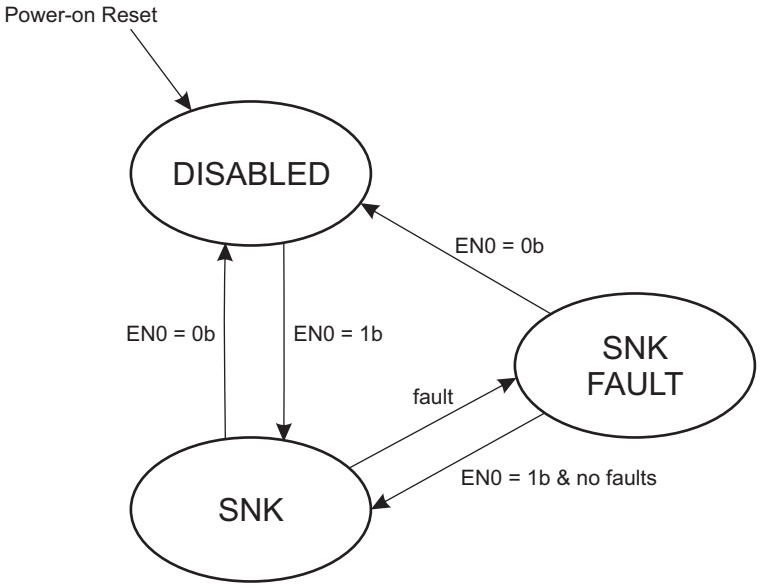


图 15. TPS6612x State Diagram

7.4.1.1 DISABLED State

In the DISABLED state, EN0 = 0. While in the DISABLED state:

- PPHV power path is disabled
- PPHV overtemperature, reverse-current, and VBUS overvoltage protections are disabled
- VIN and VBUS undervoltage lockout are enabled
- SNK state if (EN1 = 0) and (EN0 = 1) and (VBUS UVLO event not detected)

7.4.1.2 SNK State

In the SNK state, EN0 = 1. While in the SNK state:

- PPHV power path is enabled
- PPHV overtemperature, VBUS overvoltage (if OVP terminal not grounded) and reverse-current protections are enabled
- VIN and VBUS undervoltage lockout are enabled
- DISABLED state if:
  - (EN1 = 0) and (EN0 = 0)
- SNK FAULT state if:
  - VBUS OVP (if OVP terminal not grounded) event detected -or-
  - PPHV TSD event detected

7.4.2 SNK FAULT State

The SNK FAULT state is entered when any PPHV fault event is detected. Upon entering the SNK FAULT state, the PPHV power path is disabled. The following transitions are possible from the SNK FAULT state:

- DISABLED state if:
  - (EN0 = 0)
- SNK state if:
  - (EN0 = 1) -and-

Device Functional Modes (接下页)

– PPHV TSD, VBUS OVP (if OVP terminal not grounded) events are not detected

7.4.3 Device Functional Mode Summary

表 2 summarizes the functional modes for the TPS6612x family. As shown, the enabling and disabling of the Sink is dependent upon the voltage present on VBUS, as well as, the current device state.

表 2. TPS6612x Device Functional Modes(1)

EN0	VIN	V_{VBUS}	$\overline{FLT}$	Device State	Sink Path
0	≥ UV_VIN	X	Hi-Z	DISABLED	Disabled Safety engaged.
1	≥ UV_VIN	≥ UV_VBUS	Hi-Z	SNK	Enabled RCP, OVT enabled
			Hi-Z	SNK FAULT	Enabled with Blocking RCP event.
			L	SNK FAULT	Disabled OVP(2) or OVT event.
		< UV_VBUS	Hi-Z	SNK FAULT	Disabled VBUS UVLO event.
X	< UV_VIN	< UV_VBUS	Hi-Z	DISABLED	Disabled Safety engaged.
0	< UV_VIN	≥ UV_VBUS	Hi-Z	DISABLED	Disabled Safety engaged.
1	< UV_VIN	≥ UV_VBUS(3)	Hi-Z	SNK	Enabled RCP, OVT enabled
			Hi-Z	SNK FAULT	Enabled with Blocking RCP event.
			L	SNK FAULT	Disabled OVP(2) or OVT event.
		< UV_VBUS(3)	Hi-Z	SNK FAULT	Disabled VBUS UVLO event.

(1) X: do-not-care.
(2) When OVP function used and VBUS exceeds OVP threshold, $V_{VBUS_OVP_THRESHOLD}$.
(3) If VIN supply is not available, then VIN may be tied to GND. In this case VLDO is supplying power to the device.

7.4.4 Enabling the PPHV Sink Path

The timing diagram of enabling the PPHV Sink path is shown in 图 16.

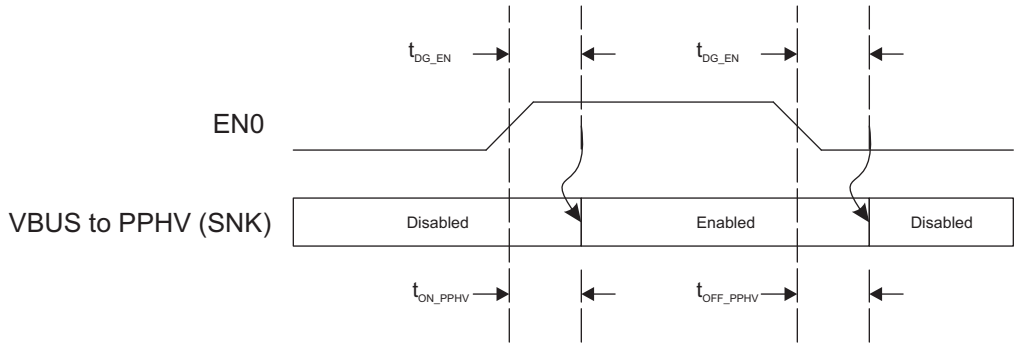


图 16. Enabling the PPHV Sink Path

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7.4.5 Faults

The TPS6612x includes a fault pin, $\overline{FLT}$. The $\overline{FLT}$ pin is an open-drain output and requires an external pull-up resistor. If the $\overline{FLT}$ pin is not required, it may be tied to GND or left floating. The $\overline{FLT}$ pin will be asserted low only under certain conditions and not all fault conditions will assert the $\overline{FLT}$ pin, see 表 3. If the $\overline{FLT}$ pin is asserted, it will remain asserted for a minimum of tHOLD_FLT regardless if the fault condition is removed. After t_{HOLD_FLT}, if all fault conditions have surpassed, the $\overline{FLT}$ pin is released.

7.4.5.1 Fault Types

表 3 summarizes the various fault types available and when the $\overline{FLT}$ shall be asserted.

表 3. Fault Types

Fault Name	Fault	$\overline{FLT}$	Description
VBUS_UVLO	VBUS undervoltage Lockout	Hi-Z	If VBUS supply is below the VBUS UVLO threshold, the PPHV path is disabled automatically if enabled or remains disabled. If the SNK state is selected to be entered, the device will remain in the DISABLED state until the UVLO event is removed. If the SNK state has been entered successfully and a UVLO event occurs, the PPHV path is disabled automatically.
VBUS_OVP(1)	VBUS overvoltage Protection	Low	If the SNK state is selected to be entered or device currently is in the SNK state and the VBUS supply rises above the VBUS OVP threshold, the PPHV path is disabled automatically and the $\overline{FLT}$ pin will be asserted.
VBUS_RCP	VBUS Reverse-Current Protection	Hi-Z	If the SNK state is selected to be entered or device currently is in the SNK state and a reverse-current condition is detected, the PPHV path is disabled automatically, but the $\overline{FLT}$ is not asserted.. If the reverse-current condition is removed, the PPHV path will automatically re-enable.
PPHV_OVT	PPHV overtemperature Protection	Low	If the SNK state is selected to be entered or device currently is in the SNK state and the local temperature of PPHV power path exceeds TSD_PPHV_R, the PPHV path is disabled automatically and the $\overline{FLT}$ pin will be asserted. PPHV power path will remain disabled until temperature falls below TSD_PPHV_F.

(1) OVP terminal is not connected to GND.

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8 Application and Implementation

> **注**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The typical applications of the TPS6612x include chargers, notebooks, tablets, ultra-books, dongles and any other product supporting USB Type-C and/or USB-PD as a power source or power sink. The typical applications outlined in the following sections detail a Fully-Featured USB Type-C using a single 5-V supply and another using a separate 3.3-V supply.

8.2 Typical Application

图 17 shows a USB Type-C single port design using a power delivery controller. For this system, a single 5-V supply in the system is used to supply power to the external load switch, as well as, the connector VCONN power. The VIN terminal of the TPS66121 is tied to GND and the TPS66121 is powered by the VBUS LDO once VBUS is present. In addition, the TPS66121 supplies power to the 5-V supply of the PD controller via the VLDO output. The PPHV integrated power path provides power to the system and battery charger from VBUS when the TPS66121 Sink path is enabled. An external 5-V load switch is shown to provide power to VBUS when system is configured as a Source.

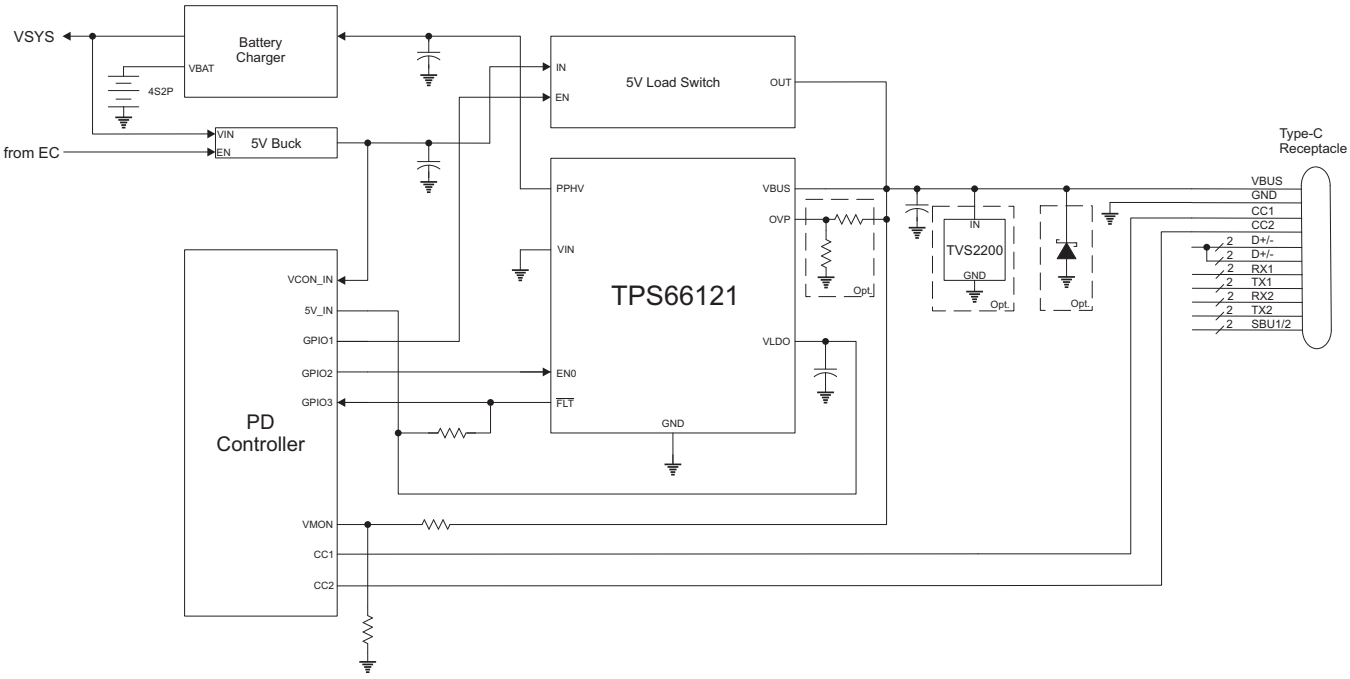


图 17. Single Port Type-C PD Port Using a 5-V Supply.

8.2.1 Design Requirements

For a single port notebook application, 表 4 lists the input voltage requirements and expected current capabilities.

表 4. Single-Port Notebook Application Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE(S)	POWER PATH DIRECTION
5-V Load Switch Voltage and Current Capabilities	5V/3A	Source from 5-V load switch to VBUS

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Typical Application (接下页)

表 4. Single-Port Notebook Application Design Parameters (接下页)

DESIGN PARAMETERS	EXAMPLE VALUE(S)	POWER PATH DIRECTION
VCON_IN Input Voltage and Current Capabilities	5V/300mA (1.5W)	Source to VCONN
VBUS Input Voltage and Current Capabilities	5V/3A, 9V/3A, 15V/3A, 20V/3A	Sink from VBUS to PPHV
5V_IN Input Voltage and Current Capabilities	4.5-5.5V/30mA	5-V PD Controller Supply
3V_IN Input Voltage and Current Capabilities	3.0-3.6V/30mA	3.3-V PD Controller Supply

8.2.2 Detailed Design Procedure

8.2.2.1 External VLDO Capacitor (CVLDO)

For all capacitances, the DC operating voltage must be factored into the derating of ceramic capacitors. Generally, the effective capacitance is 35-50% of the nominal capacitance with voltage applied. Assuming VLDO = 5 V, and a minimum derated capacitance of 2.5 uF, a 10-V rated 4.7-uF capacitor is sufficient.

8.2.2.2 PPHV, VBUS Power Path Capacitance

The PPHV power path is a Sink. The capacitance on the PPHV shown in 图 17 represents capacitance of the charger sub-system. In a typical application, this capacitance can be in the range of 47 uF up to 100 uF, far exceeding the 1-uF minimum specification for the TPS6612x, so no external capacitance is required to meet this requirement in most cases. As per the PD Specification, the total capacitance on VBUS should be maximum 10 uF at connection.

The TPS6612x PPHV power path has soft start circuitry to control in-rush current when the PPHV power path is enabled. DC loading should be minimized during soft start since the PPHV path may experience high power dissipation especially at higher VBUS voltages. This in turn may lead to a PPHV overtemperature protection event.

8.2.2.3 VBUS TVS Protection (Optional)

It is recommended that each VBUS port in the system have TVS protection to protect the VBUS terminal. Inductive ringing during momentary disconnects and reconnects due to mechanical vibration or plug removal while sinking large current loads may cause large peak voltages to be present on the VBUS terminal that may exceed the absolute maximums of the TPS6612x. Under such events, the TVS2200 clamps the VBUS terminal and prevents VBUS from exceeding the maximum specification. The TVS trip point should be chosen to be safely above the normal operating ranges of the device. For this case, it is assumed VBUS voltage contracts are less than 22-V maximum which is below the minimum breakdown voltage of the TVS2200. The maximum clamping voltage of 28.3 V of the TVS2200 is sufficient to protect the VBUS terminal of the TPS6612x.

8.2.2.4 VBUS Schottky Diode Protection (Optional)

To prevent the possibility of large ground currents into the TPS6612x during sudden disconnects because of inductive effects in a cable, it is recommended that a Schottky diode be placed from VBUS to GND. The NSR20F30NXT5G or comparable device is recommended.

8.2.2.5 VBUS Overvoltage Protection (Optional)

VBUS Overvoltage Protection (OVP) is optional. If VBUS OVP is not required, then the OVP terminal should be tied to ground as shown in 图 6. VBUS OVP is used to detect voltages on VBUS that exceed a set threshold. Upon detection, the PPHV power path is disabled quickly to help protect components connected downstream of the PPHV terminal. It should be noted that VBUS OVP is not a replacement for VBUS TVS protection which is protecting the VBUS terminal itself.

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The VBUS OVP threshold is set by a resistor divider from the VBUS terminal to ground as shown in 图 5. For this design, R1 and R2 are fixed values to provide VBUS OVP protection at the highest voltage contract level. Using R1 = 432-kΩ and R2 =20-kΩ sets a nominal VBUS OVP threshold of 22.6 V. For some applications, it may be desirable to dynamically change the VBUS OVP level based on the negotiated power contract. One possible way is shown in 图 7. In this case, the PD controller via GPIO, selects the proper divider ratio to set the VBUS OVP threshold based on the negotiated voltage contract level.

8.2.2.6 Dead Battery Support

The TPS6612x integrates a high-voltage VBUS LDO that can be used to supply power to a PD Controller and other supporting circuitry when only VBUS power is available, such as in a dead battery condition. As shown in 图 17 the TPS66121 VLDO output supplies power to the PD Controller's 5V_IN supply. During a dead battery condition, the PD Controller presents its Type-C RPD pull-downs on the CC1 and CC2 lines. Upon connection to a Type-C/PD Source, 5 V is provided to VBUS from the Source partner which powers the TPS6612x. The 5-V VBUS LDO is enabled and provides power to the PD Controller. Once powered, the PD Controller can decide to enable the TPS6612x PPHV Sink path by asserting EN0 high and use the 5-V VBUS to charge the battery or it may choose to negotiate a higher voltage contract first. Either way, once the contract is negotiated, the PD Controller will enable the PPHV Sink path and charge the system. Once the system is sufficiently charged, the VIN terminal will rise and will exceed the VIN UVLO threshold. If VIN remains above the UVLO threshold for t_{VIN_STABLE}, VLDO will be supplied from VIN and the VBUS LDO will be disabled.

8.2.3 Application Curves

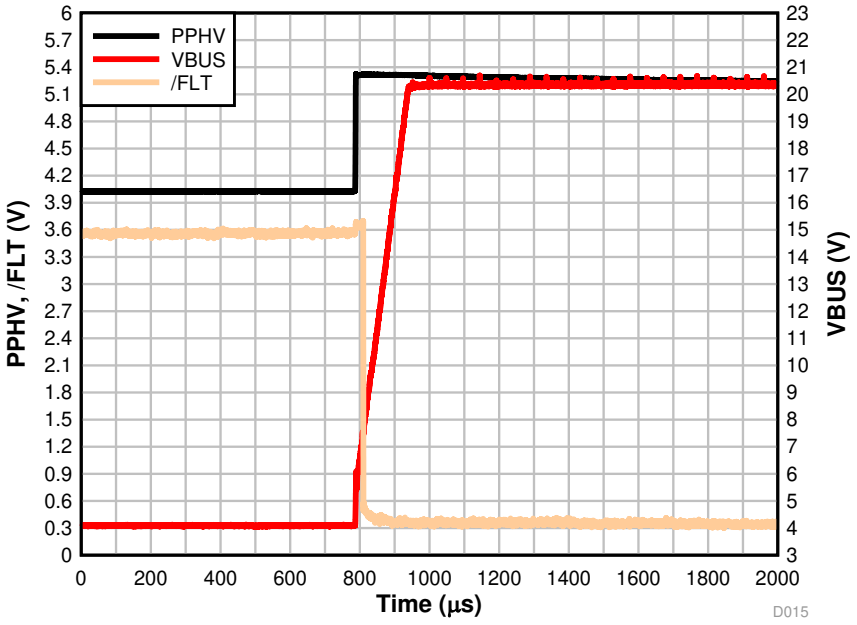


图 18. VBUS OVP Response with 6-V Threshold

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9 Power Supply Recommendations

The device has a single input supply, VIN. A 1-uF or higher ceramic bypass capacitor between VIN and GND is recommended as close to the VIN as possible for local noise decoupling.

USB Specification Revisions 2.0 and 3.1 require VBUS voltage at the connector to be between 4.75 V to 5.5 V. Depending on layout and routing from supply to the connector the voltage droop on VBUS has to be tightly controlled. Locate the input supply close to the device. For all applications, a maximum 10-μF ceramic bypass capacitor between VBUS and GND is recommended as close to the Type-C connector of the device as possible for local noise decoupling. The input power supply should be rated higher than the current limit set to avoid voltage droops during overcurrent and short-circuit conditions.

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10 Layout

10.1 Layout Guidelines

1. PPHV and VBUS traces must be as short and wide as possible to accommodate for high currents.
2. A ceramic 4.7 uF (X7R/X5R) 10-V rated capacitor is placed as close as possible to the VLDO terminal of the TPS6612x.

10.2 Layout Example

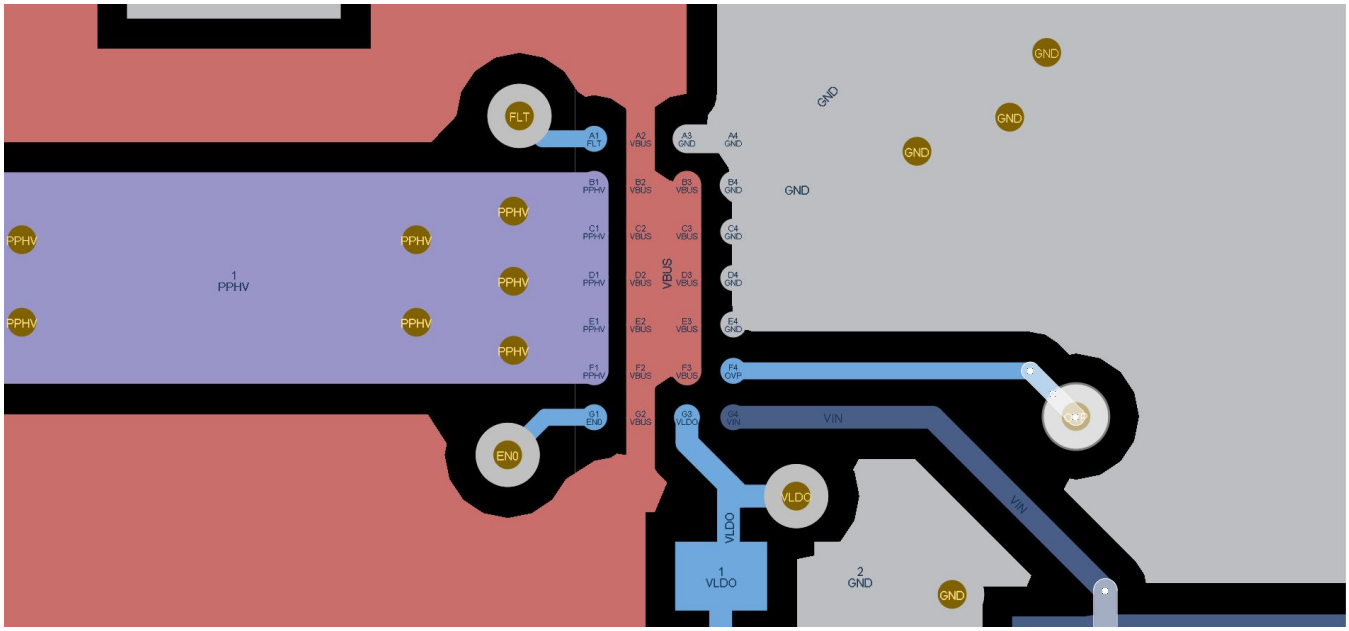


图 19. Layout Example

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11 器件和文档支持

11.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 5. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
TPS66120	单击此处	单击此处	单击此处	单击此处	单击此处
TPS66121	单击此处	单击此处	单击此处	单击此处	单击此处

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 商标

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11.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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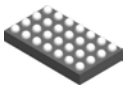
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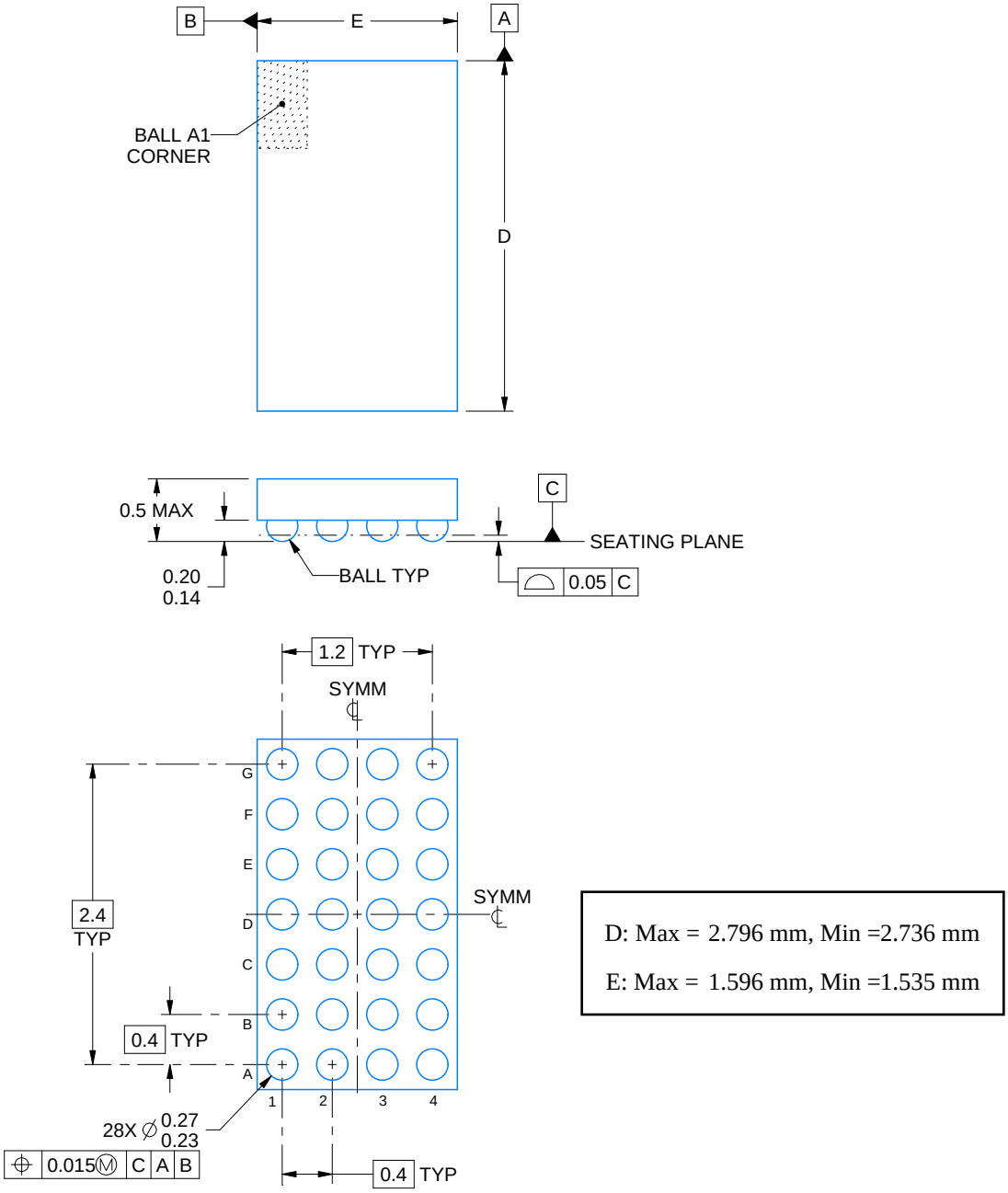
PACKAGE OUTLINE

YBG0028



DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 2.796 mm, Min =2.736 mm

E: Max = 1.596 mm, Min =1.535 mm

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NOTES:

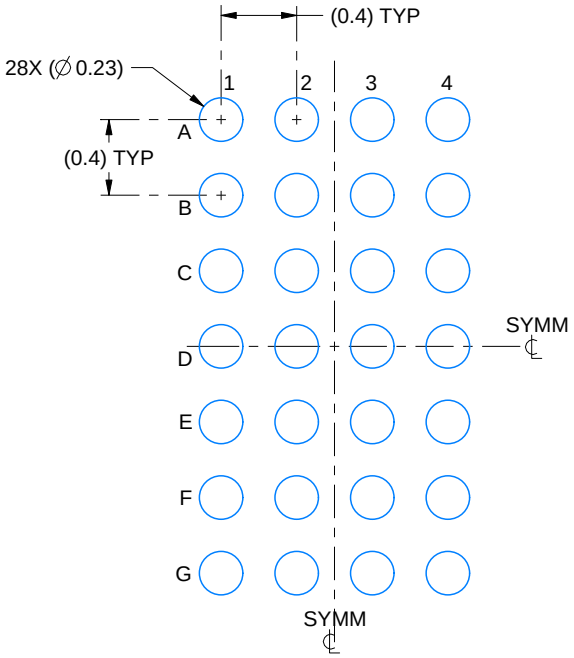
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

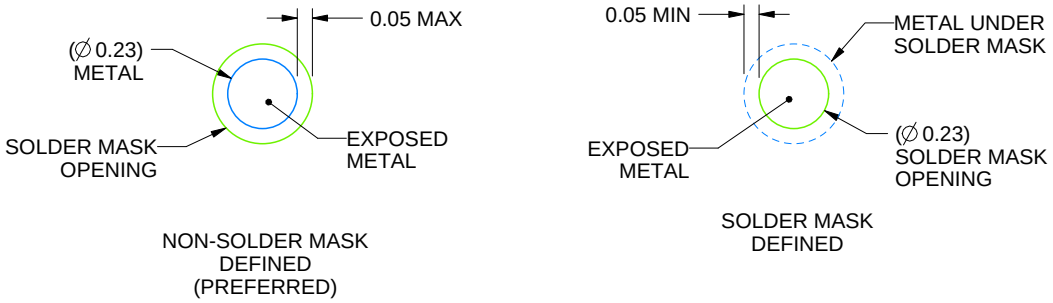
YBG0028

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

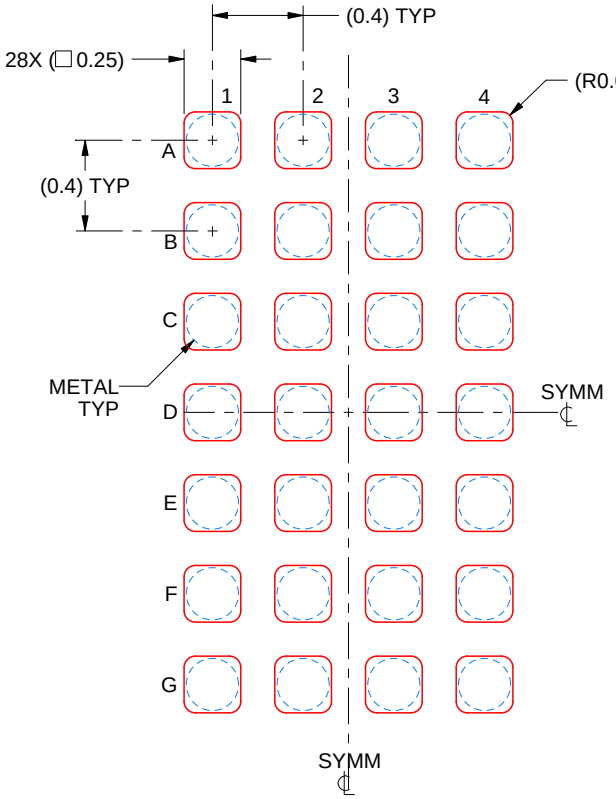


SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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