CD4027B CMOS 双路 J-K 触发器

1 特性

- 置位/复位功能
- 静态触发器运行 – 以*高*或*低*时钟电平无限期地保持状态
- 中速运行 – 在 10V 下具有 16MHz（典型值）的时钟切换速度
- 标准化对称输出特性
- 针对 20V 下的静态电流进行了 100% 测试
- 在全封装温度范围内，18V 时的最大输入电流为 1μA；18V 和 25°C 时为 100nA
- 噪声容限（在全封装温度范围内）：
  - V_{DD} = 5V 时为 1V
  - V_{DD} = 10V 时为 2V
  - V_{DD} = 15V 时为 2.5V
- 5V、10V 和 15V 参数额定值
- 符合 JEDEC 第 138 号暂行标准，这是*用于描述“B”系列 CMOS 器件的标准规范*

2 应用

- 寄存器、计数器和控制电路

3 说明

CD4027B 是一款包含两个相同互补对称 J-K 触发器的单片芯片集成电路。每个触发器都提供了单独的 J、K、置位、复位和时钟输入信号，以及缓冲 Q 和 $\overline{Q}$ 输出信号。借助此输入/输出，可实现与 RCA-CD4013B 双路 D 型触发器的兼容操作。

CD4027B 适用于执行控制、寄存器和切换功能。J 和 K 输入端的逻辑电平以及内部自操纵控制每个触发器的状态；触发器状态的变化与时钟脉冲的正向转换同步。置位和复位功能独立于时钟，并在置位或复位输入端出现高电平信号时启动。

CD4027B 型采用 16 引脚气密性双列直插式陶瓷封装（后缀为 F3A）、16 引脚双列直插式塑料封装（后缀为 E）、16 引脚小外形封装（后缀为 M、M96、MT 和 NSR）和 16 引脚薄型紧缩小外形封装（后缀为 PW 和 PWR）。

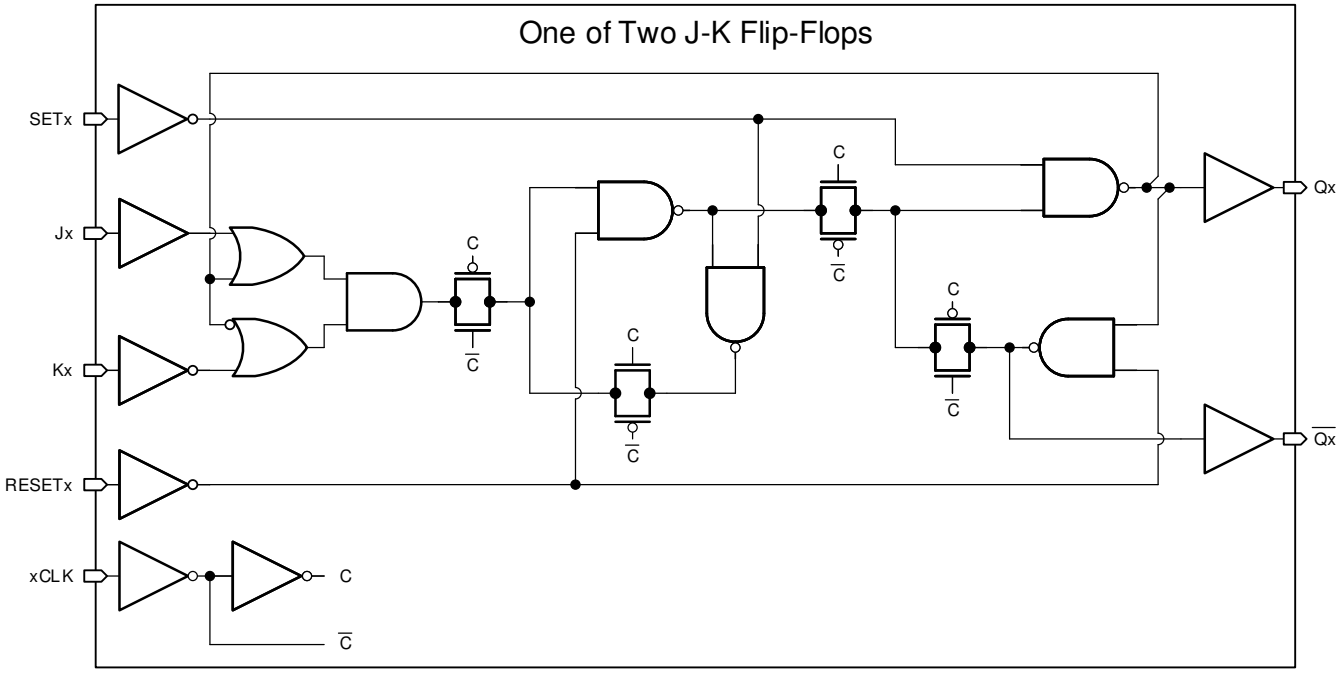

图 3-1. 逻辑图

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4 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (October 2003) to Revision D (July 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

5 Pin Configuration and Functions

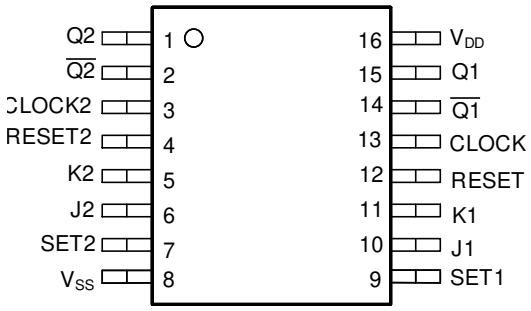


图 5-1. Terminal Assignment

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLOCK1	13	I	Clock input for channel 1
CLOCK2	3	I	Clock input for channel 2
J1	10	I	J input for channel 1
J2	6	I	J input for channel 2
K1	11	I	K input for channel 1
K2	5	I	K input for channel 2
Q1	15	O	Q output for channel 1
$\overline{Q1}$	14	O	Inverted Q output for channel 1
Q2	1	O	Q output for channel 2
$\overline{Q2}$	2	O	Inverted Q output for channel 2
RESET1	12	I	Reset input for channel 1
RESET2	4	I	Reset input for channel 2
SET1	9	I	Set input for channel 1
SET2	7	I	Set input for channel 2
V_{DD}	16	—	Supply
V_{SS}	8	—	Ground

6 Specifications

6.1 Absolute Maximum Ratings

			MIN	MAX	UNIT
V_{DD}	DC Supply Voltage Range	Voltages referenced to V_{SS} Terminal	– 0.5	20	V
All Inputs	Input Voltage Range		– 0.5	V_{DD} + 0.5	V
Any One Input	DC Input Current			±10	mA
P_D	Power Dissipation per Package	For T_A = – 55°C to + 100°C		500	mW
		For T_A = +100°C to +125°C	12mW/°C	200	mW
	Device Dissipation per Output Transistor	For T_A = Full package-temperature range (all package types)		100	mW
T_A	Operating- Temperature Range		– 55	125	°C
T_{stg}	Storage temperature		– 65	150	°C
	Lead Temperatur (During Soldering)	At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max		265	°C

6.2 Recommended Operating Conditions

at T_A = 25℃, except as noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC			V_{DD} (V)	LIMITS		UNIT
				ALL PACKAGES		
				MIN	MAX	
	Supply-Voltage Range	For T_A = Full Package Temperature Range		3	18	V
t_S	Data Setup Time		5	200		ns
			10	75		
			15	50		
t_W	Clock Pulse Width		5	140		ns
			10	60		
			15	40		
f_{CL}	Clock Input Frequency (Toggle Mode)		5		3.5	MHz
			10	dc	8	
			15		12	
t_rCL, t_fCL(1)	Clock Rise or Fall Time		5		45	μs
			10		5	
			15		2	
t_W	Set or Reset Pulse Width		5	180		ns
			10	80		
			15	50		

(1) If more than one unite is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transitiopn time of the output driving stage for the estimated capacitive load.

6.3 Static Electrical Characteristics

CHARACTERISTIC	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNIT
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25			
								MIN	TYP	MAX	
Quiescent		0, 5	5	1	1	30	30		0.02	1	μa
Device		0, 10	10	2	2	60	60		0.02	2	
Current		0, 15	15	4	4	120	120		0.02	4	
I_{DD} Max.		0, 20	20	20	20	600	600		0.04	20	
Output Low (Sink)	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1		mA
Current	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6		
I_{OL} Min.	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8		
Output High	4.6	0, 5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1		mA
(Source)	2.5	0, 5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2		
Current	9.5	0, 10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6		
I_{OH} Min.	13.5	0, 15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8		
Output Voltage		0, 5	5	0.05					0	0.05	V
Low-Level		0, 10	10	0.05					0	0.05	
V_{OL} Max.		0, 15	15	0.05					0	0.05	
Output Voltage		0, 5	5	4.95				4.95	5		V
High-Level		0, 10	10	9.95				9.95	10		
V_{OH} Min.		0, 15	15	14.95				14.95	15		
Input Low	0,5, 4.5		5	1.5						1.5	V
Voltage	1, 9		10	3						3	
V_{IL} Max.	1.5, 13.5		15	4						4	
Input High	0.5, 4.5		5	3.5				3.5			V
Voltage	1, 9		10	7				7			
V_{IH} Min.	1.5, 13.5		15	11				11			
Input Current, V_{IH} Max.		0, 18	18	±0.1	±0.1	±1	±1		$±10^{-5}$	±0.1	μA

6.4 Dynamic Electrical Characteristics

at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS			UNIT
		ALL PACKAGES			
		MIN	TYP	MAX	
Propagation Delay Time	5		150	300	ns
Clock to Q or $\overline{Q}$ Outputs	10		65	130	
t_{PHL}, t_{PLH}	15		45	90	
Set to Q or Reset to $\overline{Q}$, t_{PLH}	5		150	300	ns
	10		65	130	
	15		45	90	
Set to $\overline{Q}$ or Reset to Q, t_{PHL}	5		200	400	ns
	10		85	170	
	15		60	120	
Transition Time	5		100	200	ns
t_{THL}, t_{TLH}	10		50	100	
	15		40	80	

6.4 Dynamic Electrical Characteristics (continued)

at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS			UNIT
		ALL PACKAGES			
		MIN	TYP	MAX	
Maximum Clock Input Frequency (Toggle Mode)(1) f_{CL}	5	3.5	7		MHz
	10	8	16		
	15	12	24		
Minimum Clock Pulse Width, t_W	5		70	140	
	10		30	60	
	15		20	40	
Minimum Set or Reset Pulse Width, t_W	5		90	180	ns
	10		40	80	
	15		25	50	
Minimum Data Setup Time, t_S	5		100	200	ns
	10		35	75	
	15		25	50	
Clock Input Rise or Fall Time t_{rCL}, t_{fCL}	5			45	μs
	10			5	
	15			2	
Input Capacitance, C_I			5	7.5	pF

(1) Input t_r, t_f = 5 ns

6.5 Typical Characteristics

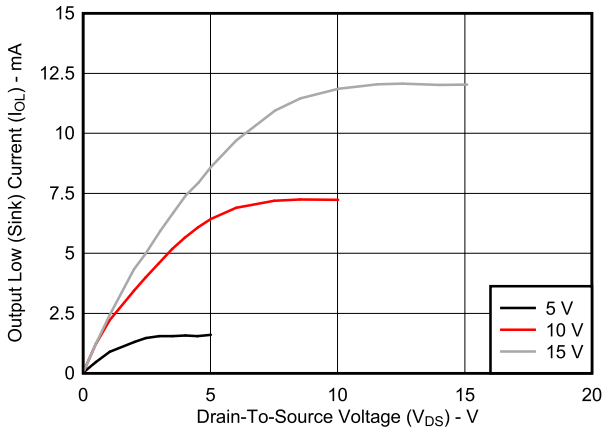


图 6-1. Typical Output Low (Sink) Current Characteristics

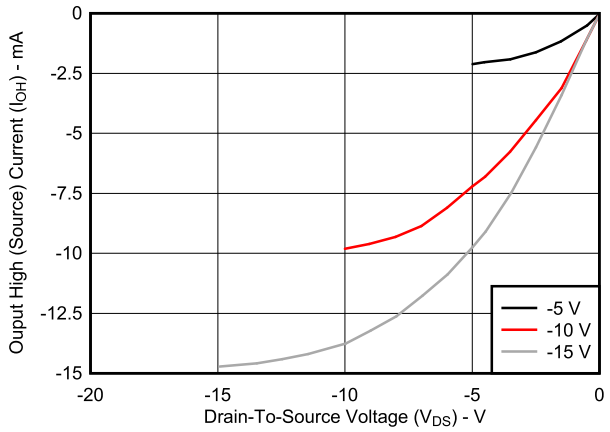


图 6-2. Typical Output High (Source) Current Characteristics

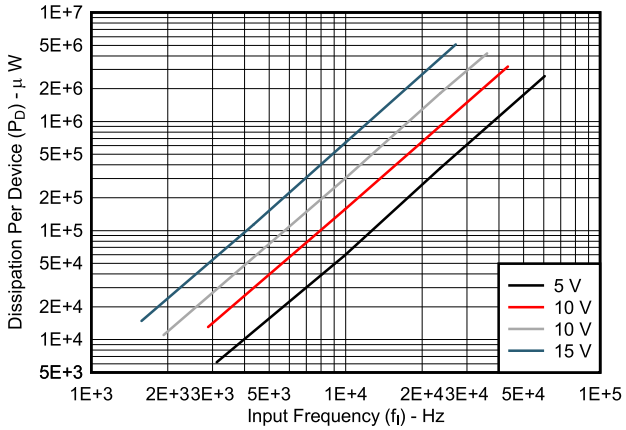


图 6-3. Typical Power Dissipation vs Frequency

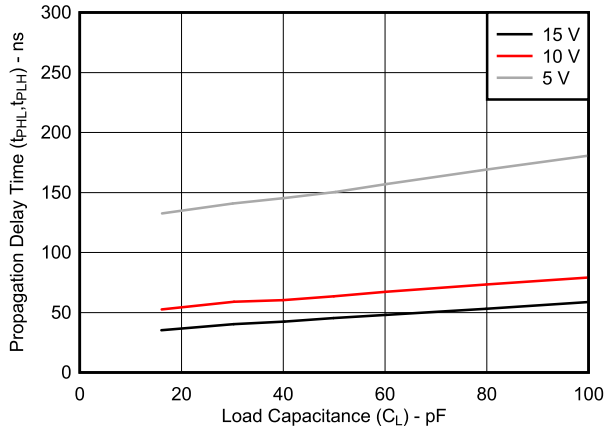


图 6-4. Typical Propagation Delay Time vs Load Capacitance (Clock or Set to Q, Clock or Reset to $\overline{Q}$)

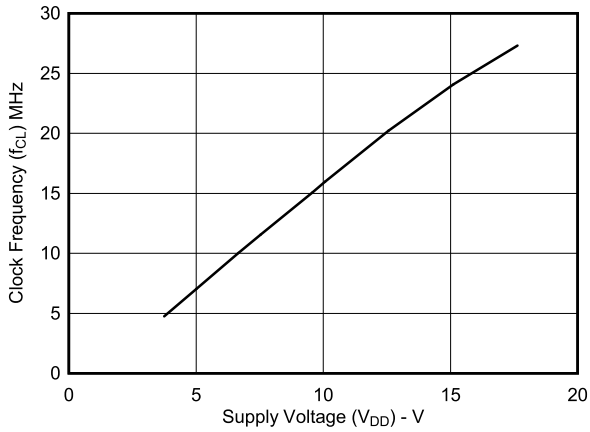


图 6-5. Typical Maximum Clock Frequency vs Supply Voltage (Toggle Mode)

7 Parameter Measurement Information

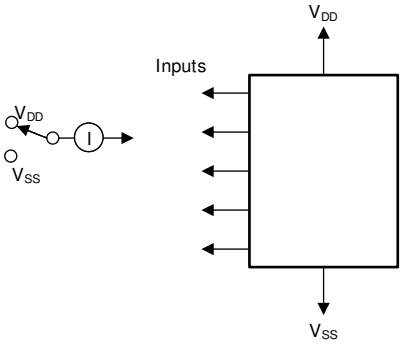


图 7-1. Input Current Test Circuit

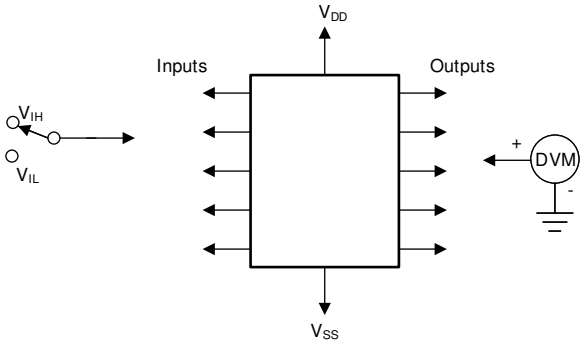


图 7-2. Input-Voltage Test Circuit

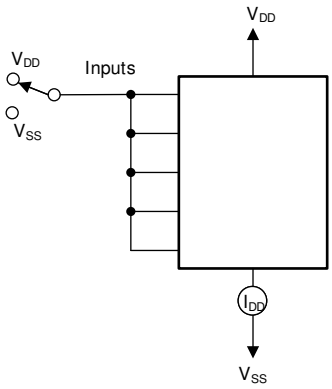
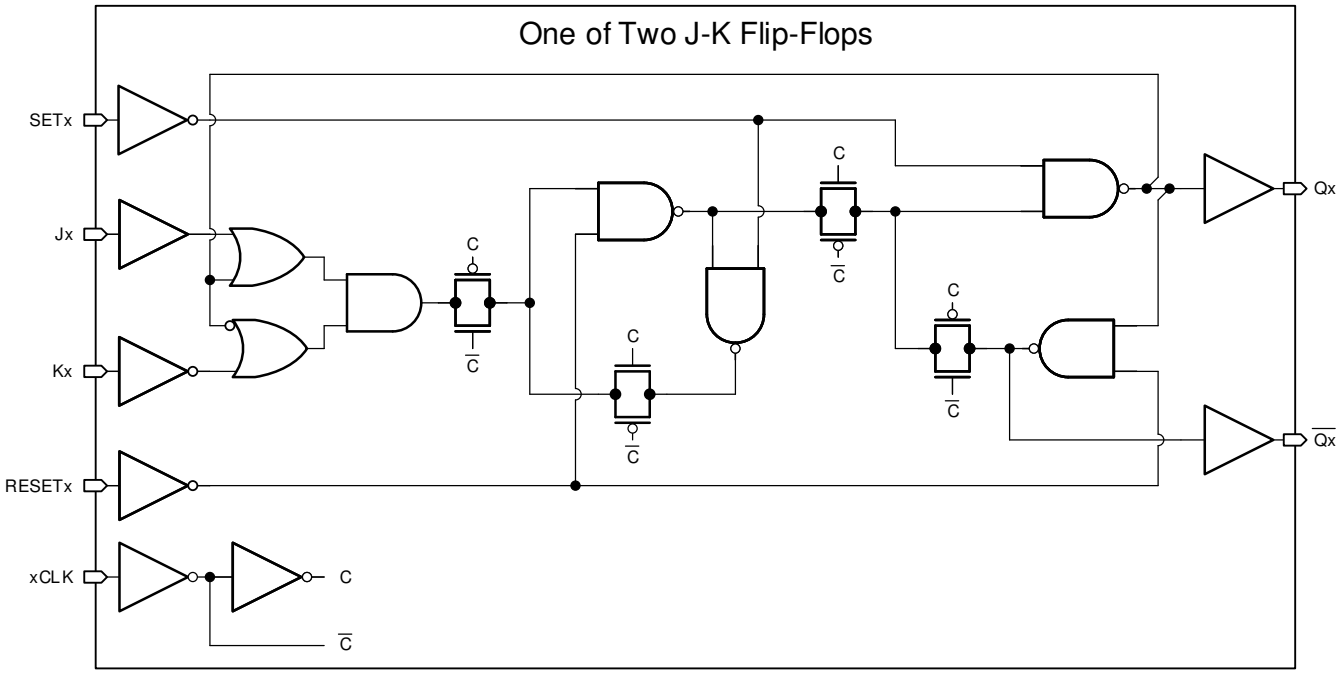


图 7-3. Quiescent Device Current Test Circuit

8 Detailed Description

8.1 Functional Block Diagram



8.2 Device Functional Modes[1]

PRESENT STATE					CL[2]	NEXT STATE	
INPUTS				OUTPUT		OUTPUTS	
J	K	S	R	O	_⎍	O	$\overline{O}$
I	X	O	O	O	_⎍	I	O
X	O	O	O	I	_⎍	I	O
O	X	O	O	O	_⎍	O	I
X	I	O	O	I	_⎍	O	I
X	X	O	O	X	¯_	No change	No change
X	X	I	O	X	X	I	O
X	X	O	I	X	X	O	I
X	X	I	I	X	X	I	I

(1) Logic I = High Level, Logic O = Low Level, X = Do not care
(2) Level change

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

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邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4027BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4027BE	Samples
CD4027BEE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4027BE	Samples
CD4027BF	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4027BF	Samples
CD4027BF3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4027BF3A	Samples
CD4027BM	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM	Samples
CD4027BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM	Samples
CD4027BM96E4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM	Samples
CD4027BME4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM	Samples
CD4027BMT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM	Samples
CD4027BNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027B	Samples
CD4027BNSRG4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027B	Samples
CD4027BPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM027B	Samples
CD4027BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM027B	Samples
CD4027BPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM027B	Samples
JM38510/05152BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 05152BEA	Samples
M38510/05152BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 05152BEA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD4027B, CD4027B-MIL :

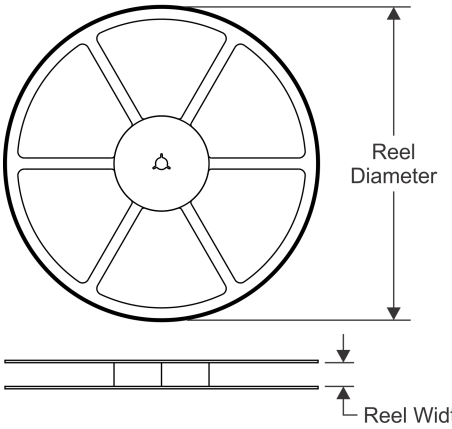
- Catalog : CD4027B
- Military : CD4027B-MIL

NOTE: Qualified Version Definitions:

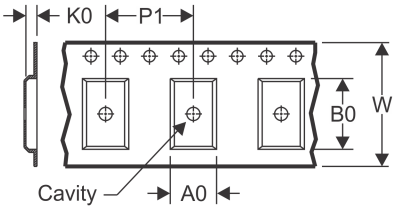
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

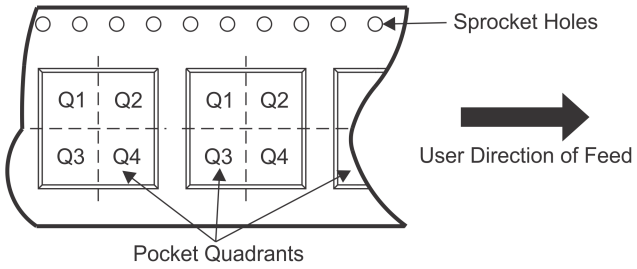


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

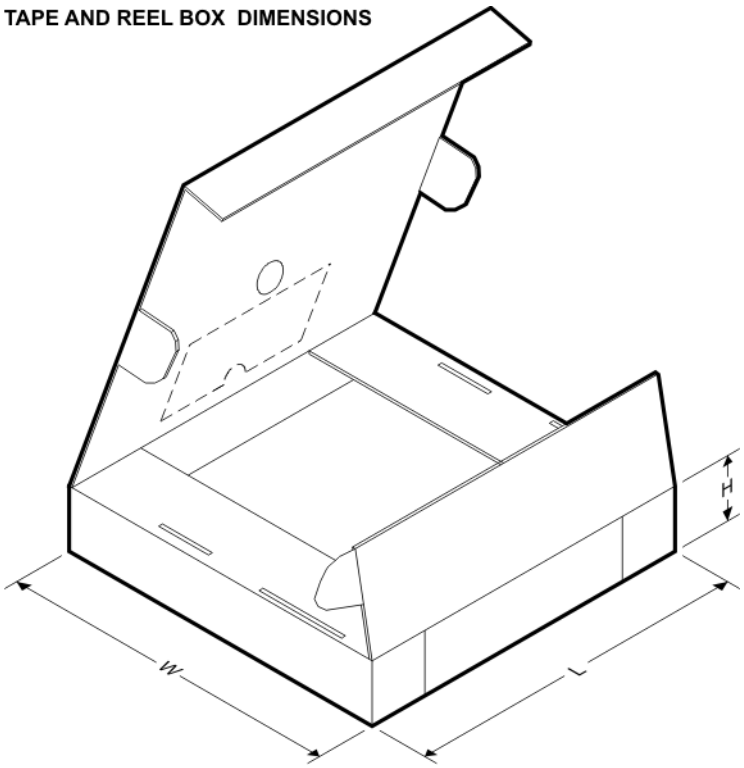
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4027BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4027BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4027BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

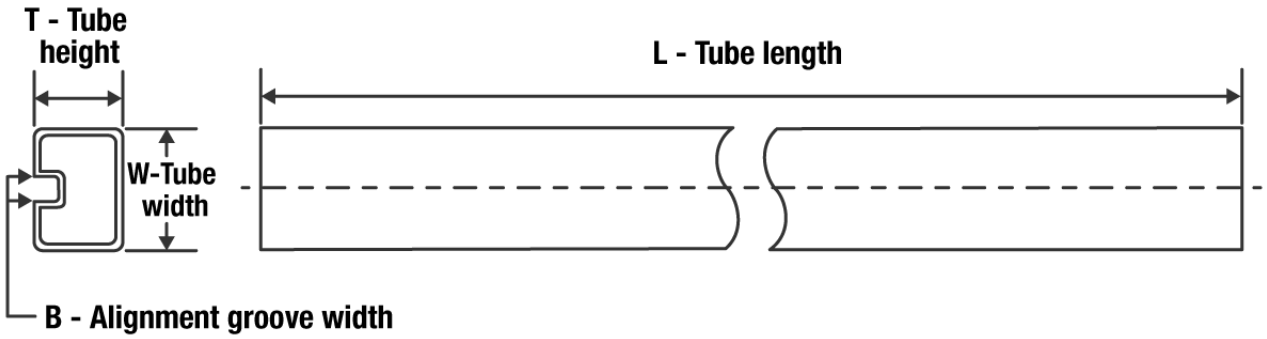
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4027BM96	SOIC	D	16	2500	340.5	336.1	32.0
CD4027BNSR	SO	NS	16	2000	853.0	449.0	35.0
CD4027BPWR	TSSOP	PW	16	2000	853.0	449.0	35.0

TUBE



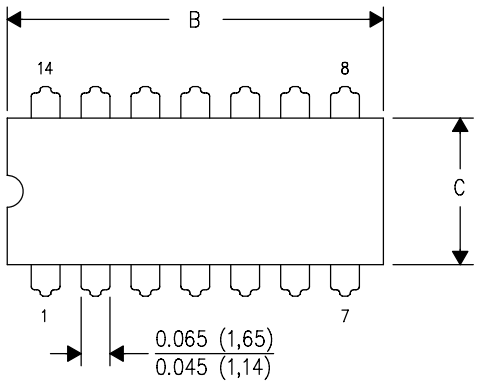
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4027BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BM	D	SOIC	16	40	507	8	3940	4.32
CD4027BME4	D	SOIC	16	40	507	8	3940	4.32
CD4027BPW	PW	TSSOP	16	90	530	10.2	3600	3.5

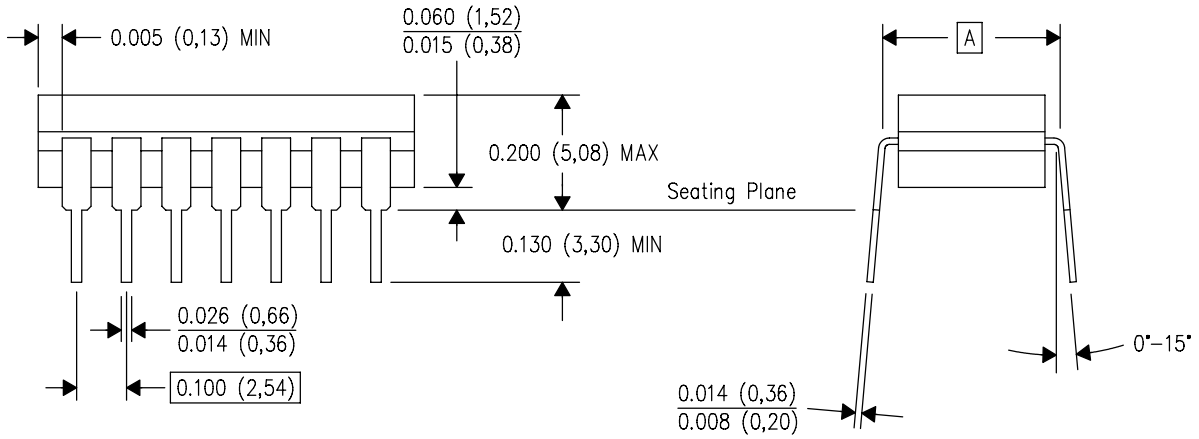
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



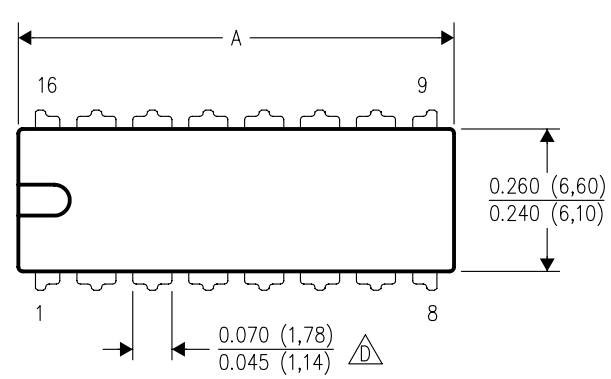
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

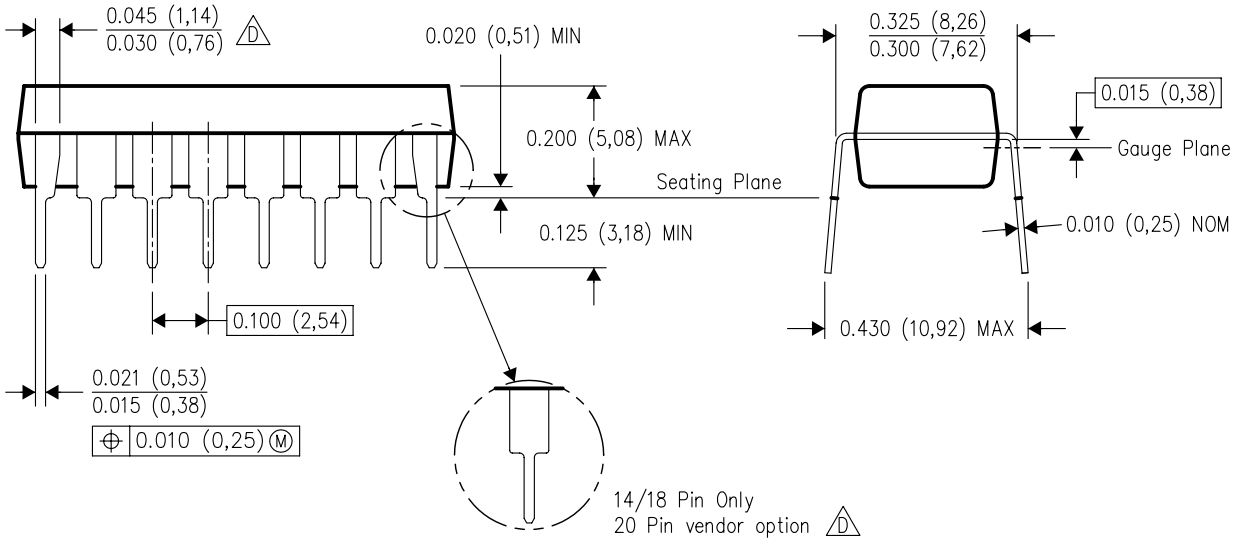
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

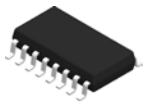


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

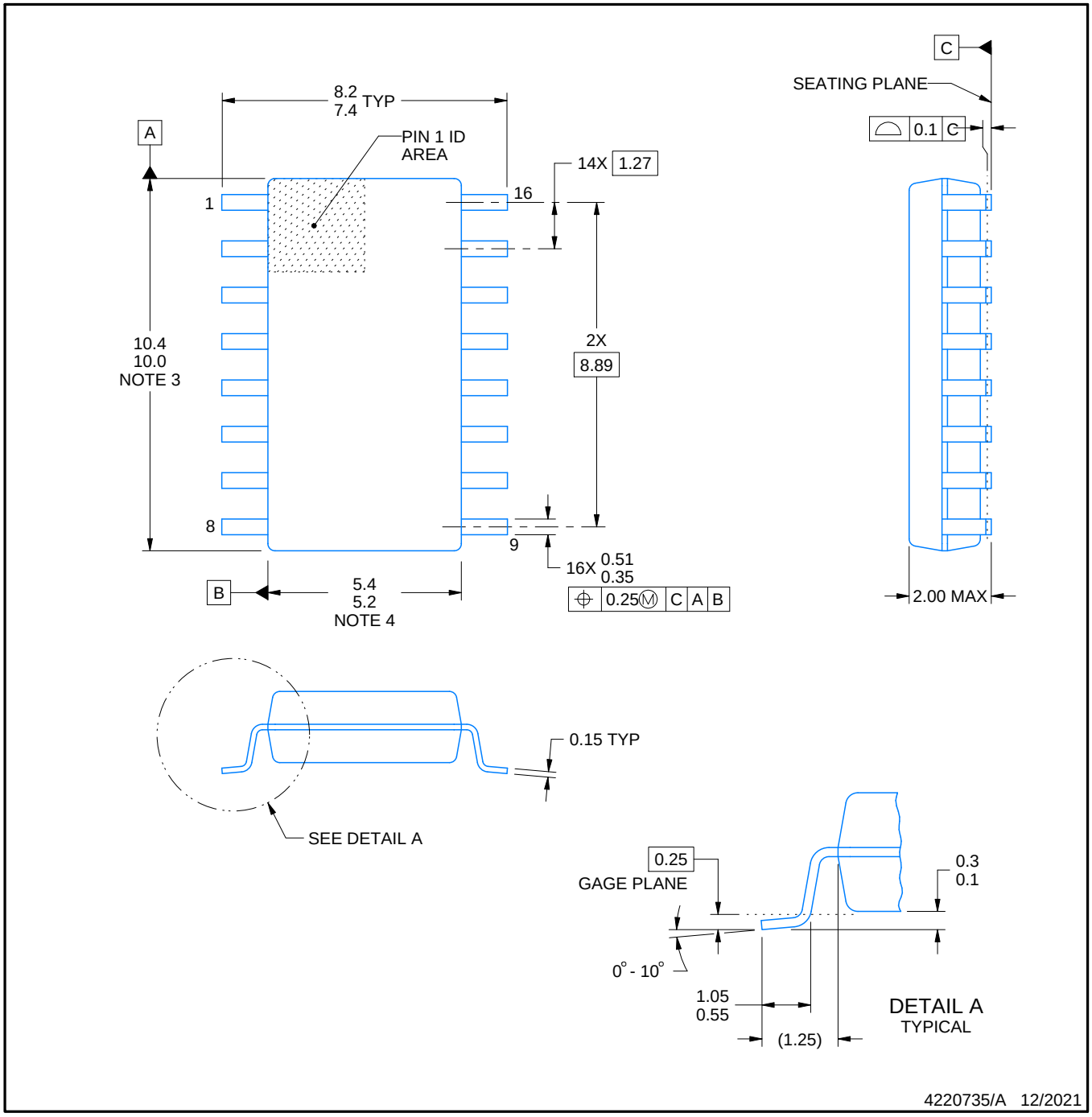


PACKAGE OUTLINE

NS0016A

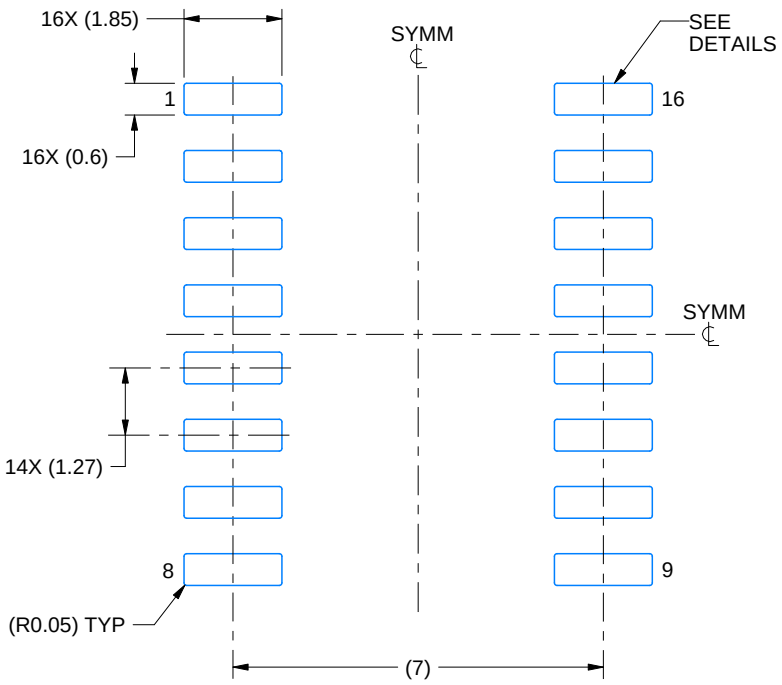
SOP - 2.00 mm max height

SOP

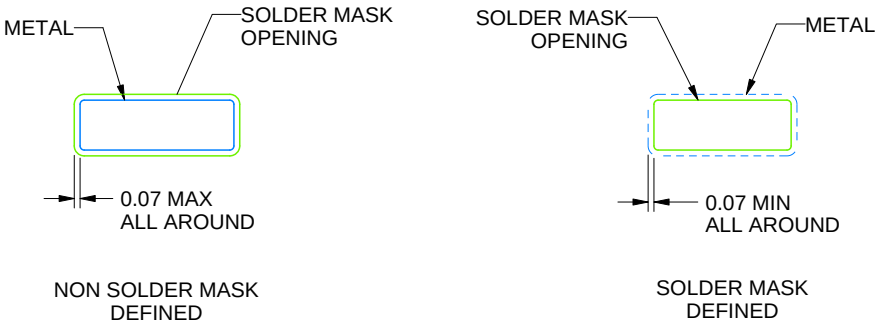


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

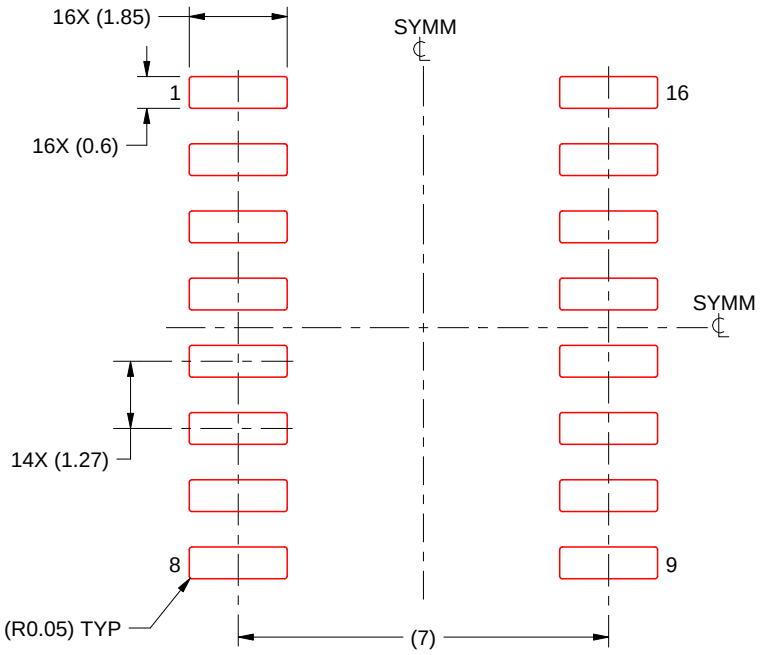
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



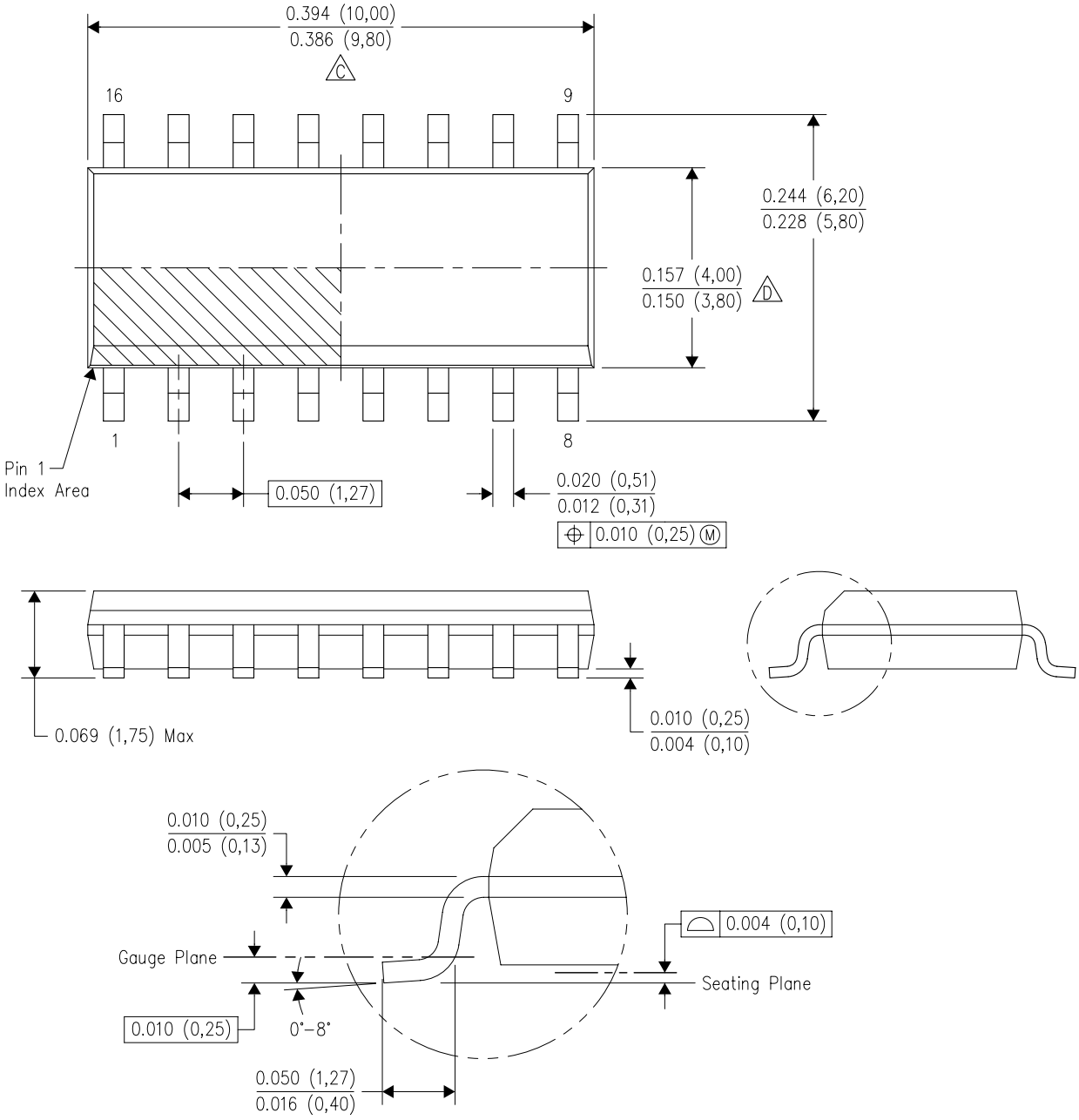
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

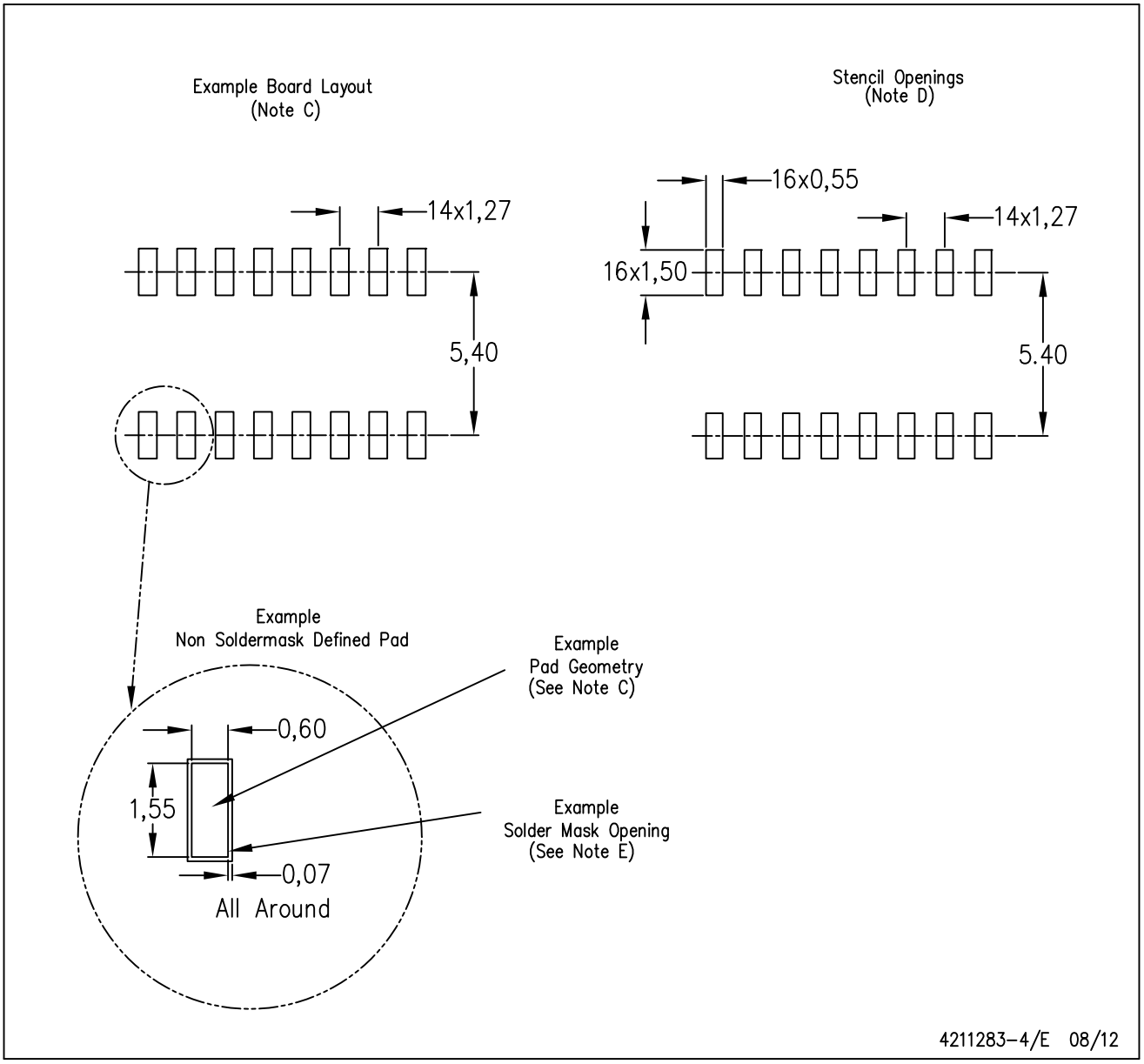
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



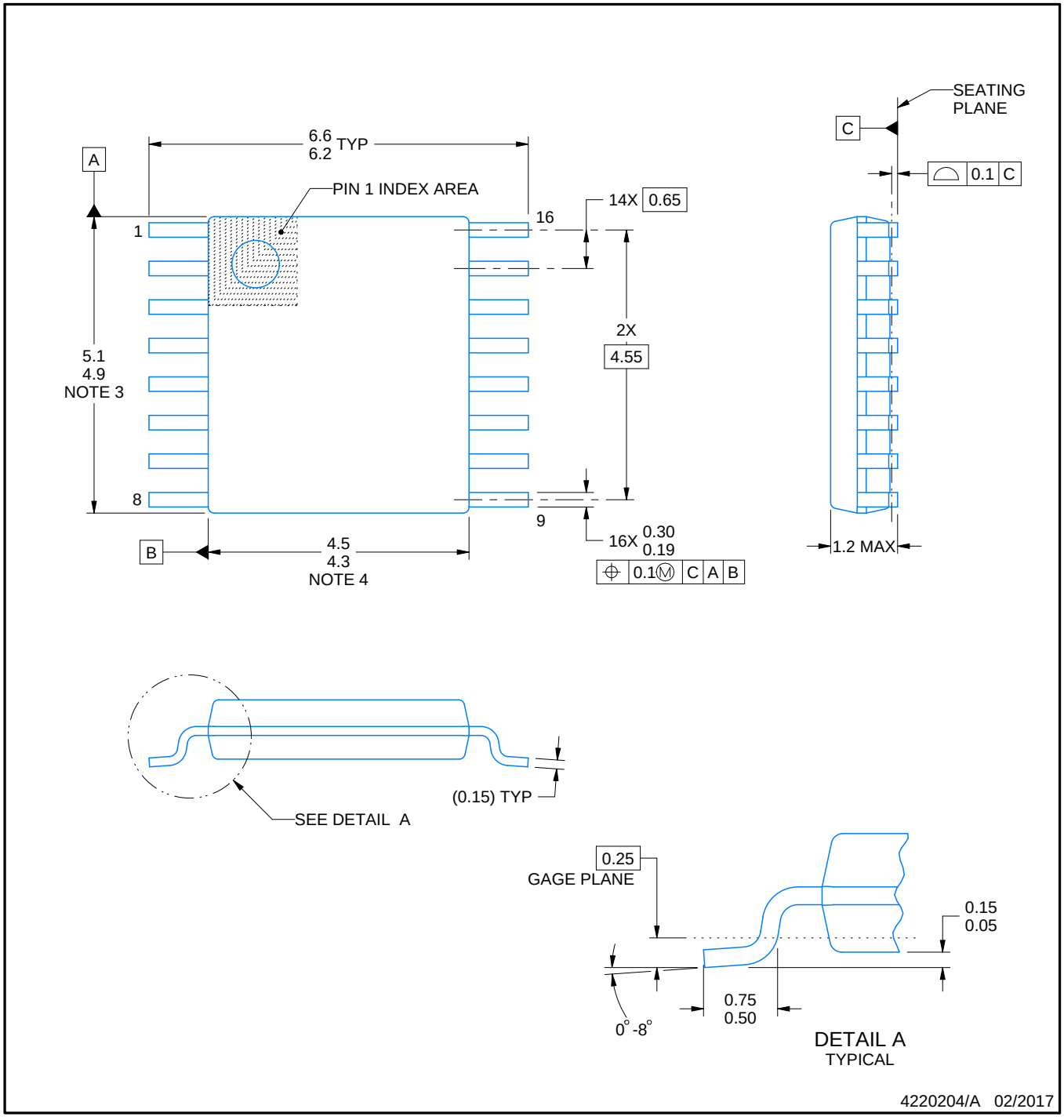
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

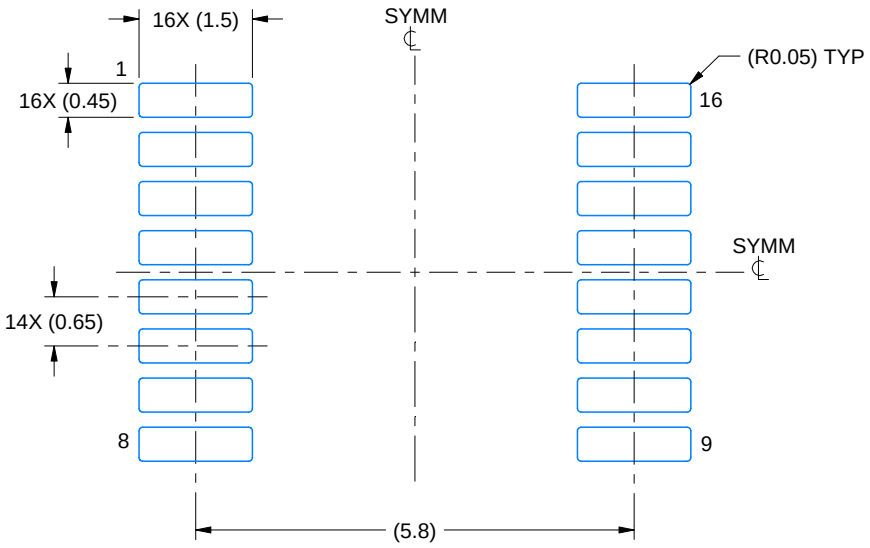
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

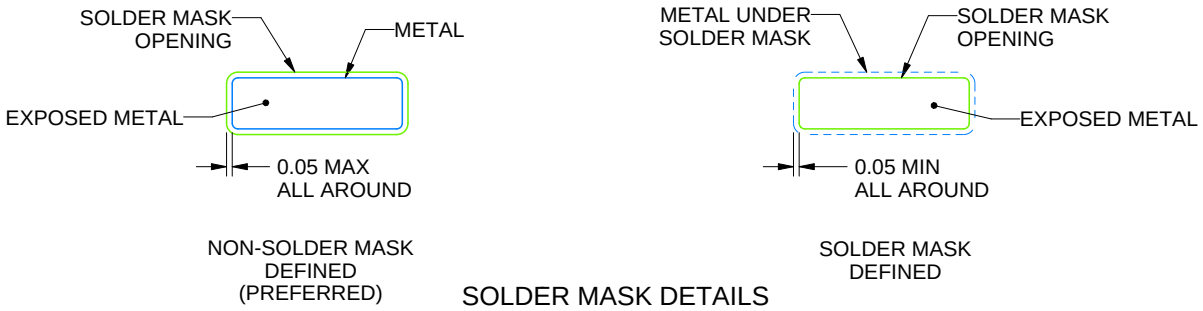


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

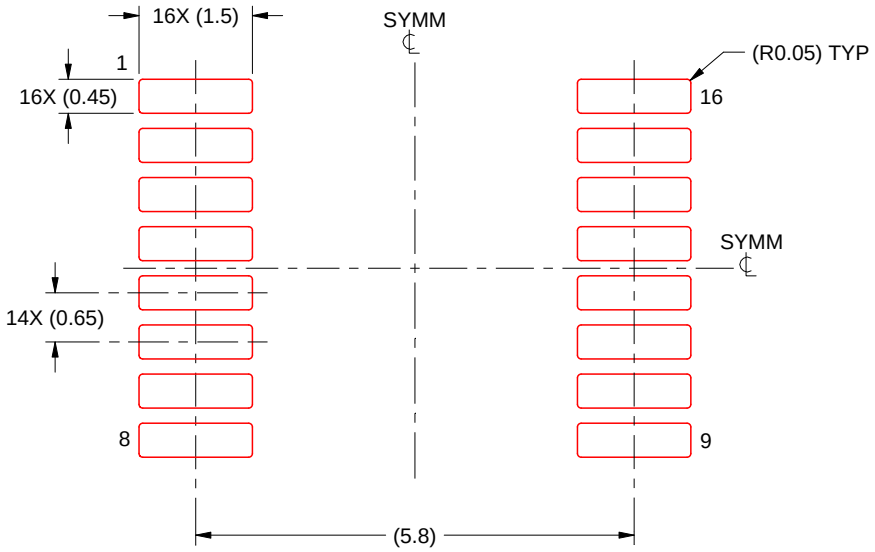


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

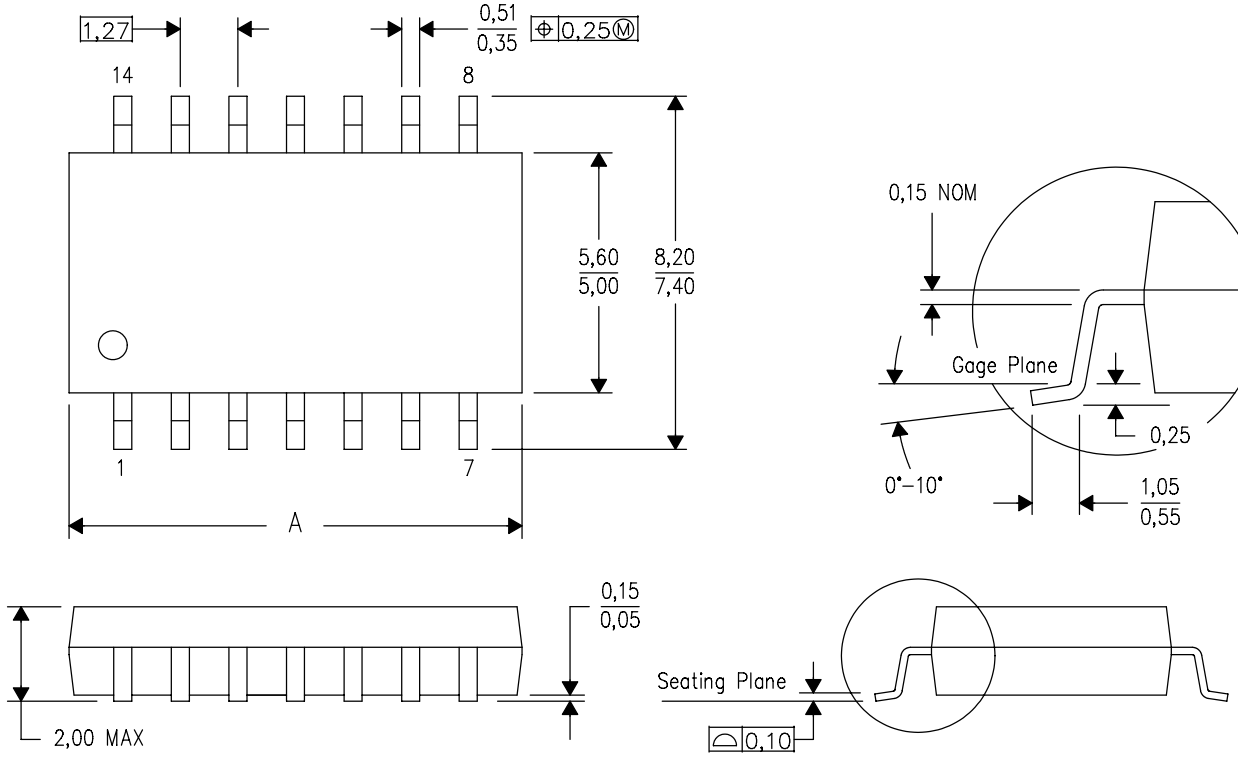
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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