DUAL OUTPUT BOOST REGULATOR USING SINGLE INDUCTOR

FEATURES

- **2.5-V to 6-V Input Voltage Range**
- **Two Outputs Each up to 27 V**
- **0.7-A Integrated Switch**
- **Built-In Power Diode**
- **1.2-MHz PWM for WLED Driver**
- **PFM for OLED Supply**
- **Individually Programmable Output**
- **Input to Output Isolation**
- **Short-Circuit Protection**
- **Built-In Soft Start**
- **Overvoltage Protection**
- **Up to 82% Efficiency**
- **Up to 30 kHz PWM Dimming Frequency**
- **Available in a 10 Pin, 3 × 3 mm QFN Package**

APPLICATIONS

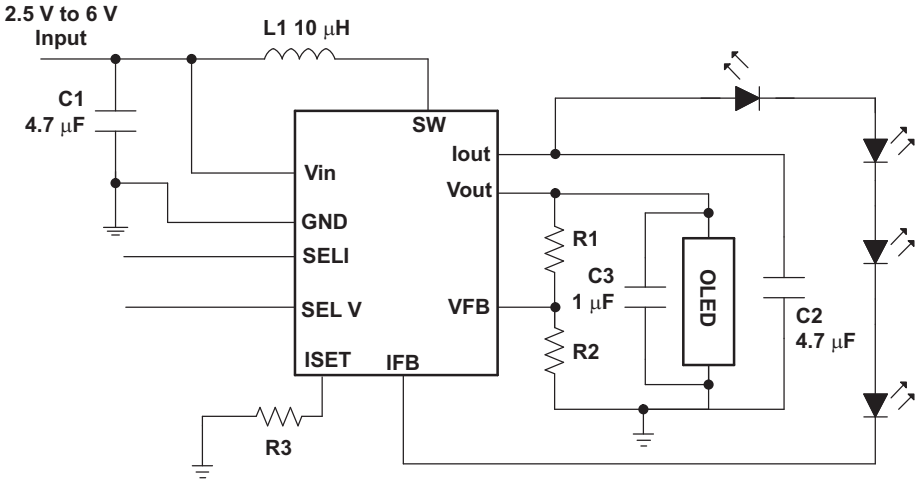
- **Clamshell Phone With OLED/LCD Screen**

DESCRIPTION

The TPS61140/1 is a dual output boost converter IC. It is intended to be configured as a highly integrated power solution providing regulated voltage and current output with one boost converter. This device is ideal for driving the OLED sub display and WLED backlight for the LCD main display in clam shell phones. The voltage and current can be individually programmed through external resistors. There is a dedicated selection pin for each output, so the two outputs can be turned on separately or simultaneously. When only the voltage output is enabled, the boost converter is controlled by pulse frequency modulation (PFM) in order to achieve high efficiency over a wide load range. If the current output is selected, the device adopts a 1.2-MHz pulse width modulation control (PWM) method in order to maximize output current. Applying an external PWM signal to the select pin (SELI) reduces the output current thereby allowing WLED dimming.

The TPS61140/1 has a built-in power MOSFET and power diode; thereby, eliminating the needs for any external active power components. In addition, the high switching frequency reduces the external inductor and capacitor sizes. Overall, the IC provides a highly compact solution with high efficiency and plenty of flexibility.

TYPICAL APPLICATION



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

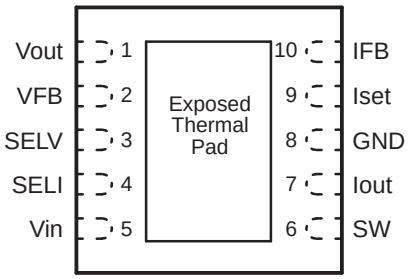
ORDERING INFORMATION

T_A	PACKAGE(1)	OVP (typ)	PACKAGE MARKING
–40 to 85°C	TPS61140DRCR	28 V	BCP
–40 to 85°C	TPS61141DRCR	22 V	BRG
–40 to 85°C	TPS61140DRCT	28 V	BCP
–40 to 85°C	TPS61141DRCT	22 V	BRG

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

DEVICE INFORMATION

10 pin 3*3 mm QFN PACKAGE
(TOP VIEW)



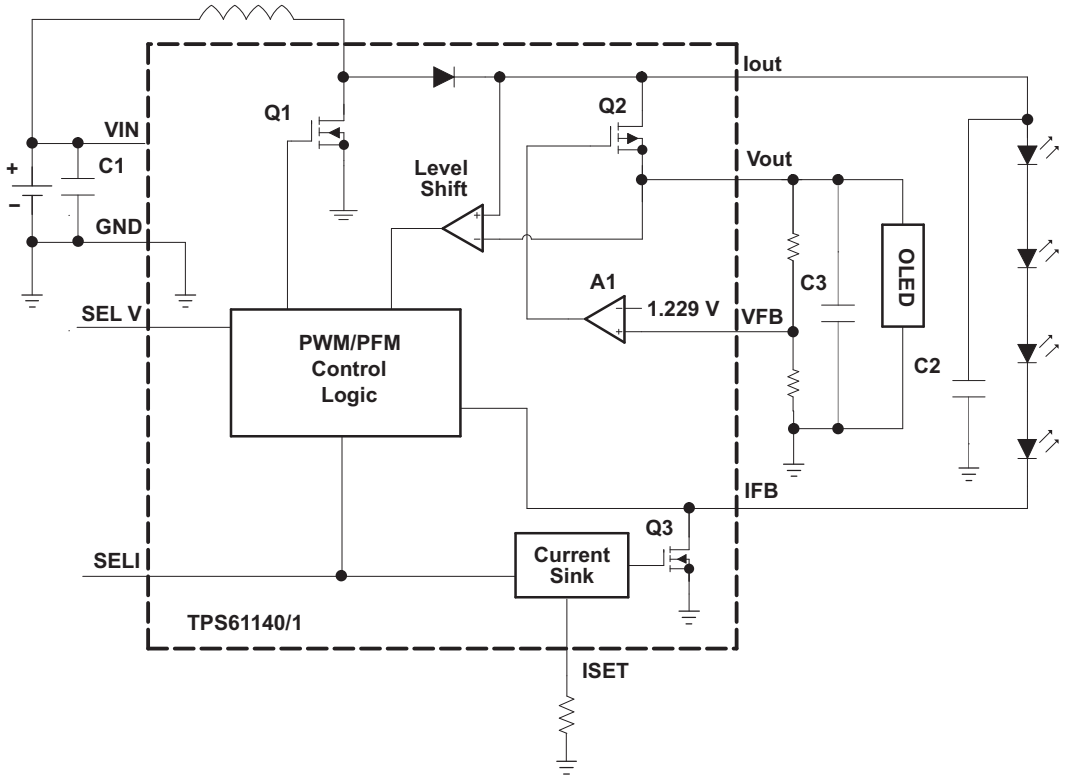
TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
VIN	5	I	The input pin to the IC. It provides the current to the boost regulator output, and also powers the IC circuit. When the Vin voltage is below the undervoltage lockout threshold, the IC turns off and disables outputs.
GND	8	O	The ground of the IC. Connect the input and output capacitors very close to this pin.
SW	6	I	This is the switching node of the IC where the PWM switching Is created.
IOUT	7	O	The output of the constant current supply. It is directly connected to the boost regulator output.
VOUT	1	O	The output of the voltage regulator. There is a low dropout linear regulator (LDO) between the Iout and Vout pins which regulates the Vout voltage. Turning off the LDO disconnects the Vout from Iout.
VFB	2	I	The voltage feedback pin for Vout regulation. It is regulated to an internal reference voltage. An external voltage divider connected to this pin programs the output voltage.
IFB	10	I	The return path for the Iout regulation. The current regulator is connected to this pin, and it can be disabled by opening the current path.
ISET	9	I	The current output programming pin. The resistor connected to the pin programs the regulated current of the Iout pin.
SELI, SELV	4, 3	I	Mode selection pins. See Table 1 for details.
Thermal Pad			The thermal pad should be soldered to the analog ground. If possible, use thermal via to connect to ground plane for ideal power dissipation.

Table 1. TPS61140/1 mode selection

SELV	SELI	Vout	Iout
H	L	Enable	Disable
L	H	Disable	Enable
H	H	Enable	Enable
L	L	IC Shutdown	

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

	VALUE	UNIT
Supply voltages on pin VIN(2)	–0.3 to 7	V
Voltages on pins SELI, SELV, ISET and VFB(2)	–0.3 to 7	V
Voltage on pin Iout, SW, Vout and IFB(2)	30	V
Continuous power dissipation	See Dissipation Rating Table	
Operating junction temperature range	–40 to 150	°C
Storage temperature range	–65 to 150	°C
Lead temperature (soldering, 10 sec)	260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	$T_A \leq 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
QFN (1)	270°C/W	370 mW	204 mW	148 mW
QFN(2)	48.7°C/W	2.05 W	1.13 W	821 mW

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_I	Input voltage range	2.5		6	V
V_O	Output voltage range	V_I		27	V
L	Inductor(1)		10		µH
C_i	Input capacitor(1)	4.7			µF
C_{O1}	Output capacitor on Iout(1)	1	4.7		µF
C_{O2}	Output capacitor on Vout (1)	1			µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) See Application Section for further information.

ELECTRICAL CHARACTERISTICS

V_I = 3.6 V, SELx = Vin, Rset = 80 kΩ, V_O = 15 V, V_{IO} = 15 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range		2.5		6	V
I_Q	Operating quiescent current into Vin	Device not switching			0.125	mA
		Device PWM switching no load			2	
$I_{Q(Iout)}$	Operating quiescent current into Iout				50	µA
I_{SD}	Shutdown current	SELx = GND			1.5	µA
V_{UVLO}	Undervoltage lockout threshold	Vin falling		1.65	1.8	V
V_{hys}	Undervoltage lockout hysterisis			70		mV
ENABLE AND SOFT START						
$V_{(selh)}$	SEL logic high voltage	Vin = 2.7 V to 6 V	1.2			V
$V_{(sell)}$	SEL logic low voltage	Vin = 2.7 V to 6 V			0.4	V
$R_{(en)}$	Enable pull down resistor		300	700		kΩ
T_{off}	EN pulse width to disable	EN high to low	40			ms
K_{ss}	IFB soft start current steps			16		
T_{ss}	Soft start time step	Measured as clock divider		64		
T_{ss_en}	Soft start enable time	Time between falling and rising edges of two adjacent SELI pulses	40			ms

ELECTRICAL CHARACTERISTICS (Continued)

V_I = 3.6 V, SELx = Vin, Rset = 80 kΩ, V_O = 15 V, V_{IO} = 15 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE AND CURRENT CONTROL						
I_{FB}	Voltage feedback input bias current	V_{FB} = 1.229 V			100	nA
V_{FB}	Voltage feedback regulation voltage		1.204	1.229	1.254	V
$V_{(ISET)}$	ISET pin voltage		1.204	1.229	1.254	V
$K_{(ISET)}$	Current multipiler	Iout/Iset	820	900	990	
$V_{(IFB)}$	IFB Regulation voltage		300	330	360	mV
$V_{(IFB_L)}$	IFB low threshold (1)			60		mV
t_{sink}	Current sink settle time	Measured from SELx rising edge (2)			6	µs
I_{lkg}	IFB pin leakage current	IFB voltage = 25 V			1	µA
$V_{(delta)}$	Iout-Vout regulation threshold	Iout-Vout	270	330	380	mV
$V_{(delta_l)}$	Iout-Vout low threshold (3)			45		mV
$I_{(LDO_leak)}$	LDO leakage current	Iout = 25 V, Vout = 0 V			1	µA
PSRR	LDO PSRR	Iout–Vout = 330 mV, 2 mA, 20 kHz		20		dB
POWER SWITCH AND DIODE						
$r_{DS(on)}$	N-channel MOSFET on-resistance	$V_I = V_{GS}$ = 3.6 V		0.6	0.9	Ω
$I_{(LN_NFET)}$	N-channel leakage current	V_{DS} = 25 V			1	µA
V_F	Power diode forward voltage	Id = 0.7 A		0.83	1.0	V
OC AND OVP						
I_{LIM}	N-Channel MOSFET current limit (4)	Dual output, V(Iout) = 15 V, D = 76%	0.75	1.0	1.26	A
		Single output (PFM)	0.30	0.35	0.40	
		Single output (PWM), V(Iout) = 15 V, D = 76%	0.40	0.55	0.70	
$I_{(LDO_MAX)}$	LDO max output current	Iout–Vout = 330 mV	35			mA
$I_{(IFB_MAX)}$	Current sink max output current	IFB = 330 mV	35			mA
V_{OVP}	Overvoltage threshold	TPS61140	27	28	29	V
		TPS61141	21	22	23	
$V_{OVP(hys)}$	Overvoltage hysteresis	TPS61140		550		mV
		TPS61141		440		
PWM AND PFM CONTROL						
f_S	Oscillator frequency		1	1.2	1.5	MHz
D_{max}	Maximum duty cycle	PWM, VFB = 1 V	90	93		%
t_{on_max}	Maximum on time	PFM only		5.7		µs
t_{off_min}	Minimum off time	PFM only		413		ns
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
T_{hys}	Thermal shutdown threshold hysteresis			15		°C

(1) When the IFB pin voltage drops this amount below $V_{(IFB)}$, the IFB pin is used as the boost converter feedback if the Iout-Vout voltage is in regulation. This only occurs in BOTH-ON mode.
(2) This specification determines the minimum on time required for PWM dimming. Using this specification, the maximum PWM dimming frequency can be calculated from the minimum duty cycle required in the application.
(3) When Iout-Vout voltage drops this amount below $V_{(delta)}$, Iout-Vout is used as the boost converter feedback input regardless of the IFB voltage. This only occurs in BOTH-ON mode.
(4) Measured with DC current. See APPLICATION INFORMATION for details.

TYPICAL CHARACTERISTICS

Table of Graphs

TITLE	CONDITIONS	FIGURES
K value over current	Vin = 3.6 V, Iload = 2 mA to 25 mA	Figure 1
OLED efficiency vs load current	Vin = 3.3 V, 3.6 V and 4 V, Vout = 15 V	Figure 2
WLED efficiency vs load current	Vin = 3.3 V, 3.6 and 4 V, 3 WLED, WLED voltage = 11 V	Figure 3
WLED efficiency vs load current	Vin = 3.3 V, 3.6 V and 4 V, 4 WLED, WLED voltage = 15 V	Figure 4
WLED efficiency vs load current	Vin = 3.3 V, 3.6 V and 4 V, 5 WLED, WLED voltage = 19 V	Figure 5
WLED efficiency vs load current	Vin = 3.3 V, 3.6 V and 4 V, 6 WLED, WLED voltage = 23 V	Figure 6
OLED load regulation	Vin = 3.6 V, Iout = 15 V, Iload = 2 mA to 20 mA	Figure 7
OLED line regulation	Vin = 3 V to 5 V, Iout = 15 V, Iload = 10 mA	Figure 8
OLED ripple voltage waveform	Vin = 3.6 V, Vout = 15 V, Iload = 20, 2mA	Figure 9, 10
WLED PWM dimming waveform		Figure 11
WLED PWM dimming linearity	Frequency = 20 kHz and 30 KHz	Figure 12
Transition between OLED+WLED and OLED only	4 WLED and Vout=15V	Figure 13
WLED start up waveform		Figure 14
OLED start up waveform		Figure 15
PWM Mode Overcurrent Limit	WLED Only	Figure 16
PWM Mode Overcurrent Limit	WLED + OLED	Figure 17

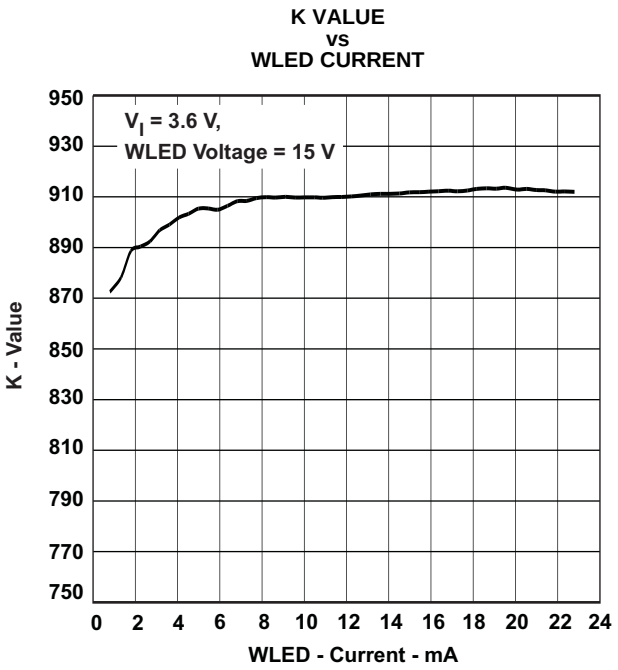


Figure 1.

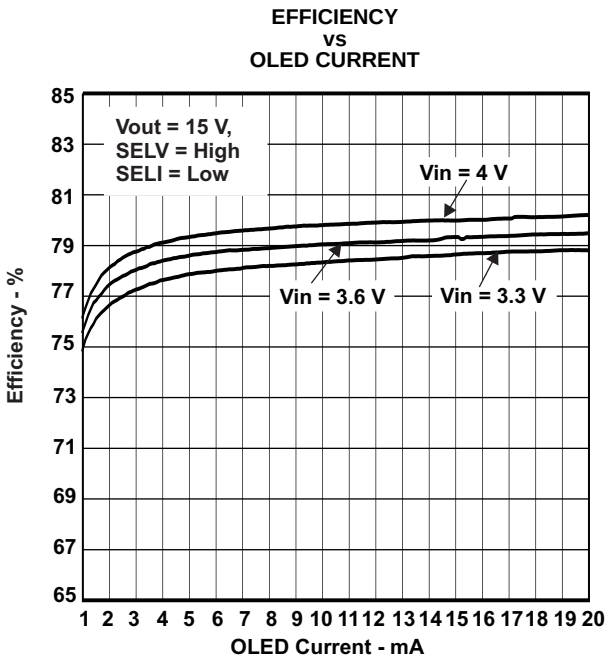


Figure 2.

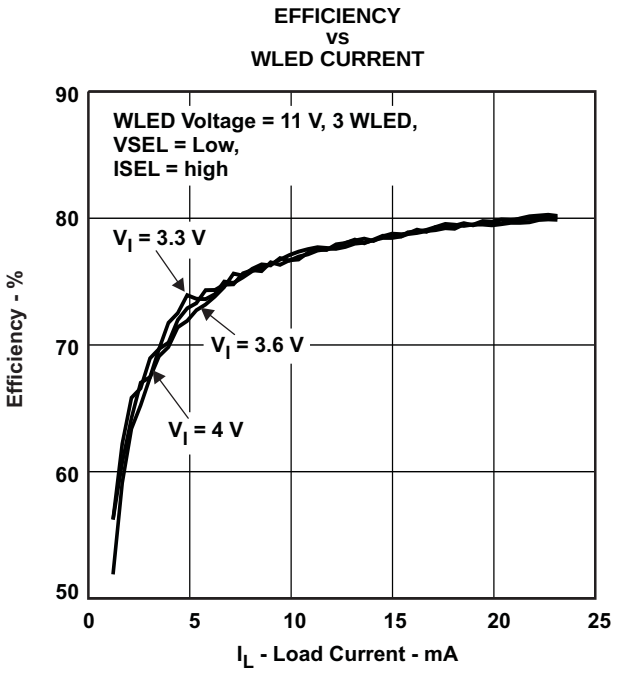


Figure 3.

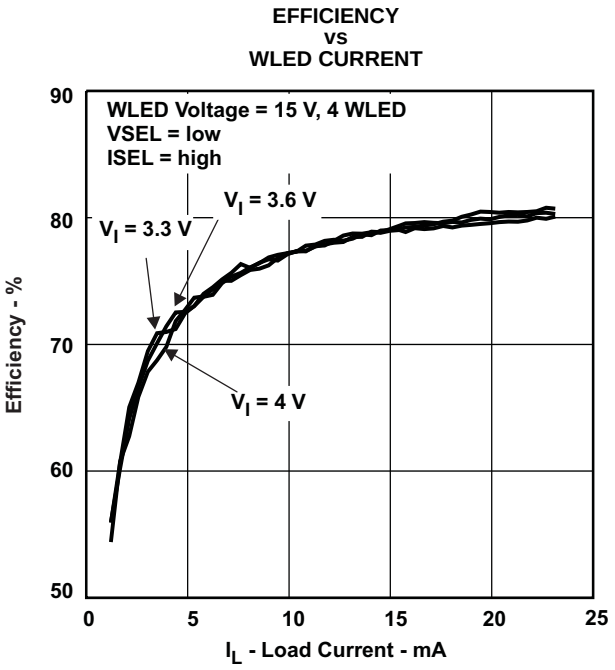


Figure 4.

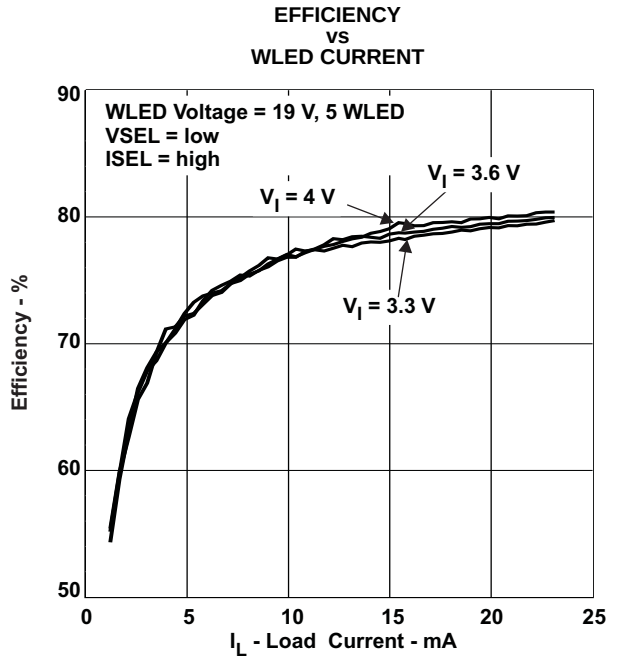


Figure 5.

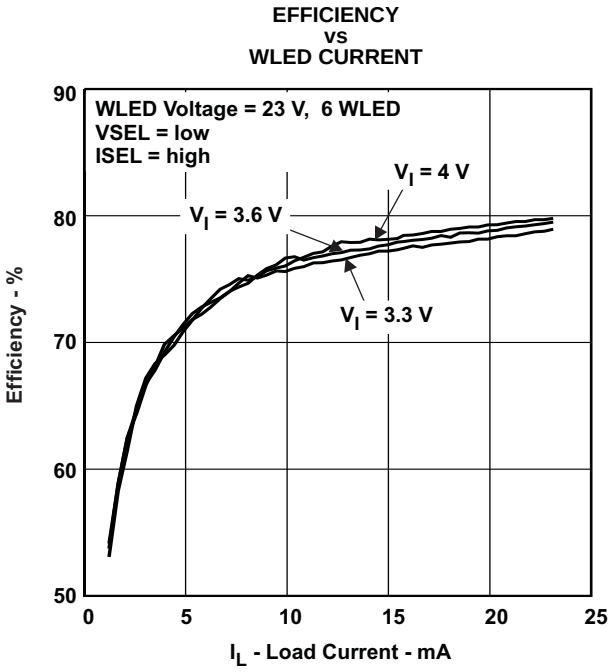


Figure 6.

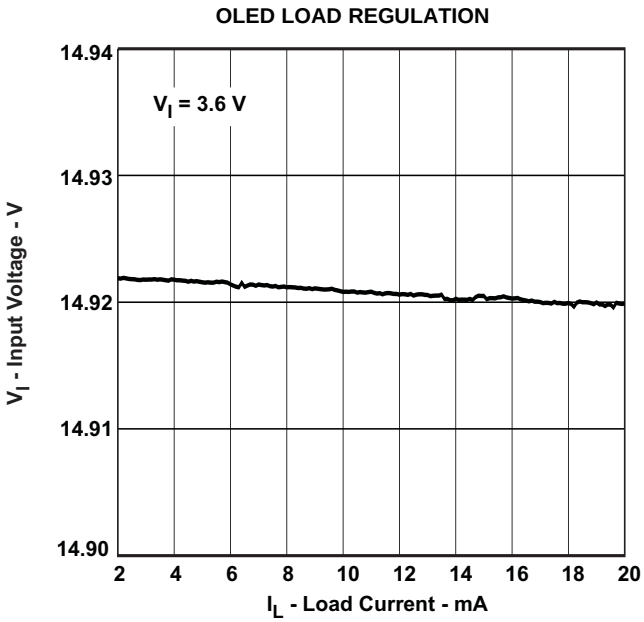


Figure 7.

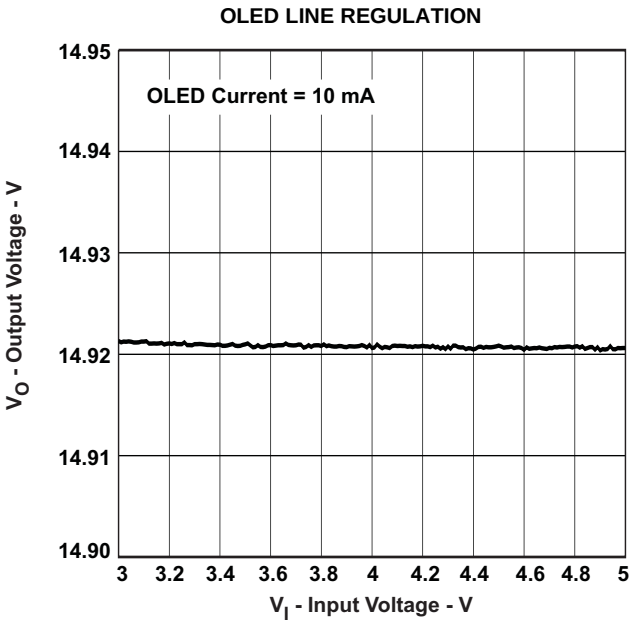


Figure 8.

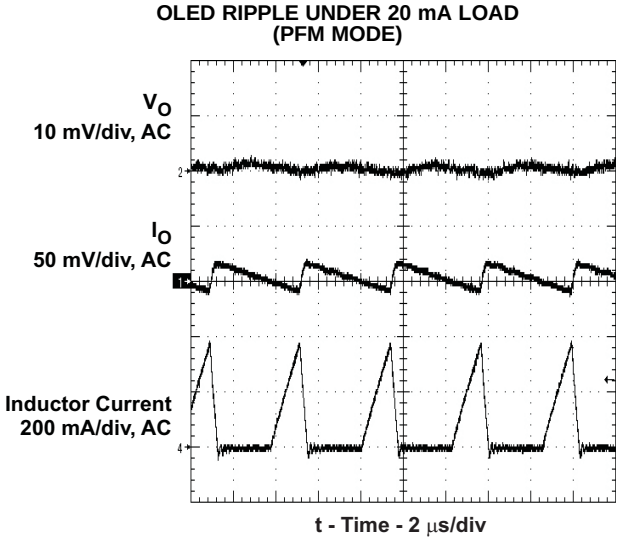


Figure 9.

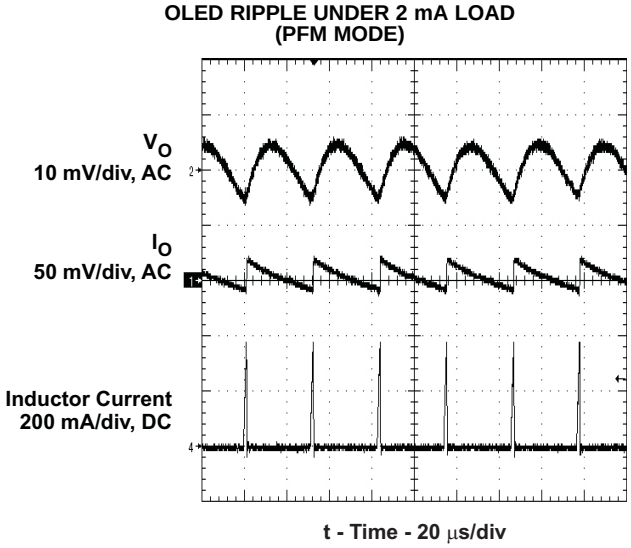


Figure 10.

WLED PWM BRIGHTNESS DIMMING

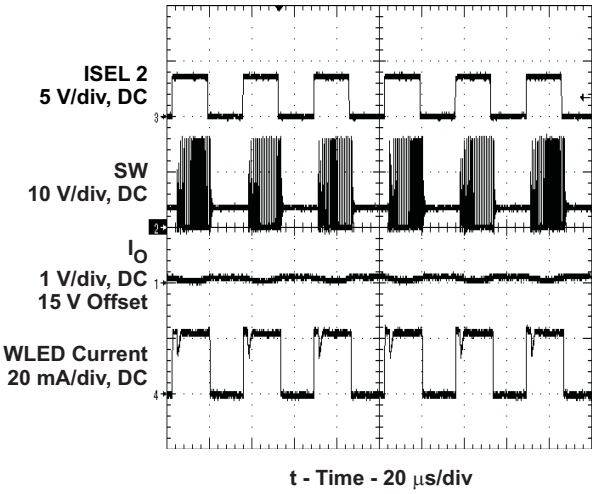


Figure 11.

WLED PWM BRIGHTNESS DIMMING LINEARITY

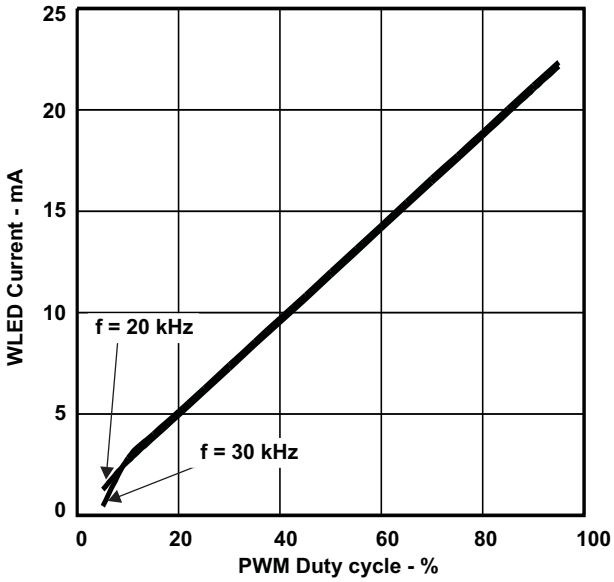


Figure 12.

TRANSITION BETWEEN 4WLED+OLED AND OLED ONLY (SELV ALWAYS HIGH)

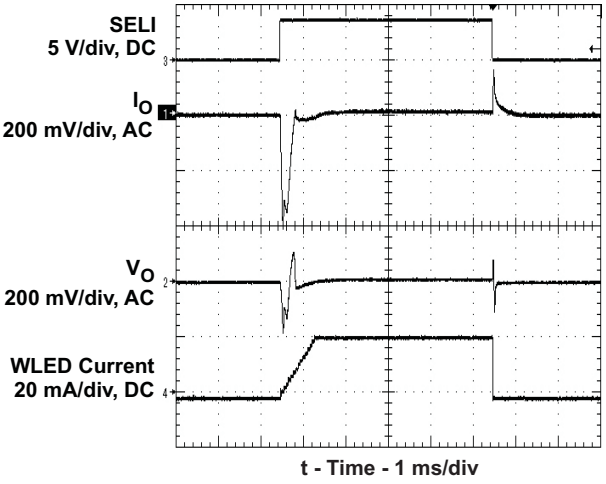


Figure 13.

WLED START UP

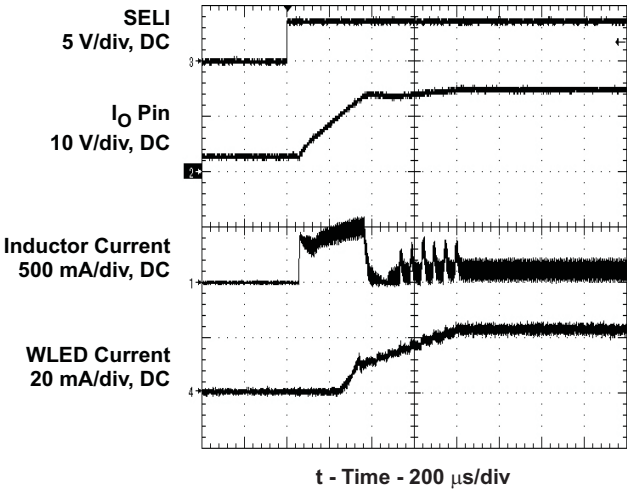


Figure 14.

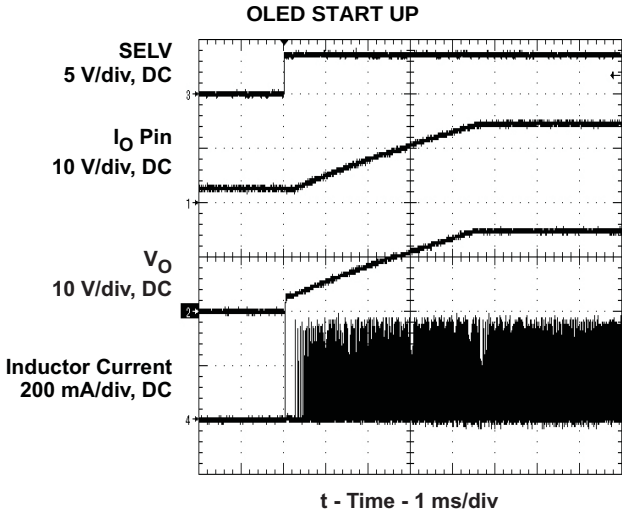


Figure 15.

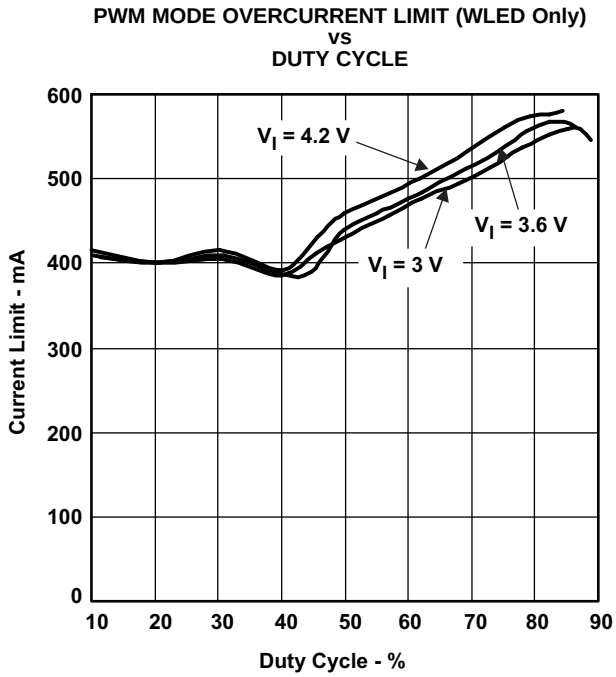


Figure 16.

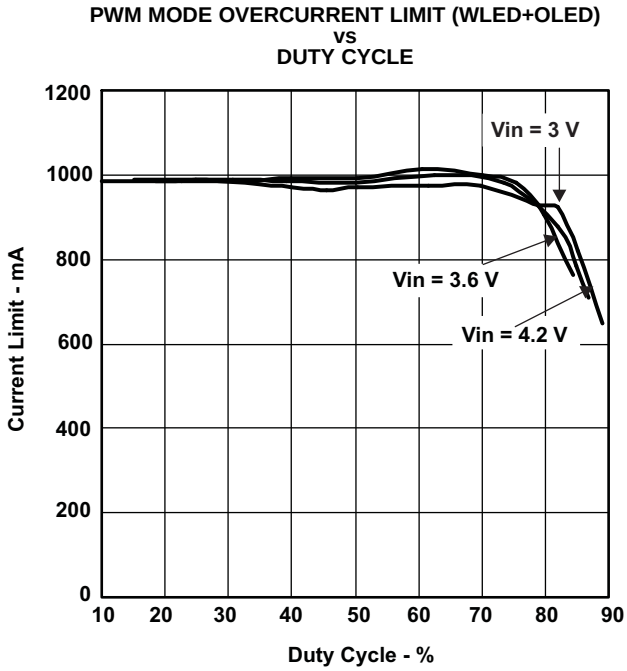


Figure 17.

DETAILED DESCRIPTION

The TPS61140/1 uses a single boost converter to provide pre-regulated power for the device's current output and voltage output. The current output is regulated by a low side current sink connected to the IFB pin, while a low dropout linear regulator (LDO) on the output of the boost regulator provides the voltage output. The LDO is used for its low ripple and fast transient response. The device automatically sets the boost output voltage to minimize power losses of the linear circuits (i.e., the current sink and LDO), and yet provide enough headroom for their dc operation and transient response. Such an implementation takes advantage of the high quality output of linear circuits, while maintaining high efficiency offered by the boost converter.

VOLTAGE OUTPUT MODE

When only the voltage output is enabled (i.e., SELV high and SELI low), LDO pass element Q2, shown in the block diagram, regulates Vout per the external resistor divider connected to the VFB pin. Current sink Q3 turns off, thereby opening the current path. The boost converter operates in PFM (pulse frequency modulation) mode for high efficiency over a wide load range. Operating in PFM mode, the device turns on the power switch Q1 when the voltage drop across the LDO (i.e., $V(I_{OUT})–V_{OUT}$) falls below the regulation voltage (V_{delta}). The input voltage is applied across the inductor, and its current linearly increases until reaching current limit, upon which Q1 is turned off. At this time, the built-in power diode is then forward biased and releases the inductor energy to the output. After the minimum off time, Q1 is allowed to turn back on again only if the voltage across the LDO is still below the threshold. Otherwise, Q1 stays off to reduce the switching losses and IC quiescent current. The minimum off time ensures discontinuous operation (DCM) in which inductor current always ramps down to zero in each switching cycle. DCM operation is required for feedback loop stability. There is also a maximum Q1 on time which turns off Q1 even if the current is still below the current limiting threshold. By minimizing the voltage drop across the LDO, the LDO maintains high efficiency. For 15V output, the LDO accounts for approximately 2% of efficiency loss.

Because PFM control reduces the switch frequency at light load, the boost regulator produces higher output ripple. Fortunately, the LDO's high PSRR (power supply rejection ratio) attenuates the ripple on the VOUT pin for optimal OLED display performance.

The output voltage of the Vout pin can be programmed by the resistor divider connected to the VFB pin, as shown in the Typical Application.

$$Vout = VFB \times \frac{(R1 + R2)}{R2} \quad (1)$$

Where VFB = reference voltage of the VFB pin

CURRENT OUTPUT MODE

When only the current output is selected (i.e., SELV low and SELI high), the LDO, and therefore VOUT is turned off, and the current sink device Q3, shown in the block diagram, regulates the current output. The boost converter uses fixed frequency PWM control to provide high output current and low output ripple noises. In this mode, the feedback loop regulates the IFB pin to a threshold voltage (V_{IFB}), giving current sink circuit minimum headroom to operate and minimizing losses across the current sink circuit.

The regulation current is set by the resistor on the Iset pin based on

$$I_O = \frac{V_{ISET}}{R_{SET}} \times K_{ISET} \quad (2)$$

where

I_O = output current
V_{ISET} = Iset pin voltage (1.229V typical)
R_{SET} = Iset pin resistor value
K_{ISET} = current multiplier (900 typical)

DETAILED DESCRIPTION (continued)

BOTH ON MODE

When both the voltage and current outputs are enabled (i.e., SELV high and SELI high), the boost converter operates in the PWM mode and regulates to the one requiring higher I_{OUT} pin voltage by choosing the smaller of $V(I_{OUT})–V_{OUT}$ and $V_{(IFB)}$ as the feedback signal. For example, if voltage regulation requires higher boost output, $V(I_{OUT})–V_{OUT}$ is automatically selected as feedback signal for the boost converter. During this time, the IFB pin voltage is higher than its regulation voltage (V_{IFB}). However, if the IFB pin voltage drops below its regulation voltage by the IFB low threshold (V_{IFB_L}), the PWM loop switches its feedback path to the IFB pin to ensure the proper operation of current sink circuit. The same operation occurs if the current output requires higher boost output. When both $V(I_{OUT})–V_{OUT}$ and V(IFB) are below their respective low thresholds, the $V(I_{OUT})–V_{OUT}$ takes priority as the boost converter's feedback signal.

The overall efficiency in this mode depends on the voltage difference between the current and voltage loads. A large difference reduces the efficiency due to additional power losses across the linear circuits (i.e., either the LDO or current sink circuit).

START UP

During start up, two feedback loops for the boost converter and linear regulators, are trying to establish steady state simultaneously. Figure 14 and Figure 15 demonstrate the start up waveform for WLED only and OLED only outputs.

When only the voltage output is enabled, the Vout ramp time is set by the LDO. The LDO uses an internal RC circuit to slow down the startup ramp and limit in-rush current. The boost converter output $V(I_{OUT})$ ramps up with the LDO output V_O maintaining a fixed voltage across the LDO. The boost converter charges both C2 and C3 shown in the block diagram, and the peak inductor current is clamped by the overcurrent limit circuitry.

When only the current output is enabled, Q3 control circuitry ramps up the sink current in 16 steps with each step taking 64 clock cycles. This soft start mode makes the current sink loop slower than the boost converter’s loop. Therefore, the boost output can only slowly comes up as the current sink circuitry increases its needed voltage. This ensures smooth start up and avoids any in rush current.

Soft start is also important for transitioning from voltage only to both on mode. During transition, soft start slowly adds the load, thereby giving the boost converter enough time to ramp the inductor current and preventing LDO drop out or V_O voltage dip.

OVERVOLTAGE PROTECTION

To prevent the boost output run away as the result of WLED disconnection, there is an overvoltage protection (OVP) circuit which stops the boost converter from switching as soon as its output exceeds the OVP threshold. When the voltage falls below the OVP threshold, the converter resumes switching.

The two OVP options offer the choices to prevent a 25-V rated output capacitor or the internal 30-V FET from breaking down.

UNDERVOLTAGE LOCKOUT

An undervoltage lockout prevents mis-operation of the device for input voltages below 1.65 V (typical). When the input voltage is below the undervoltage threshold, the device remains off and both the boost converter and linear circuit are turned off, providing isolation between input and output.

THERMAL SHUTDOWN

An internal thermal shutdown turns off the IC when the typical junction temperature of 160°C is exceeded. The thermal shutdown has a hysteresis of typically 15°C.

DETAILED DESCRIPTION (continued)

ENABLE

Pulling either the SELI or SELV pin low turns off the corresponding output. If both SELI and SELV are low for more than 40 ms, the IC shuts down and consumes less than 1 µA current. When only the current output is selected for driving WLED, the SELI pin can be used for PWM brightness dimming. To improve PWM dimming linearity, soft start is disabled if the time between falling and rising edges of two adjacent SELI pulses is less than 40 ms. See APPLICATION INFORMATION for details on PWM dimming.

Each SELx input pin has an internal pull down resistor to disable the device when the pin is floating.

APPLICATION INFORMATION

MAXIMUM OUTPUT CURRENT – PWM CONTROL

The over-current limit in a boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change maximum current output. Since current limit clamps peak inductor current, ripple has to be subtracted to derive maximum DC current. The ripple current is a function of switching frequency, inductor value and duty cycle. The following equations take into account of all the above factors for maximum output current calculation.

$$I_p = \frac{1}{\left[L \times \left(\frac{1}{Viout + Vf - Vin} + \frac{1}{Vin}\right) \times Fs\right]} \tag{3}$$

where

Ip = inductor peak to peak ripple

L = inductor value

Vf = power diode forward voltage

Fs = Switching frequency

Viout = boost output voltage. It is equal to the higher of either 330 mV + Vout or 330 mV + voltage drop across WLED.

$$Iout_max = \frac{Vin \times \left(Ilim - \frac{I_p}{2}\right) \times \eta}{Viout} \tag{4}$$

where

Iout_max = Maximum output current of the boost converter

Ilim = overcurrent limit

η = efficiency

To keep a tight range of the overcurrent limit, The TPS61140/1 uses the Vin and Iout pin voltage to compensate for the overcurrent limit variation caused by the slope compensation. However, the current threshold still has residual dependency on the Vin and Iout voltage. Use Figure 16 and Figure 17 to identify the typical overcurrent limit in your application, and use ±25% tolerance to account for temperature dependency and process variations.

The maximum output current can also be limited by the current capability of the LDO and the current sink circuitry. Both are designed to provide maximum 35 mA current regardless of the current capability of the boost converter.

MAXIMUM OUTPUT CURRENT – PFM CONTROL

When only voltage output is selected, the boost operates in PFM mode, and the maximum output current can be calculated as,

$$T_{on} = \frac{L \times I_{lim}}{V_{in}} \tag{5}$$

$$T_{off} = \frac{L \times I_{lim}}{V_{iout} + V_f - V_{in}} \tag{6}$$

$$I_{out_max} = \frac{\eta \times I_{lim} \times V_{IN}}{2V_{iout}} \frac{T_{on} + T_{off}}{T_{on} + T_{off_min}} \tag{7}$$

T_{off_min} = minimum off time

APPLICATION INFORMATION (continued)

To estimate worse case maximum output current, use following conditions

Vin = lowest input voltage

Vf = 1 V

In applications, overcurrent limit I_{lim} in the PFM mode is typically 60mA higher than the value listed in the ELECTRICAL CHARACTERISTICS which is measured with DC current. In reality, the inductor current ramps pass specification value due to the delay of the overcurrent limit comparator.

The LDO has 35 mA maximum output current, regardless of the current output capability of the boost converter.

WLED BRIGHTNESS DIMMING

There are three ways to dynamically change the output current *'on the fly"* for WLED dimming. The first method parallels an additional resistor with the ISET pin resistor as shown in Figure 18 . The switch, Q1, can change the ISET pin resistance, and therefore, modify the output current. This method is simple, but can only provide limited dimming steps.

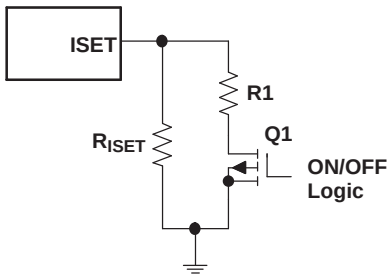


Figure 18. Switching In/Out an Additional Resistor to Change Output Current

Alternatively, a PWM dimming signal at the SELI pin will modulate the output current by the duty cycle of the signal. The logic high of the signal turns on the current sink circuit, while the logic low turns it off. This operation creates an averaged dc output current proportional to the duty cycle of the PWM signal. The frequency of the PWM signal must be high enough to avoid flashing of the WLEDs. The soft start of the current sink circuit is disabled during the PWM dimming to improve linearity.

PWM dimming in the audible frequency range can cause audible noises from the inductor and/or output capacitor of the boost converter. A voltage ripple in the audible frequency range causes the output capacitor to vibrate at the same frequency. Because the TPS61140/1 disconnects the WLEDs from the output capacitor when the SELI pin is low, the output capacitor is not discharged by the WLEDs, which reduces the voltage ripple, and potential for audible noise from the output capacitor.

Audible noises from both the inductor and output capacitor can be prevented by using a PWM dimming frequency above or below the audible frequency range. The maximum PWM dimming frequency of the TPS61140/1 is determined by the current settling time (Tisink) which is the time required for the circuit sink circuit to reach steady state after the SELI pin transitions from low to high. The maximum dimming frequency can be calculated by:

$$F_{PWM_MAX} = \frac{D_{min}}{T_{isink}} \tag{8}$$

D_{min} = min duty cycle of the PWM dimming required in the application.

For 20% D_{min}, PWM dimming frequency up to 33 kHz is possible, which is above the audible range.

The third method uses an external dc voltage and resistor as shown in Figure 19 to change the ISET pin current, and thus control the output current. The dc voltage can be the output of a filtered PWM signal. The equation to calculate the output current is either

$$I_{WLED} = K_{ISET} \times \left(\frac{1.229}{R_{ISET}} + \frac{1.229 - V_{DC}}{R_1} \right) \text{ for DC voltage input} \tag{9}$$

APPLICATION INFORMATION (continued)

OR

$$I_{WLED} = K_{ISET} \times \left(\frac{1.229}{R_{ISET}} + \frac{1.229 - V_{DC}}{R_1 + 10K} \right) \text{ for PWM signal input} \quad (10)$$

where K_{ISET} = current multiplier between the ISET pin current and the IFB pin current.

V_{DC}= voltage of the DC voltage source or the DC value of the PWM signal source.

Figure 19. Analog Dimming Uses an External Voltage Source to Control the Output Current

INDUCTOR SELECTION

Because the selection of the inductor affects the power supply's steady state operation (e.g., efficiency and output ripple), transient behavior and loop stability, the inductor is the most important component in power regulator design. There are three specifications most important to the performance of the inductor, inductor value, DC resistance and saturation current. Considering inductor value alone is not enough.

The inductor's inductance value determines the inductor ripple current. It is generally recommended setting the peak to peak ripple current given by Equation 3 to 30–40% of the dc current. It is a good compromise of power losses and inductor size. For this reason, 10 µH inductors are recommended for TPS61140/1. Inductor DC current can be calculated as

$$I_{L_DC} = \frac{V_{iout} \times I_{out}}{V_{in} \times \eta} \quad (11)$$

Use the maximum load current and minimum Vin for calculation.

The internal loop compensation for PWM control is optimized for the external component values, including typical tolerances, shown in the typical application circuit. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20 to 35% from the 0A value depending on how the inductor vendor defines saturation. Using an inductor with a smaller inductance value forces discontinuous PWM operation in which the inductor current ramps down to zero before the end of each switching cycle. It reduces the boost converter's maximum output current, and causes large input voltage ripple. An inductor with larger inductance will reduce the gain and phase margin of the feedback loop, possibly resulting in instability.

Inductor selection is also important for PFM operation. As seen in $I_{(out_max)}$ calculation, the maximum output current in PFM mode goes up with the inductor's inductance value. A smaller value inductor, such as 4.7 µH, reduces the available output current, while a larger inductor raises the risk of instability by entering continuous operation.

Regulator efficiency is dependent on the resistance of its high current path and switching losses associated with the PWM switch and power diode. Although the TPS61140/1 has optimized the internal switches, the overall efficiency still relies on inductor's DC resistance (DCR); Lower DCR improves efficiency. However, there is a trade off between DCR and inductor size, furthermore, shielded inductors typically have higher DCR than unshielded ones. DCR in range of 150 mΩ to 350 mΩ is suitable for applications requiring both on mode. DCR is the range of 250 mΩ to 450 mΩ is a good choice for single output application. Table 2 and Table 3 list recommended inductor models.

Table 2. Recommended Inductors for Single Output

	L (μH)	DCR Typ (mΩ)	Isat (A)	SIZE (L×W×H mm)
TDK				
VLF3012AT-100MR49	10	360	0.49	2.8×3.0×1.2
VLCF4018T-100MR74-2	10	163	0.74	4.0×4.0×1.8
Sumida				
CDRH2D11/HP	10	447	0.52	3.2×3.2×1.2
CDRH3D16/HP	10	230	0.84	4.0×4.0×1.8

Table 3. Recommended Inductors for Both-On Mode

	L (μH)	DCR Typ (mΩ)	Isat (A)	SIZE (L×W×H mm)
TDK				
VLCF4018T-100MR74-2	10	163	0.74	4X4.0X1.8
VLF4012AT-100MR79	10	300	0.85	3.5X3.7X1.2
Sumida				
CDRH3D16/HP	10	230	0.84	4X4.0X1.8
CDRH4D11/HP	10	340	0.85	4.8X4.8X1.2

INPUT AND OUTPUT CAPACITOR SELECTION

The output capacitor is mainly selected to minimize the output ripple from the converter. This ripple voltage is the sum of the ripple caused by the capacitor's capacitance and its equivalent series resistance (ESR). Assuming fixed frequency PWM operation and a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by

$$C_{out} = \frac{\left(V_{iout} - V_{in}\right) I_{out}}{V_{iout} \times Fs \times V_{ripple}} \tag{12}$$

V_{ripple} = Peak-to-peak output ripple.

For V_I = 3.6 V, V_O = 20 V, and F_s = 1.2 MHz, 0.1% ripple (20 mV) would require 4.7-μF capacitor. For this value, ceramic capacitors are the best choice for its size, cost and availability.

The additional output ripple component caused by ESR is calculated using:

$V_{(ripple_ESR)} = I_{out} \times R_{(ESR)}$

$V_{(ripple_ESR)}$ can be neglected for ceramic capacitors due to their low ESR, but must be considered if tantalum or electrolytic capacitors are used.

During a load transient, the capacitor at the output of the boost converter has to supply or absorb additional current before the inductor current ramps up the steady state value. Larger capacitors always help to reduce the voltage over and under shoot during a load transient. A larger capacitor also helps improve loop stability. When the OLED output is enabled, a load transient disturbs the output of the boost converter when the WLED output is enabled or disabled. Although the LDOs PSRR (power supply rejection ratio) reduces the disturbance propagated to the V_O, additional capacitance may be needed if a high precision OLED voltage is required. For its stability, the LDO requires a minimum output capacitance (C3 in the block diagram) of 1 μF. Additional capacitance improves the LDO's PSRR for low frequency noises.

Care must be taken when evaluating a ceramic capacitors derating due to applied dc voltage, aging and over frequency. For example, larger form factor capacitors (in 1206 size) have their self resonant frequencies in the range of the TPS61140/1's switching frequency. So the effective capacitance is significantly lower. Therefore, it may be necessary to use small capacitors in parallel instead of one large capacitor.

The popular vendors for high value ceramic capacitors are:

TDK (http://www.component.tdk.com/components.php)

Murata (http://www.murata.com/cap/index.html)

Table 4. Recommended Input and Output Capacitors

	Capacitance (μF)	Voltage (V)	Case
TDK			
C3216X5R1E475K	4.7	25	1206
C2012X5R1E105K	1	25	805
C1005X5R0J105K	1	6.3	402
Murata			
GRM319R61E475KA12D	4.7	25	1206
GRM216R61E105KA12D	1	25	805
GRM155R60J105KE19D	1	6.3	402

LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor needs not only to be close to the Vin pin, but also to the GND pin in order to reduce the input ripple seen by the IC. The Vin and SW pins are conveniently located on the edges of the IC, therefore the inductor can be placed close to the IC. The output capacitor needs to be placed near the load to minimize ripple and maximize transient performance.

It is also beneficial to have the ground of the output capacitor close to the GND pin since there will be large ground return current flowing between them. When laying out signal ground, it is recommended to use short traces separated from power ground traces, and connect them together at a single point.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA00234DRCRG4	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BCP	Samples
TPS61140DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BCP	Samples
TPS61140DRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BCP	Samples
TPS61140DRCTG4	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BCP	Samples
TPS61141DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRG	Samples
TPS61141DRCRG4	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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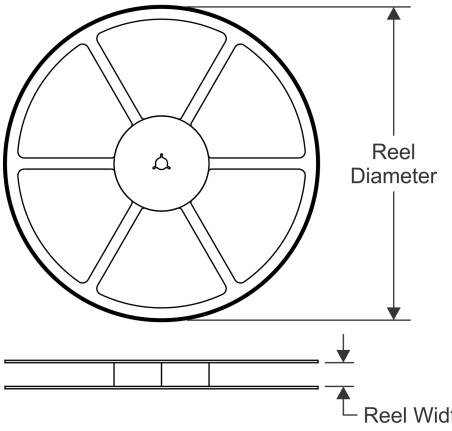
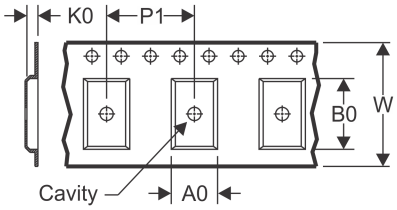
TAPE AND REEL INFORMATION

REEL DIMENSIONS

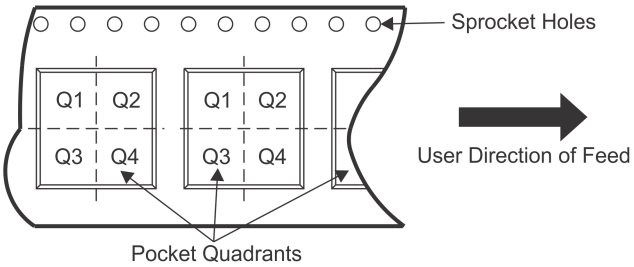


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

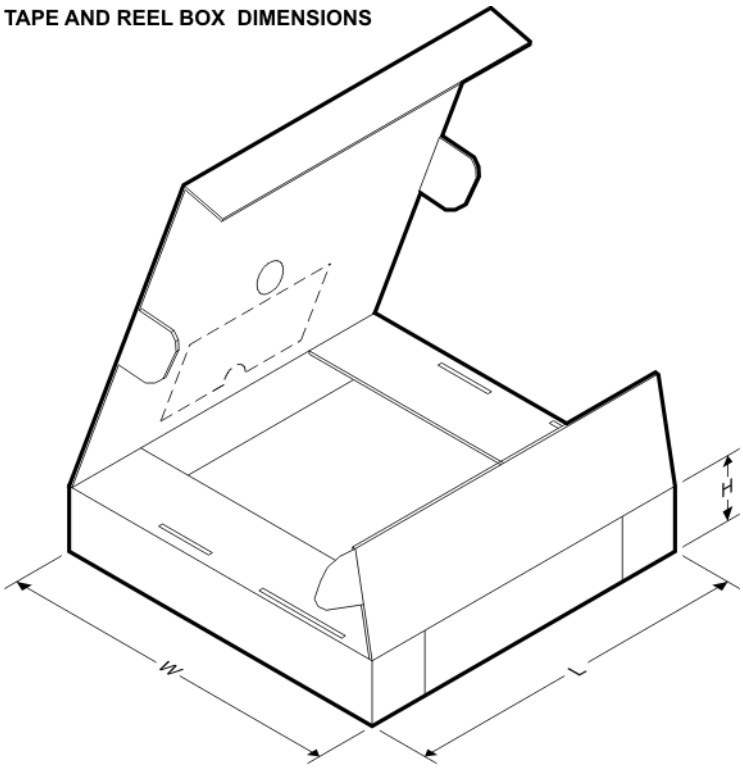
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61140DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61140DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61141DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61140DRCR	VSON	DRC	10	3000	853.0	449.0	35.0
TPS61140DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS61141DRCR	VSON	DRC	10	3000	853.0	449.0	35.0

GENERIC PACKAGE VIEW

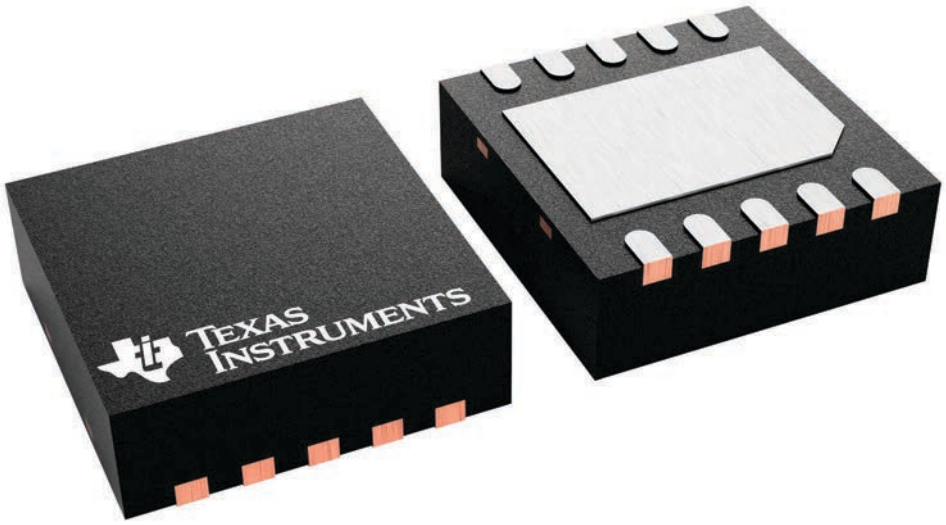
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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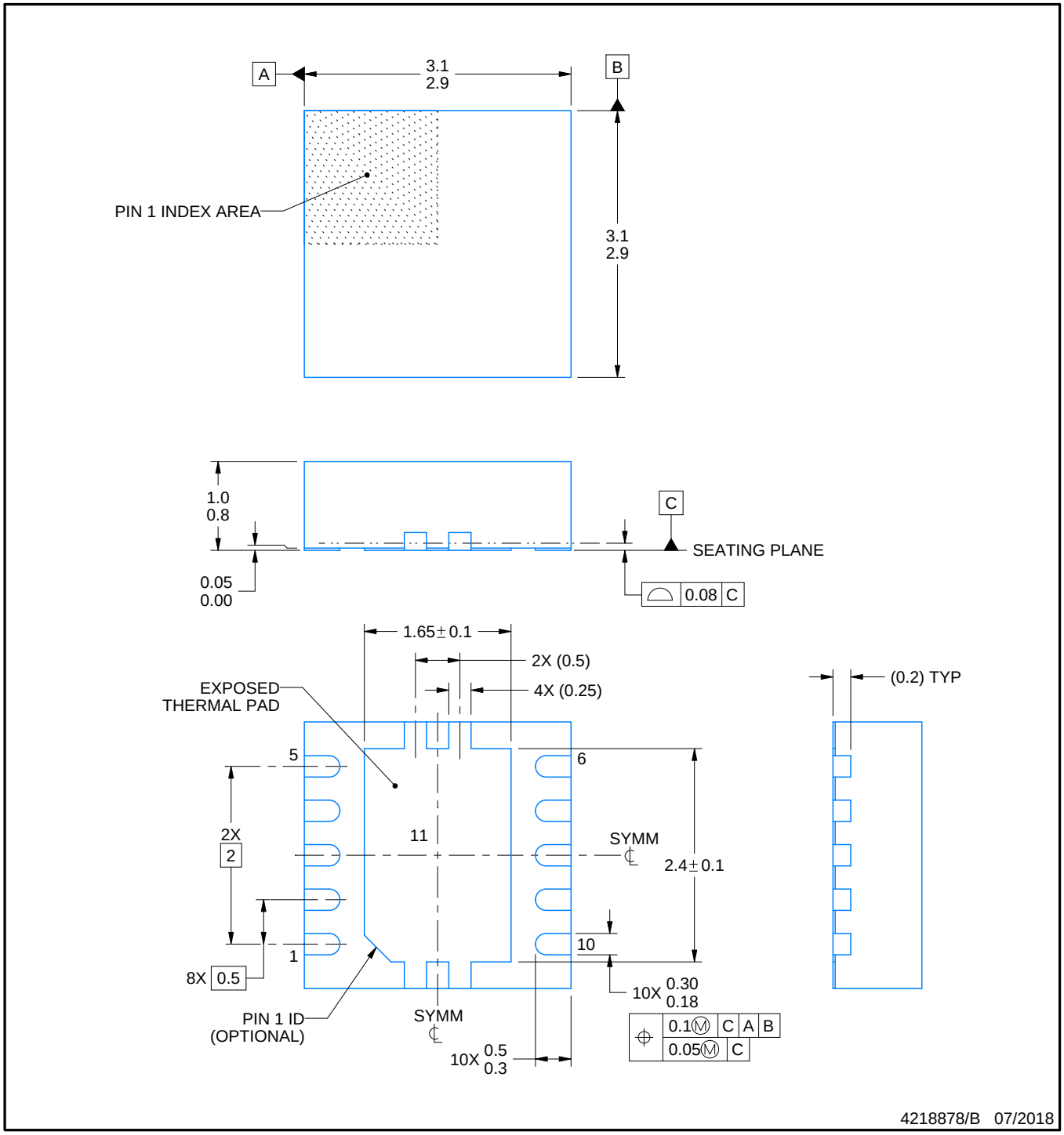
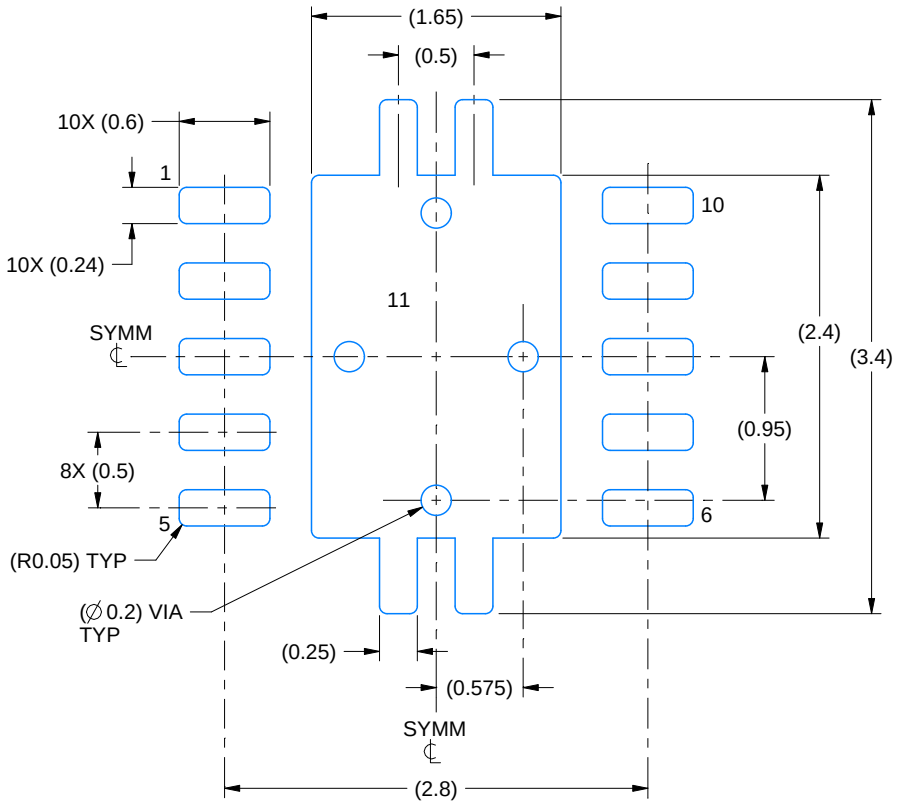
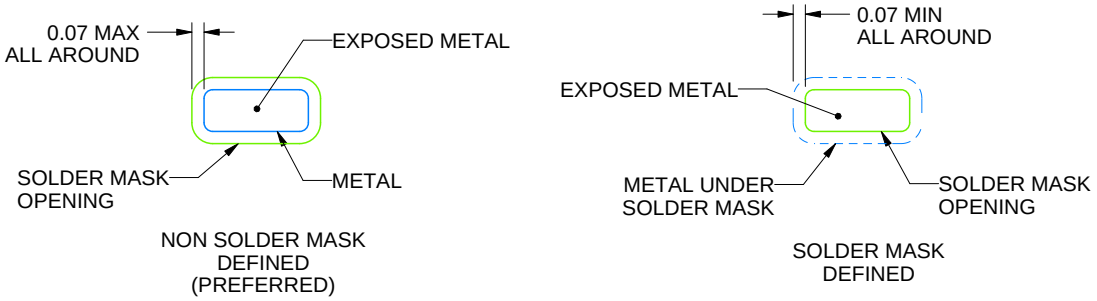


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

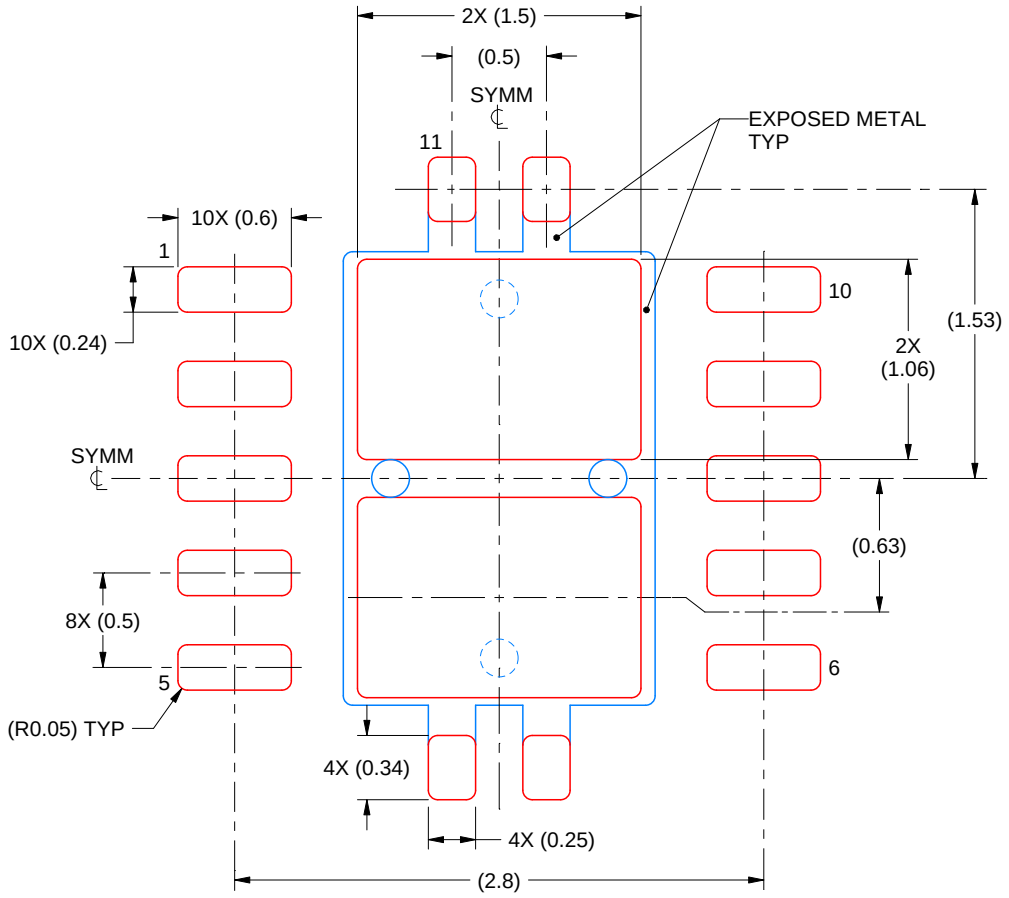


SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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