

# ADSxx54 双路高速 16 位、14 位和 12 位 同步采样模数转换器

## 1 特性

- 16 位、14 位和 12 位引脚兼容系列
- 双通道同步采样
- 支持全差分输入
- 高速：
  - ADS8354: 16 位, 700kSPS
  - ADS7854: 14 位, 1MSPS
  - ADS7254: 12 位, 1MSPS
- 出色的直流性能：
  - ADS8354:
    - 16 位丢码率 (NMC) 差分非线性 (DNL),  $\pm 2.5$  最低有效位 (LSB), 最大积分非线性 (INL)
  - ADS7854:
    - 14 位 NMC DNL,  $\pm 1.5$  LSB, 最大 INL
  - ADS7254:
    - 12 位 NMC DNL,  $\pm 1$  LSB, 最大 INL
- 出色的交流性能：
  - ADS8354:
    - 93dB 信噪比 (SNR), -100dB 总谐波失真 (THD)
  - ADS7854:
    - 88dB SNR, -95dB THD
  - ADS7254:
    - 72dB SNR, -90dB THD
- 双路、可编程和经缓冲的 2.5V 内部基准电压
- 在  $-40^{\circ}\text{C}$  至  $125^{\circ}\text{C}$  的扩展工业温度范围内完全额定运行
- 小封装尺寸：  
16 引脚超薄型四方扁平无引线 (WQFN) 封装

(3mm x 3mm) 和 16 引脚薄型小外形尺寸 (TSSOP) 封装

## 2 应用

- 电机控制：  
使用编码器进行位置测量
- 光纤网络：掺铒光纤放大器 (EDFA) 增益控制环路
- 保护中继器
- 电源质量测量
- 三相电源控制
- 可编程逻辑控制器

## 3 说明

ADS8354、ADS7854 和 ADS7254 均属于引脚兼容的双路高速同步采样模数转换器 (ADC) 产品系列, 支持全差分模拟输入。

每个器件均包含两个可独立编程的基准电压源, 可用于系统级的增益校准。并且配有一个可在宽电源供电范围内运行的灵活串行接口, 从而轻松实现与多种主机控制器的通信。该系列器件支持两种低功耗模式, 可针对给定输出优化功耗。所有器件都在扩展工业温度范围 ( $-40^{\circ}\text{C}$  至  $+125^{\circ}\text{C}$ ) 内完全额定运行, 并且采用引脚兼容的 WQFN-16 (3mm x 3mm) 和 TSSOP-16 封装。

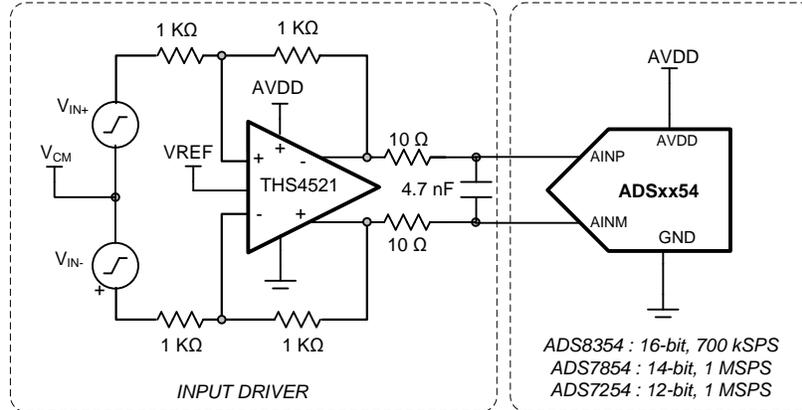
器件信息<sup>(1)</sup>

部件号	封装	封装尺寸 (标称值)
ADSxx54	TSSOP (16)	5.00mm x 4.40mm
	WQFN (16)	3.00mm x 3.00mm

(1) 如需了解所有可用封装, 请见数据表末尾的可订购产品附录。



典型应用图



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## 4 修订历史记录

<b>Changes from Revision A (July 2014) to Revision B</b>	<b>Page</b>
• 更改了 ADS8354 预览器件并移动到了生产数据状态 .....	1
• 将文档状态从混合状态更改为生产数据 .....	1
• Corrected cross-reference for <a href="#">Figure 98</a> .....	47

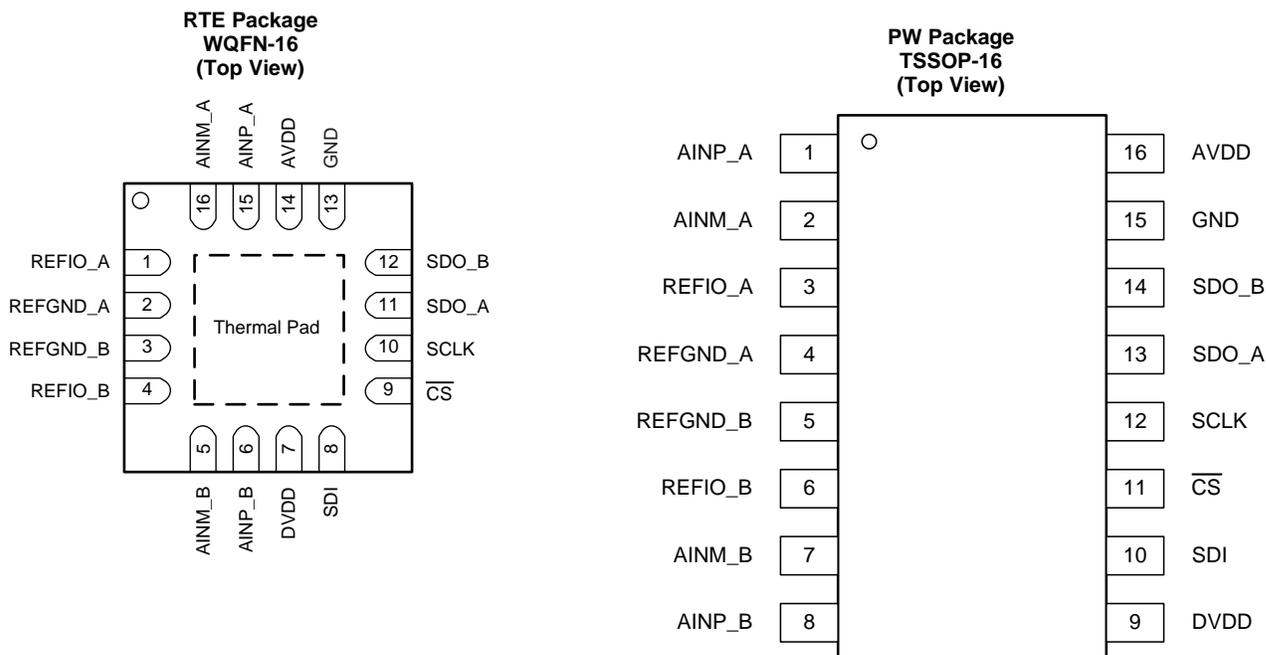
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<b>Changes from Original (October 2013) to Revision A</b>	<b>Page</b>
• 更改了产品预览数据表 .....	1

## 5 Device Comparison Table

PRODUCT	RESOLUTION (Bits)	INPUT CONFIGURATION	NMC (Bits)	INL (LSB)	SNR (dB)
ADS8354	16	Fully-differential	16	±2.5	93 (typ)
ADS7854	14	Fully-differential	14	±1.5	88 (typ)
ADS7254	12	Fully-differential	12	±1	74 (typ)
ADS8353	16	Single-ended and pseudo-differential	16	±2.5	89 (typ)
ADS7853	14	Single-ended and pseudo-differential	14	±2	84 (typ)
ADS7253	12	Single-ended and pseudo-differential	12	±1	73.5 (typ)

## 6 Pin Configurations and Functions



### Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	TSSOP	WQFN		
AINM_A	2	16	Analog input	Negative analog input, channel A
AINM_B	7	5	Analog input	Negative analog input, channel B
AINP_A	1	15	Analog input	Positive analog input, channel A
AINP_B	8	6	Analog input	Positive analog input, channel B
AVDD	16	14	Supply	Supply voltage for ADC operation
$\overline{\text{CS}}$	11	9	Digital input	Chip-select signal; active low
DVDD	9	7	Digital I/O supply	Digital I/O supply
GND	15	13	Supply	Digital ground
REFGND_A	4	2	Supply	Reference ground potential A
REFGND_B	5	3	Supply	Reference ground potential B
REFIO_A	3	1	Analog input/output	Reference voltage input/output, channel A
REFIO_B	6	4	Analog input/output	Reference voltage input/output, channel B
SCLK	12	10	Digital input	Clock for serial communication
SDI	10	8	Digital input	Data input for serial communication
SDO_A	13	11	Digital output	Data output for serial communication, channel A and channel B
SDO_B	14	12	Digital output	Data output for serial communication, channel B
Thermal pad	—	Thermal pad	Supply	Exposed thermal pad (only for WQFN). TI recommends connecting this pin to the printed circuit board (PCB) ground.

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
AVDD to REFGND_x or DVDD to GND	-0.3	6	V
Analog (AINP_x and AINM_x) and reference input (REFIO_x) voltage with respect to REFGND_x	REFGND_x - 0.3	AVDD + 0.3	V
Digital input voltage with respect to GND	GND - 0.3	DVDD + 0.3	V
Ground voltage difference  REFGND_x-GND		0.3	V
Input current to any pin except supply pins		±10	mA
Maximum virtual junction temperature, T <sub>J</sub>		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 Handling Ratings

		MIN	MAX	UNIT	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	-2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	-500	500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage		5		V
DVDD	Digital supply voltage		3.3		V

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ADS8354, ADS7854, ADS7254		UNIT
		RTE (WQFN)	PW (TSSOP)	
		16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	33.3	86.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	29.5	21	
R <sub>θJB</sub>	Junction-to-board thermal resistance	7.3	39.1	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.2	0.8	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	7.4	38.4	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	0.9	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics: ADS8354

All minimum and maximum specifications are at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF\_A} = V_{REF\_B} = V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 700\text{ kSPS}$ , unless otherwise noted.

Typical values are at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ , and  $DVDD = 3.3\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>RESOLUTION</b>						
Resolution			16			Bits
<b>DC ACCURACY<sup>(1)</sup></b>						
NMC	No missing codes	32-clock mode	16			Bits
INL	Integral nonlinearity	32-clock mode	-2.5	±1	2.5	LSB
DNL	Differential nonlinearity	32-clock mode	-0.99	±0.7	2	LSB
$E_{IO}$	Input offset error		-1	±0.5	1	mV
	$E_{IO}$ match	ADC_A to ADC_B	-1	±0.5	1	mV
$dE_{IO}/dT$	Input offset thermal drift			±1		$\mu\text{V}/^\circ\text{C}$
$E_G$	Gain error	Referenced to the voltage at REFIO_x	-0.1	±0.05	0.1	%FS
	$E_G$ match	ADC_A to ADC_B	-0.1	±0.05	0.1	%FS
$dE_G/dT$	Gain error thermal drift	Referenced to the voltage at REFIO_x		±1		ppm/ $^\circ\text{C}$
CMRR	Common-mode rejection ratio	Both ADCs, dc to 20 kHz		70		dB
<b>AC ACCURACY<sup>(2)</sup></b>						
SINAD	Signal-to-noise + distortion	$V_{REF} = 2.5\text{ V}$ , $\pm V_{REF}$ input range, 32-clock mode		88.6		dB
		$V_{REF} = 2.5\text{ V}$ , $\pm 2 \times V_{REF}$ input range, 32-clock mode		88.4		dB
		$V_{REF} = 5\text{ V}$ (external), $\pm V_{REF}$ input range, 32-clock mode		92.2		dB
SNR	Signal-to-noise ratio	$V_{REF} = 2.5\text{ V}$ , $\pm V_{REF}$ input range, 32-clock mode		89		dB
		$V_{REF} = 2.5\text{ V}$ , $\pm 2 \times V_{REF}$ input range, 32-clock mode		89		dB
		$V_{REF} = 5\text{ V}$ (external), $\pm V_{REF}$ input range, 32-clock mode		93		dB
THD	Total harmonic distortion	$V_{REF} = 2.5\text{ V}$ , $\pm V_{REF}$ input range, 32-clock mode		-99		dB
		$V_{REF} = 2.5\text{ V}$ , $\pm 2 \times V_{REF}$ input range, 32-clock mode		-97.5		dB
		$V_{REF} = 5\text{ V}$ (external), $\pm V_{REF}$ input range, 32-clock mode		-100		dB
SFDR	Spurious-free dynamic range	$V_{REF} = 2.5\text{ V}$ , $\pm V_{REF}$ input range, 32-clock mode		100		dB
		$V_{REF} = 2.5\text{ V}$ , $\pm 2 \times V_{REF}$ input range, 32-clock mode		99		dB
		$V_{REF} = 5\text{ V}$ (external), $\pm V_{REF}$ input range, 32-clock mode		100		dB
ISOXT	ADC-to-ADC isolation	$f_{IN} = 15\text{ kHz}$ at 10 %FS, $f_{NOISE} = 25\text{ kHz}$ at FS		-110		dB

(1) LSB = least significant bit.

(2) All ac parameters are tested at -0.5 dBFS and a 20-kHz input frequency.

## 7.6 Electrical Characteristics: ADS7854

All minimum and maximum specifications are at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF\_A} = V_{REF\_B} = V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 1\text{ MSPS}$ , unless otherwise noted.

Typical values are at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ , and  $DVDD = 3.3\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>RESOLUTION</b>						
Resolution			14			Bits
<b>DC ACCURACY<sup>(1)</sup></b>						
NMC	No missing codes	32-clock mode	14			Bits
		16-clock mode	13			Bits
INL	Integral nonlinearity	32-clock mode	-1.5	±0.5	1.5	LSB
		16-clock mode	-2	±0.8	2	LSB
DNL	Differential nonlinearity	32-clock mode	-0.99	±0.4	1	LSB
		16-clock mode	-1	±0.7	2	LSB
E <sub>IO</sub>	Input offset error		-1	±0.5	1	mV
	E <sub>IO</sub> match	ADC_A to ADC_B	-1	±0.5	1	mV
dE <sub>IO</sub> /dT	Input offset thermal drift			±1		µV/°C
E <sub>G</sub>	Gain error	Referenced to the voltage at REFIO_x	-0.1	±0.05	0.1	%FS
	E <sub>G</sub> match	ADC_A to ADC_B	-0.1	±0.05	0.1	%FS
dE <sub>G</sub> /dT	Gain error thermal drift	Referenced to the voltage at REFIO_x		±1		ppm/°C
CMRR	Common-mode rejection ratio	Both ADCs, dc to 20 kHz		70		dB
<b>AC ACCURACY<sup>(2)</sup></b>						
SINAD	Signal-to-noise + distortion	V <sub>REF</sub> = 2.5 V, ±V <sub>REF</sub> input range	32-clock mode	81.8	83.7	dB
			16-clock mode		82.9	dB
		V <sub>REF</sub> = 2.5 V, ±2 × V <sub>REF</sub> input range	32-clock mode		83.7	dB
			16-clock mode		82.9	dB
		V <sub>REF</sub> = 5 V (external), ±V <sub>REF</sub> input range	32-clock mode		84.6	dB
			16-clock mode		84.1	dB
SNR	Signal-to-noise ratio	V <sub>REF</sub> = 2.5 V, ±V <sub>REF</sub> input range	32-clock mode	82	84	dB
			16-clock mode		83.5	dB
		V <sub>REF</sub> = 2.5 V, ±2 × V <sub>REF</sub> input range	32-clock mode		84	dB
			16-clock mode		83.5	dB
		V <sub>REF</sub> = 5 V (external), ±V <sub>REF</sub> input range	32-clock mode		85	dB
			16-clock mode		84.5	dB
THD	Total harmonic distortion	V <sub>REF</sub> = 2.5 V, ±V <sub>REF</sub> input range	32-clock mode	-95		dB
			16-clock mode		-92	dB
		V <sub>REF</sub> = 2.5 V, ±2 × V <sub>REF</sub> input range	32-clock mode		-95	dB
			16-clock mode		-92	dB
		V <sub>REF</sub> = 5 V (external), ±V <sub>REF</sub> input range	32-clock mode		-98	dB
			16-clock mode		-93	dB
SFDR	Spurious-free dynamic range	V <sub>REF</sub> = 2.5 V, ±V <sub>REF</sub> input range	32-clock mode		97.5	dB
			16-clock mode		95	dB
		V <sub>REF</sub> = 2.5 V, ±2 × V <sub>REF</sub> input range	32-clock mode		97.5	dB
			16-clock mode		95	dB
		V <sub>REF</sub> = 5 V (external), ±V <sub>REF</sub> input range	32-clock mode		99	dB
			16-clock mode		95	dB
ISOXT	ADC-to-ADC isolation	f <sub>IN</sub> = 15 kHz at 10 %FS, f <sub>NOISE</sub> = 25 kHz at FS		-90		dB

(1) LSB = least significant bit.

(2) All ac parameters are tested at -0.5 dBFS and a 20-kHz input frequency.

## 7.7 Electrical Characteristics: ADS7254

All minimum and maximum specifications are at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF\_A} = V_{REF\_B} = V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 1\text{ MSPS}$ , unless otherwise noted.

Typical values are at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ , and  $DVDD = 3.3\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>RESOLUTION</b>						
Resolution			12			Bits
<b>DC ACCURACY<sup>(1)</sup></b>						
NMC	No missing codes		12			Bits
INL	Integral nonlinearity		-1	±0.25	1	LSB
DNL	Differential nonlinearity		-0.99	±0.25	1	LSB
$E_{IO}$	Input offset error		-1	±0.5	1	mV
	$E_{IO}$ match	ADC_A to ADC_B	-1	±0.5	1	mV
$dE_{IO}/dT$	Input offset thermal drift			±1		µV/°C
$E_G$	Gain error	Referenced to the voltage at REFIO_x	-0.1	±0.05	0.1	%FS
	$E_G$ match	ADC_A to ADC_B	-0.1	±0.05	0.1	%FS
$dE_G/dT$	Gain error thermal drift	Referenced to the voltage at REFIO_x		±1		ppm/°C
CMRR	Common-mode rejection ratio	Both ADCs, dc to 20 kHz		70		dB
<b>AC ACCURACY<sup>(2)</sup></b>						
SINAD	Signal-to-noise + distortion	$V_{REF} = 2.5\text{ V}$ , ± $V_{REF}$ input range		73.4		dB
		$V_{REF} = 2.5\text{ V}$ , ±2 × $V_{REF}$ input range	72.4	73.4		dB
		$V_{REF} = 5\text{ V}$ (external), ± $V_{REF}$ input range		73.9		dB
SNR	Signal-to-noise ratio	$V_{REF} = 2.5\text{ V}$ , ± $V_{REF}$ input range		73.5		dB
		$V_{REF} = 2.5\text{ V}$ , ±2 × $V_{REF}$ input range	72.5	73.5		dB
		$V_{REF} = 5\text{ V}$ (external), ± $V_{REF}$ input range		74		dB
THD	Total harmonic distortion	$V_{REF} = 2.5\text{ V}$ , ± $V_{REF}$ input range		-92		dB
		$V_{REF} = 2.5\text{ V}$ , ±2 × $V_{REF}$ input range		-92		dB
		$V_{REF} = 5\text{ V}$ (external), ± $V_{REF}$ input range		-92		dB
SFDR	Spurious-free dynamic range	$V_{REF} = 2.5\text{ V}$ , ± $V_{REF}$ input range		95		dB
		$V_{REF} = 2.5\text{ V}$ , ±2 × $V_{REF}$ input range		95		dB
		$V_{REF} = 5\text{ V}$ (external), ± $V_{REF}$ input range		95		dB
ISOXT	ADC-to-ADC isolation	$f_{IN} = 15\text{ kHz}$ at 10 %FS, $f_{NOISE} = 25\text{ kHz}$ at FS		-100		dB

(1) LSB = least significant bit.

(2) All ac parameters are tested at -0.5 dBFS and a 20-kHz input frequency.

## 7.8 Electrical Characteristics: All Devices

All minimum and maximum specifications are at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF\_A} = V_{REF\_B} = V_{REF} = 2.5\text{ V}$ , and  $f_{DATA} = \text{maximum}$ , unless otherwise noted.

Typical values are at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ , and  $DVDD = 3.3\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG INPUT</b>						
FSR	Full-scale input range <sup>(1)</sup> (AINP_x – AINM_x)	$\pm V_{REF}$ range	$-V_{REF}$		$V_{REF}$	V
		$\pm 2 \times V_{REF}$ range, $AVDD \geq 2 \times V_{REF}$	$-2 \times V_{REF}$		$2 \times V_{REF}$	V
$V_{IN}$	Absolute input voltage (AINP_x and AINM_x to REFGND)	$\pm V_{REF}$ range	0		$V_{REF}$	V
		$\pm 2 \times V_{REF}$ range, $AVDD \geq 2 \times V_{REF}$	0		$2 \times V_{REF}$	V
$V_{CM}$	Common-mode voltage range (AINP_x + AINM_x) / 2	$\pm V_{REF}$ range	$(V_{REF} / 2) - 0.1$	$V_{REF} / 2$	$(V_{REF} / 2) + 0.1$	V
		$\pm 2 \times V_{REF}$ range	$V_{REF} - 0.1$	$V_{REF}$	$V_{REF} + 0.1$	V
$C_i$	Input capacitance	In sample mode		40		pF
		In hold mode		4		pF
$I_{lkg(i)}$	Input leakage current			0.1		$\mu\text{A}$
<b>INTERNAL VOLTAGE REFERENCE</b>						
$V_{REFOUT}$	Reference output voltage	REFDAC_x = 1FFh (default), at $25^\circ\text{C}$	2.495	2.500	2.505	V
$V_{REF-match}$	$V_{REF\_A}$ to $V_{REF\_B}$ matching	REFDAC_x = 1FFh (default), at $25^\circ\text{C}$		$\pm 1$		mV
		REFDAC_x resolution <sup>(2)</sup>		1.1		mV
$dV_{REFOUT}/dT$	Reference voltage temperature drift	REFDAC_x = 1FFh (default)		$\pm 10$		ppm/ $^\circ\text{C}$
$dV_{REFOUT}/dt$	Long-term stability	1000 hours		150		ppm
$R_O$	Internal reference output impedance			1		$\Omega$
$I_{REFOUT}$	Reference output dc current			2		mA
$C_{REFOUT}$	Recommended output capacitor			10		$\mu\text{F}$
$t_{REFON}$	Reference output settling time	For $C_{REF} = 10\ \mu\text{F}$		8		ms
<b>VOLTAGE REFERENCE INPUT</b>						
$V_{REF}$	Reference voltage (input)	$\pm V_{REF}$ range	2.4	2.5	AVDD	V
		$\pm 2 \times V_{REF}$ range	2.4	2.5	AVDD / 2	V
$I_{REF}$	Average Reference input current	Per ADC		300		$\mu\text{A}$
$C_{REF}$	External ceramic reference capacitance			10		$\mu\text{F}$
$I_{lkg(dc)}$	DC leakage current			$\pm 0.1$		$\mu\text{A}$
<b>SAMPLING DYNAMICS</b>						
$t_A$	Aperture delay			8		ns
		$t_A$ match	ADC_A to ADC_B		40	ps
$t_{AJIT}$	Aperture jitter			50		ps

(1) Ideal input span, does not include gain or offset error.

(2) Refer to the [Reference](#) section for more details.

**Electrical Characteristics: All Devices (continued)**

All minimum and maximum specifications are at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF\_A} = V_{REF\_B} = V_{REF} = 2.5\text{ V}$ , and  $f_{DATA} = \text{maximum}$ , unless otherwise noted.

Typical values are at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ , and  $DVDD = 3.3\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>DIGITAL INPUTS<sup>(3)</sup></b>							
$V_{IH}$	High-level input voltage	$DVDD > 2.3\text{ V}$	0.7 DVDD		DVDD + 0.3	V	
		$DVDD \leq 2.3\text{ V}$	0.8 DVDD		DVDD + 0.3	V	
$V_{IL}$	Low-level input voltage	$DVDD > 2.3\text{ V}$	-0.3		0.3 DVDD	V	
		$DVDD \leq 2.3\text{ V}$	-0.3		0.2 DVDD	V	
	Input current			±10		nA	
<b>DIGITAL OUTPUTS<sup>(3)</sup></b>							
$V_{OH}$	High-level output voltage	$I_{OH} = 500\text{-}\mu\text{A}$ source	0.8 DVDD		DVDD	V	
$V_{OL}$	Low-level output voltage	$I_{OH} = 500\text{-}\mu\text{A}$ sink	0		0.2 DVDD	V	
<b>POWER SUPPLY</b>							
$AVDD$	Analog supply voltage (AVDD to AGND)	$\pm V_{REF}$ range	Internal reference	4.5	5.0	5.5	V
			External reference: $V_{EXT\_REF} < 4.5\text{ V}$	4.5	5.0	5.5	V
			External reference: $V_{EXT\_REF} > 4.5\text{ V}$	$V_{EXT\_REF}$	5.0	5.5	V
		$\pm 2 \times V_{REF}$ range	Internal reference	5.0	5.0	5.5	V
			External reference	$2 \times V_{REF\_EXT}$	5.0	5.5	V
$DVDD$	Digital supply voltage (DVDD to AGND)		1.65		5.5	V	
$AIDD$	Analog supply current	$AVDD = 5\text{ V}$ , fastest throughput internal reference		8.5	10	mA	
		$AVDD = 5\text{ V}$ , fastest throughput external reference <sup>(4)</sup>		7.5		mA	
		$AVDD = 5\text{ V}$ , no conversion internal reference		5.5	7	mA	
		$AVDD = 5\text{ V}$ , no conversion external reference <sup>(4)</sup>		4.5		mA	
		$AVDD = 5\text{ V}$ , STANDBY mode Internal Reference		2.5		mA	
		$AVDD = 5\text{ V}$ , STANDBY mode external reference <sup>(4)</sup>		1		mA	
		Power-down mode		10	50	μA	
$DIDD$	Digital supply current	$DVDD = 3.3\text{ V}$ , $C_{LOAD} = 10\text{ pF}$ , fastest throughput		0.5		mA	
		$DVDD = 5\text{ V}$ , $C_{LOAD} = 10\text{ pF}$ fastest throughput		1		mA	
$P_D$	Power dissipation (normal operation)	$AVDD = 5\text{ V}$ , fastest throughput, internal reference		42.5	50	mW	

(3) Specified by design; not production tested.

(4) With internal reference powered down,  $CFR.B6 = 0$ .

## 7.9 Timing Requirements: Interface Mode<sup>(1)</sup>

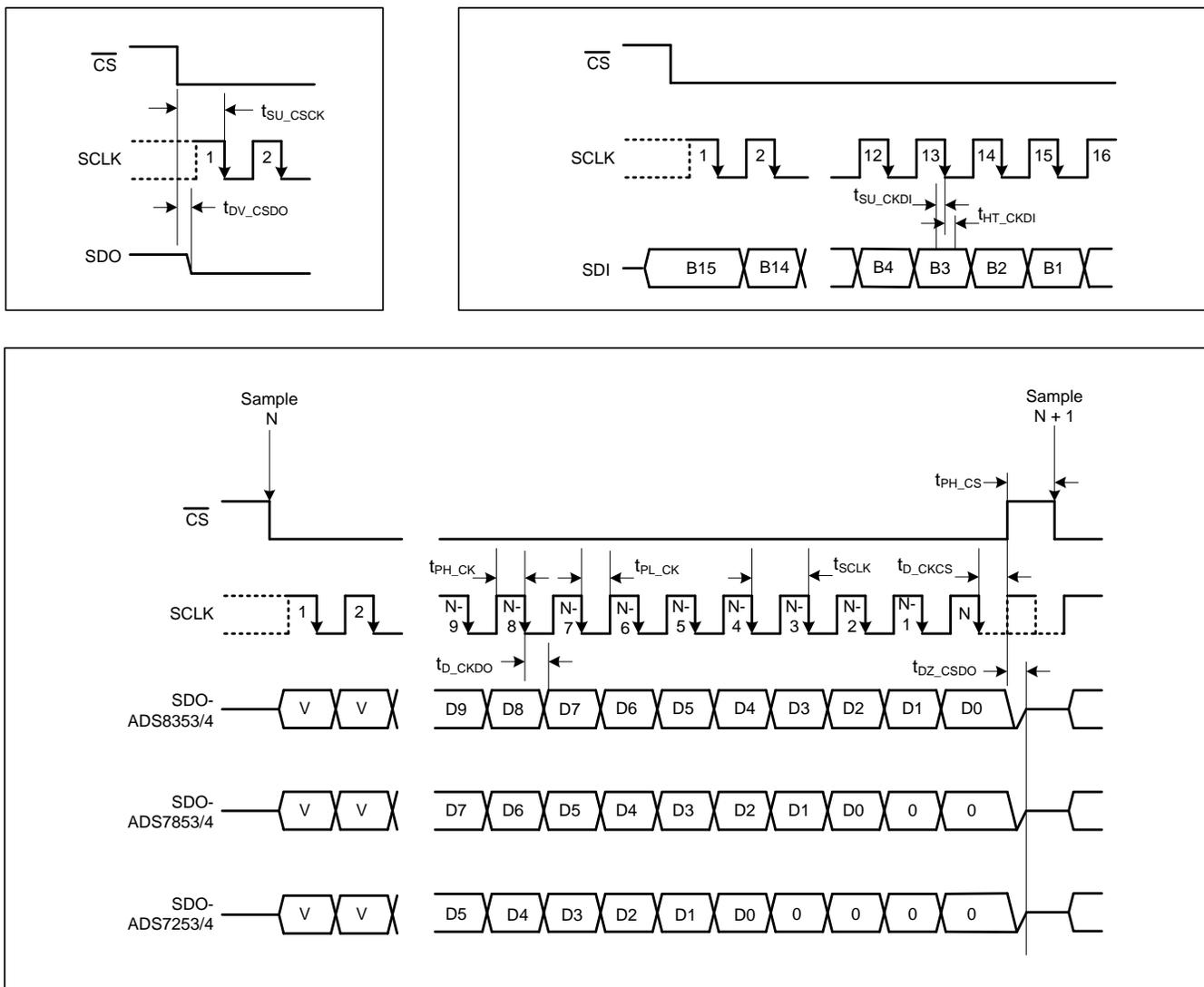
PARAMETER		ASSOCIATED FIGURES
t <sub>CLK</sub>	CLOCK period	Figure 1, Figure 90, Figure 91, Figure 92, Figure 93
t <sub>ACQ</sub>	Acquisition time	Figure 90, Figure 91, Figure 92, Figure 93
t <sub>CONV</sub>	Conversion time	Figure 90, Figure 91, Figure 92, Figure 93

(1) These parameters are specific to the interface mode of operation. Refer to the [Conversion Data Read](#) section for more details.

## 7.10 Timing Characteristics: Serial Interface

PARAMETER	TEST CONDITIONS	ASSOCIATED FIGURES	MIN	TYP	MAX	UNIT	
<b>TIMING REQUIREMENTS</b>							
t <sub>PH_CK</sub>	CLOCK high time	Figure 1	0.4		0.6	t <sub>CLK</sub>	
t <sub>PL_CK</sub>	CLOCK low time		0.4		0.6	t <sub>CLK</sub>	
f <sub>CLK</sub>	CLOCK frequency				1 / t <sub>CLK</sub>	MHz	
t <sub>PH_CS</sub>	$\overline{CS}$ high time	Figure 1	40			ns	
t <sub>PH_CS_SHRT</sub>	$\overline{CS}$ high time after frame abort	ADS8354	150			ns	
		ADS7854	100			ns	
		ADS7254	70			ns	
t <sub>SU_CSCK</sub>	Setup time: $\overline{CS}$ falling edge to SCLK falling edge	Figure 1	15			ns	
t <sub>D_CKCS</sub>	Delay time: Last SCLK falling edge to $\overline{CS}$ rising edge		15			ns	
t <sub>SU_CKDI</sub>	Setup time: DIN data valid to SCLK falling edge		5			ns	
t <sub>HT_CKDI</sub>	Hold time: SCLK falling edge to (previous) data valid on DIN		5			ns	
t <sub>PU_STDBY</sub>	Power-up time from STANDBY mode	Figure 95	1			μs	
t <sub>PU_SPD</sub>	Power-up time from SPD mode	With internal reference	3			ms	
		With external reference	1			ms	
<b>TIMING SPECIFICATIONS</b>							
t <sub>THROUGHPUT</sub>	Throughput time	ADS8354	32-CLK mode	Figure 90, Figure 91	1.425		μs
		ADS7854	32-CLK mode	Figure 92, Figure 93	1		μs
			16-CLK mode		1		μs
		ADS7254	32-CLK mode	Figure 90, Figure 91	1		μs
			16-CLK mode	Figure 92, Figure 93	1		μs
f <sub>THROUGHPUT</sub>	Throughput	Figure 90, Figure 91, Figure 92, Figure 93		1 / t <sub>THROUGHPUT</sub>		KSPS	
t <sub>DV_CSDO</sub>	Delay time: $\overline{CS}$ falling edge to data enable	Figure 1			12	ns	
t <sub>DZ_CSDO</sub>	Delay time: $\overline{CS}$ rising edge to data going to 3-state				12	ns	
t <sub>D_CKDO</sub>	Delay time: SCLK falling edge to next data valid				20	ns	

Figure 1 shows the details of the serial interface between the device and the digital host controller.



**Figure 1. Serial Interface Timing Diagram**

### 7.11 Typical Characteristics: ADS8354

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 700\text{ kSPS}$ , unless otherwise noted.

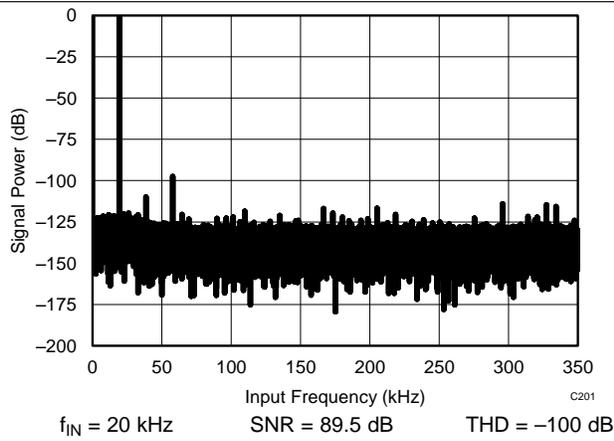


Figure 2. Typical FFT

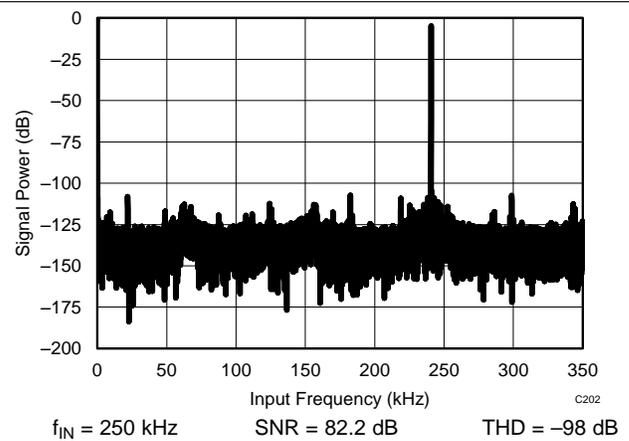


Figure 3. Typical FFT

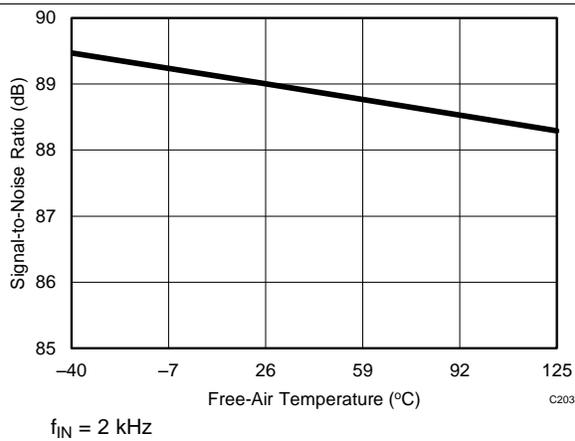


Figure 4. SNR vs Temperature

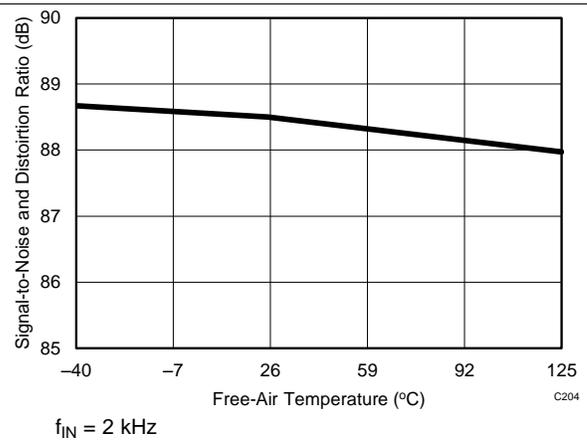


Figure 5. SINAD vs Temperature

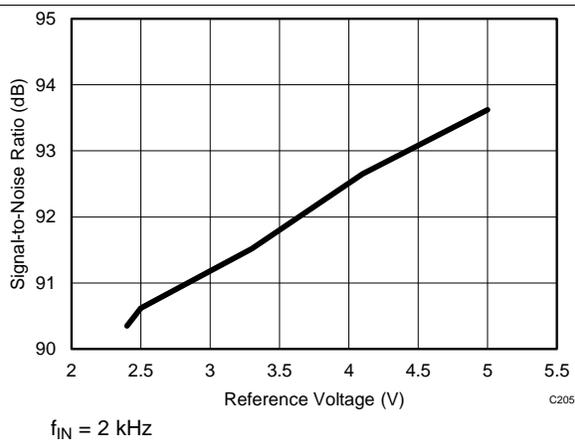


Figure 6. SNR vs Reference Voltage

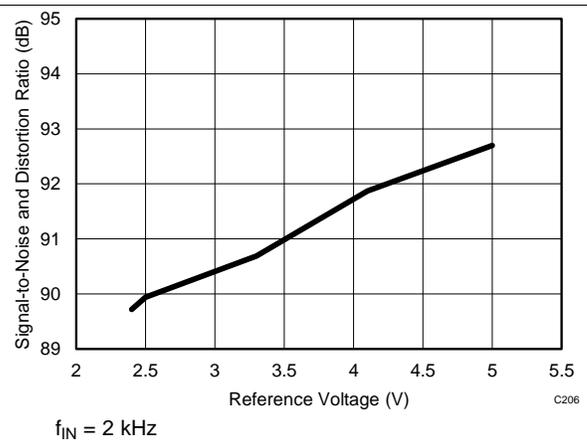
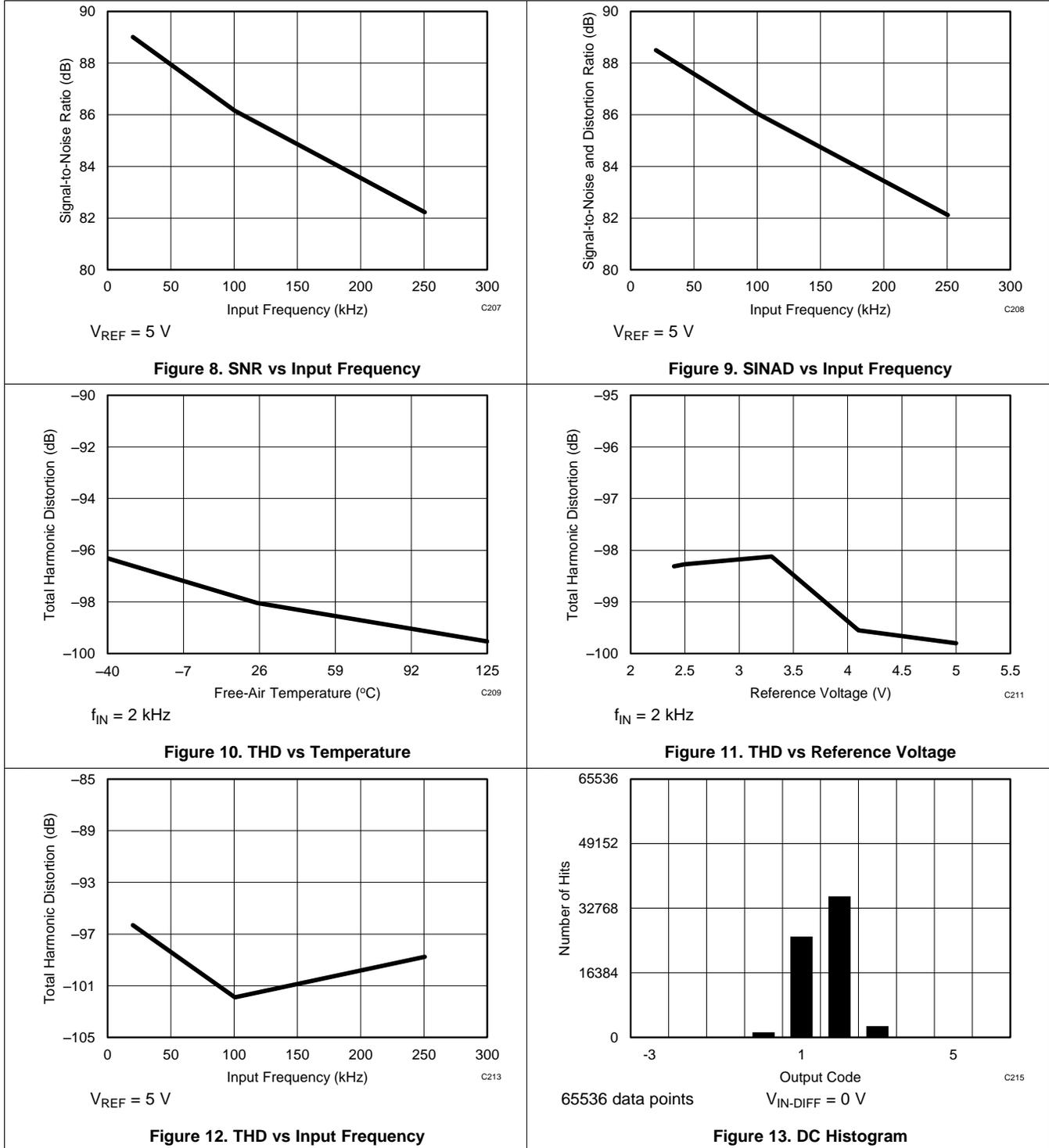


Figure 7. SINAD vs Reference Voltage

Typical Characteristics: ADS8354 (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  (internal), and  $f_{\text{DATA}} = 700\text{ kSPS}$ , unless otherwise noted.



**Typical Characteristics: ADS8354 (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 700\text{ kSPS}$ , unless otherwise noted.

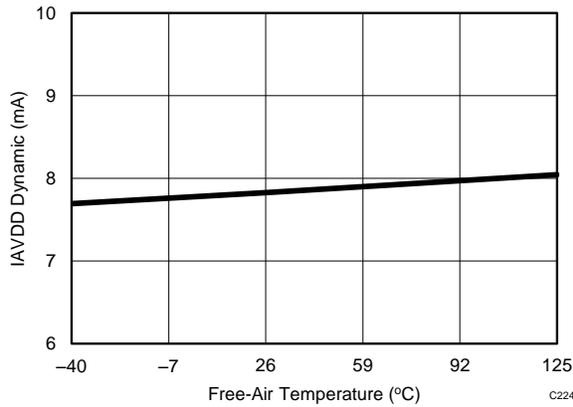


Figure 14. Analog Supply Current vs Temperature

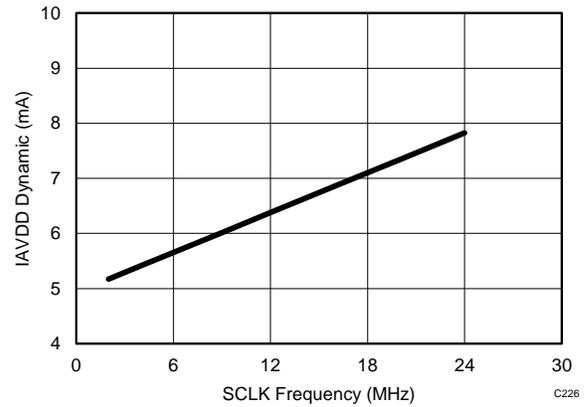


Figure 15. Analog Supply Current vs SCLK Frequency

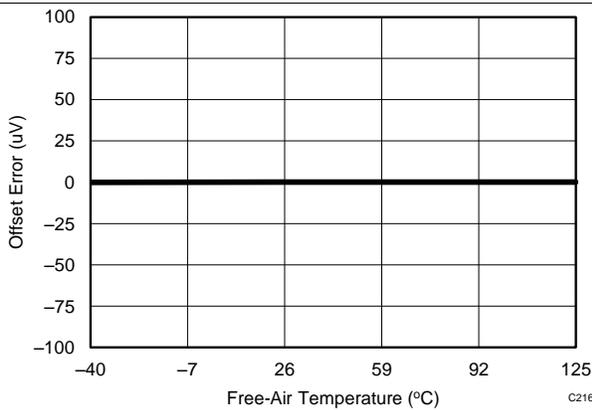


Figure 16. Offset Error vs Temperature

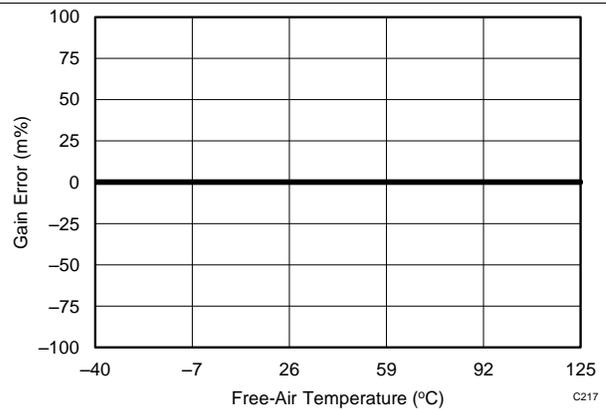


Figure 17. Gain Error vs Temperature

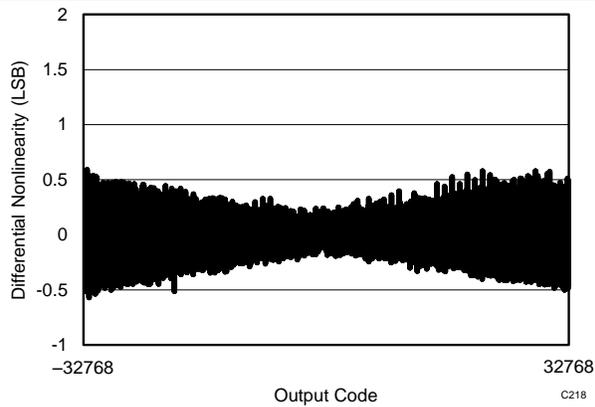


Figure 18. Typical DNL

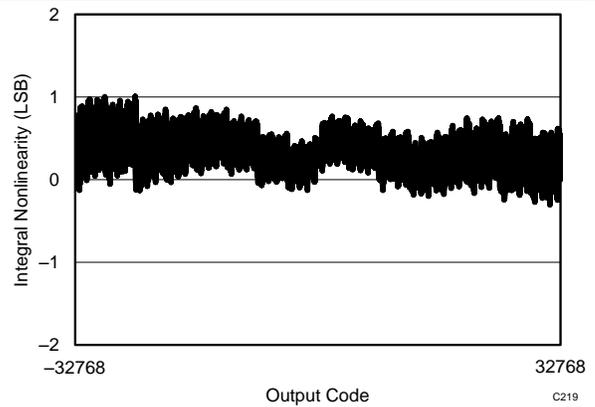
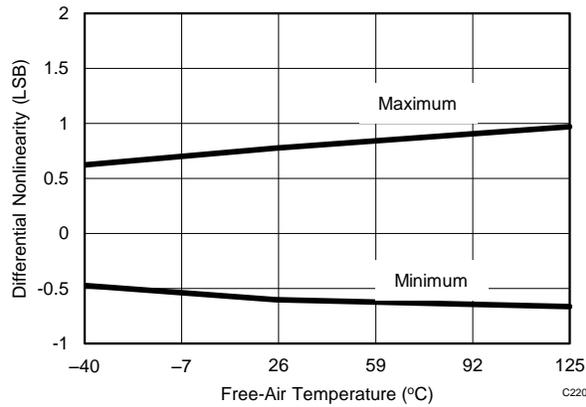


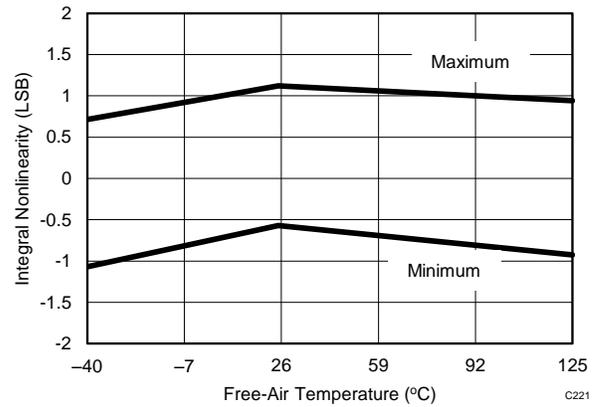
Figure 19. Typical INL

**Typical Characteristics: ADS8354 (continued)**

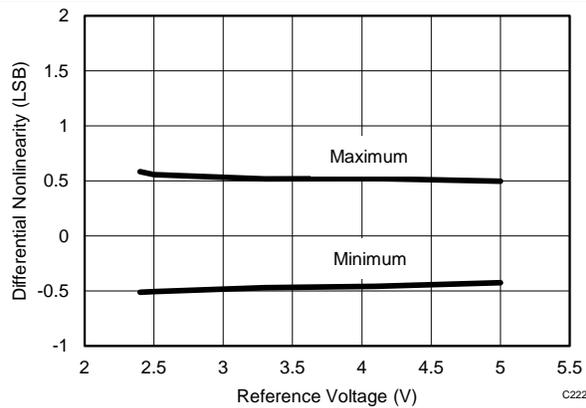
At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 700\text{ kSPS}$ , unless otherwise noted.



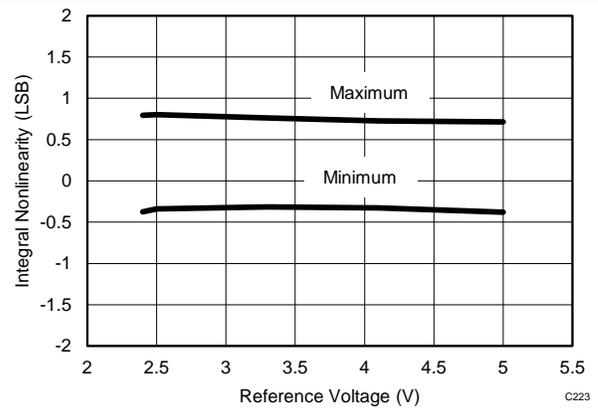
**Figure 20. DNL vs Temperature**



**Figure 21. INL vs Temperature**



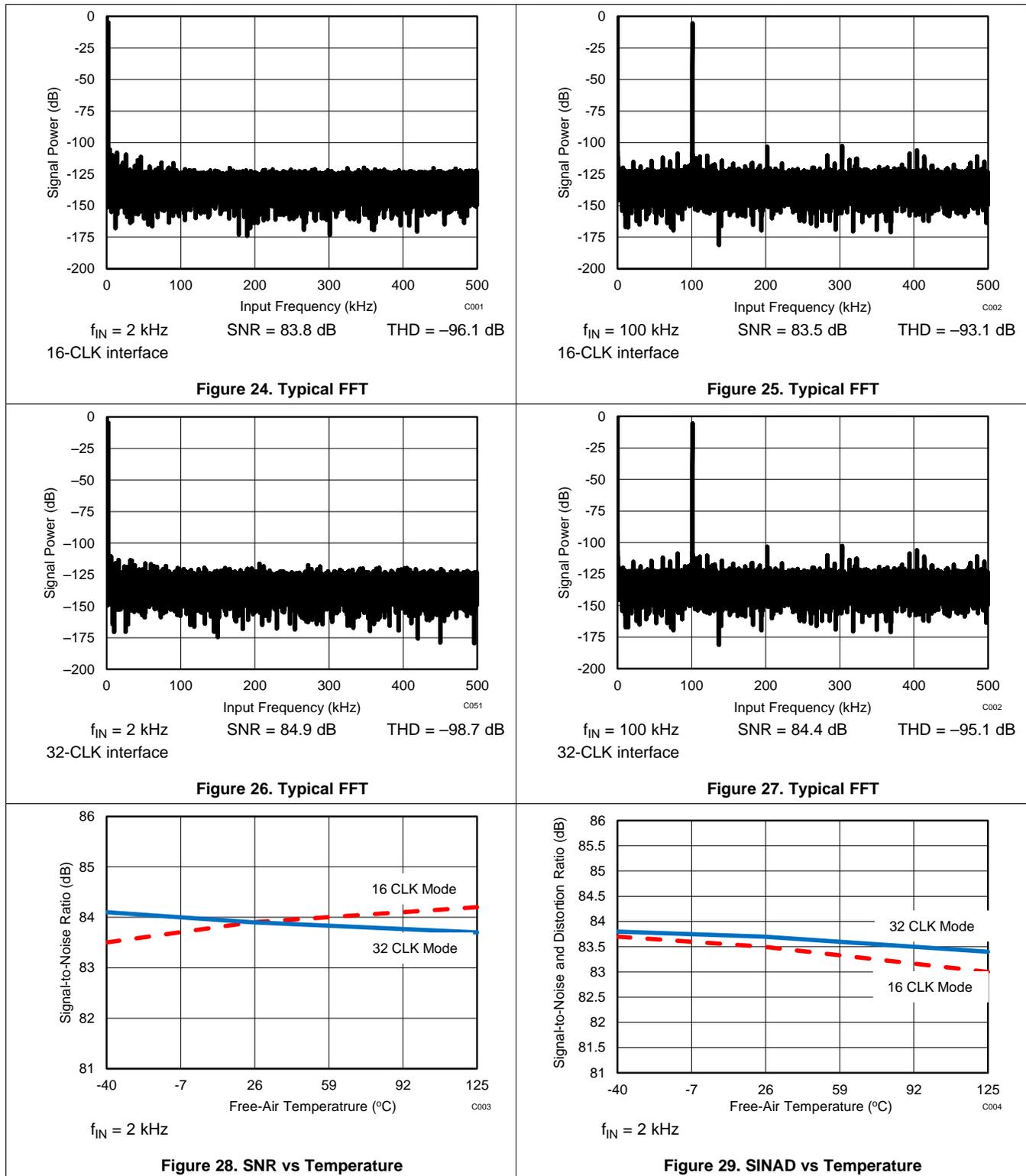
**Figure 22. DNL vs Reference Voltage**



**Figure 23. INL vs Reference Voltage**

### 7.12 Typical Characteristics: ADS7854

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 1\text{ MSPS}$ , unless otherwise noted.



Typical Characteristics: ADS7854 (continued)

At  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = 5\text{ V}$ ,  $DV_{DD} = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 1\text{ MSPS}$ , unless otherwise noted.

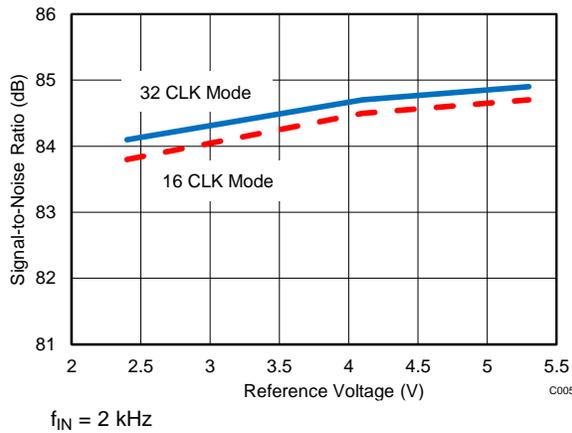


Figure 30. SNR vs Reference Voltage

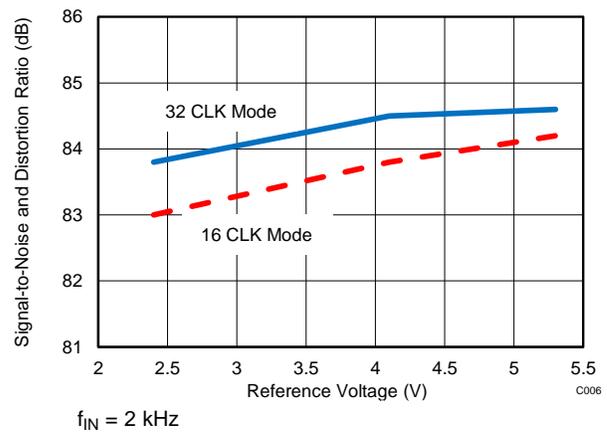


Figure 31. SINAD vs Reference Voltage

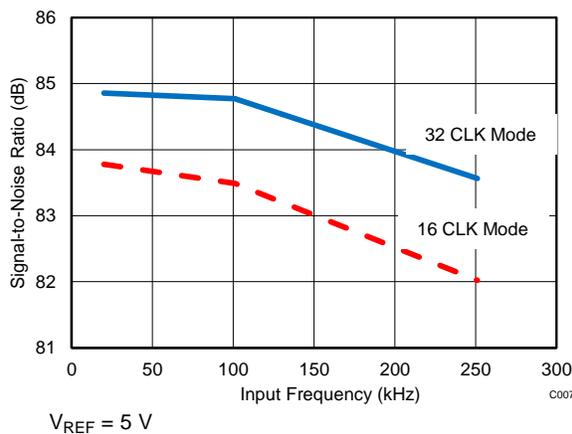


Figure 32. SNR vs Input Frequency

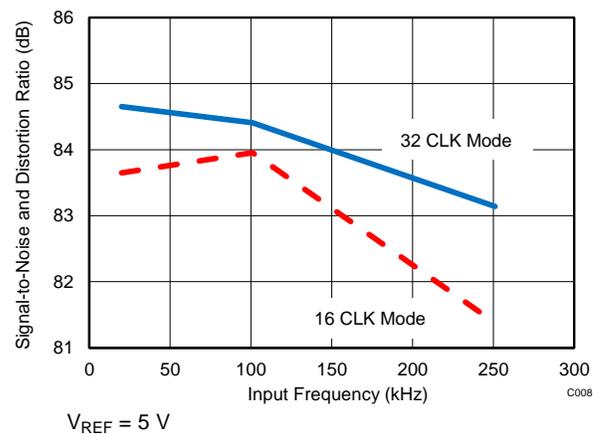


Figure 33. SINAD vs Input Frequency

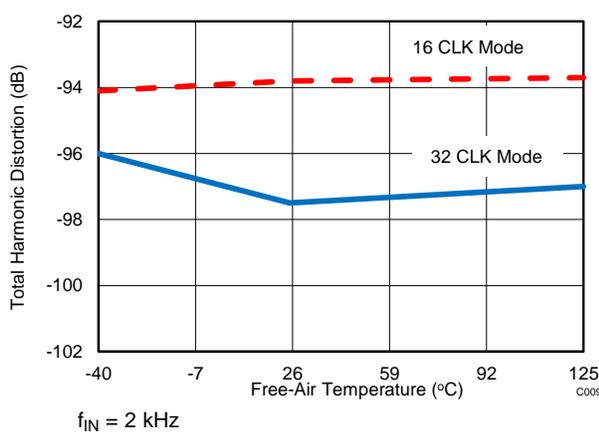


Figure 34. THD vs Temperature

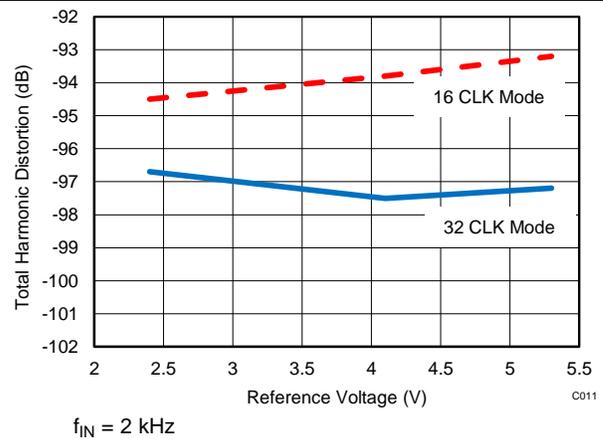


Figure 35. THD vs Reference Voltage

Typical Characteristics: ADS7854 (continued)

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 1\text{ MSPS}$ , unless otherwise noted.

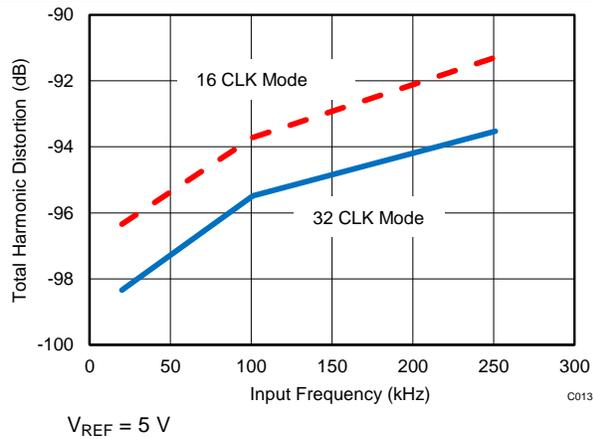


Figure 36. THD vs Input Frequency

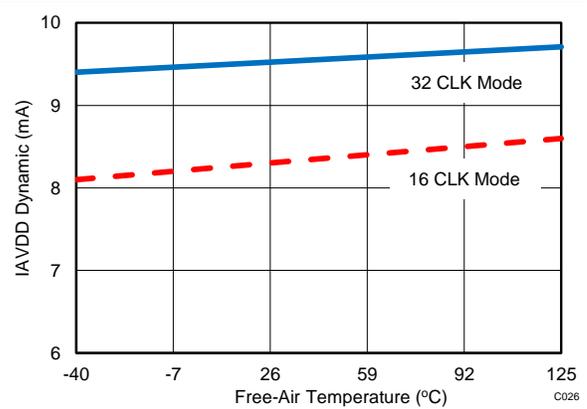


Figure 37. Analog Supply Current vs Temperature

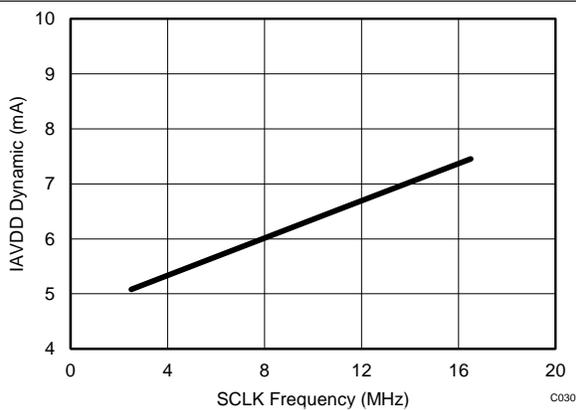


Figure 38. Analog Supply Current vs SCLK Frequency

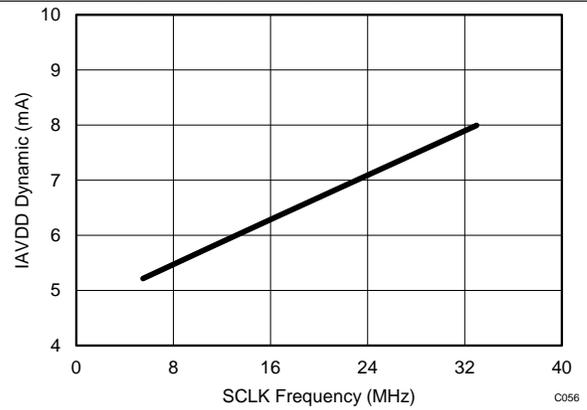


Figure 39. Analog Supply Current vs SCLK Frequency

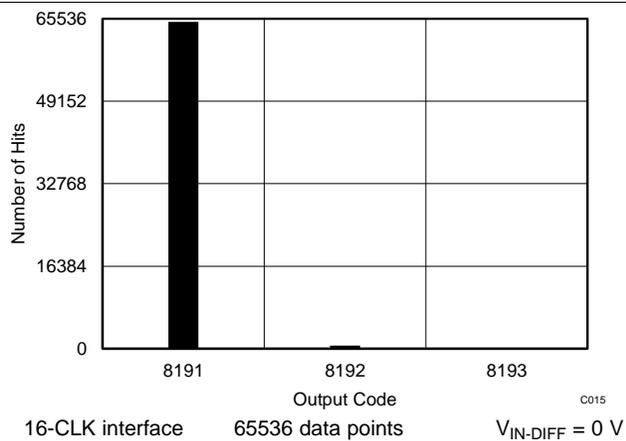


Figure 40. DC Histogram

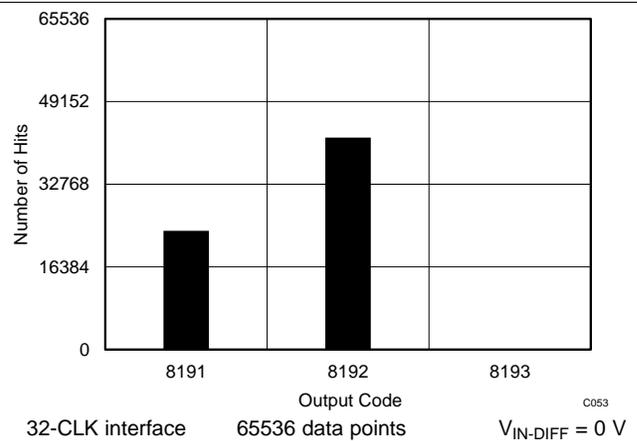


Figure 41. DC Histogram

Typical Characteristics: ADS7854 (continued)

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 1\text{ MSPS}$ , unless otherwise noted.

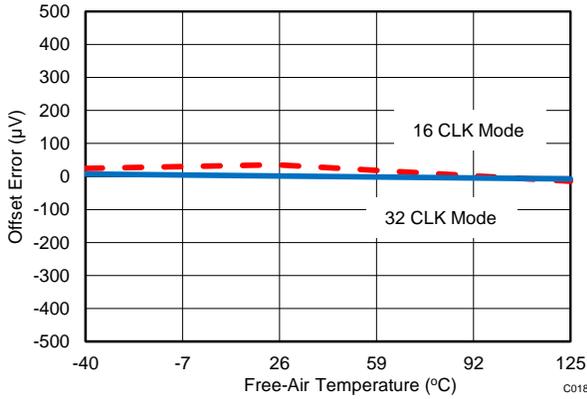


Figure 42. Offset Error vs Temperature

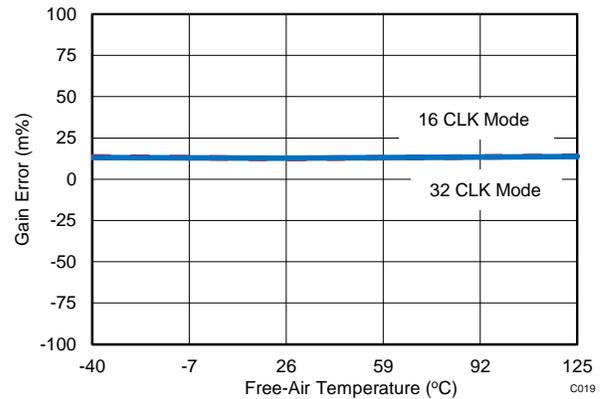
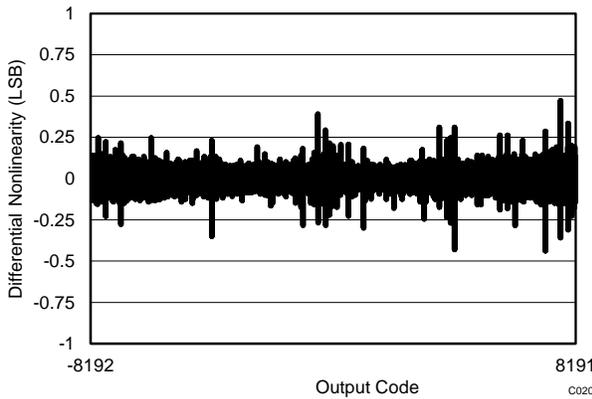
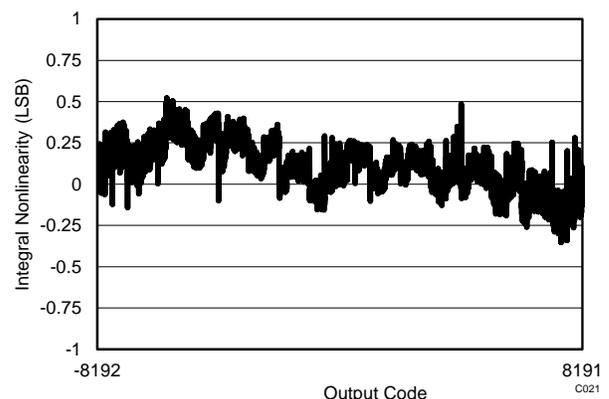


Figure 43. Gain Error vs Temperature



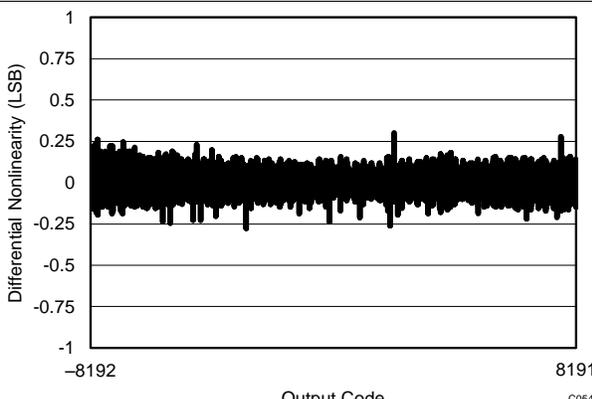
16-CLK interface

Figure 44. Typical DNL



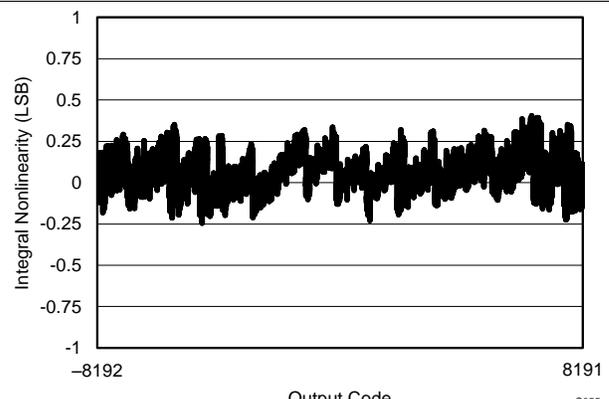
16-CLK interface

Figure 45. Typical INL



32-CLK interface

Figure 46. Typical DNL



32-CLK interface

Figure 47. Typical INL

**Typical Characteristics: ADS7854 (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 1\text{ MSPS}$ , unless otherwise noted.

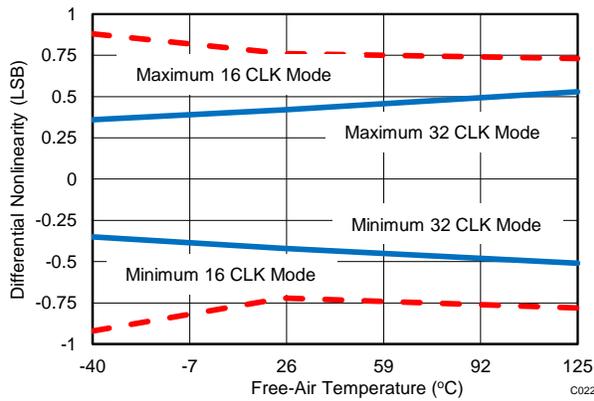


Figure 48. DNL vs Temperature

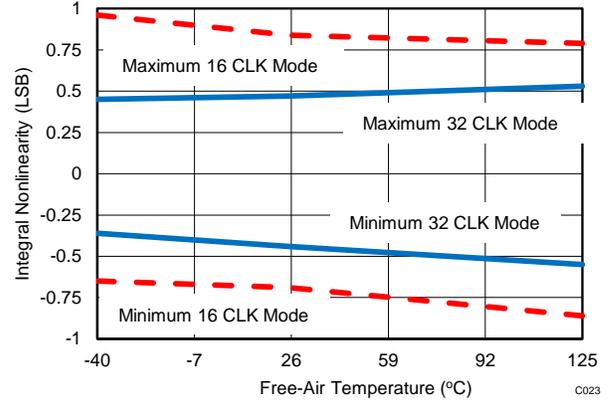


Figure 49. INL vs Temperature

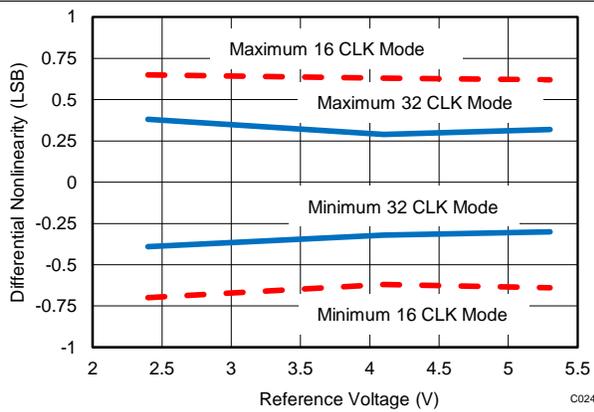


Figure 50. DNL vs Reference Voltage

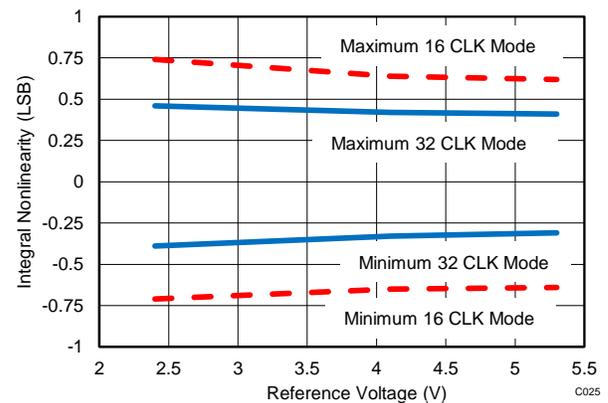


Figure 51. INL vs Reference Voltage

### 7.13 Typical Characteristics: ADS7254

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 1\text{ MSPS}$ , unless otherwise noted.

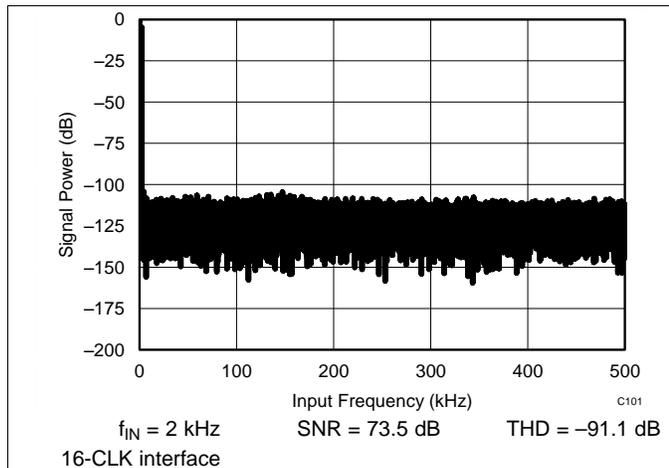


Figure 52. Typical FFT

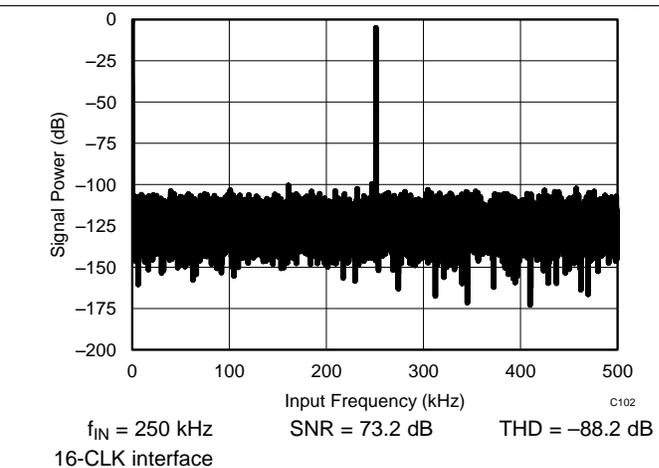


Figure 53. Typical FFT

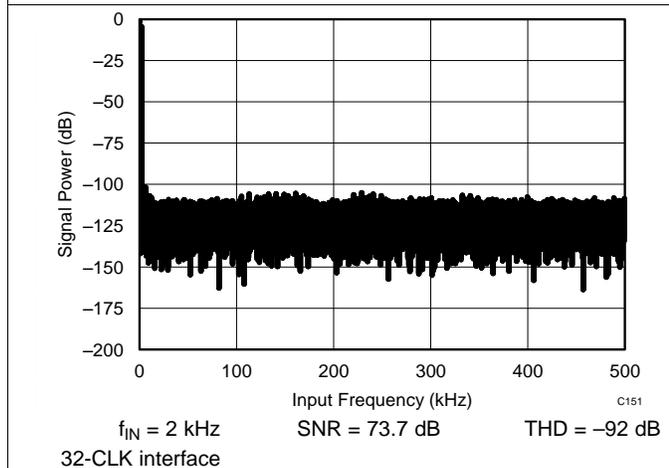


Figure 54. Typical FFT

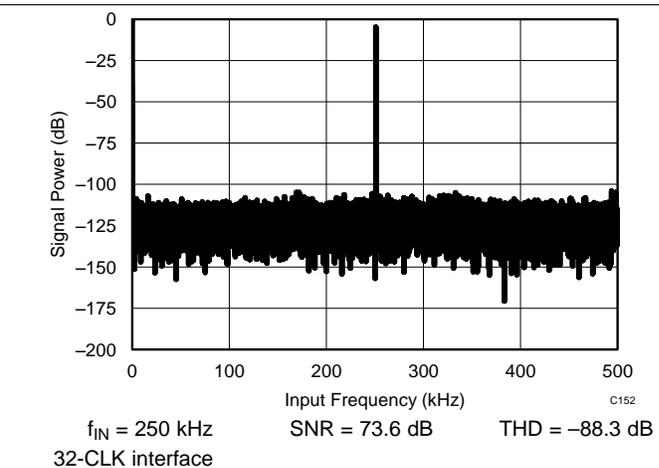


Figure 55. Typical FFT

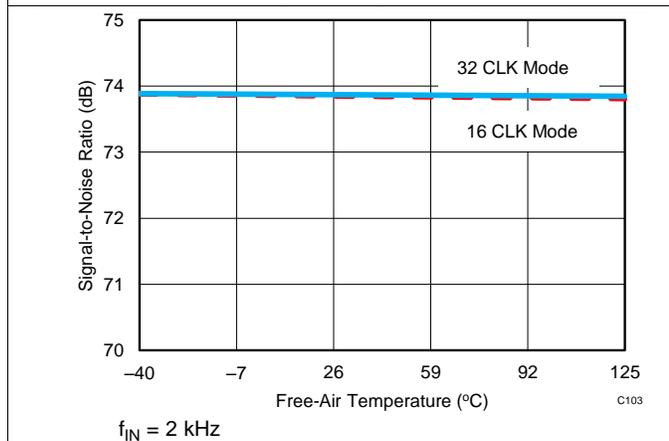


Figure 56. SNR vs Temperature

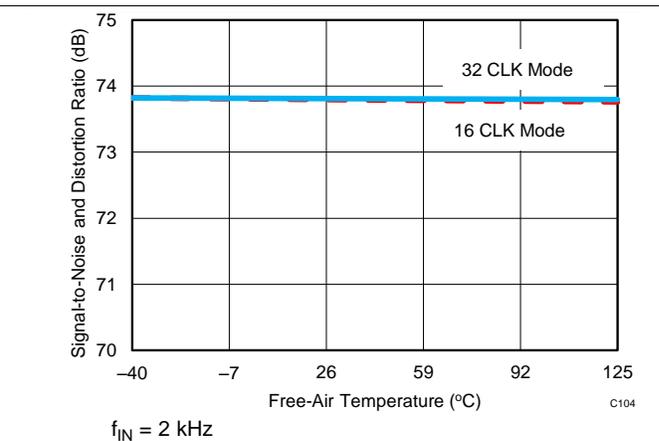
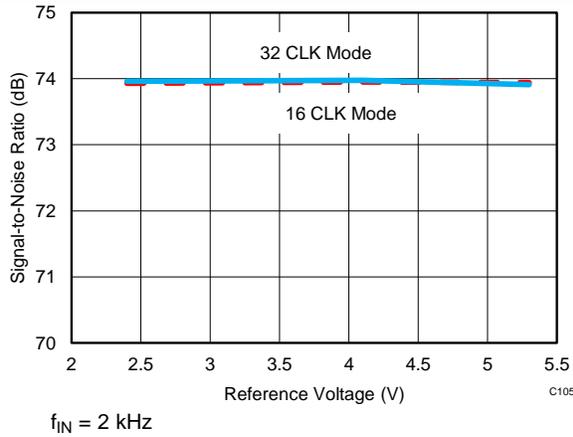


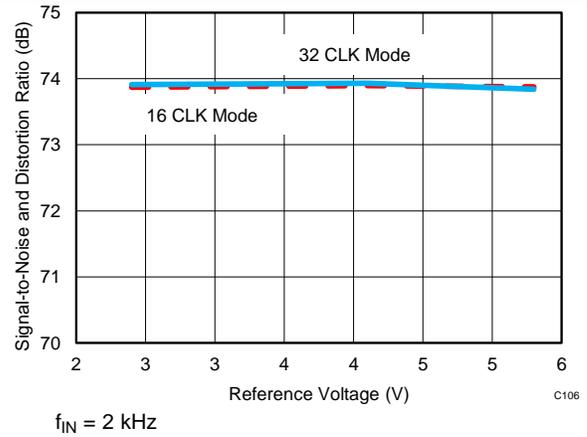
Figure 57. SINAD vs Temperature

**Typical Characteristics: ADS7254 (continued)**

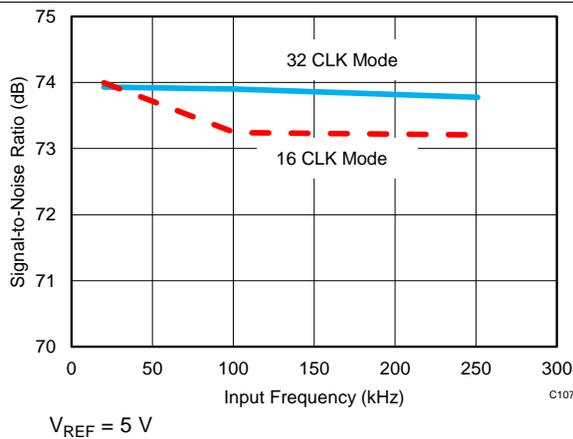
At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 1\text{ MSPS}$ , unless otherwise noted.



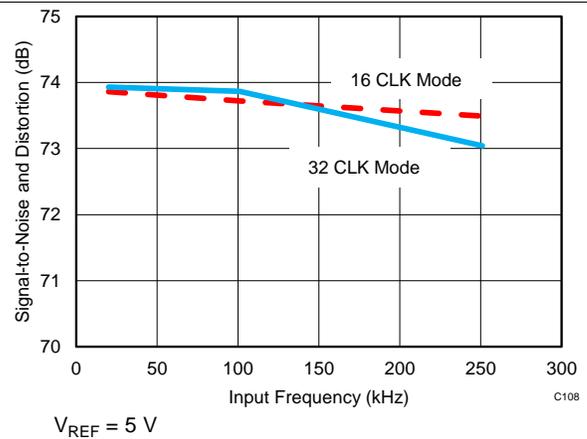
**Figure 58. SNR vs Reference Voltage**



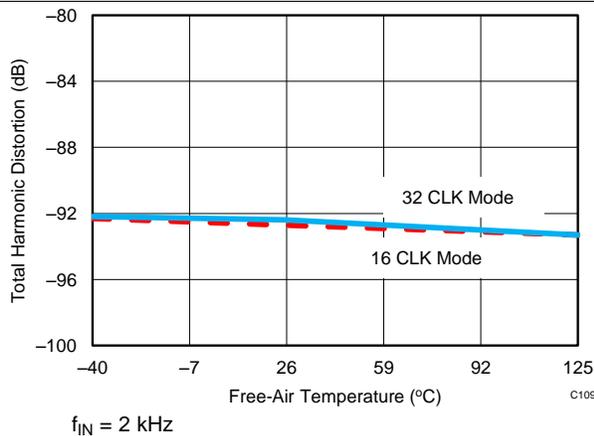
**Figure 59. SINAD vs Reference Voltage**



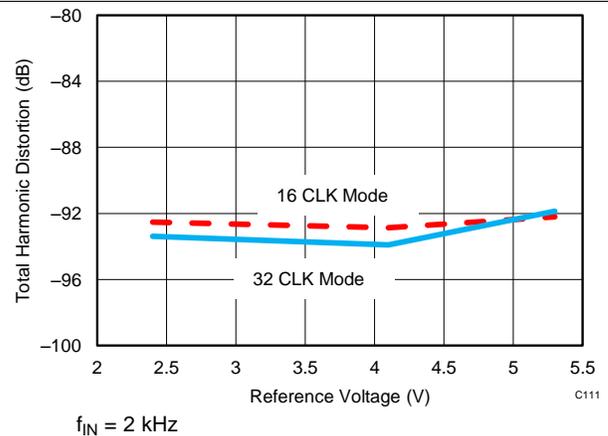
**Figure 60. SNR vs Input Frequency**



**Figure 61. SINAD vs Input Frequency**



**Figure 62. THD vs Temperature**



**Figure 63. THD vs Reference Voltage**

Typical Characteristics: ADS7254 (continued)

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 1\text{ MSPS}$ , unless otherwise noted.

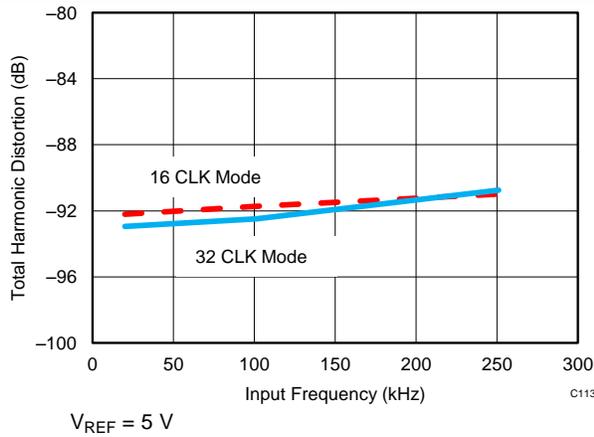


Figure 64. THD vs Input Frequency

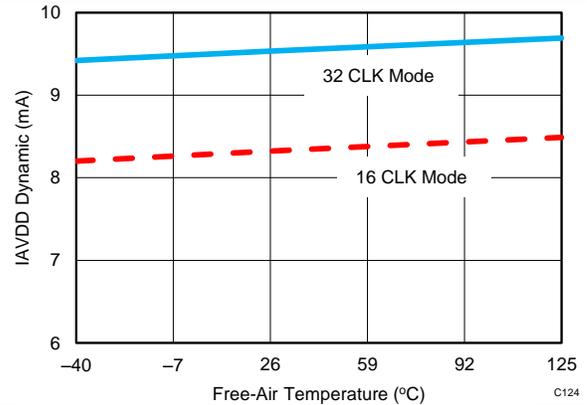


Figure 65. Analog Supply Current vs Temperature

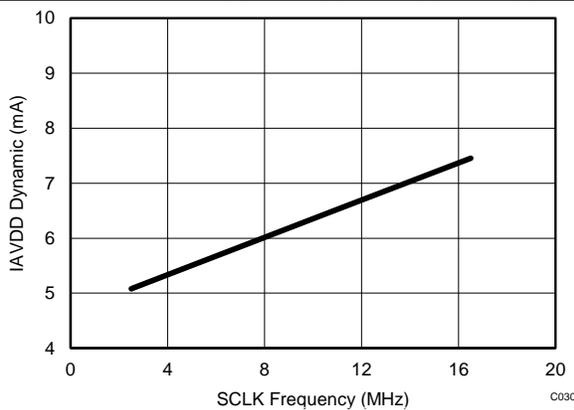


Figure 66. Analog Supply Current vs SCLK Frequency

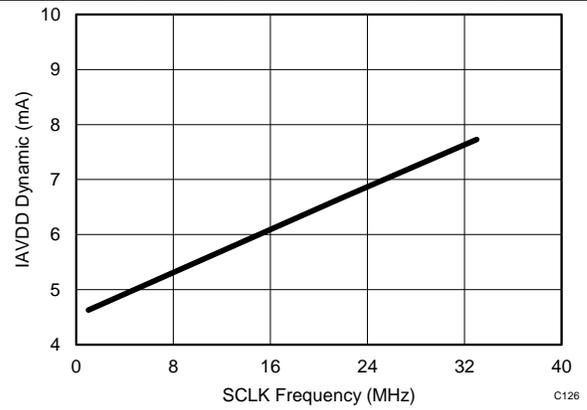


Figure 67. Analog Supply Current vs SCLK Frequency

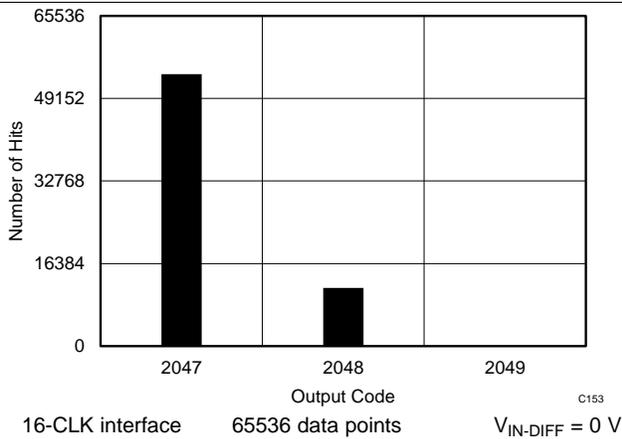


Figure 68. DC Histogram

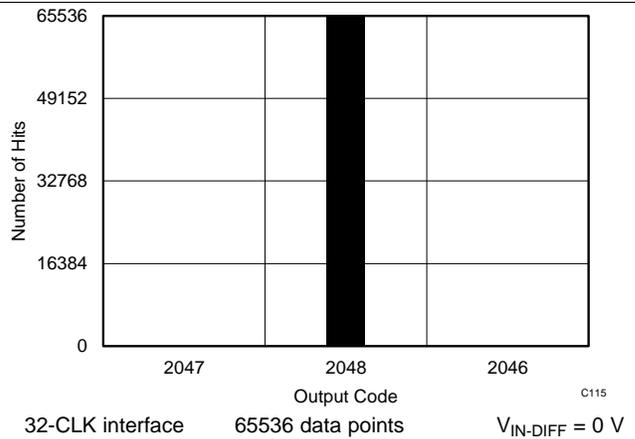


Figure 69. DC Histogram

Typical Characteristics: ADS7254 (continued)

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 1\text{ MSPS}$ , unless otherwise noted.

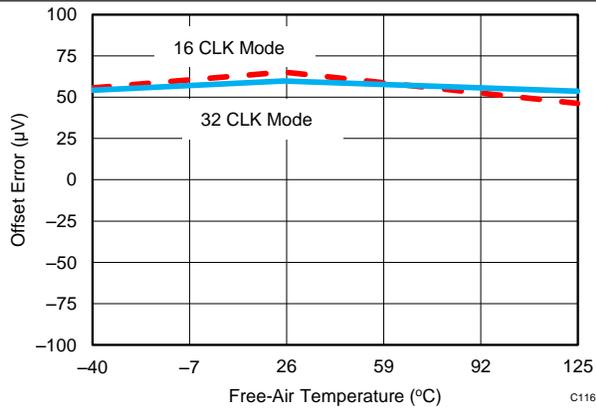


Figure 70. Offset Error vs Temperature

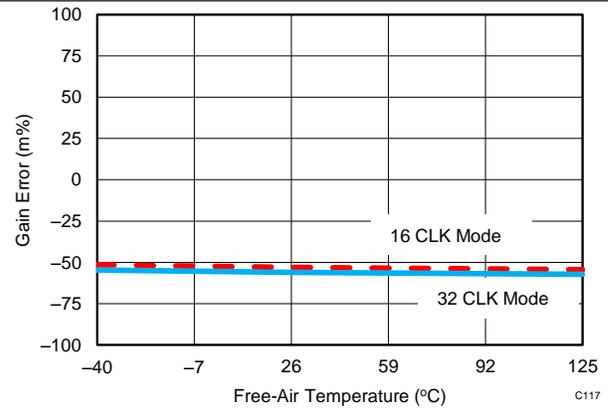


Figure 71. Gain Error vs Temperature

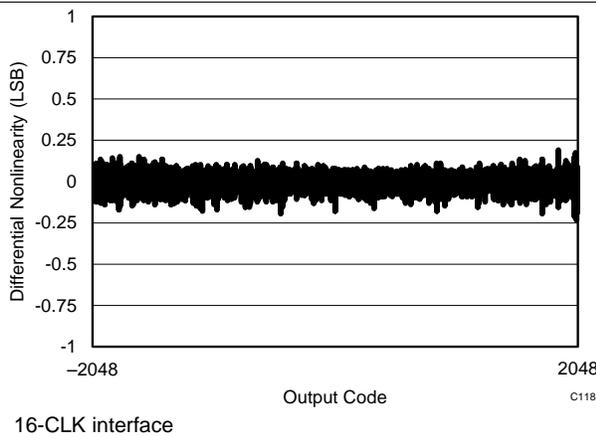


Figure 72. Typical DNL

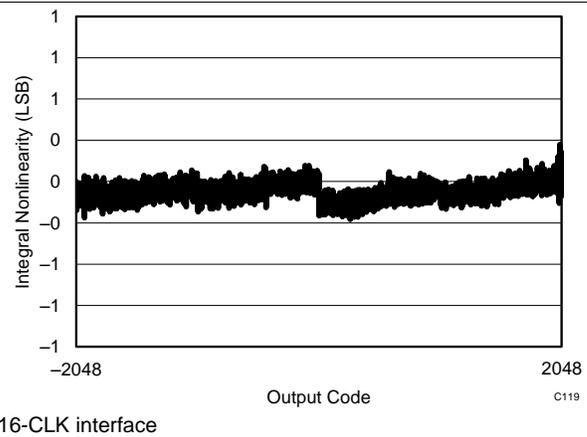


Figure 73. Typical INL

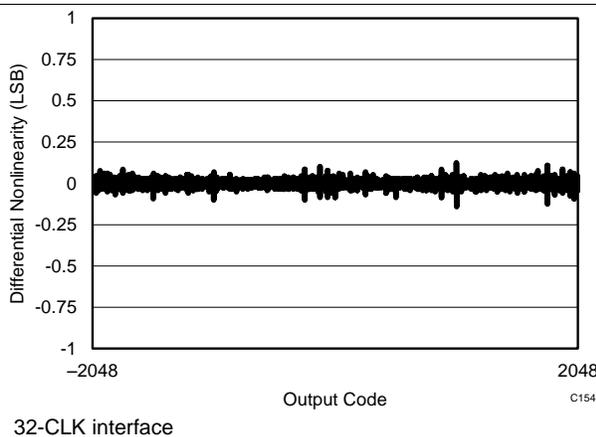


Figure 74. Typical DNL

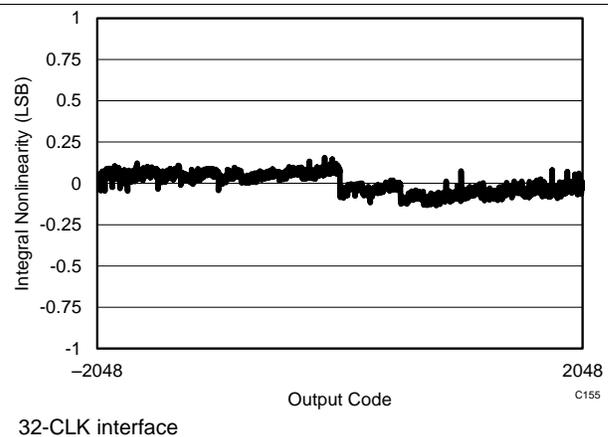
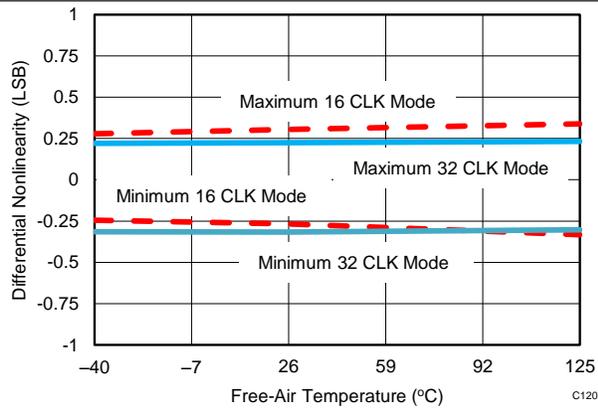


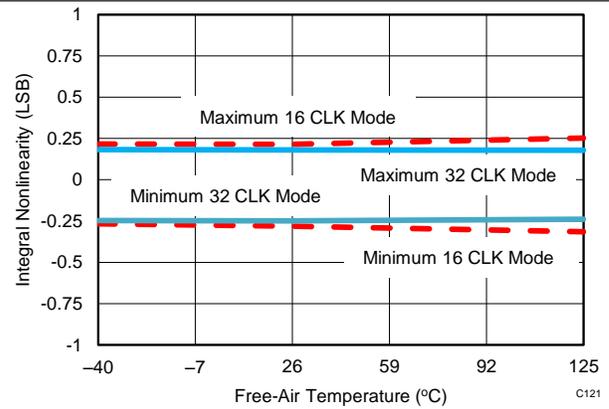
Figure 75. Typical INL

**Typical Characteristics: ADS7254 (continued)**

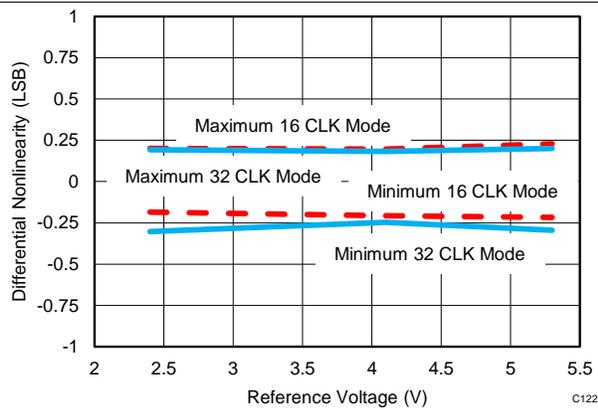
At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = 1\text{ MSPS}$ , unless otherwise noted.



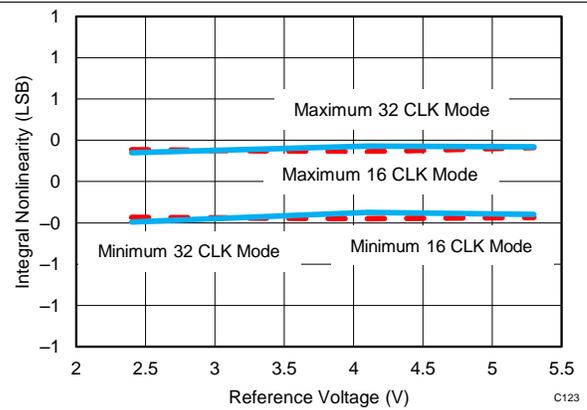
**Figure 76. DNL vs Temperature**



**Figure 77. INL vs Temperature**



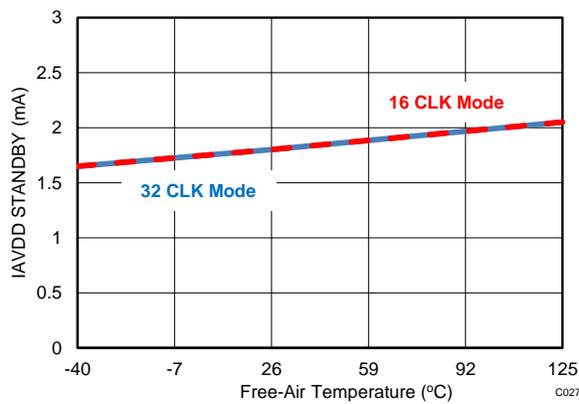
**Figure 78. DNL vs Reference Voltage**



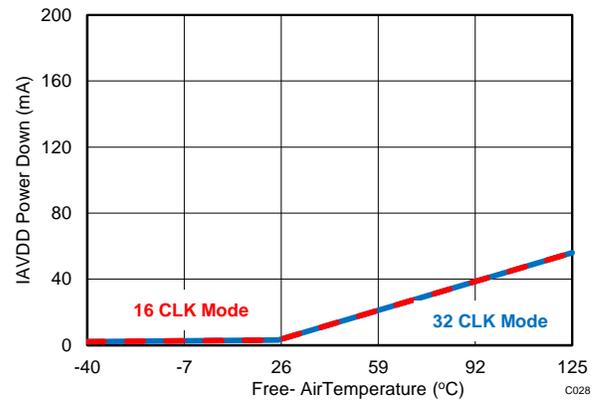
**Figure 79. INL vs Reference Voltage**

**7.14 Typical Characteristics: Common to ADS8354, ADS7854, and ADS7254**

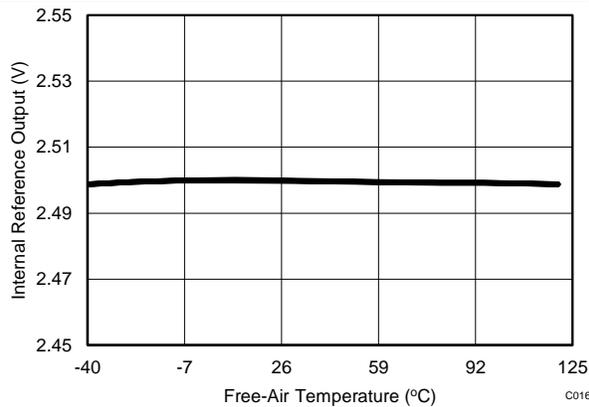
At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  (internal), and  $f_{DATA} = \text{maximum}$ , unless otherwise noted.



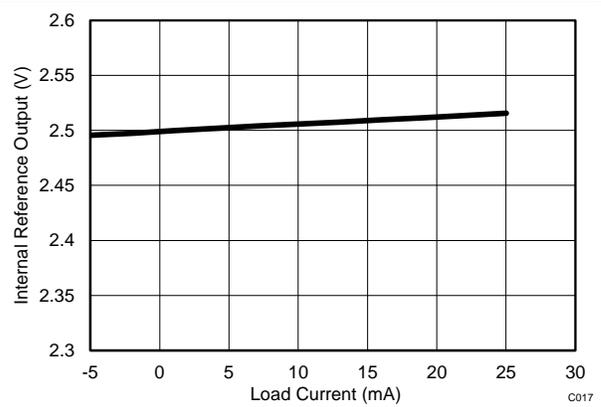
**Figure 80. STANDBY Current vs Temperature**



**Figure 81. Power-Down Current vs Temperature**



**Figure 82. Internal Reference Output vs Temperature**



$R_{OUT} = 0.67\ \Omega$

**Figure 83. Internal Reference Output Impedance**

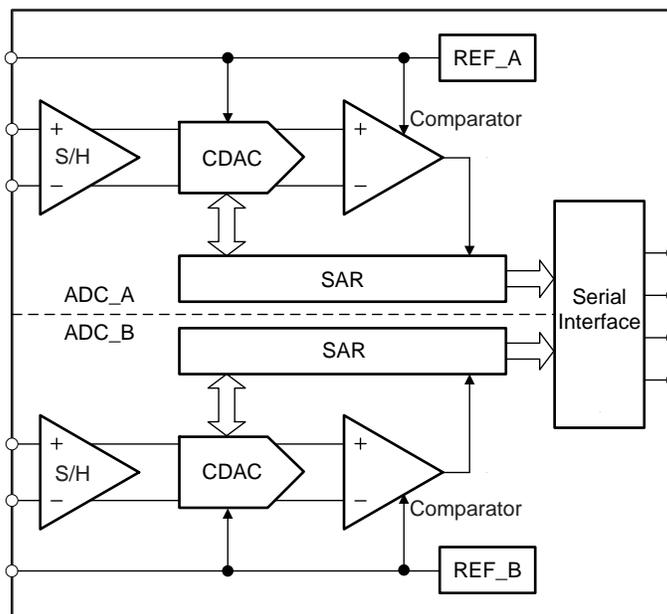
## 8 Detailed Description

### 8.1 Overview

These devices belong to a family of pin-compatible, dual, high-speed, simultaneous-sampling, analog-to-digital converters (ADCs). The ADS8354, ADS7854, and ADS7254 support fully-differential input signals. The devices provide a simple, serial interface to the host controller and operate over a wide range of analog and digital power supplies.

These devices have two independently programmable internal references to achieve system-level gain error correction. The [Functional Block Diagram](#) section provides a functional block diagram of the device.

### 8.2 Functional Block Diagram

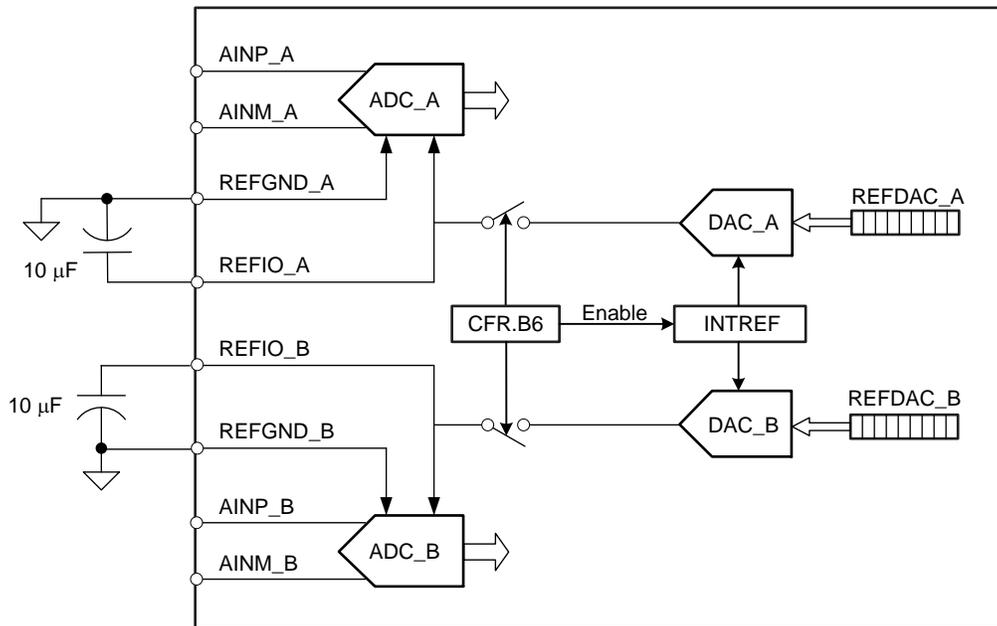


## 8.3 Feature Description

### 8.3.1 Reference

The device has two simultaneous sampling ADCs (ADC\_A and ADC\_B). ADC\_A and ADC\_B operate with reference voltages  $V_{REF\_A}$  and  $V_{REF\_B}$  present on the REFIO\_A and REFIO\_B pins, respectively. The REFIO\_A and REFIO\_B pins should be decoupled with the REFGND\_A and REFGND\_B pins, respectively, with 10- $\mu$ F decoupling capacitors.

The device supports operation either with an internal or external reference source, as shown in [Figure 84](#). The reference voltage source is determined by setting bit 6 of the configuration register (CFR.B6). Note that this bit is common to ADC\_A and ADC\_B.



**Figure 84. Reference Configurations and Connections**

When CFR.B6 is 0, the device shuts down the internal reference source (INTREF) and ADC\_A and ADC\_B operate on external reference voltages provided by the user on the REFIO\_A and REFIO\_B pins, respectively.

When CFR.B6 is 1, the device operates with the internal reference source (INTREF) connected to REFIO\_A and REFIO\_B via DAC\_A and DAC\_B, respectively. In this configuration,  $V_{REF\_A}$  and  $V_{REF\_B}$  can be changed independently by writing to the respective user-programmable registers, REFDAC\_A and REFDAC\_B, respectively. Refer to the [REFDAC Registers \(REFDAC\\_A and REFDAC\\_B\)](#) section for more details.

## Feature Description (continued)

### 8.3.2 Analog Inputs

The ADS8354, ADS7854, and ADS7254 support fully-differential analog input signals on both ADC channels. These inputs are sampled and converted simultaneously by the two ADCs, ADC\_A and ADC\_B. ADC\_A samples and converts ( $V_{AINP\_A} - V_{AINM\_A}$ ), and ADC\_B samples and converts ( $V_{AINP\_B} - V_{AINM\_B}$ ).

Figure 85a and Figure 85b show equivalent circuits for the ADC\_A and ADC\_B analog input pins, respectively. Series resistance,  $R_S$ , represents the on-state sampling switch resistance (typically 50  $\Omega$ ) and  $C_{SAMPLE}$  is the device sampling capacitor (typically 40 pF).

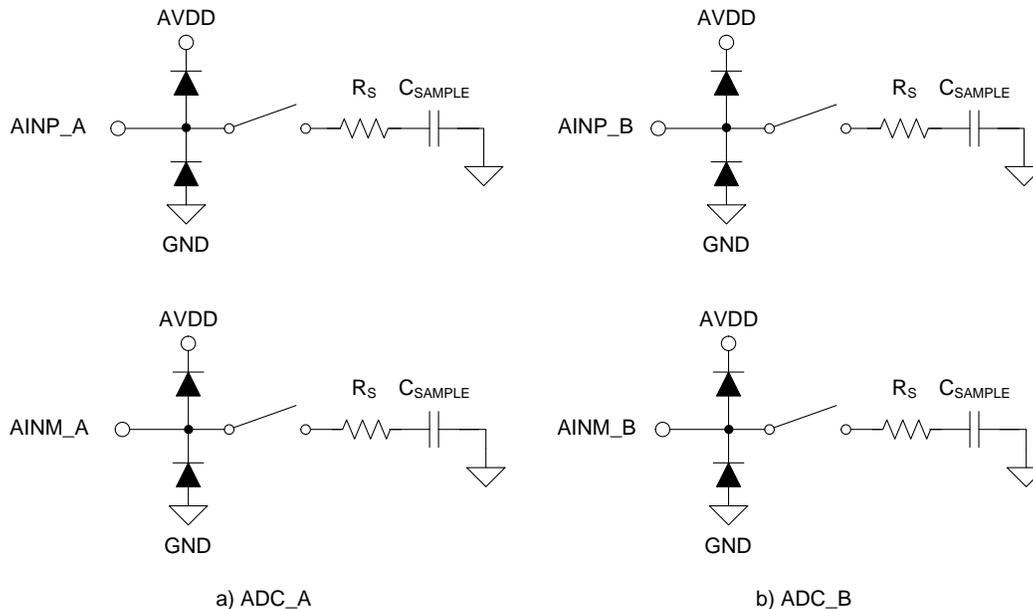


Figure 85. Equivalent Circuit for the Analog Input Pins

#### 8.3.2.1 Analog Input: Full-Scale Range Selection

The full-scale range (FSR) supported at the analog inputs of the device is programmable with bit B9 of the configuration register (CFR.B9). This bit is common for both ADCs (ADC\_A and ADC\_B). The FSR is given by Equation 1 and Equation 2 :

$$\text{For CFR.B9} = 0, \text{FSR\_ADC\_A} = \pm V_{REF\_A} \text{ and } \text{FSR\_ADC\_B} = \pm V_{REF\_B} \quad (1)$$

$$\text{For CFR.B9} = 1, \text{FSR\_ADC\_A} = \pm 2 \times V_{REF\_A} \text{ and } \text{FSR\_ADC\_B} = \pm 2 \times V_{REF\_B}$$

where:

- $V_{REF\_A}$  and  $V_{REF\_B}$  are the reference voltages going to ADC\_A and ADC\_B, respectively (as described in the Reference section). (2)

Therefore, with appropriate settings of the REFDAC\_A and REFDAC\_B registers and CFR.B9, the maximum dynamic range of the ADC can be used.

Note that while using CFR.B9 set to 1, care must be taken so that the ADC analog supply (AVDD) is as in Equation 3 and Equation 4:

$$2 \times V_{REF\_A} \leq AVDD \leq AVDD(\text{max}) \quad (3)$$

$$2 \times V_{REF\_B} \leq AVDD \leq AVDD(\text{max}) \quad (4)$$

**Feature Description (continued)**
**8.3.2.2 Analog Input: Common-Mode Voltage Range**

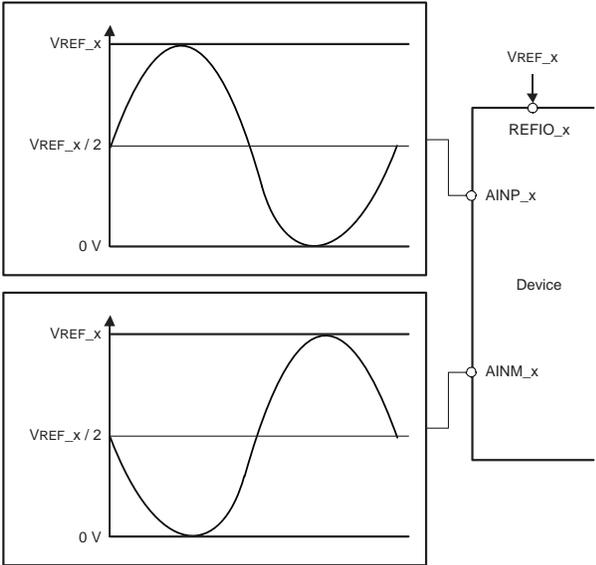
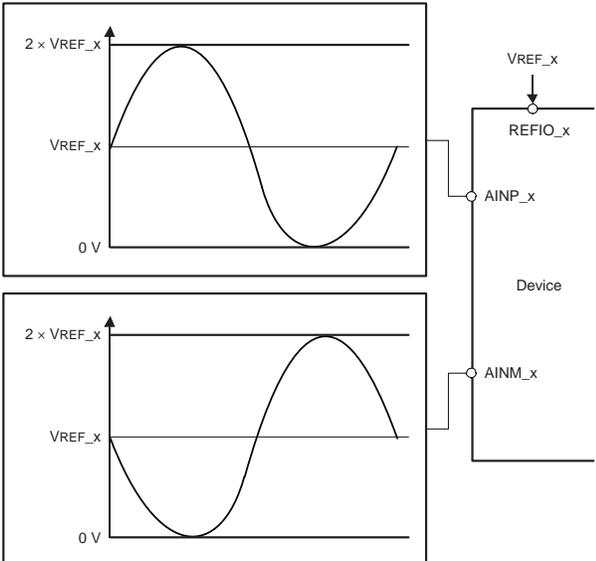
The ADS8354, ADS7854, and ADS7254 support fully-differential input signals. Equation 5 and Equation 6 provide the common-mode voltage for the ADC\_A and ADC\_B differential inputs.

$$V_{CM,A} = FSR\_ADC\_A / 2 \quad (5)$$

$$V_{CM,B} = FSR\_ADC\_B / 2 \quad (6)$$

The various input configurations supported by the device are shown in Table 1.

**Table 1. Input Configurations**

INPUT RANGE SELECTION	INPUT COMMON-MODE RANGE	CONNECTION DIAGRAM
CFR.B9 = 0 (FSR_ADC_A = ±V <sub>REF_A</sub> ) (FSR_ADC_B = ±V <sub>REF_B</sub> )	$V_{CM,A} = \left[ \frac{V_{REF,A}}{2} \right] \pm 0.1 \text{ V}$ $V_{CM,B} = \left[ \frac{V_{REF,B}}{2} \right] \pm 0.1 \text{ V}$	
CFR.B9 = 1 (FSR_ADC_A = ±2 × V <sub>REF_A</sub> ) (FSR_ADC_B = ±2 × V <sub>REF_B</sub> )	$V_{CM,A} = V_{REF,A} \pm 0.1 \text{ V}$ $V_{CM,B} = V_{REF,B} \pm 0.1 \text{ V}$	

### 8.3.3 Transfer Function

The device output is in twos complement format. Device resolution for a fully-differential input is calculated by Equation 7:

$$1 \text{ LSB} = (2 \times \text{FSR\_ADC\_x}) / (2^N)$$

where:

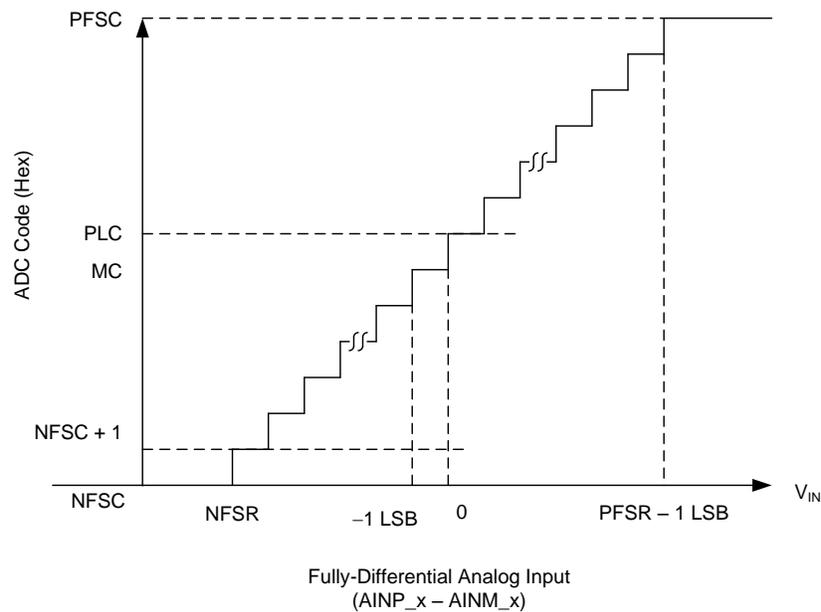
- N = 16 (ADS8354), 14 (ADS7854), or 12 (ADS7254)
- FSR\_ADC\_x is the full-scale input range of the ADC (refer to the *Analog Input* section for more details) (7)

Table 2 shows the different input voltages and the corresponding output codes from the device.

**Table 2. Transfer Characteristics**

INPUT VOLTAGE (AINP_x – AINM_x), ±V <sub>REF_x</sub> RANGE	INPUT VOLTAGE (AINP_x – AINM_x), ±2 × V <sub>REF_x</sub> RANGE	INPUT VOLTAGE	OUTPUT CODE (Hex)			
			CODE	ADS8354	ADS7854	ADS7254
< -V <sub>REF_x</sub>	< -2 × V <sub>REF_x</sub>	NFSC	NFSC	8000	2000	800
-V <sub>REF_x</sub> + 1 LSB	-2 × V <sub>REF_x</sub> + 1 LSB	NFSR	NFSC + 1	8001	2001	801
-1 LSB	-1 LSB	-1 LSB	MC	FFFF	3FFF	FFF
0	0	0	PLC	0000	0000	000
> V <sub>REF_x</sub> - 1 LSB	> 2 × V <sub>REF_x</sub> - 1 LSB	PFSR - 1 LSB	PFSC	7FFF	1FFF	7FF

Figure 86 shows the ideal transfer characteristics for the device.



**Figure 86. Ideal Transfer Characteristics for a Fully-Differential Analog Input**

## 8.4 Device Functional Modes

The device provides three user-programmable registers: the configuration register (CFR), the REFDAC\_A register, and the REFDAC\_B register. These registers support write (refer to the [Write to User Programmable Registers](#) section) and readback (refer to the [Reading User-Programmable Registers](#) section) operations and allow the user to customize ADC behavior for specific application requirements.

The device supports four interface modes (refer to the [Conversion Data Read](#) section), two low-power modes (refer to the [Low-Power Modes](#) section), and short-cycling/reconversion feature (refer to the [Frame Abort, Reconversion, or Short-Cycling](#) section).

## 8.5 Register Maps and Serial Interface

### 8.5.1 Serial Interface

The device uses the serial clock (SCLK) for synchronizing data transfers in and out of the device.

The  $\overline{CS}$  signal defines one conversion and serial transfer frame. A frame starts with a  $\overline{CS}$  falling edge and ends with a  $\overline{CS}$  rising edge. Between the start and end of the frame, a minimum of  $N$  SCLK falling edges must be provided to validate the read or write operation. As shown in [Table 3](#),  $N$  depends upon the interface mode used to read the conversion result. When  $N$  SCLK falling edges are provided, the write operation attempted in the frame is validated and the internal user-programmable registers are updated on the subsequent  $\overline{CS}$  rising edge. This  $\overline{CS}$  rising edge also ends the frame.

**Table 3. SCLK Falling Edges for a Valid Write Operation**

INTERFACE MODE	MINIMUM SCLK FALLING EDGES REQUIRED TO VALIDATE WRITE OPERATION $N$
32-CLK, dual-SDO mode (default). See the <a href="#">32-CLK, Dual-SDO Mode</a> section.	32
32-CLK, single-SDO mode. See the <a href="#">32-CLK, Single-SDO Mode</a> section.	48
16-CLK, dual-SDO mode. See the <a href="#">16-CLK, Dual-SDO Mode</a> section.	16
16-CLK, single SDO mode. See the <a href="#">16-CLK, Single SDO Mode</a> section.	32

If  $\overline{CS}$  is brought high before providing  $N$  SCLK falling edges, the write operation attempted in the frame is not valid. Refer to the [Frame Abort, Reconversion, or Short-Cycling](#) section for more details.

### 8.5.2 Write to User Programmable Registers

The device features three user-programmable registers: the configuration register (CFR), the REFDAC\_A register, and the REFDAC\_B register. These registers can be written with the device SDI pin. The first 16 bits of data on SDI are latched into the device on the first 16 SCLK falling edges. However, the new configuration takes effect only when the read or write operation is validated. If these registers are not required to update, SDI must remain low during the respective frames.

The first four SDI data bits (B[15:12]) determine what operation is performed (that is, either a read or write operation or no operation), which register address the operation uses, and the function of the next 12 SDI data bits (B[11:0]). [Table 4](#) lists the various combinations supported for B[15:12].

**Table 4. Data Write Operation**

B15	B14	B13	B12	OPERATION	FUNCTION OF BITS B[11:0]
0	0	0	0	No operation is performed	These bits are ignored
0	0	0	1	REFDAC_A read	000h; see the <a href="#">Reading User-Programmable Registers</a> section
0	0	1	0	REFDAC_B read	000h; see the <a href="#">Reading User-Programmable Registers</a> section
0	0	1	1	CFR read	000h; see the <a href="#">Reading User-Programmable Registers</a> section
1	0	0	0	CFR write	See the <a href="#">Configuration Register (CFR)</a> section
1	0	0	1	REFDAC_A write	See the <a href="#">REFDAC_A</a> section
1	0	1	0	REFDAC_B write	See the <a href="#">REFDAC_B</a> section
1	0	1	1	No operation is performed	These bits are ignored
X	1	X	X	No operation is performed	These bits are ignored

### 8.5.2.1 Configuration Register (CFR)

The device operation configuration is controlled by the configuration register (CFR) status. Data written into the CFR in a valid frame (F) determine the device configuration for frame (F+1). The bit functions are outlined in [Figure 87](#). On power-up, all bits in the CFR default to 0.

**Figure 87. CFR Bit Functions**

15	14	13	12	11	10	9	8
WRITE/READ	0	ADDR1	ADDR0	RD_CLK_MODE	RD_DATA_LINES	INPUT_RANGE	0
7	6	5	4	3	2	1	0
0	REF_SEL	STANDBY	0	0	0	0	0

**Table 5. Configuration Register (CFR) Field Descriptions**

Bit	Field	Type	Reset	Description
15	WRITE/READ	W	0h	These bits select the user-programmable register. 1000 = Select this combination to write to the CFR register and to enable bits 11:0
14	0	R/W	0h	
13	ADDR1	R/W	0h	
12	ADDR0	R/W	0h	
11	RD_CLK_MODE	R/W	0h	This bit provides clock mode selection for the serial interface. 0 = Selects 32-CLK mode (default) 1 = Selects 16-CLK mode (Note that the ADS8354 only supports 32-CLK mode. This bit is ignored for the ADS8354.)
10	RD_DATA_LINES	R/W	0h	This bit provides data line selection for the serial interface. 0 = Use SDO_A to output ADC_A data and SDO_B to output of ADC_B data (default) 1 = Use only SDO_A to output of ADC_A data followed by ADC_B data
9	INPUT_RANGE	R/W	0h	This bit selects the maximum input range for the ADC as a function of the reference voltage provided to the ADC. See the <a href="#">Analog Inputs</a> section for more details. 0 = FSR equals $\pm V_{REF}$ 1 = FSR equals $\pm 2 \times V_{REF}$
8:7	0	R/W	0h	This bit must be set to 0 (default)
6	REF_SEL	R/W	0h	This bit selects the ADC reference voltage source. Refer to the <a href="#">Reference</a> section for more details. 0 = Use external reference (default) 1 = Use internal reference
5	STANDBY	W	0h	This bit is used by the device to enter or exit STANDBY mode. Refer to the <a href="#">STANDBY Mode</a> section for more details.
4	0	R/W	0h	This bit must be set to 0 (default)
3:0	0	R/W	0h	These bits must be set to 0 (default)

### 8.5.2.2 REFDAC Registers (REFDAC\_A and REFDAC\_B)

The REFDAC registers, bit functions, and resolution information are described in this section.

**Figure 88. REFDAC\_X Bit Functions**

15	14	13	12	11	10	9	8
WRITE/READ	0	ADDR1	ADDR0	D8	D7	D6	D5
7	6	5	4	3	2	1	0
D4	D3	D2	D1	D0	0	0	0

**Table 6. REFDAC Registers Field Descriptions**

Bit	Field	Type	Reset	Description
15	WRITE/READ	W	0h	These bits select the configurable register address. 1001 = Select this combination to write to the REFDAC_A register 1010 = Select this combination to write to the REFDAC_B register
14	0	R/W	0h	
13	ADDR1	R/W	0h	
12	ADDR0	R/W	0h	
11:3	D[8:0]	R/W	0h	Data to program the individual DAC output voltage. Note: These bits are valid only for bits 15:12 = 1001 or bits 15:12 = 1010. Table 7 shows the relationship between the REFDAC_x programmed value and the DAC_x output voltage.
2:0	0	R/W	0h	This bit must be set to 0 (default)

**Table 7. REFDAC Settings**

REFDAC_x VALUE (Bits 11:3 in Hex)	B[2:0]	Typical DAC_x OUPUT VOLTAGE (V) <sup>(1)</sup>
1FF (default)	000	2.5000
1FE	000	2.4989
1FD	000	2.4978
—	—	—
1D7	000	2.45
—	—	—
1AE	000	2.40
—	—	—
186	000	2.35
—	—	—
15D	000	2.30
—	—	—
134	000	2.25
—	—	—
10C	000	2.20
—	—	—
0E3	000	2.15
—	—	—
0BA	000	2.10
—	—	—
091	000	2.05
—	—	—
069	000	2.00
—	—	—
064 to 000	000	Do not use

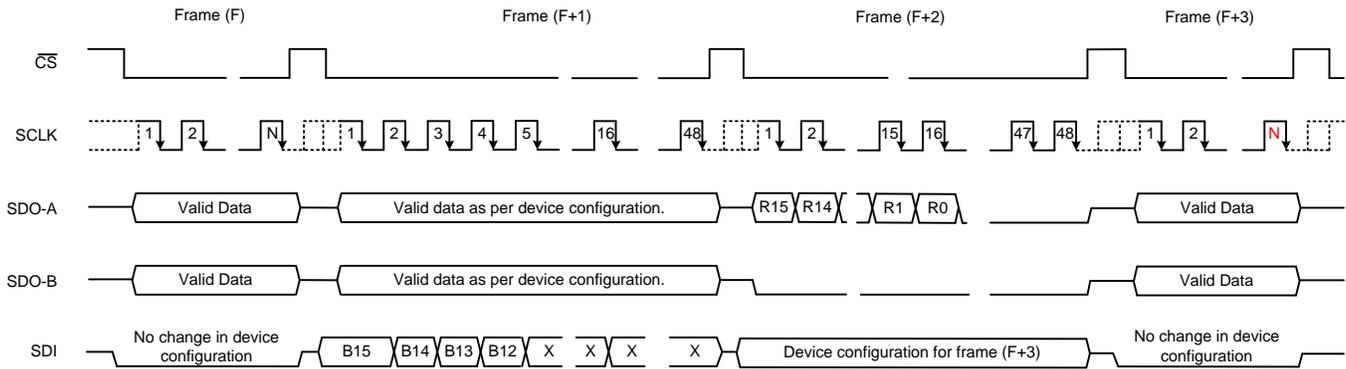
(1) Actual output voltage may vary by a few millivolts from the specified value. To obtain the desired output voltage, TI recommends starting with the specified register setting and then experimenting with five codes on either side of the specified register setting.

### 8.5.3 Data Read Operation

The device supports two types of read operations: reading user-programmable registers and reading conversion results.

#### 8.5.3.1 Reading User-Programmable Registers

The device supports a readback option for all user-programmable registers: CFR, REFDAC\_A, and REFDAC\_B. Figure 89 shows a detailed timing diagram for this operation.



Note that *N* is a function of the device configuration, as described in Table 3.

Figure 89. Register Readback Timing

To readback the user-programmable register settings, the appropriate control word should be transmitted to the device during frame (F+1), as shown in Table 8. Frame (F+1) must have at least 48 SCLK falling edges.

Table 8. Control Word to Readback User-Programmable Registers

USER-PROGRAMMABLE REGISTER	CONTROL WORD TO BE PROGRAMMED IN FRAME (F+1)	
	B[15:12] (Binary)	B[11:0] (Hex)
CFR	0011b	000h
REFDAC_A	0001b	000h
REFDAC_B	0010b	000h

Frame (F+2) must have at least 48 SCLK falling edges. During frame (F+2), SDO\_A outputs the contents of the selected user-programmable register on the first 16 SCLK falling edges (as shown in Table 9) and then outputs 0s for any subsequent SCLK falling edges. The SDO\_B pin outputs 0s for all the SCLK falling edges.

Table 9. Register Data Read Back

USER-PROGRAMMABLE REGISTER	DATA READ ON SDO-A IN FRAME (F+2)									
	R15	R14	R13	R12	R11	—	R3	R2	R1	R0
CFR	0	0	1	1	CFG.B11	—	CFG.B3	CFG.B2	CFG.B1	CFG.B0
REFDAC_A	0	0	0	1	REFDAC_A.D8	—	REFDAC_A.D0	0	0	0
REFDAC_B	0	0	1	0	REFDAC_B.D8	—	REFDAC_B.D0	0	0	0

Register settings programmed during frame (F+2) determine the device configuration in frame (F+3).

### 8.5.3.2 Conversion Data Read

The device provides four different interface modes to the user for reading the conversion result. These modes offer flexible hardware connections and firmware programming. Table 10 shows how to select one of the four interface modes.

**Table 10. Interface Mode Selection**

CFR.B11	CFR.B10	INTERFACE MODE	MINIMUM SCLK FALLING EDGES REQUIRED TO VALIDATE WRITE OPERATION N
0	0	32-CLK, dual-SDO mode (default)	32
0	1	32-CLK, single-SDO mode	48
1	0	16-CLK, dual-SDO mode	16
1	1	16-CLK, single SDO mode	32

In the 32-CLK interface modes, the device uses an internal clock to convert the sampled analog signal. The conversion is completed during the first 16 periods of SCLK and the conversion result can be read on the subsequent SCLK falling edges. All devices in the family (that is, ADS8354, ADS7854, and ADS7254) support the 32-CLK interface modes.

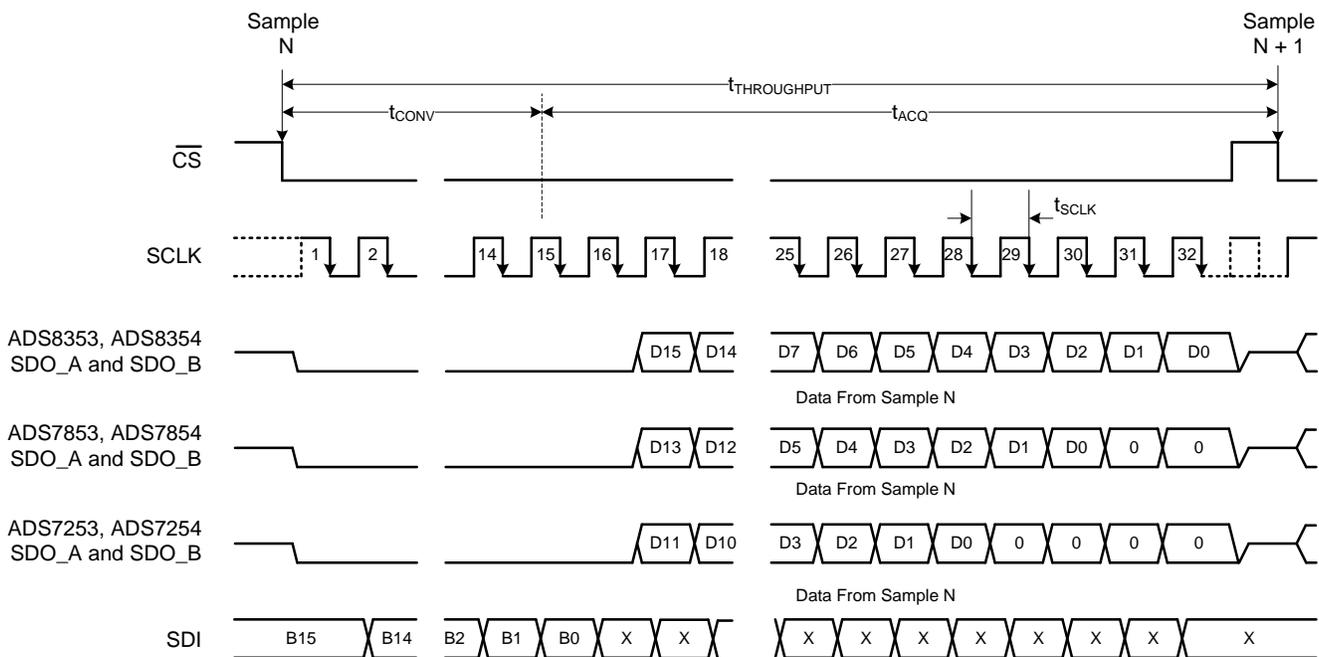
In addition to the 32-CLK interface modes, the ADS7854 and ADS7254 also support the 16-CLK interface modes. By using the 16-CLK interface modes, the same throughput can be achieved at much lower SCLK speeds.

The following sections detail the various interface modes supported by the device.

#### 8.5.3.2.1 32-CLK, Dual-SDO Mode (CFR.B11 = 0, CFR.B10 = 0, Default)

The 32-CLK, dual-SDO mode is the default mode supported by all devices. This mode can also be selected by writing CFR.B11 = 0 and CFR.B10 = 0.

In this mode, the SDO\_A pin outputs the ADC\_A conversion result and the SDO\_B pin outputs the ADC\_B conversion result. Figure 90 shows a detailed timing diagram for this mode.



**Figure 90. 32-CLK, Dual-SDO Mode Timing Diagram**

A  $\overline{CS}$  falling edge brings the serial data bus out of 3-state and also outputs a 0 on the SDO\_A and SDO\_B pins. The device converts the sampled analog input during the conversion time ( $t_{CONV}$ ). SDO\_A and SDO\_B read 0 during this period. After completing the conversion process, the sample-and-hold circuit returns to sample mode. The device outputs the MSBs of ADC\_A and ADC\_B on SDO\_A and SDO\_B pins, respectively, on the 16th SCLK falling edge. The subsequent SCLK falling edges are used to shift out the rest of the bits of the conversion result, as shown in [Table 11](#).

**Table 11. Data Launch Edge**

DEVICE	PINS	LAUNCH EDGE												
		$\overline{CS}$	SCLK											$\overline{CS}$
		↓	↓1	—	↓15	↓16	—	↓27	↓28	↓29	↓30	↓31	↓32 ...	↑
ADS8354	SDO-A	0	0	—	0	D15_A	—	D4_A	D3_A	D2_A	D1_A	D0_A	0 ...	Hi-Z
	SDO-B	0	0	—	0	D15_B	—	D4_B	D3_B	D2_B	D1_B	D0_B	0 ...	Hi-Z
ADS7854	SDO-A	0	0	—	0	D13_A	—	D2_A	D1_A	D0_A	0	0	0 ...	Hi-Z
	SDO-B	0	0	—	0	D13_B	—	D2_B	D1_B	D0_B	0	0	0 ...	Hi-Z
ADS7254	SDO-A	0	0	—	0	D11_A	—	D0_A	0	0	0	0	0 ...	Hi-Z
	SDO-B	0	0	—	0	D11_B	—	D0_B	0	0	0	0	0 ...	Hi-Z

In this mode, at least 32 SCLK falling edges must be given to validate the read or write frame. A  $\overline{CS}$  rising edge ends the frame and puts the serial bus into 3-state.

Refer to [Table 12](#) for timing specifications specific to this serial interface mode.

**Table 12. 32-CLK, Dual-SDO Interface Specific Timing**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TIMING REQUIREMENTS</b>					
$t_{CLK}$	CLOCK period	ADS8354	41.66		ns
		ADS7854	29.4		ns
		ADS7254	29.4		ns
$t_{ACQ}$	Acquisition time	$33 \times t_{CLK} - t_{CONV}$			ns
<b>TIMING SPECIFICATIONS</b>					
$t_{CONV}$	Conversion time	ADS8354	640		ns
		ADS7854	450		ns
		ADS7254	450		ns

8.5.3.2.2 32-CLK, Single-SDO Mode (CFR.B11 = 0, CFR.B10 = 1)

The 32-CLK, single-SDO mode provides the option of using only one SDO pin (SDO\_A) to read conversion results from both ADCs (ADC\_A and ADC\_B). SDO\_B remains in 3-state and can be treated as a no connect (NC) pin.

This mode can be selected by writing CFR.B11 = 0 and CFR.B10 = 1. Figure 91 shows a detailed timing diagram for this mode.

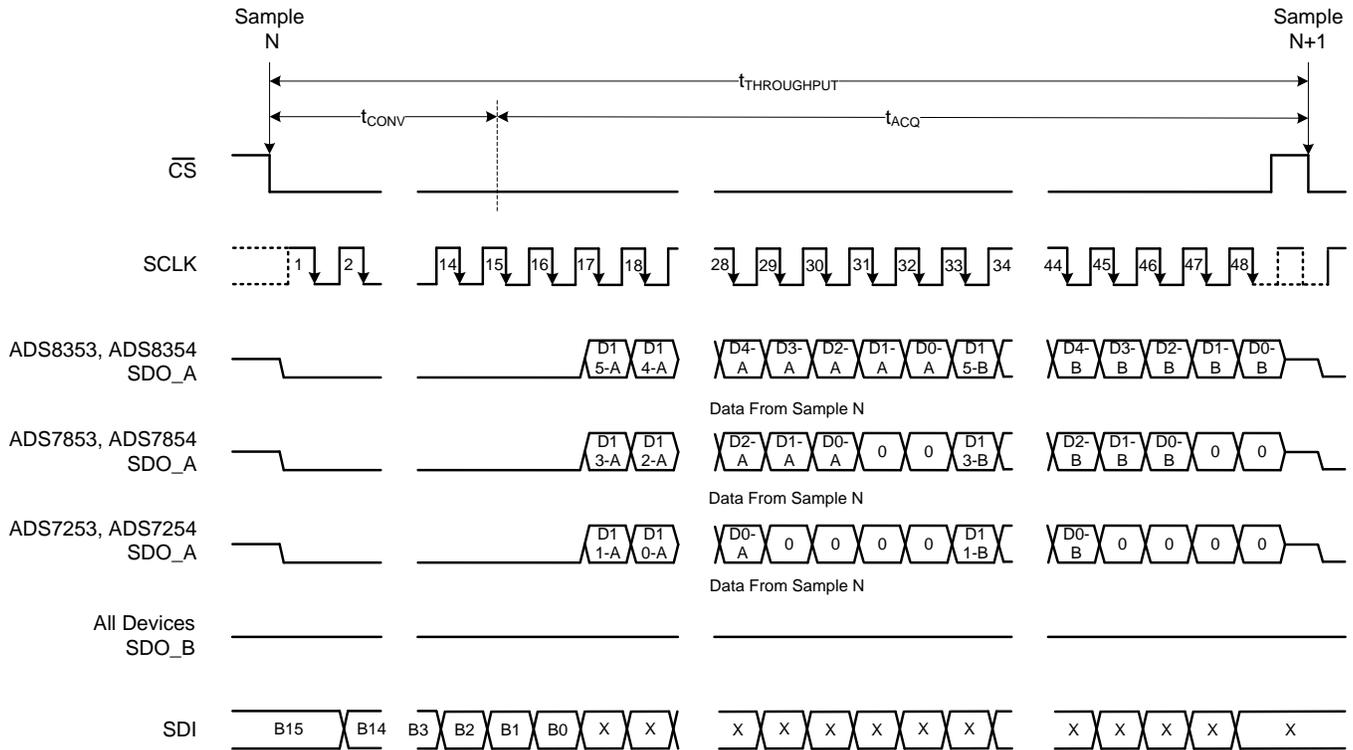


Figure 91. 32-CLK, Single-SDO Mode Timing Diagram

A  $\overline{CS}$  falling edge brings the serial data bus out of 3-state and also outputs a 0 on the SDO\_A pin. The device converts the sampled analog input during the conversion time ( $t_{CONV}$ ). SDO\_A reads 0 during this period. After completing the conversion process, the sample-and-hold circuit goes back into sample mode. The device outputs the MSB of ADC\_A on the SDO\_A pin on the 16th SCLK falling edge. The subsequent SCLK falling edges are used to shift out the conversion result of ADC\_A followed by the conversion result of ADC\_B on the SDO\_A pin, as shown in Table 13.

Table 13. Data Launch Edge

DEVICE	PIN	LAUNCH EDGE																			
		$\overline{CS}$		SCLK																$\overline{CS}$	
		↓	↓1	—	↓15	↓16	—	↓27	↓28	↓29	↓30	↓31	↓32	—	↓43	↓44	↓45	↓46	↓47	↓48 ...	↑
ADS8354	SDO-A	0	0	—	0	D15_A	—	D4_A	D3_A	D2_A	D1_A	D0_A	D15_B	—	D4_B	D3_B	D2_B	D1_B	D0_B	0 ...	Hi-Z
ADS7854	SDO-A	0	0	—	0	D13_A	—	D2_A	D1_A	D0_A	0	0	0	—	D2_B	D1_B	D0_B	0	0	0 ...	Hi-Z
ADS7254	SDO-A	0	0	—	0	D11_A	—	D0_A	0	0	0	0	0	—	D0_B	0	0	0	0	0 ...	Hi-Z

In this mode, at least 48 SCLK falling edges must be given to validate the read or write frame. A  $\overline{CS}$  rising edge ends the frame and puts the serial bus into 3-state.

Refer to Table 14 for timing specifications specific to this serial interface mode.

Table 14. 32-CLK, Single-SDO Interface Specific Timing

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TIMING REQUIREMENTS</b>					
$t_{CLK}$	CLOCK period	ADS8354		41.66	ns
		ADS7854		29.4	ns
		ADS7254		29.4	ns
$t_{ACQ}$	Acquisition time		$49 \times t_{CLK} - t_{CONV}$		ns
<b>TIMING SPECIFICATIONS</b>					
$t_{CONV}$	Conversion time	ADS8354		640	ns
		ADS7854		450	ns
		ADS7254		450	ns

8.5.3.2.3 16-CLK, Dual-SDO Mode (CFR.B11 = 1, CFR.B10 = 0)

The 16-CLK, dual-SDO mode is designed to support the maximum throughput at lower SCLK frequencies. This interface mode is not supported by the ADS8354.

For the ADS7854 and ADS7254, this interface mode can be selected by writing CFR.B11 = 1 and CFR.B10 = 0. In this mode, the SDO\_A pin outputs the ADC\_A conversion result and the SDO\_B pin outputs the ADC\_B conversion result. Figure 92 shows a detailed timing diagram for this mode.

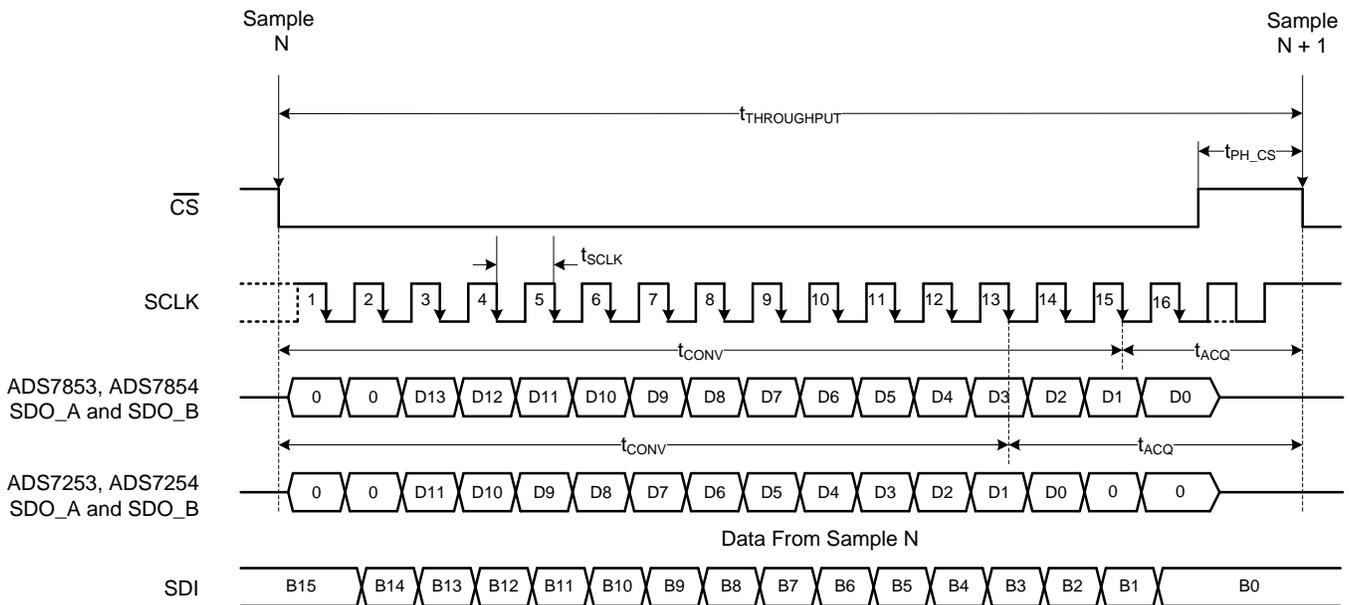


Figure 92. 16-CLK, Dual-SDO Mode Timing Diagram

A  $\overline{CS}$  falling edge brings the serial data bus out of 3-state and also outputs a 0 on the SDO\_A and SDO\_B pins. The subsequent SCLK falling edges are used for conversion and for data transfer using the serial interface, as shown in [Table 15](#).

The sample-and-hold circuit goes back into sample mode as soon as the conversion process is over.

**Table 15. Data Launch Edge**

DEVICE	PINS	LAUNCH EDGE								
		$\overline{CS}$	SCLK							$\overline{CS}$
		↓	↓1	↓2	—	↓13	↓14	↓15	↓16 ...	↑
ADS7854	SDO-A	0	0	D13_A	—	D2_A	D1_A	D0_A	0 ...	Hi-Z
	SDO-B	0	0	D13_B	—	D2_B	D1_B	D0_B	0 ...	Hi-Z
ADS7254	SDO-A	0	0	D11_A	—	D0_A	0	0	0 ...	Hi-Z
	SDO-B	0	0	D11_B	—	D0_B	0	0	0 ...	Hi-Z

In this mode, at least 16 SCLK falling edges must be given to validate the read or write frame. A  $\overline{CS}$  rising edge ends the frame and puts the serial bus into 3-state.

Refer to [Table 16](#) for timing specifications specific to this serial interface mode.

**Table 16. 16-CLK, Dual-SDO Interface Specific Timing**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TIMING REQUIREMENTS</b>					
$t_{CLK}$	CLOCK period	ADS7854	55.5		ns
		ADS7254	55.5		ns
$t_{ACQ}$	Acquisition time	ADS7854		$4 \times t_{CLK}$	ns
		ADS7254		$6 \times t_{CLK}$	ns
<b>TIMING SPECIFICATIONS</b>					
$t_{CONV}$	Conversion time	ADS7854		$14 \times t_{CLK}$	ns
		ADS7254		$12 \times t_{CLK}$	ns

8.5.3.2.4 16-CLK, Single-SDO Mode (CFR.B11 = 1, CFR.B10 = 1)

The 16-CLK, single-SDO mode provides the option of using only one SDO pin (SDO\_A) and a lower-speed clock to read the conversion results of both ADCs. This interface mode is not supported by the ADS8354.

For the ADS7854 and ADS7254, this mode can be selected by writing CFR.B11 = 1 and CFR.B10 = 1. The SDO\_A pin is used to output the conversion results of both ADCs (ADC\_A and ADC\_B). SDO\_B remains in 3-state and can be treated as a no connect (NC) pin. Figure 93 shows a detailed timing diagram for this mode.

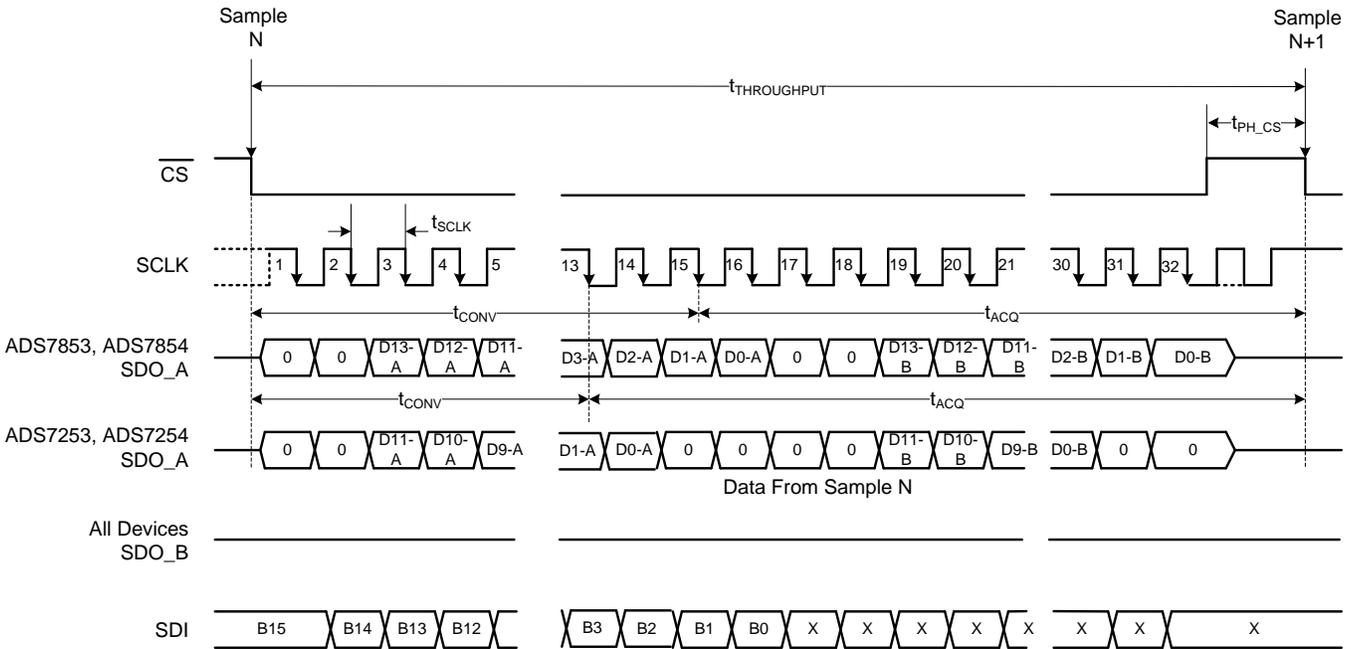


Figure 93. 16-CLK, Single-SDO Mode Timing Diagram

A  $\overline{CS}$  falling edge brings the serial data bus out of 3-state and also outputs a 0 on the SDO\_A pin. The subsequent SCLK falling edges are used for conversion and for data transfer using the serial interface, as shown in Table 17.

The sample-and-hold circuit goes back into sample mode as soon as the conversion process is over.

Table 17. Data Launch Edge

DEVICE	PIN	LAUNCH EDGE															
		$\overline{CS}$	SCLK													$\overline{CS}$	
		↓	↓1	↓2	—	↓13	↓14	↓15	↓16	↓17	↓18	—	↓29	↓30	↓31	↓32 ...	↑
ADS7854	SDO-A	0	0	D13_A	—	D2_A	D1_A	D0_A	0	0	D13_B	—	D2_B	D1_B	D0_B	0 ...	Hi-Z
ADS7254	SDO-A	0	0	D11_A	—	D0_A	0	0	0	0	D11_B	—	D0_B	0	0	0 ...	Hi-Z

In this mode, at least 32 SCLK falling edges must be given to validate the read/write frame. A  $\overline{CS}$  rising edge ends the frame and puts the serial bus into 3-state.

Refer to [Table 18](#) for timing specifications specific to this serial interface mode.

**Table 18. 16-CLK, Single-SDO Interface Specific Timing**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TIMING REQUIREMENTS</b>					
$t_{CLK}$	CLOCK period	ADS7854		55.5	ns
		ADS7254		55.5	ns
$t_{ACQ}$	Acquisition time	ADS7854		$19 \times t_{CLK}$	ns
		ADS7254		$21 \times t_{CLK}$	ns
<b>TIMING SPECIFICATIONS</b>					
$t_{CONV}$	Conversion time	ADS7854		$14 \times t_{CLK}$	ns
		ADS7254		$12 \times t_{CLK}$	ns

### 8.5.4 Low-Power Modes

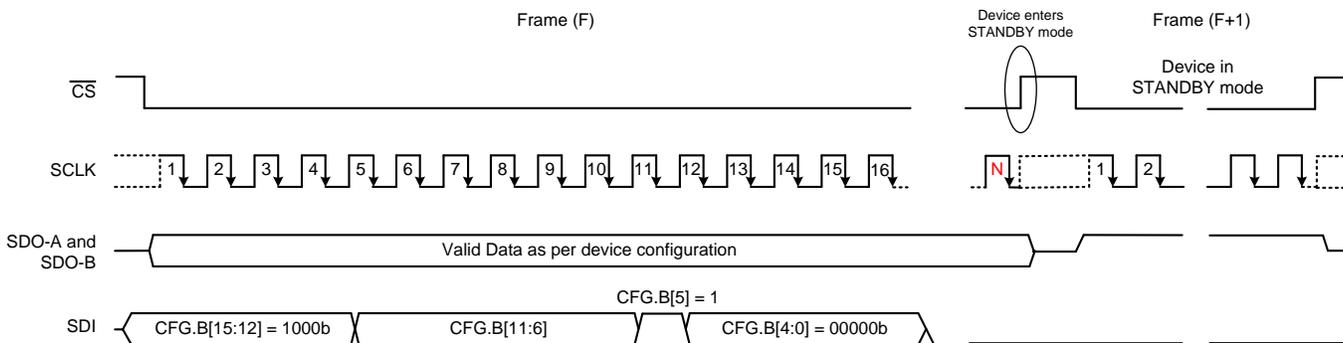
In normal mode of operation, all internal circuits of the device are always powered up and the device is always ready to commence a new conversion. This mode enables the device to support the rated throughput. The device also supports two low-power modes to optimize the power consumption at lower throughputs: STANDBY mode and software power-down (SPD) mode.

#### 8.5.4.1 STANDBY Mode

The device supports a STANDBY mode of operation where some of the internal circuits of the device are powered down. However, if bit 6 in configuration register is set to 1 (CFR.B6 = 1), then the internal reference is not powered down and the contents of the REFDAC\_A and REFDAC\_B registers are retained to enable faster power-up to a normal mode of operation.

As shown in [Figure 94](#), a valid write operation in frame (F) to program the configuration register with B5 set to 1 (CFR.B5 = 1) places the device into a STANDBY mode of operation on the following  $\overline{CS}$  rising edge. While in STANDBY mode, SDO\_A and SDO\_B output all 1s when  $\overline{CS}$  is low and remain in 3-state when  $\overline{CS}$  is high.

To remain in STANDBY mode, SDI must remain low in the subsequent frames.

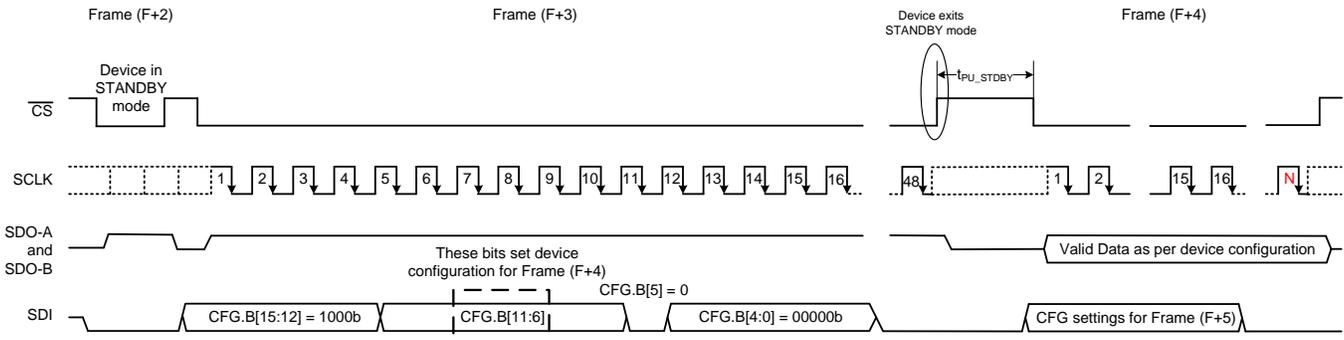


Note that  $N$  is a function of the device configuration, as described in [Table 3](#).

**Figure 94. Enter STANDBY Mode**

As shown in [Figure 95](#), a valid write operation in frame (F+3) by writing the configuration register with B5 set to 0 (CFR.B5 = 0) brings the device out of STANDBY mode on the following  $\overline{\text{CS}}$  rising edge. Frame (F+3) must have at least 48 SCLK falling edges.

After exiting the STANDBY mode, a delay of  $t_{\text{PU\_STDBY}}$  must elapse for the internal circuits to fully power-up and resume normal operation in frame (F+4). Device configuration for frame (F+4) is determined by the status of the CFR.B[11:6] bits programmed during frame (F+3).



Note that  $N$  is a function of the device configuration, as described in [Table 3](#).

**Figure 95. Exit STANDBY Mode**

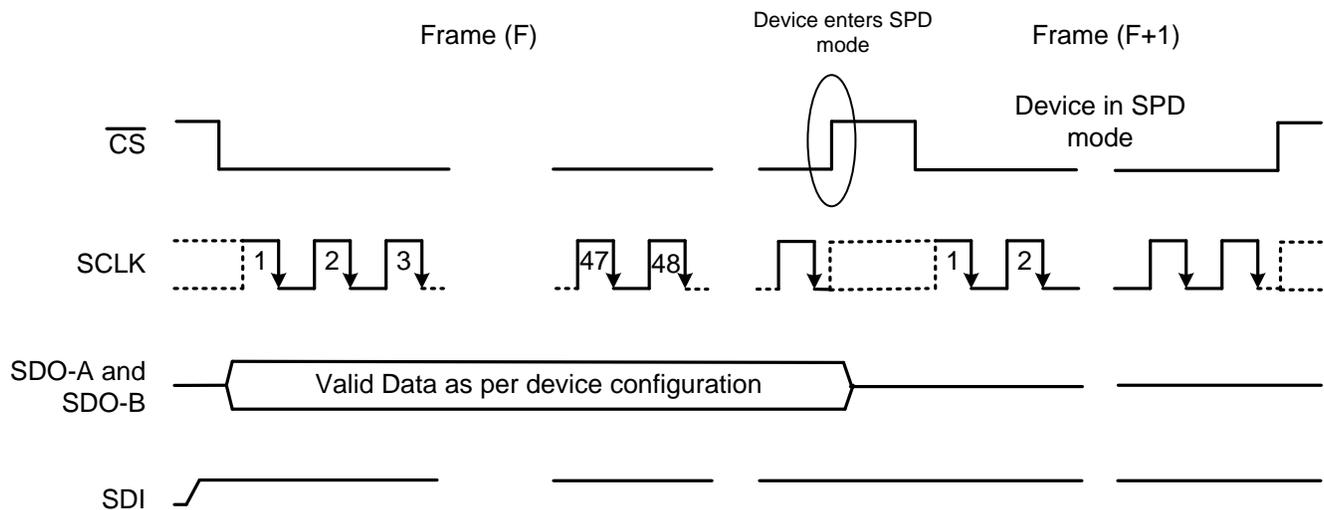
Refer to the [Timing Characteristics: Serial Interface](#) for timing specifications for this operating mode.

### 8.5.4.2 Software Power-Down (SPD) Mode

In software power-down (SPD) mode, all internal circuits (including the internal references) are powered down. However, the contents of the REFDAC\_A and REFDAC\_B registers are retained.

As shown in [Figure 96](#), to enter SPD mode, the device must be selected (by bringing  $\overline{CS}$  low) and SDI must be kept high for a minimum of 48 SCLK cycles during frame (F). The device goes to SPD on the  $\overline{CS}$  rising edge following frame (F). While in SPD mode, SDO\_A and SDO\_B go to 3-state irrespective of the status of the  $\overline{CS}$  signal.

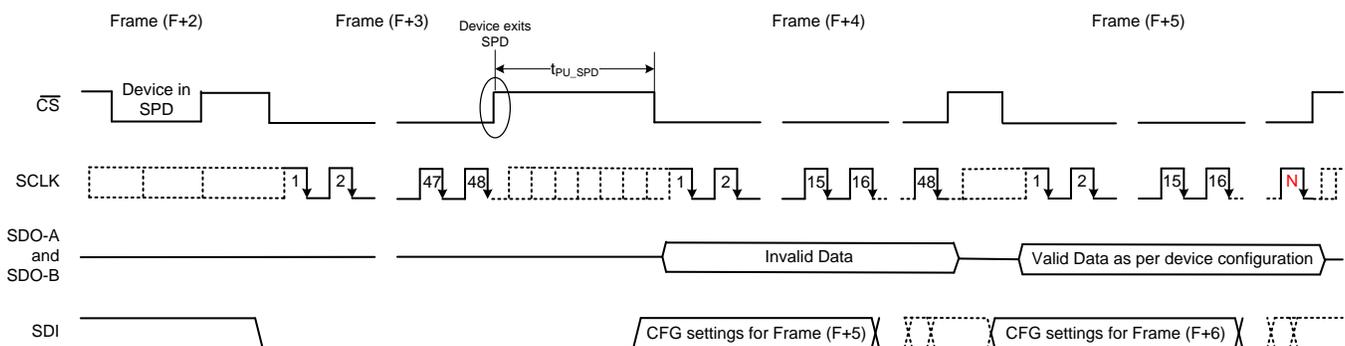
To remain in SPD mode, SDI must remain high in subsequent frames.



**Figure 96. Enter SPD Mode**

As shown in [Figure 97](#), to exit SPD mode, the device must be selected (by bringing  $\overline{CS}$  low) and SDI must be kept low for a minimum of 48 SCLK cycles during frame (F+3). The device starts powering-up on a  $\overline{CS}$  rising edge following frame (F+3). After frame (F+3), a delay of  $t_{PU\_SPD}$  must elapse before programming the configuration register.

A valid write operation in frame (F+4) sets the device configuration for frame (F+5). Frame (F+4) must have at least 48 SCLK falling edges. The output data in frame (F+4) should be discarded.



Note that  $N$  is a function of the device configuration, as described in [Table 3](#).

**Figure 97. Exit SPD Mode**

Refer to the [Timing Characteristics: Serial Interface](#) for timing specifications for this operating mode.

### 8.5.5 Frame Abort, Reconversion, or Short-Cycling

As discussed in Figure 98, the minimum number of SCLK falling edges (N) that must be provided between the beginning and end of the frame depends on the serial interface mode. The SCLK falling edges (N) program the device and retrieve the conversion result. If  $\overline{\text{CS}}$  is brought high before the expected number of SCLK falling edges are provided, the current frame is aborted and the device starts sampling the new analog input signal.

If frame (F) is aborted, then the register write operation attempted in frame (F) is considered invalid and the internal registers are not updated. The device continues to have the same configuration in frame (F+1) from frame (F).

The output data bits latched before the  $\overline{\text{CS}}$  rising edge are still valid data that correspond to sample N.

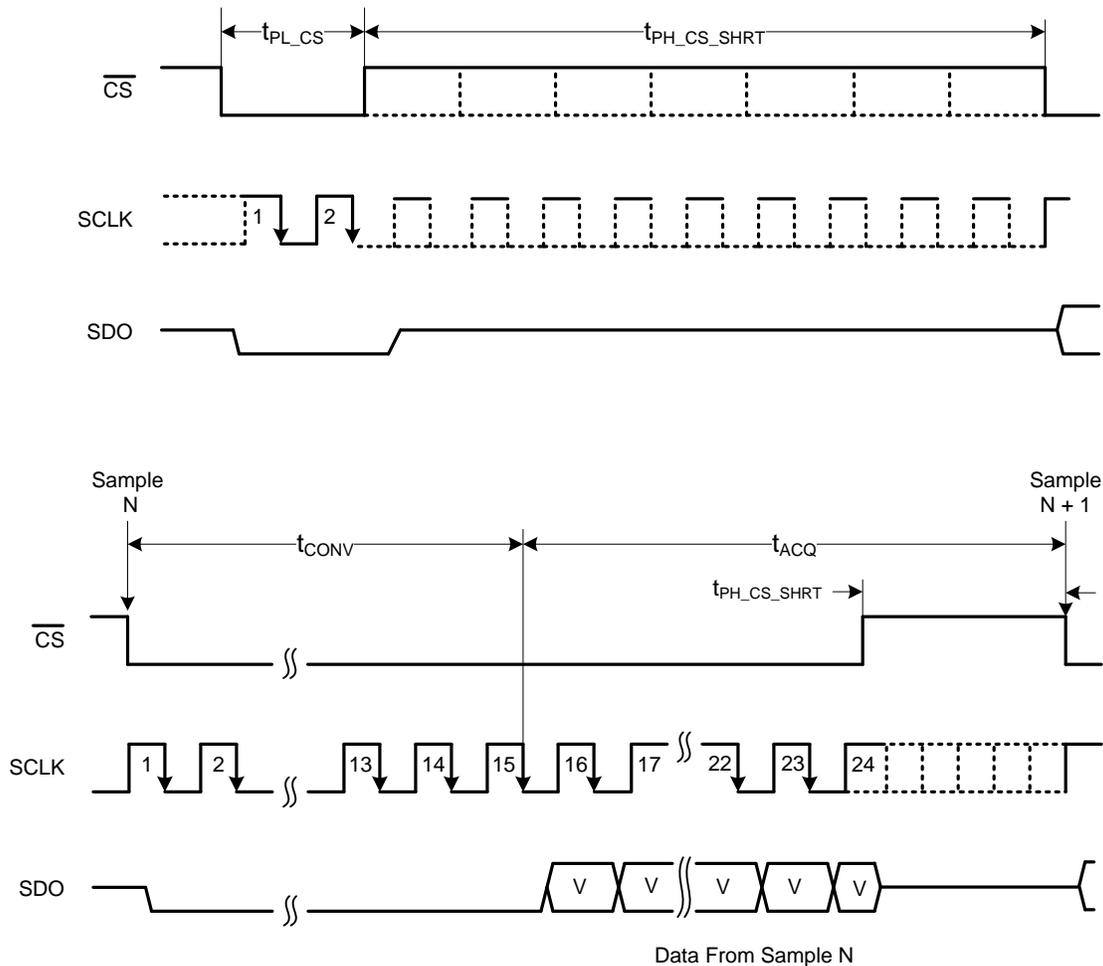


Figure 98. Frame Abort, Reconversion, or Short-Cycling Feature

Refer to the [Timing Characteristics: Serial Interface](#) for timing specifications for this operating mode.

## 9 Application and Implementation

### 9.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing these circuits, and some application circuits designed using these devices.

The device supports operation either with an internal or external reference source. Refer to the [Reference](#) section for details about the decoupling requirements.

The reference source to the ADC must provide low-drift and very accurate dc voltage and support the dynamic charge requirements without affecting the noise and linearity performance of the device. The output broadband noise (typically in the order of a few 100  $\mu\text{V}_{\text{RMS}}$ ) of the reference source must be appropriately filtered by using a low-pass filter with a cutoff frequency of a few hundred hertz. After band-limiting the noise from the reference source, the next important step is to design a reference buffer that can drive the dynamic load posed by the reference input of the ADC. At the start of each conversion, the reference buffer must regulate the voltage of the reference pin within 1 LSB of the intended value. This condition necessitates the use of a large filter capacitor at the reference pin of the ADC. The amplifier selected to drive the reference input pin must be stable while driving this large capacitor and should have low output impedance, low offset, and temperature drift specifications. To reduce the dynamic current requirements and crosstalk between the channels, a separate reference buffer is recommended for driving the reference input of each ADC channel.

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC and functions as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

#### 9.1.1 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type and the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- *Small-signal bandwidth.* Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter at the ADC inputs. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, the amplifier bandwidth should be selected as described in [Equation 8](#):

$$\text{Unity - Gain Bandwidth} \geq 4 \times \left( \frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}} \right) \quad (8)$$

- *Noise.* Noise contribution of the front-end amplifiers should be as low as possible to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit should be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band-limited by designing a low cutoff frequency RC filter and is calculated by [Equation 9](#):

$$N_G \times \sqrt{2} \times \sqrt{\left( \frac{V_{1/f\_AMP\_PP}}{6.6} \right)^2 + e_{n\_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left( \frac{SNR(dB)}{20} \right)}$$

where:

- $V_{1/f\_AMP\_PP}$  is the peak-to-peak flicker noise in  $\mu\text{V}$ ,
- $e_{n\_RMS}$  is the amplifier broadband noise density in  $\text{nV}/\sqrt{\text{Hz}}$ ,
- $f_{-3dB}$  is the 3-dB bandwidth of the RC filter, and
- $N_G$  is the noise gain of the front-end circuit, which is equal to 1 in a buffer configuration. (9)

## Application Information (continued)

- **Distortion.** Both the ADC and the input driver introduce nonlinearity in a data acquisition block. As a rule of thumb, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver should be at least 10 dB lower than the distortion of the ADC, as shown in Equation 10.

$$\text{THD}_{\text{AMP}} \leq \text{THD}_{\text{ADC}} - 10 \text{ (dB)} \quad (10)$$

- **Settling Time.** For dc signals with fast transients that are common in a multiplexed application, the input signal must settle to the desired accuracy at the inputs of the ADC during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired accuracy. Therefore, the settling behavior of the input driver should always be verified by TINA™-SPICE simulations before selecting the amplifier.

### 9.1.2 Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an analog, antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass, RC filter, for which the 3-dB bandwidth is optimized based on specific application requirements. For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the ADC inputs during the small acquisition time window. For ac signals, the filter bandwidth should be kept low to band-limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system.

A filter capacitor,  $C_{\text{FLT}}$ , connected across the ADC inputs (as shown in Figure 99), filters the noise from the front-end drive circuitry, reduces the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor should be at least 10 times the specified value of the ADC sampling capacitance. For these devices, the input sampling capacitance is equal to 40 pF. Thus, the value of  $C_{\text{FLT}}$  should be greater than 400 pF. The capacitor should be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors ( $R_{\text{FLT}}$ ) are used at the output of the amplifiers. A higher value of  $R_{\text{FLT}}$  is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of  $R_{\text{FLT}}$  requires balancing the stability and distortion of the design. For these devices, TI recommends limiting the value of  $R_{\text{FLT}}$  to a maximum of 22  $\Omega$  in order to avoid any significant degradation in linearity performance. The tolerance of the selected resistors can be chosen as 1% because the use of a differential capacitor at the input balances the effects resulting from any resistor mismatch.

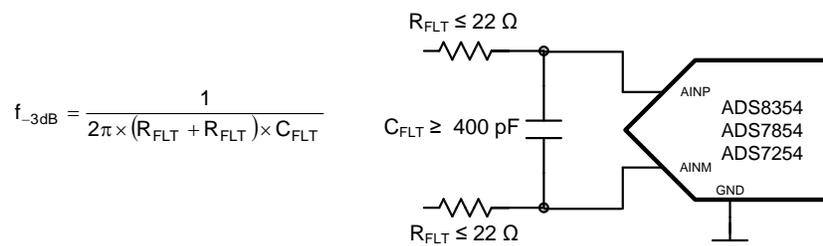
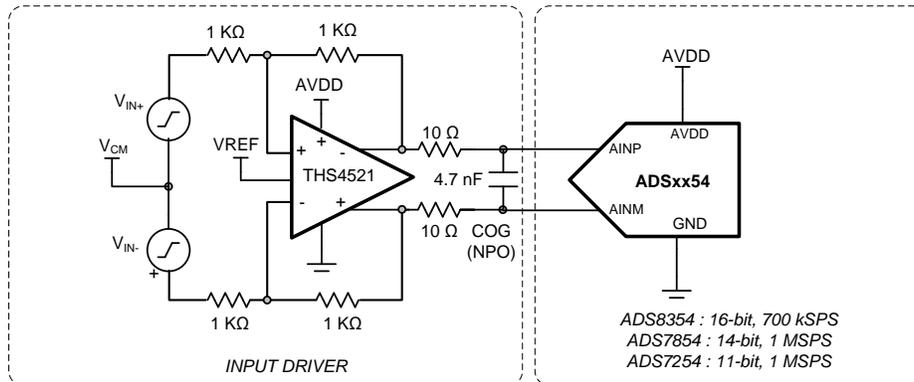


Figure 99. Antialiasing Filter

The input amplifier bandwidth should be much higher than the cutoff frequency of the antialiasing filter. TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected filter. If an amplifier has less than a 40° phase margin with 22- $\Omega$  resistors, using a different amplifier with higher bandwidth or reducing the filter cutoff frequency with a larger differential capacitor is advisable.

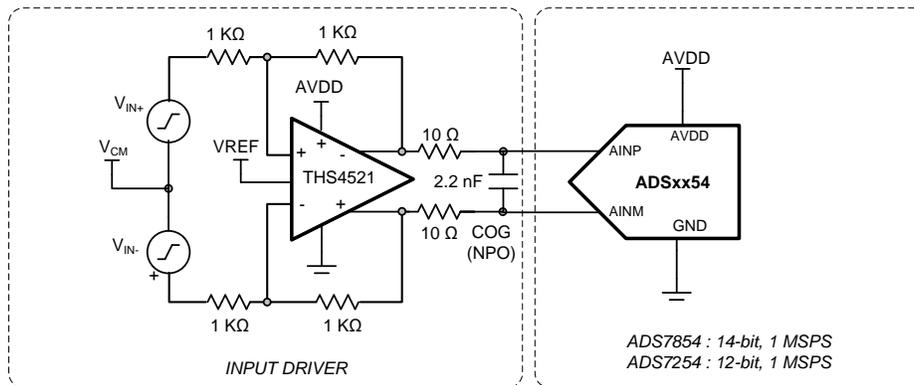
## 9.2 Typical Applications

### 9.2.1 DAQ Circuit to Achieve Maximum SINAD for a 10-kHz Input Signal at Full Throughput



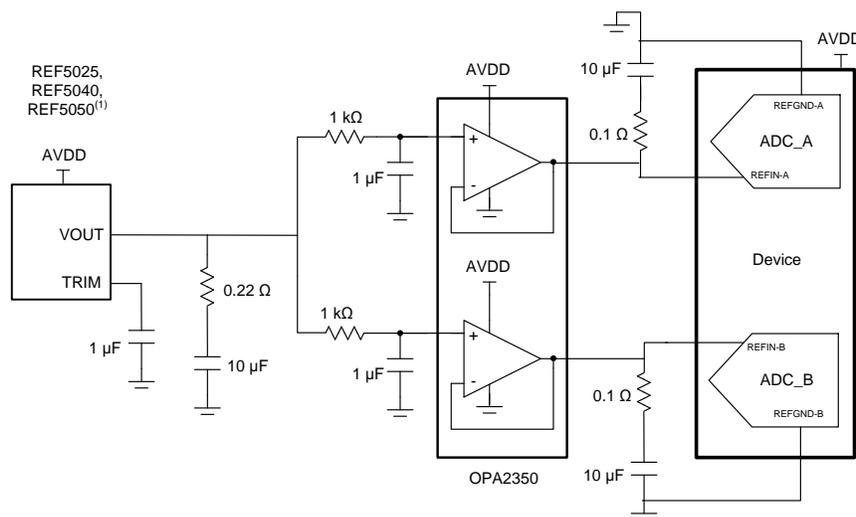
NOTE: Only one ADC channel is shown in this diagram. Replicate the same circuit for other ADC channels.

**Figure 100. DAQ Circuit: Maximum SINAD for a 10-kHz Input Signal at Full Throughput, 32-CLK Interface**



NOTE: Only one ADC channel is shown in this diagram. Replicate the same circuit for other ADC channels.

**Figure 101. DAQ Circuit: Maximum SINAD for a 10-kHz Input Signal at Full Throughput, 16-CLK Interface**



(1) When using the REF5050, AVDD must be set to 5.5 V.

**Figure 102. Reference Drive Circuit**

## Typical Applications (continued)

### 9.2.1.1 Design Requirements

To design an application circuit optimized to achieve target specifications listed in [Table 19](#).

**Table 19. Target Specifications**

TARGET SPECIFICATIONS		TEST CONDITIONS			
SNR	THD	DEVICE	INPUT SIGNAL FREQUENCY	THROUGHPUT	INTERFACE MODE
> 88 dB	< -100 dB	ADS8354	10 kHz	Maximum supported	32-CLK, dual-SDO
> 83.5 dB	< -95 dB	ADS7854	10 kHz	Maximum supported	32-CLK, dual-SDO
> 80.5 dB	< -88 dB	ADS7854	10 kHz	Maximum supported	16-CLK, dual-SDO
> 72.5 dB	< -88 dB	ADS7254	10 kHz	Maximum supported	32-CLK, dual-SDO
> 71.5 dB	< -85 dB	ADS7254	10 kHz	Maximum supported	16-CLK, dual-SDO

### 9.2.1.2 Detailed Design Procedure

Best practice is for the distortion from the input driver to be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using a fully-differential amplifier (FDA) that establishes a fixed common-mode level at the ADC input. The low-power [THS4521](#), used as an input driver, provides exceptional ac performance because of its extremely low-distortion and high-bandwidth specifications. The output common-mode voltage of the THS4521 is set by the voltage provided on its  $V_{OCM}$  pin. In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

The application circuit illustrated in [Figure 100](#) is optimized to achieve the lowest distortion and lowest noise for a 10-kHz input signal fed to the ADS8354 or ADS7854 or ADS7254 operating at full throughput with the default 32-CLK, dual-SDO interface mode. The input signal is processed through a high-bandwidth, low-distortion, fully-differential amplifier and a low-pass RC filter before being fed into the device.

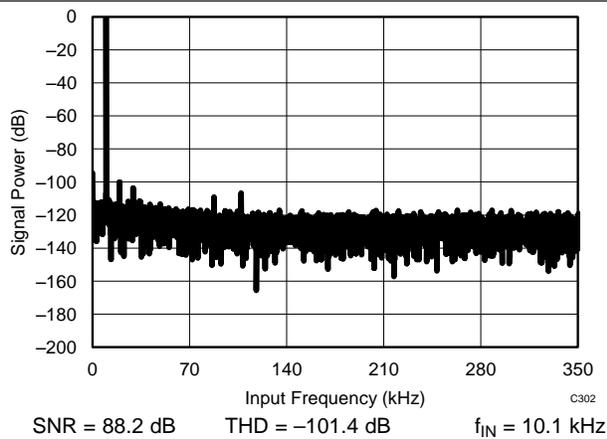
The ADS7854 and the ADS7254 also support 16-CLK interface modes that achieve the rated throughput rate at much lower SCLK frequencies. However, when using the 16-CLK interface modes, the device receives less acquisition time when compared to the 32-CLK interface modes. The application circuit illustrated in [Figure 101](#) is optimized to achieve the lowest distortion and lowest noise for a 10-kHz input signal fed to the ADS7854 or ADS7254 operating at full throughput with the 16-CLK, dual-SDO interface mode. The input signal is processed through a high-bandwidth, low-distortion, fully-differential amplifier and a low-pass RC filter before being fed into the device.

[Figure 102](#) illustrates the reference driver circuit when operation with an external reference is desired. The reference voltage is generated by the high-precision, low-noise [REF50xx](#) circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz. The decoupling capacitor on each reference pin is selected to be 10  $\mu$ F. The low output impedance, low noise, and fast settling time makes the [OPA2350](#) a good choice for driving this high capacitive load.

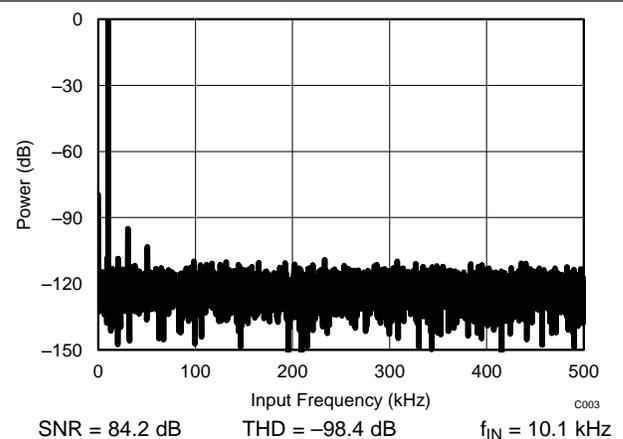
### 9.2.1.3 Application Curves

To minimize external components and to maximize the dynamic range of the ADC, device is configured to operate with internal reference (CFR.B6 = 1) and  $\pm 2 \times V_{REF\_X}$  input full scale range (CFR.B9 = 1).

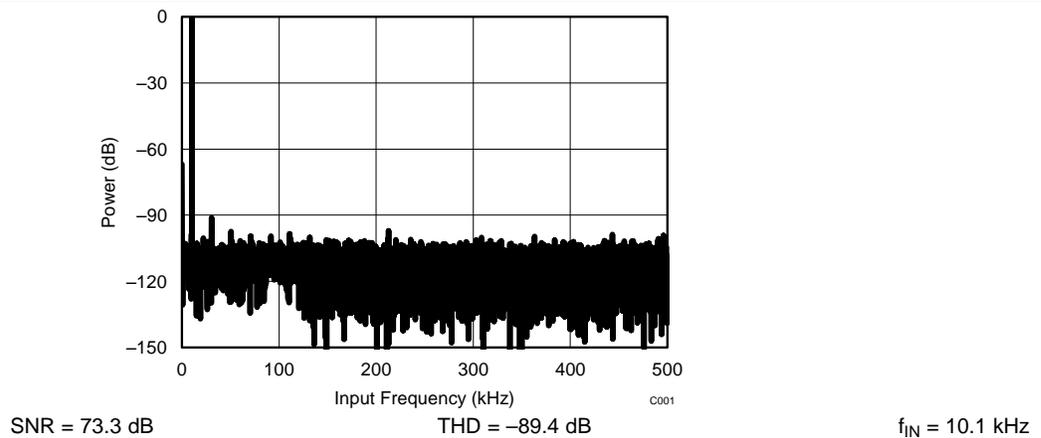
Figure 103, Figure 104, and Figure 105, show the FFT plots and test results obtained with the ADS8354, ADS7854, and ADS7254, respectively, operating at full throughput with a 32-CLK interface and the circuit configuration of Figure 100.



**Figure 103. ADS8354 in 32-CLK Interface Mode**

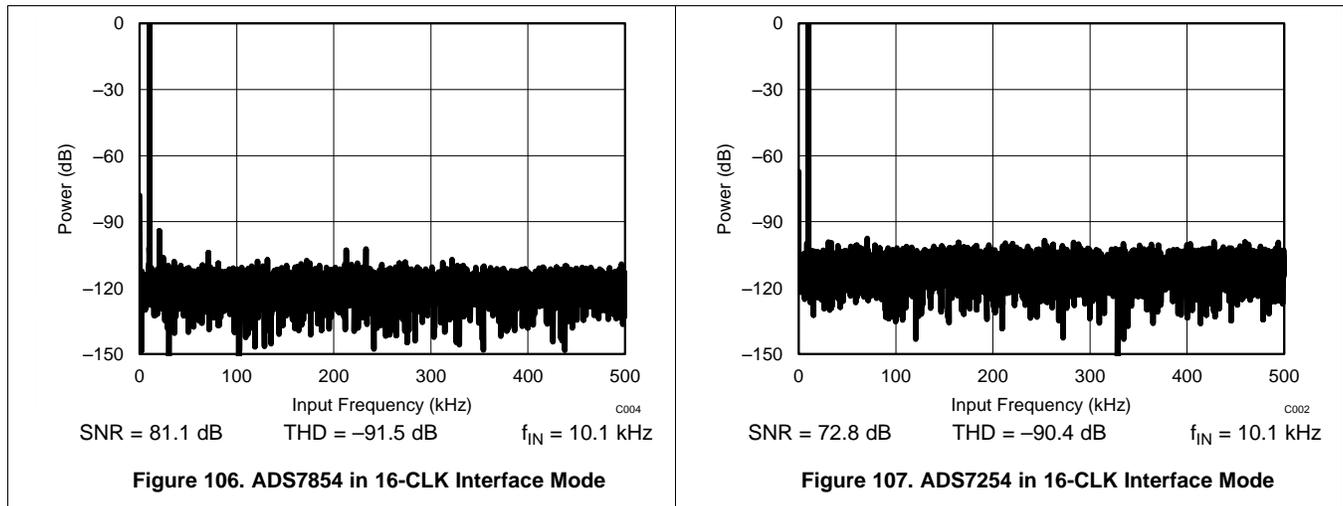


**Figure 104. ADS7854 in 32-CLK Interface Mode**

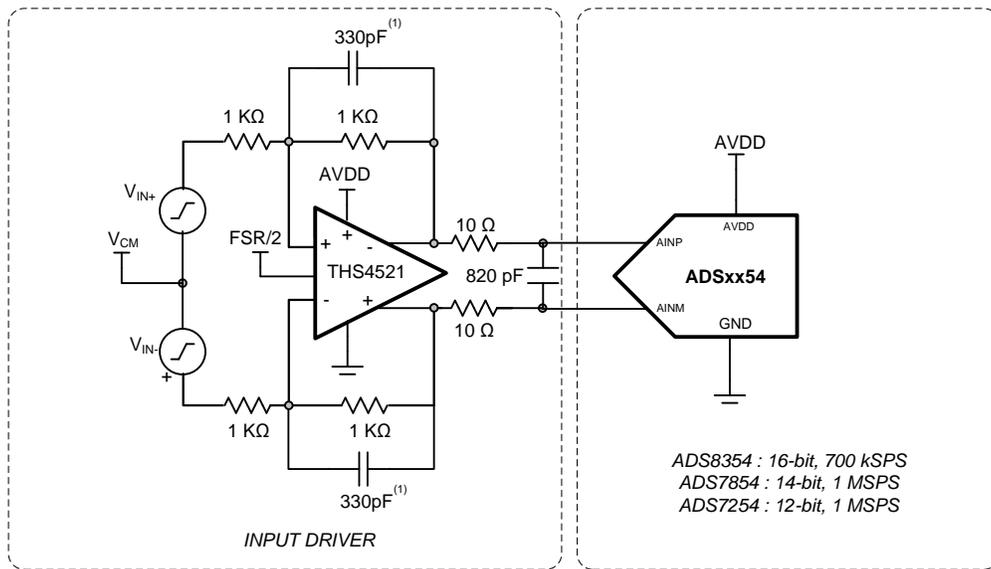


**Figure 105. ADS7254 in 32-CLK Interface Mode**

Figure 106 and Figure 107 show the FFT plots and test results obtained with the ADS7854 and ADS7254, respectively, operating at full throughput with 16-CLK interface and the circuit configuration of Figure 101.



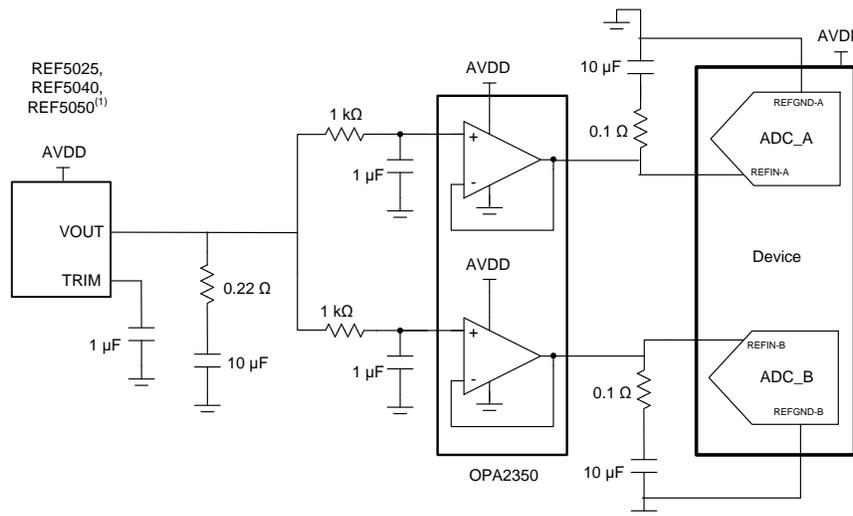
9.2.2 DAQ Circuit to Achieve Maximum SINAD for a 100-kHz Input Signal at Full Throughput



NOTE: Only one ADC channel is shown in this diagram. Replicate the same circuit for other ADC channels.

(1) The 330 pF capacitors are not required for ADS7854 and ADS7254.

Figure 108. DAQ Circuit: Maximum SINAD for a 100-kHz Input Signal at Full Throughput



(1) When using the REF5050, AVDD must be set to 5.5 V.

Figure 109. Reference Drive Circuit

### 9.2.2.1 Design Requirements

To design an application circuit optimized to achieve target specifications listed in [Table 20](#).

**Table 20. Target Specifications**

TARGET SPECIFICATIONS		TEST CONDITIONS			
SNR	THD	DEVICE	INPUT SIGNAL FREQUENCY	THROUGHPUT	INTERFACE MODE
> 86 dB	< -95 dB	ADS8354	100 kHz	Maximum supported	32-CLK, dual-SDO
> 81.5 dB	< -90 dB	ADS7854	100 kHz	Maximum supported	32-CLK, dual-SDO
> 79.5 dB	< -88 dB	ADS7854	100 kHz	Maximum supported	16-CLK, dual-SDO
> 72 dB	< -88 dB	ADS7254	100 kHz	Maximum supported	32-CLK, dual-SDO
> 71 dB	< -85 dB	ADS7254	100 kHz	Maximum supported	16-CLK, dual-SDO

### 9.2.2.2 Detailed Design Procedure

Best practice is for the distortion from the input driver to be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using a fully-differential amplifier (FDA) that establishes a fixed common-mode level at the ADC input. The low-power [THS4521](#), used as an input driver, provides exceptional ac performance because of its extremely low-distortion and high-bandwidth specifications. The output common-mode voltage of the THS4521 is set by the voltage provided on its  $V_{OCM}$  pin. In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

The application circuit illustrated in [Figure 108](#) is optimized to achieve the lowest distortion and lowest noise for a 100-kHz input signal fed to the ADS8354 or ADS7854 or ADS7254 operating at full throughput. The input signal is processed through a high-bandwidth, low-distortion, fully-differential amplifier and a low-pass RC filter before being fed into the device.

[Figure 102](#) illustrates the reference driver circuit when operation with an external reference is desired. The reference voltage is generated by the high-precision, low-noise [REF50xx](#) circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz. The decoupling capacitor on each reference pin is selected to be 10  $\mu$ F. The low output impedance, low noise, and fast settling time makes the [OPA2350](#) a good choice for driving this high capacitive load.

### 9.2.2.3 Application Curves

To minimize external components and to maximize the dynamic range of the ADC, device is configured to operate with internal reference (CFR.B6 = 1) and  $\pm 2 \times V_{REF\_X}$  input full scale range (CFR.B9 = 1).

Figure 110, Figure 111, and Figure 112 show the FFT plots and test results obtained with the ADS8354, ADS7854 and ADS7254, respectively, operating at full throughput with a 32-CLK interface and the circuit configuration of Figure 108.

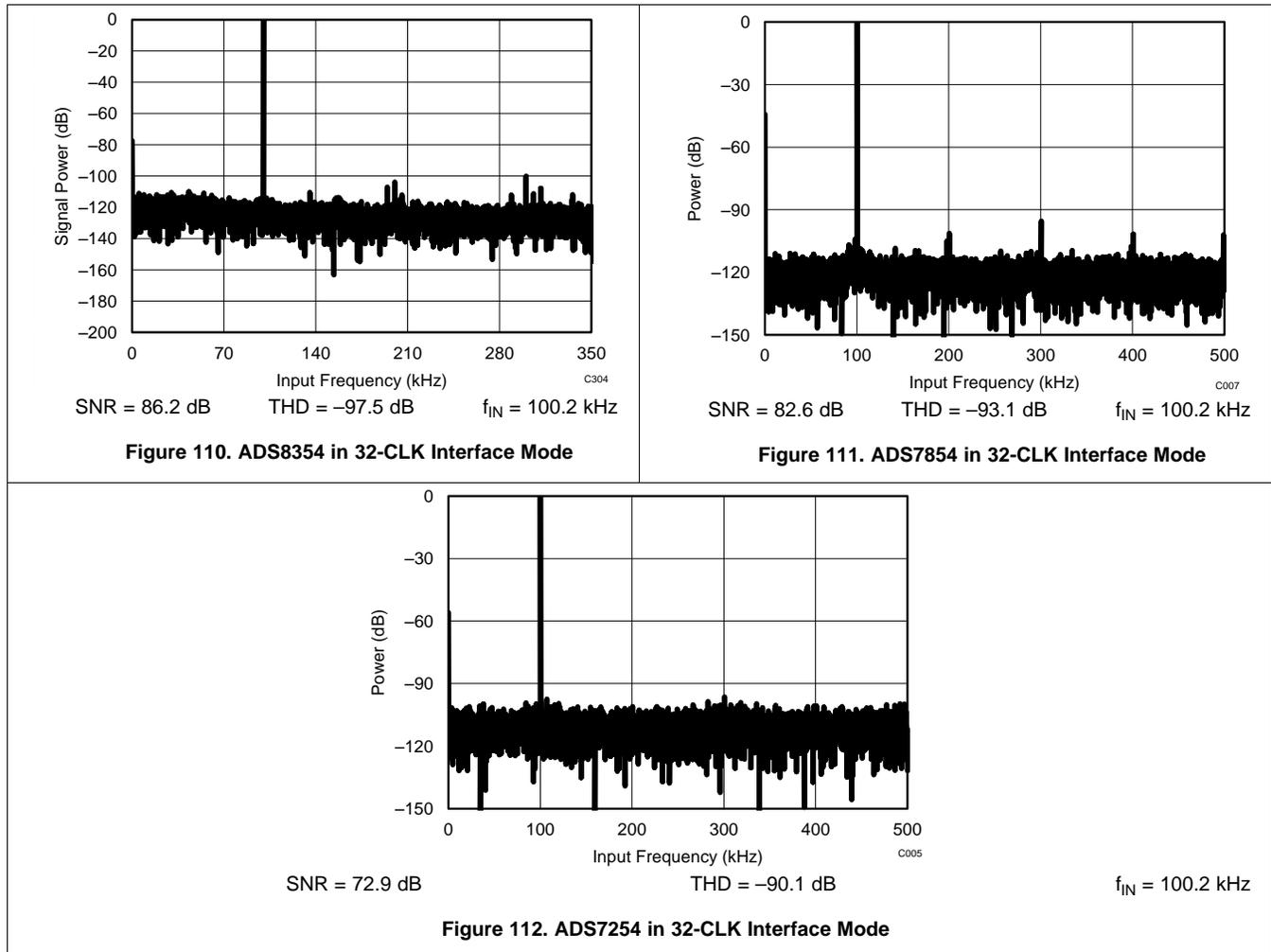
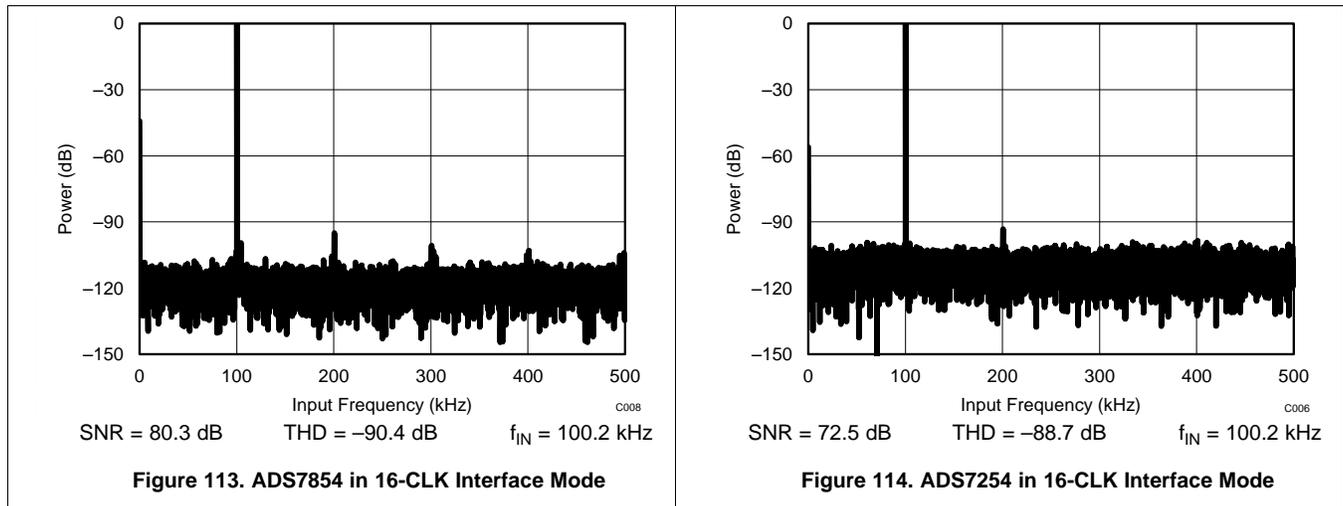


Figure 113 and Figure 114 show the FFT plots and test results obtained with the ADS7854 and ADS7254, respectively, operating with a 16-CLK interface and the circuit configuration of Figure 108.



## 10 Power-Supply Recommendations

The devices have two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible ranges.

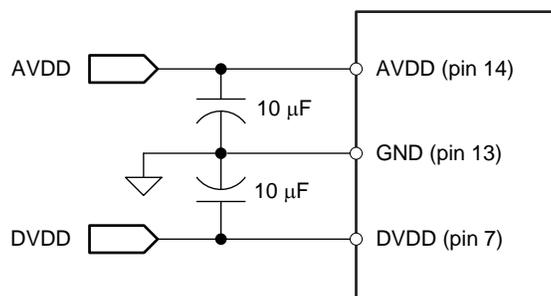
When using the device with  $\pm 2 \times V_{REF}$  input range (CFR.B9 = 1), the AVDD supply voltage value defines the permissible voltage swing on the analog input pins. To avoid saturation of output codes, and to use the full dynamic range on the analog input pins, AVDD must be set as shown in [Equation 11](#), [Equation 12](#), and [Equation 13](#):

$$AVDD \geq 2 \times V_{REF\_A} \quad (11)$$

$$AVDD \geq 2 \times V_{REF\_B} \quad (12)$$

$$4.75 \text{ V} \leq AVDD \leq 5.25 \text{ V} \quad (13)$$

Decouple the AVDD and DVDD pins with the GND pin using individual 10- $\mu\text{F}$  decoupling capacitors, as shown in [Figure 115](#).



**Figure 115. Power-Supply Decoupling**

## 11 Layout

### 11.1 Layout Guidelines

Figure 116 shows a board layout example for the ADS8354, ADS7854, and ADS7254 with the WQFN package. Use a ground plane underneath the device and partition the PCB into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. As shown in Figure 116, the analog input and reference signals are routed on the left side of the board and the digital connections are routed on the right side of the device.

The power sources to the device must be clean and well-bypassed. Use 10- $\mu$ F, ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low impedance paths.

The REFIO-A and REFIO-B reference inputs and outputs are bypassed with 10- $\mu$ F, X7R-grade, 0805-size, 16-V rated ceramic capacitors ( $C_{REF-x}$ ). Place the reference bypass capacitors as close as possible to the reference REFIO-x pins and connect the bypass capacitors using short, low-inductance connections. Avoid placing vias between the REFIO-x pins and the bypass capacitors. Small 0.1- $\Omega$  to 0.2- $\Omega$  resistors ( $R_{REF-x}$ ) are used in series with the reference bypass capacitors to improve stability.

The fly-wheel RC filters are placed immediately next to the input pins. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes. Figure 116 shows  $C_{IN-A}$  and  $C_{IN-B}$  filter capacitors placed across the analog input pins of the device.

### 11.2 Layout Example

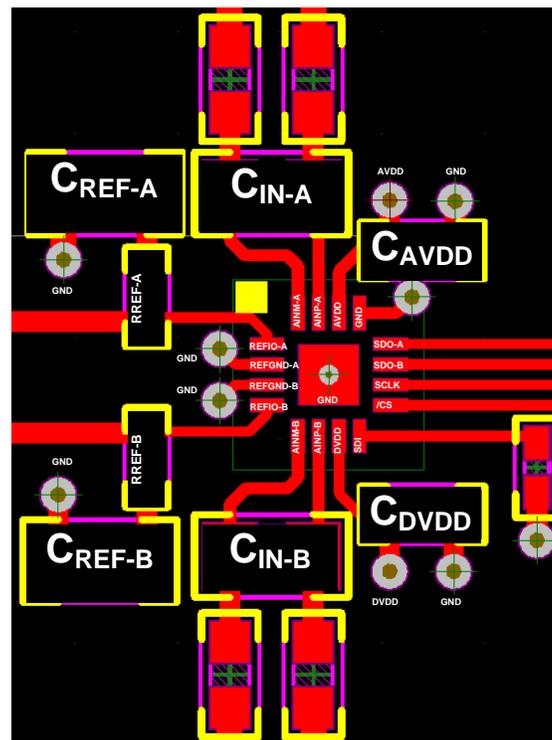


Figure 116. Recommended Layout

## 12 器件和文档支持

### 12.1 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

**Table 21. 相关链接**

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
ADS8354	<a href="#">请单击此处</a>				
ADS7854	<a href="#">请单击此处</a>				
ADS7254	<a href="#">请单击此处</a>				

### 12.2 相关文档

- TIPD117 验证设计参考指南：针对电机控制应用中光学编码器的 12 位 1MSPS 单电源双通道数据采集系统参考设计，[SLAU517](#)。
- REF5050 数据表，[SBOS410](#)。
- OPA2350 数据表，[SBOS099](#)。
- THS4521 数据表，[SBOS458](#)。

### 12.3 Trademarks

TINA is a trademark of Texas Instruments Inc..  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

## 13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7254IPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7254	<a href="#">Samples</a>
ADS7254IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7254	<a href="#">Samples</a>
ADS7254IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7254	<a href="#">Samples</a>
ADS7254IRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7254	<a href="#">Samples</a>
ADS7854IPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7854	<a href="#">Samples</a>
ADS7854IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7854	<a href="#">Samples</a>
ADS7854IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7854	<a href="#">Samples</a>
ADS7854IRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7854	<a href="#">Samples</a>
ADS8354IPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS8354	<a href="#">Samples</a>
ADS8354IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS8354	<a href="#">Samples</a>
ADS8354IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8354	<a href="#">Samples</a>
ADS8354IRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8354	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

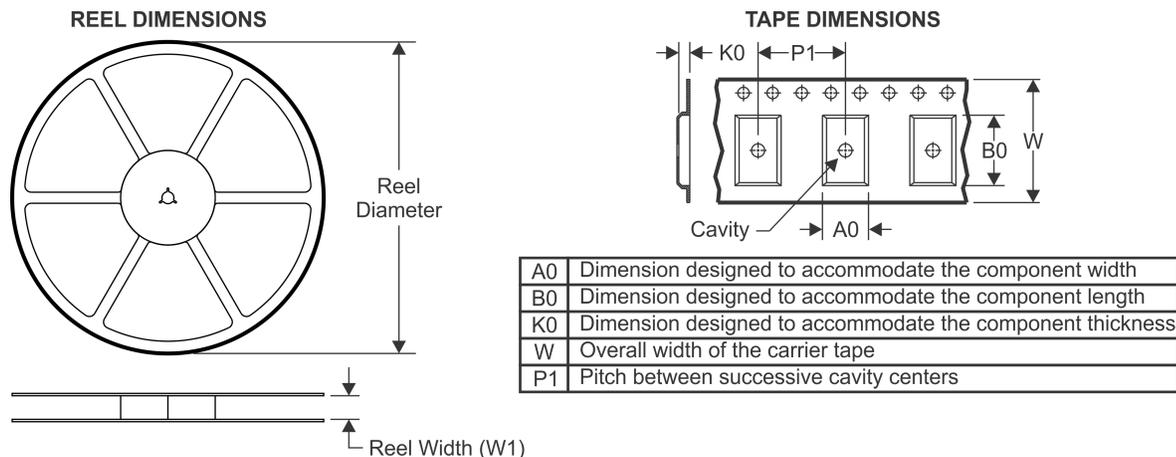
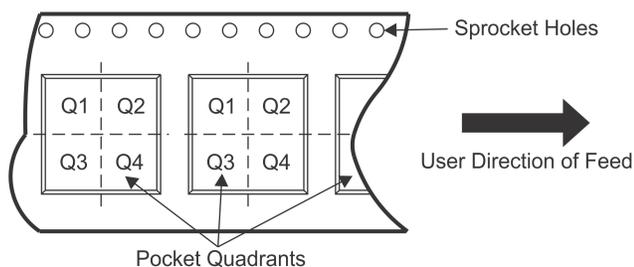
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

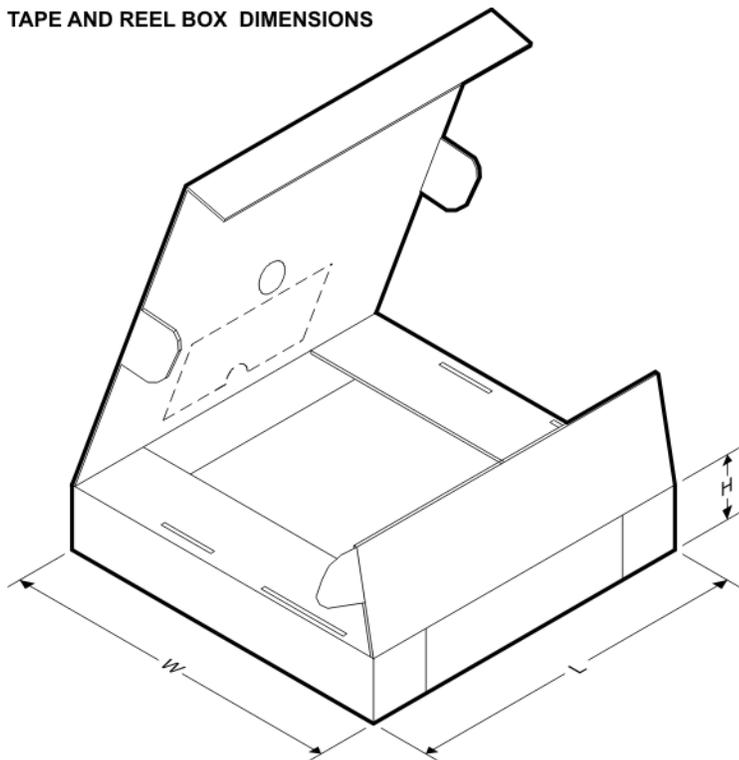
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


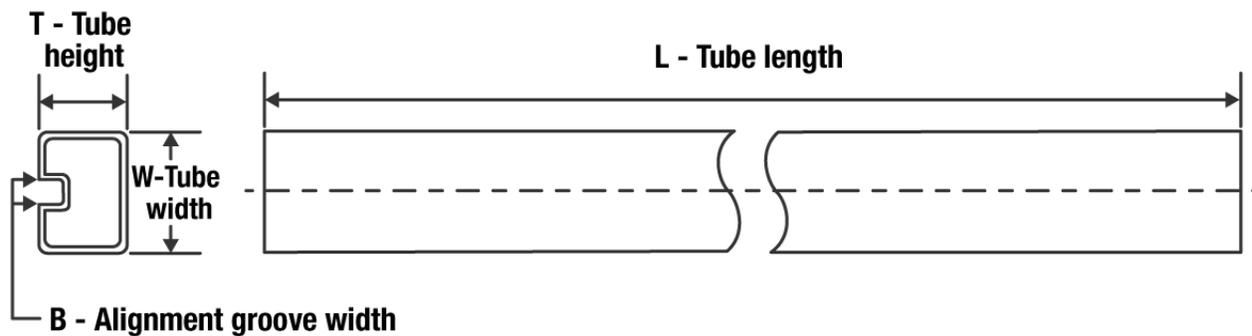
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7254IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS7254IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7254IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7854IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS7854IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7854IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8354IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS8354IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8354IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


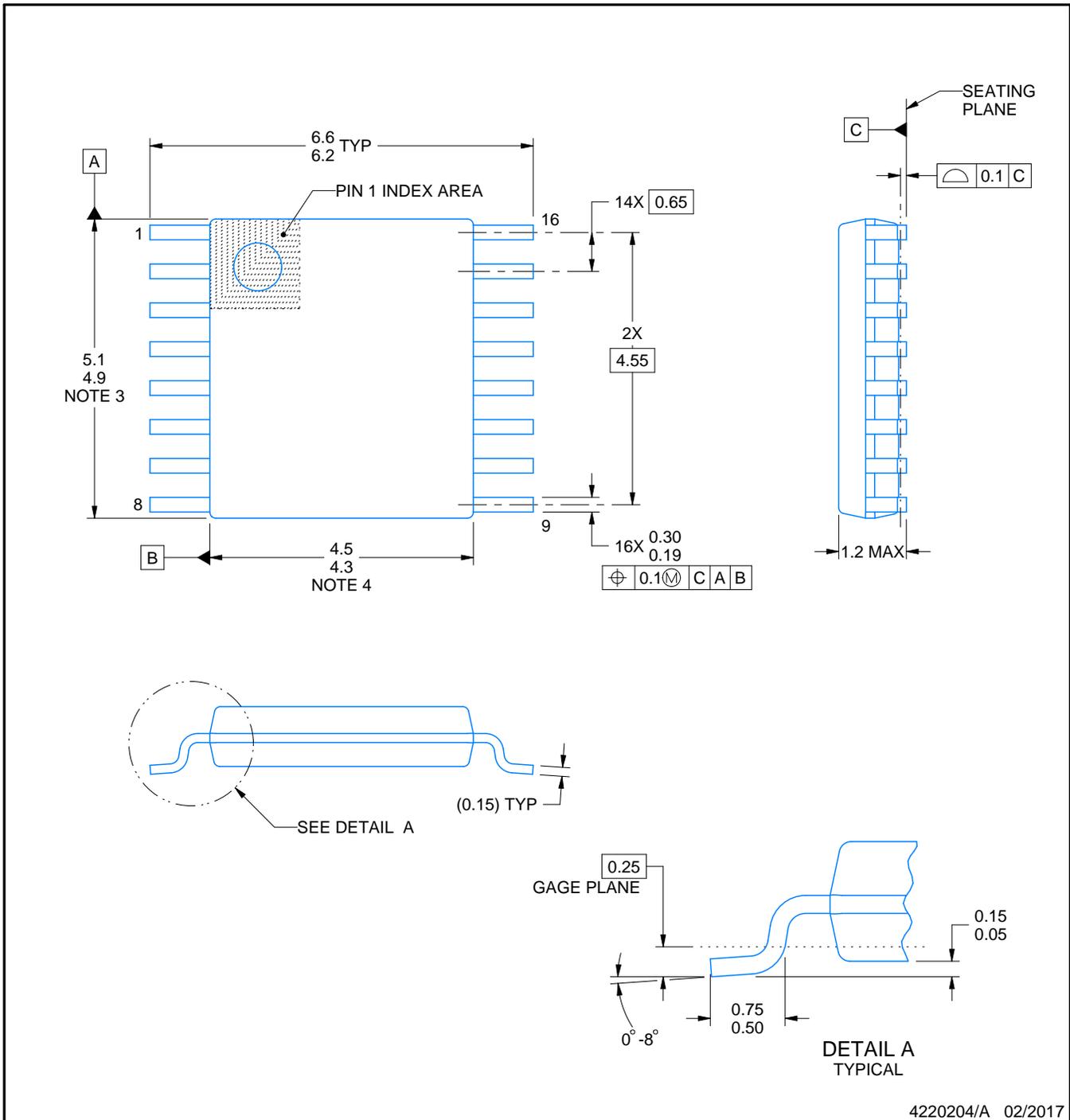
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7254IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
ADS7254IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7254IRTET	WQFN	RTE	16	250	210.0	185.0	35.0
ADS7854IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
ADS7854IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7854IRTET	WQFN	RTE	16	250	210.0	185.0	35.0
ADS8354IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
ADS8354IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS8354IRTET	WQFN	RTE	16	250	210.0	185.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
ADS7254IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
ADS7854IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
ADS8354IPW	PW	TSSOP	16	90	530	10.2	3600	3.5



4220204/A 02/2017

**NOTES:**

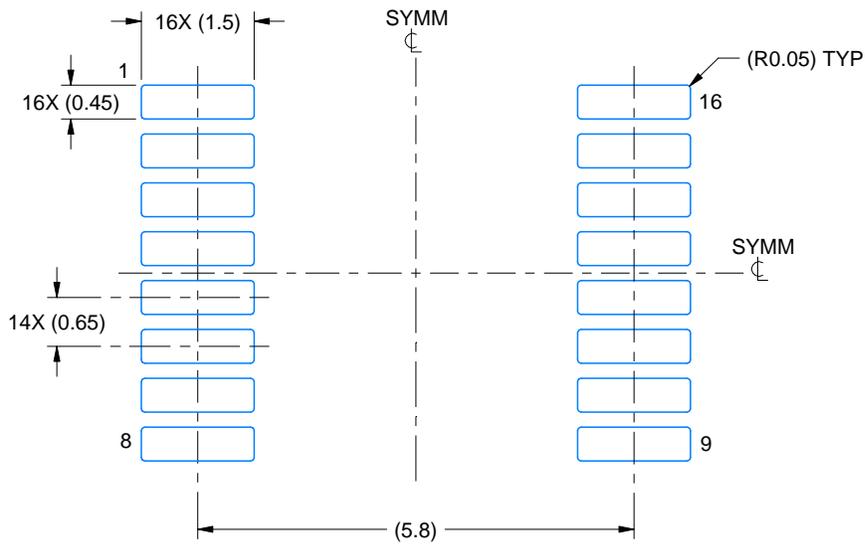
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

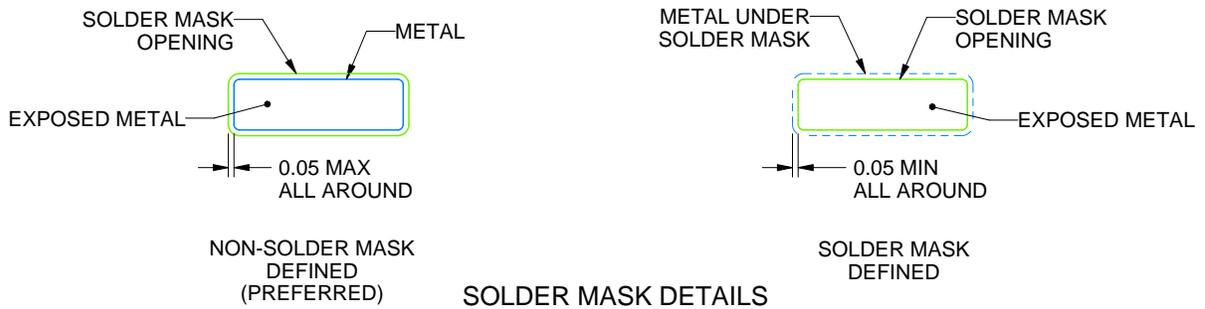
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

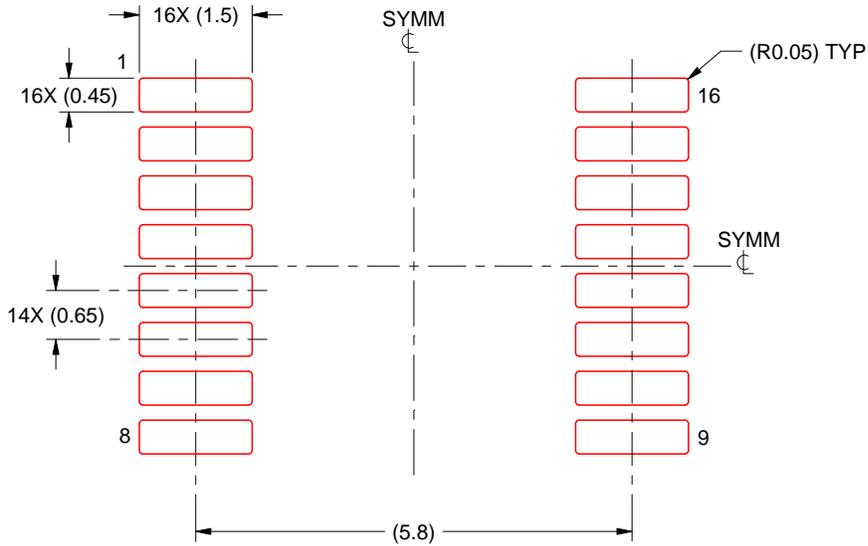
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

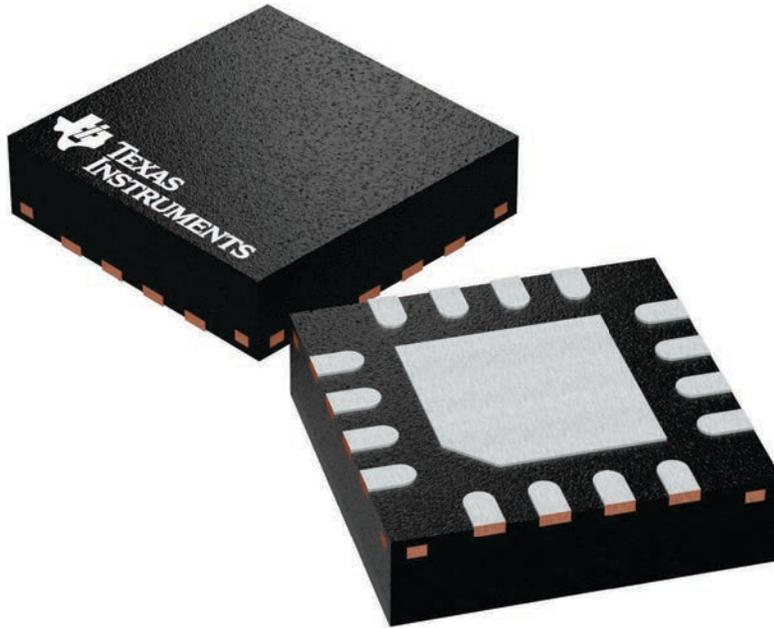
**RTE 16**

**WQFN - 0.8 mm max height**

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225944/A

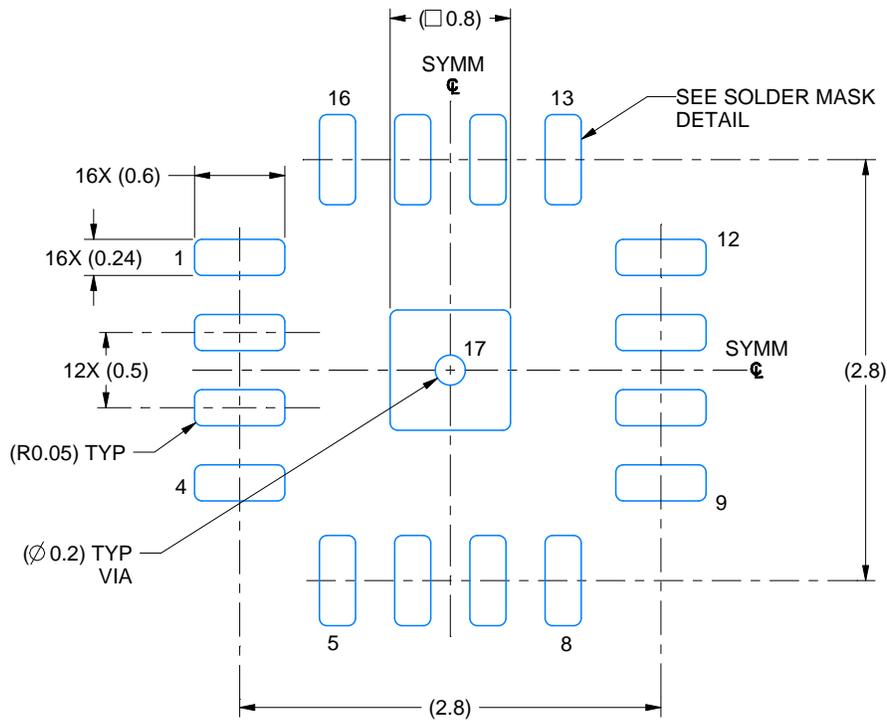


# EXAMPLE BOARD LAYOUT

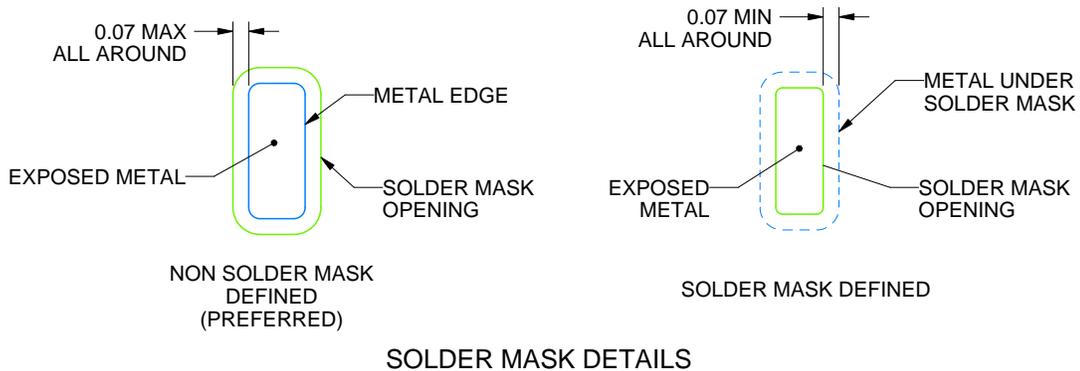
RTE0016D

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4219118/A 11/2018

NOTES: (continued)

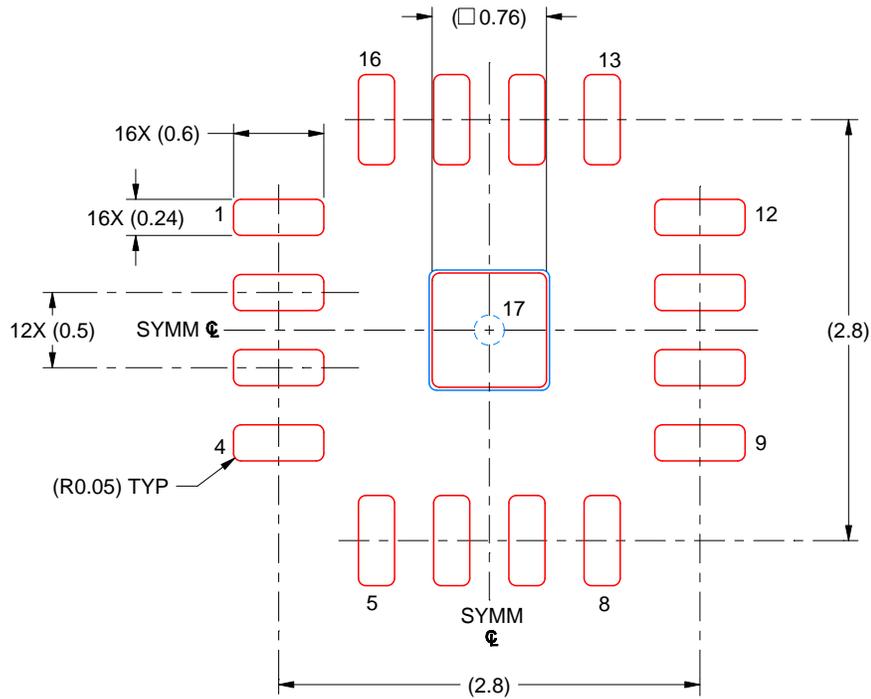
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTE0016D

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 17  
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219118/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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