2 MHz 650 mA Step Down Converter for RF Power Amplifiers in Tiny 8-pin WCSP Package

FEATURES

- **High-Efficiency Step-Down Converter**
- **Output Current up to 650 mA**
- **V_{IN} Range From 2.5 to 6.0 V**
- **2.0-MHz Fixed-Frequency Operation**
- **Clock Dithering (TPS62701)**
- **Dynamic Voltage Control With External Reference (1.3 V to 3.09 V)**
- **Fast Output-Voltage Settling (1.3 V to 3.09 V in 20 μs)**
- **Soft Start**
- **Overload Protection**
- **Undervoltage Lockout**
- **Thermal Protection**
- **8-Pin WCSP Package**

APPLICATIONS

- **Cell Phones, Smart Phones**
- **Battery-Powered RF Amplifier**

DESCRIPTION

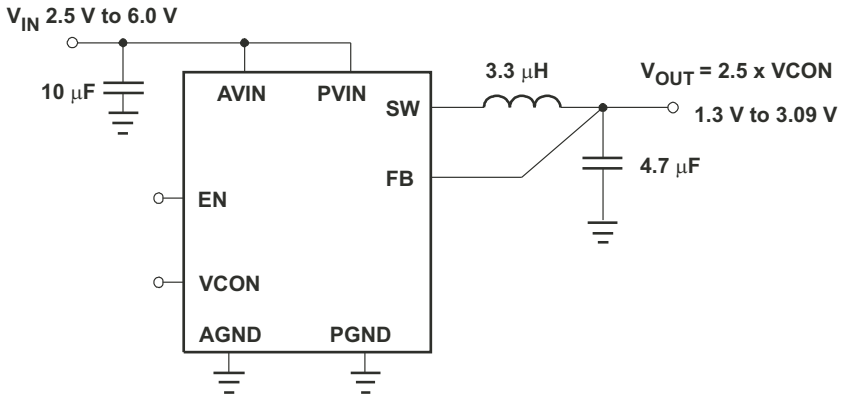
The TPS6270x device is a high-efficiency synchronous step-down DC-DC converter optimized for RF power-amplifier (PA) applications. It provides up to 650 mA of output current from a single Li-Ion cell.

The device converts input voltages from 2.5 to 6.0 V down to an output voltage set by an external analog reference voltage applied to the pin VCON. The output voltage follows the external reference by an internal gain of 2.5 within the limits of 1.3 V to 3.09 V. This scheme adjusts the output voltage of the DC/DC converter and therefore the output power of an RF-PA.

The TPS6270x operates in fixed-frequency PWM mode at a 2.0-MHz switching frequency to minimize RF interference. This converter operates with only three small external components; an input capacitor, inductor and output capacitor. The TPS62701 has in addition a built-in clock-dithering circuit to reduce RF noise.

The TPS6270x is available in a tiny 8 pin lead free WCSP package for smallest solution size.

TYPICAL APPLICATION



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

TA	PART NUMBER(1)	PACKAGE	ORDERING	PACKAGE MARKING
–30°C to 85°C	TPS62700	WCSP 8 pin	TPS62700YZF	CKL
	TPS62701		TPS62701YZF	CGJ

(1) The package is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
	Input voltage range(2)		–0.3 to 7	V
	Voltage range at EN, VCON(2)		–0.3 to V_{IN} +0.3, ≤ 7	V
	Voltage on SW(2)		–0.3 to 7	V
	Peak output current(2)		internally limited	
	ESD rating(3)	HBM Human body model	2	kV
		Machine model	200	V
T_J	Maximum operating junction temperature		–40 to 150	°C
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

DISSIPATION RATINGS(1) (2)

PACKAGE	$R_{\theta JA}$	POWER RATING FOR $T_A \le 25°C$	DERATING FACTOR ABOVE $T_A = 25°C$
YZF	110°C/W	900 mW	9 mW/°C

(1) Maximum power dissipation is a function of $T_J(max)$, θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = [T_J(max) – T_A] / \theta_{JA}$.
(2) This thermal data is measured with high-K board (4 layers board according to JESD51-7 JEDEC standard).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}, AV_{IN}, PV_{IN}	Supply voltage	2.5		6	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

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ELECTRICAL CHARACTERISTICS

PV_{IN} = AVIN = V_{IN} = 3.6 V, EN = AV_{IN}, T_A = T_J = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted), see parameter measurement information

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
AV_{IN}, PV_{IN}	Input voltage range	$I_{OUT\ max}$ = 650 mA		2.5		6	V
I_{OUT}	Output current	V_{IN} 2.5 to 6 V				650	mA
I_Q	Operating quiescent current into AVIN	VCON = 1 V, FB = 0 V, V_{IN} = 3.6V, device not switching (1)			0.1	0.3	mA
I_{SD}	Shutdown current	EN = SW=VCON = AGND, AV_{IN} = PV_{IN} = 3.6V			0.01	2	µA
ENABLE							
V_{IH}	High Level Input Voltage, EN			1.2		V_{IN}	V
V_{IL}	Low Level Input Voltage, EN			0		0.4	V
I_{IN}	Input bias Current, EN	EN = AVIN			5	10	µA
CONTROL INPUT V_{CON}							
$V_{VCON,\ MIN}$	V_{CON} Threshold forcing $V_{FB,\ MIN}$	Falling VCON signal		0.484	0.52	0.556	V
$V_{VCON,\ MAX}$	V_{CON} Threshold forcing $V_{FB,MAX}$	Rising VCON signal		1.211	1.236	1.26	V
Z_{VCON}	V_{CON} Input resistance			100			kΩ
C_{VCON}	V_{CON} Input capacitance	V_{CON} = 1 V, f = 100 kHz				20	pF
$I_{IN\ VCON}$	V_{CON} Input current					10	µA
Gain	Internal Gain V_{OUT}/V_{CON}	0.556 V ≤ V_{CON} ≤ 1.208 V			2.5		
POWER SWITCH							
$R_{DS(ON)}$	High side MOSFET on-resistance	PV_{IN} = V_{GS} = 3.6 V	T_A = T_J = 25°C	100	140	230	mΩ
			T_A = T_J = –40°C to 85°C			270	
	Low-Side MOSFET on-resistance	PV_{IN} = V_{GS} = 3.6 V	T_A = T_J = 25°C	180	200	330	mΩ
			T_A = T_J = –40°C to 85°C			430	
I_{LIMF}	Forward current limit MOSFET high side and low side	PV_{IN} = 3.6 V		935	1100	1200	mA
OSCILLATOR							
f_{SW}	Oscillator frequency	3 V < V_{IN} < 5 V		1.7	2.0	2.3	MHz
FEEDBACK/OUTPUT							
$V_{FB,\ MIN}$	Minimum feedback voltage	V_{CON} = 0.4 V (2)(3)		1.25	1.3	1.35	V
V_{FB}	Feedback voltage	V_{CON} = 1.1 V (2)(3)		2.693	2.75	2.835	V
$V_{FB,\ MAX}$	Maximum feedback voltage	V_{CON} = 1.4 V (2)(3)		3.028	3.09	3.15	V
Linearity	Linearity in V_{CON} range 0.556 V to 1.208 V	(2) (3)		–2		2	%
$T_{RESPONSE}$	V_{OUT} Rise time from 1.3 V to 3.09 V	V_{IN} = 4.2 V, C_{OUT} = 4.7 µF, L = 3.3 µH, R_{LOAD} = 5 Ω (3)(4)			20	30	µs
	V_{OUT} Fall time from 3.09 V to 1.3 V	V_{IN} = 4.2 V, C_{OUT} = 4.7 µF, L = 3.3 µH, R_{LOAD} = 10 Ω (3)(4)			20	30	
T_ON	Start-up Time	From Enable low to high transition until V_{OUT} reaches 3.09 V, C_{OUT} = 4.7 µF, L = 3.3 µH, I_{OUT} ≤ 1 mA			190	300	µs
η	Efficiency (L = 3.3µH, DCR ≤ 100mΩ)	V_{IN} = 3.6 V, V_{OUT} = 1.3 V, I_{OUT} = 150 mA (5)(3)			87		%
		V_{IN} = 3.6 V, V_{OUT} = 3.09 V, I_{OUT} = 400 mA (5)(3)			95		
V_{OUT_RIPPLE}	Ripple voltage, PWM mode	V_{IN} = 3 V to 4.5 V, V_{OUT} = 1.3 V, I_{OUT} = 10 mA to 400 mA (3)			10		mV_{p-p}
Line_tr	Line transient response	V_{IN} = 600 mV step, over V_{IN} range 3 V to 5.5 V T_{RISE} = T_{FALL} = 10 µs, V_{OUT} = 1.3 V, I_{OUT} = 100 mA (3)			50		mV_{pk}
Load_tr	Load transient response	V_{IN} = 3.1/3.6/4.5 V, V_{OUT} = 1.3 V, transients 0 mA to 100 mA, T_{RISE} = T_{FALL} = 10 µs (3)			50		mV_{pk}

(1) Device operating in 100% duty cycle mode
(2) 2.5 V ≤ V_{IN} ≤ 6 V, with V_{IN_MIN} = VOUT + 0.5 V
(3) The voltage need to be measured on the C_{OUT} using appropriate measurement probes. For the measurements, a proper PCB layout and usage of recommended inductors and capacitors are essential. See parameter measurement information.
(4) Rise/Fall time valid for V_{FB} within specified limits.
(5) Using appropriate inductor with $R_{(DCR)}$ less than 100 mΩ

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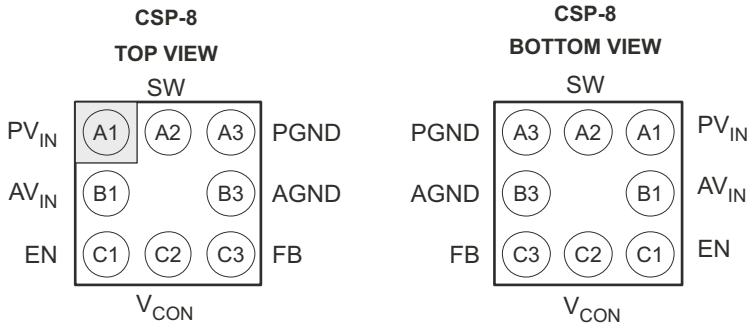
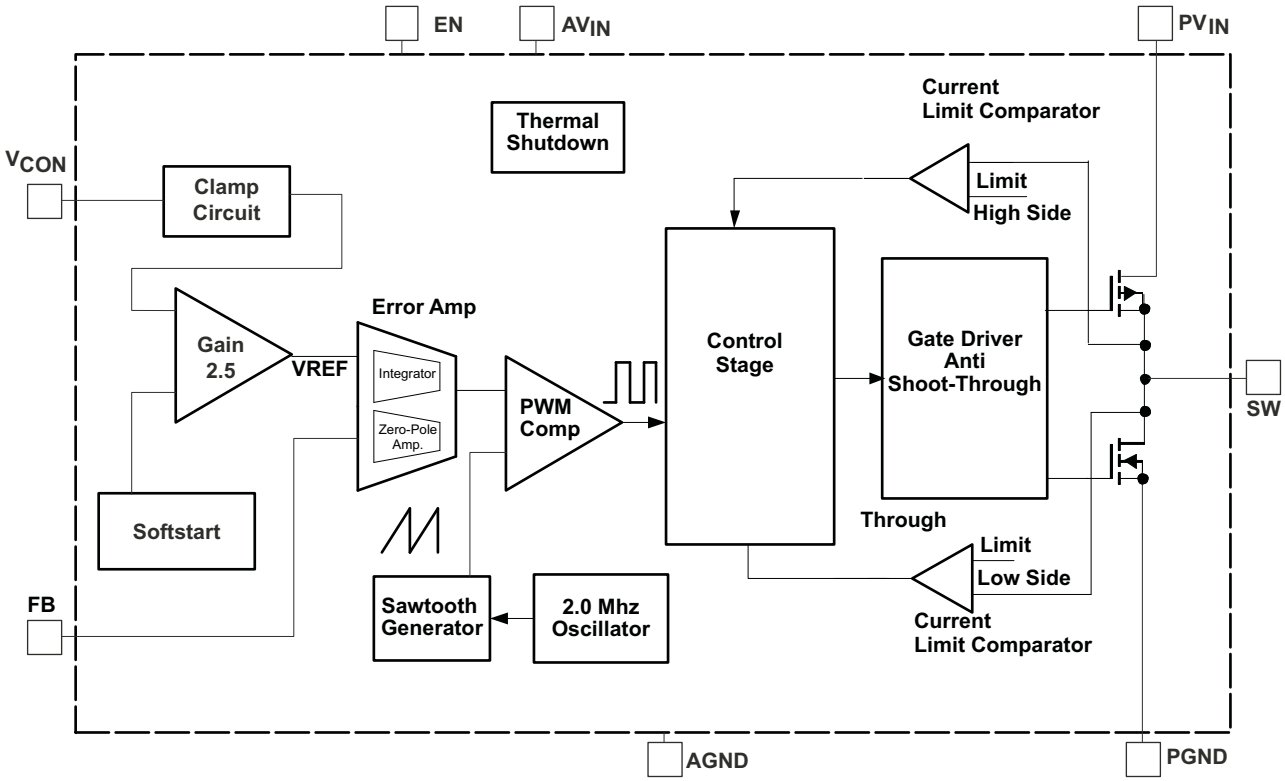
PIN ASSIGNMENTS



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO. CSP		
PV_{IN}	A1	PWR	V_{IN} power supply input for the PMOSFET
AV_{IN}	B1	PWR	V_{IN} analog supply input for the internal analog circuitry
EN	C1	I	Enable input for the device. Set high for operation, low for shutdown. This pin must be terminated.
V_{CON}	C2	I	Voltage control input. This pin controls the output voltage of the converter. The output voltage follows V_{CON} with a gain of 2.5 for 0.556 V ≤ V_{CON} ≤ 1.208 V.
FB	C3	I	Analog Feedback Input Pin for the internal regulation loop. Connect this pin directly to the output capacitor.
AGND	B3	I	Analog GND Pin for the internal analog circuitry.
PGND	A3		Power GND Pin for the NMOSFET
SW	A2		Switch Node to the internal PMOSFET and NMOSFET. Connect the external inductor between this pin and the output capacitor.

FUNCTIONAL BLOCK DIAGRAM



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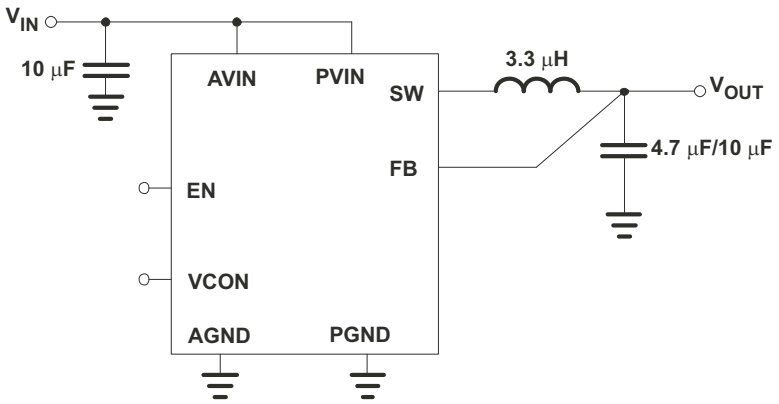
PARAMETER MEASUREMENT INFORMATION



L: LPS4018 3.3 µH, DCR 70 mΩ/VLF3014A 3.3 µH DCR 150 mΩ
C_{IN}: GRM188R60J106M 10 µF Murata 0603 size
C_{OUT}: GRM188R60J106M 10 µF Murata 0603 size
GRM188Ru60J475K 4.7 µF Murata 0603 size

DETAILED DESCRIPTION

OPERATION

The TPS6270x step down converter operates at a 2.0-MHz fixed frequency using pulse-width modulation (PWM) over the entire load range. This ensures low output-voltage ripple for RF-PA power applications.

In PWM operation, the converter uses a unique fast-response voltage-mode control scheme to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors.

At the beginning of each clock cycle initiated by the clock signal, the High-Side MOSFET switch is turned on. The current flows from the input capacitor via the High-Side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch when the current limit of the High-Side MOSFET switch is exceeded. After a short dead time to prevent shoot-through, the Low-Side MOSFET rectifier is turned on, and the inductor current ramps down. The current then flows from the inductor to the output capacitor and to the load. It turns back to the inductor through the Low-Side MOSFET rectifier.

The next cycle is initiated by the clock signal turning off the Low-Side MOSFET rectifier and turning on the High-Side MOSFET switch.

Dynamic Output Voltage Control V_{CON}

The output voltage of TPS6270x can be dynamically adjusted with an external analog voltage applied to the pin V_{CON}. This voltage is typically supplied from an external DAC to adjust the supply voltage for the RF Power amplifier, and therefore to determine the RF output power. The output voltage is set to : $V_{OUT} = 2.5 \times V_{CON}$.

The output voltage can be set in the range between $V_{FB,\ MIN}$ (1.3 V) and $V_{FB,\ MAX}$ (3.09 V). The device provides an internal voltage gain factor of 2.5. For dynamic voltage adjustment the V_{CON} voltage range is between $V_{CON,\ MIN}$ (0.52 V) and $V_{CON,\ MAX}$ (1.24 V). In Case the V_{CON} voltage is out of this range, the output voltage is internally limited to $V_{FB,\ MIN}$ (1.3 V) and $V_{FB,\ MAX}$ (3.09 V). This allows using the TPS6270x as a fixed output voltage converter where the V_{CON} Pin is connected, for example, to GND or V_{IN}.

100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty-cycle mode when the input voltage approaches the nominal output voltage. In order to maintain the output voltage, the High-Side MOSFET switch is turned on 100% for one or more cycles.

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With further decreases of V_{IN}, the High-Side MOSFET switch is turned on completely. In this case, the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the entire battery voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN\_MIN} = V_{OUT\_MIN} + I_{OUT\_MAX} \times (R_{DSON\_MAX} + R_L) \quad (1)$$

With:

I_{OUT_MAX} = maximum output current plus inductor ripple current
R_{DSON_MAX} = maximum P-channel switch R_{DSON}.
R_L = DC resistance of the inductor
V_{OUT_MAX} = nominal output voltage plus maximum output voltage tolerance

ENABLE

The device is enabled by setting the EN pin to high and at first the internal circuits are settled. Afterwards the device activates the soft start circuit and ramps up the output voltage. The output voltage is ramped up from 0 V to 3.09 V within typically 190 µs after the EN pin changes from low to high. A low signal at the EN pin sets the device in Shutdown Mode with less than 2 µA current consumption.

SHORT-CIRCUIT PROTECTION

The High-Side and Low-Side MOSFET switches are protected with maximum output current = I_{LIMF} in case a short circuit on the output occurs. When the High-Side MOSFET switch reaches its current limit, it is turned off, and the Low-Side MOSFET switch is turned on. The High-Side MOSFET switch can only turn on again, after the current in the Low-Side MOSFET switch decreases below its current limit.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the High-Side and Low-Side MOSFETs are turned-off. The device continues its operation when the junction temperature falls by typical 20°C.

UNDERVOLTAGE LOCKOUT

The device stops operation at typ. 1.5 V with falling input voltage and starts operation at typ. 1.7 V with rising input voltage. This prevents malfunction of the device due to low input voltage.

CLOCK DITHERING

In order to reduce switch frequency harmonics in the higher RF bands, the TPS62701 has a built-in clock-dithering circuit.

TYPICAL CHARACTERISTICS

Typical Characteristic Graphs

		FIGURE
Switching Frequency	vs Input Voltage (V_{IN})	Figure 1
R_{DSON}	vs V_{IN}, N-Channel	Figure 2
R_{DSON}	vs V_{IN}, P-Channel	Figure 3
Shutdown Current (I_{SD})	vs Temperature	Figure 4
Quiescent Current (I_Q) into AVIN	vs V_{IN}	Figure 5
EN High Threshold Voltage	vs V_{IN}	Figure 6
Efficiency	vs Output Current	Figure 7
Efficiency	vs Output Current	Figure 8
Efficiency	vs Output Voltage	Figure 9
Efficiency	vs Output Voltage	Figure 10

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TYPICAL CHARACTERISTICS (continued)

Typical Characteristic Graphs (continued)

		FIGURE
Output Voltage	vs Output Current (V_{OUT} = 1.3 V, T_A = 25°C)	Figure 11
Output Voltage	vs Output Current (V_{OUT} = 1.3 V, T_A = –40°C)	Figure 12
Output Voltage	vs Output Current (V_{OUT} = 1.3 V, T_A = 85°C)	Figure 13
Output Voltage	vs Output Current (V_{OUT} = 2.75 V, T_A = 25°C)	Figure 14
Output Voltage	vs Output Current (V_{OUT} = 2.75 V, T_A = –40°C)	Figure 15
Output Voltage	vs Output Current (V_{OUT} = 2.75 V, T_A = 85°C)	Figure 16
Output Voltage	vs Output Current (V_{OUT} = 3.09 V, T_A = 25°C)	Figure 17
Output Voltage	vs Output Current (V_{OUT} = 3.09 V, T_A = –40°C)	Figure 18
Output Voltage	vs. V_{CON} Voltage (V_I = 4.2 V)	Figure 19
Output Voltage	vs Output Current (V_{OUT} = 3.09 V, T_A = 85°C)	Figure 20
Output Voltage V_{OUT}	vs VCON Voltage	Figure 21
VCON Max Threshold	V_{OUT} T_A = 25°C	Figure 22
VCON Max Threshold	V_{OUT} T_A = 85°C	Figure 23
VCON Max Threshold	V_{OUT} T_A =–40°C	Figure 24
VCON Min Threshold	V_{OUT} T_A = 25°C	Figure 25
VCON Min Threshold	V_{OUT} T_A = 85°C	Figure 26
VCON Min Threshold	V_{OUT} T_A =–40°C	Figure 27
Load Transient Response V_{OUT} = 1.3 V		Figure 28
Load Transient Response V_{OUT} = 3.09 V		Figure 29
Load Transient Response V_{OUT} = 3.09 V		Figure 30
Load Transient Response V_{OUT} = 3.09 V		Figure 31
PWM Mode Operation V_{OUT} = 1.3 V		Figure 32
PWM Mode Operation V_{OUT} = 3.09 V		Figure 33
Output Voltage Ripple At High Duty Cycle Operation		Figure 34
VCON Voltage Response		Figure 35
VCON Output Voltage Response And Synchronous Applied Load Transient		Figure 36
Startup V_{OUT} 1.3 V		Figure 37
Startup V_{OUT} 3.09 V		Figure 38
Line Transient Response		Figure 39

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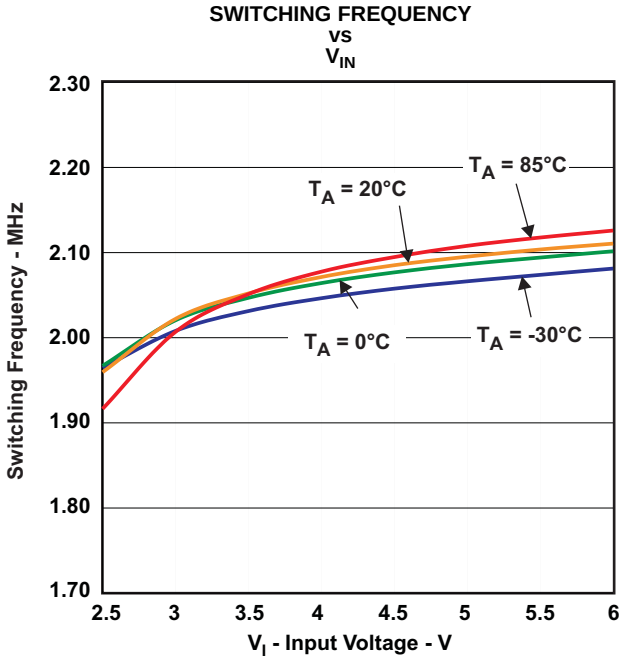


Figure 1.

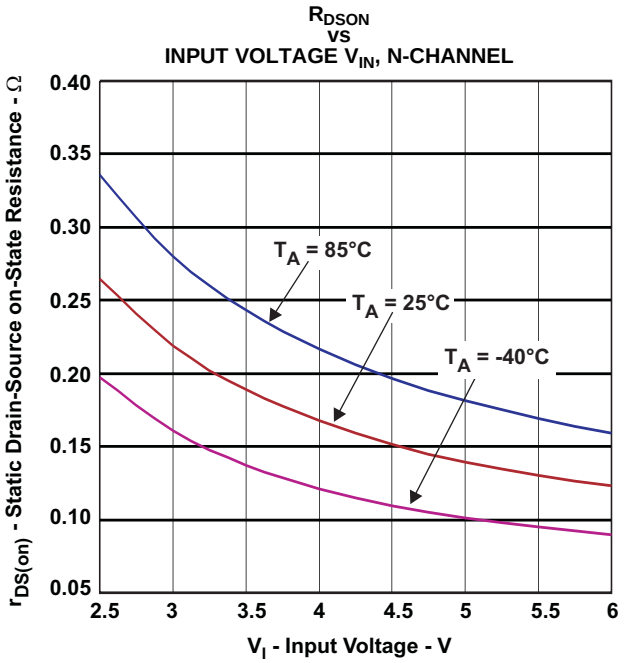
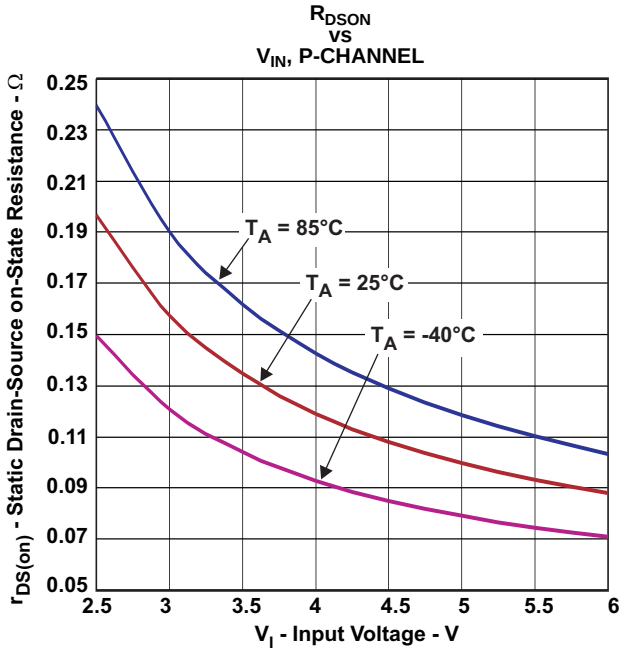


Figure 2.



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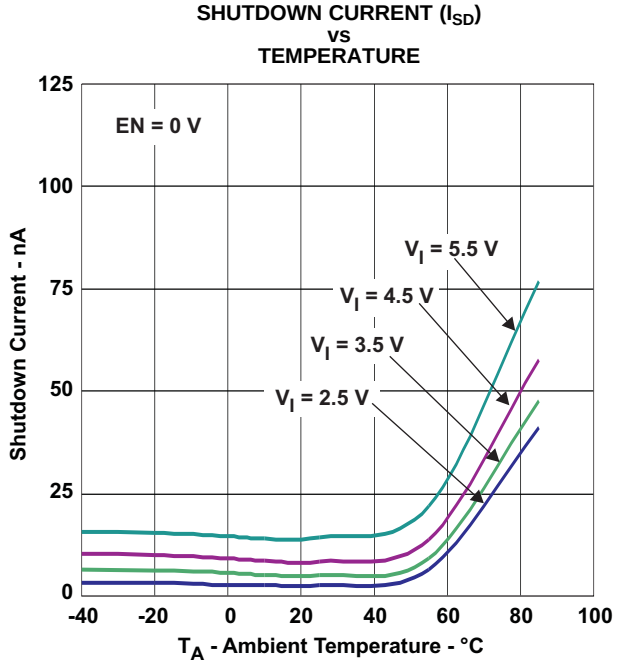

Figure 4.

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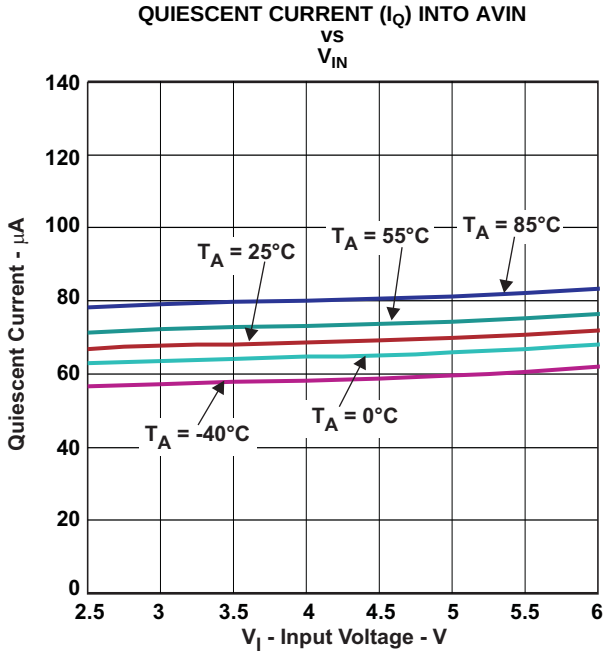

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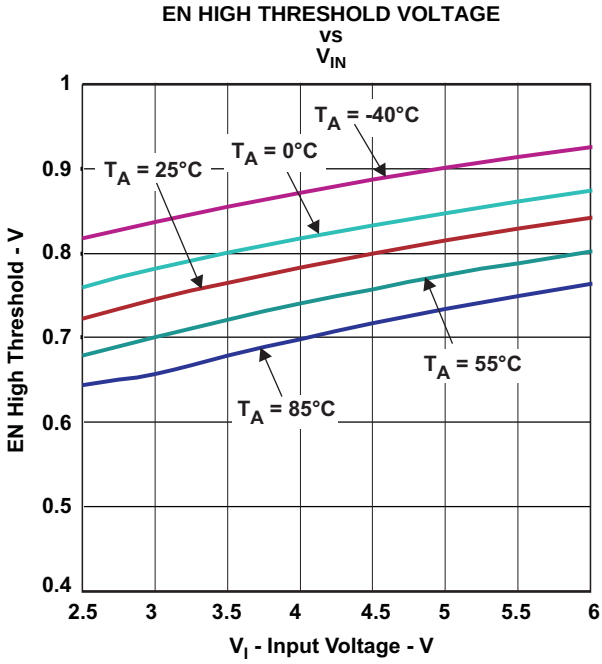

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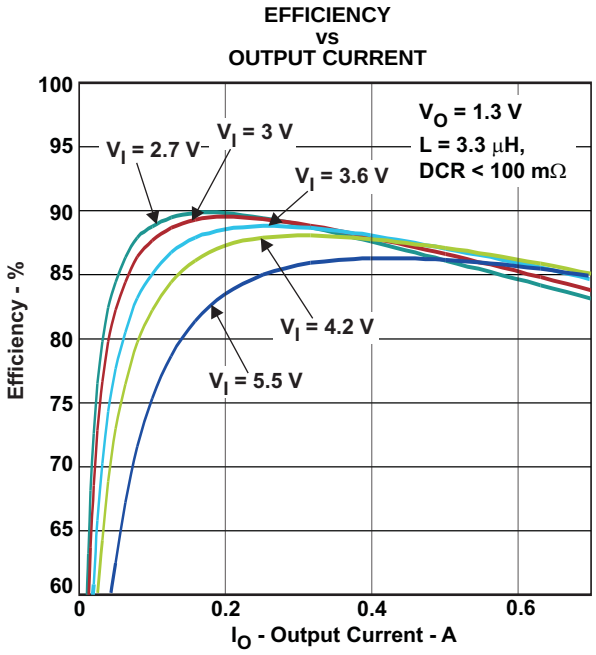

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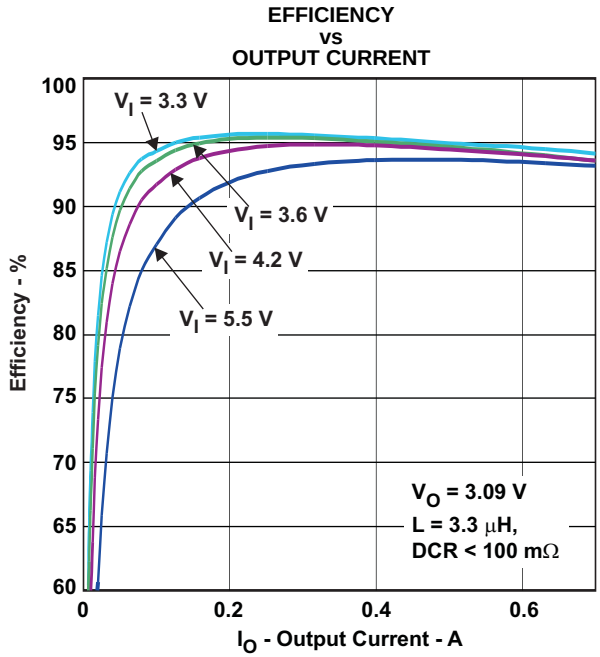

Figure 8.

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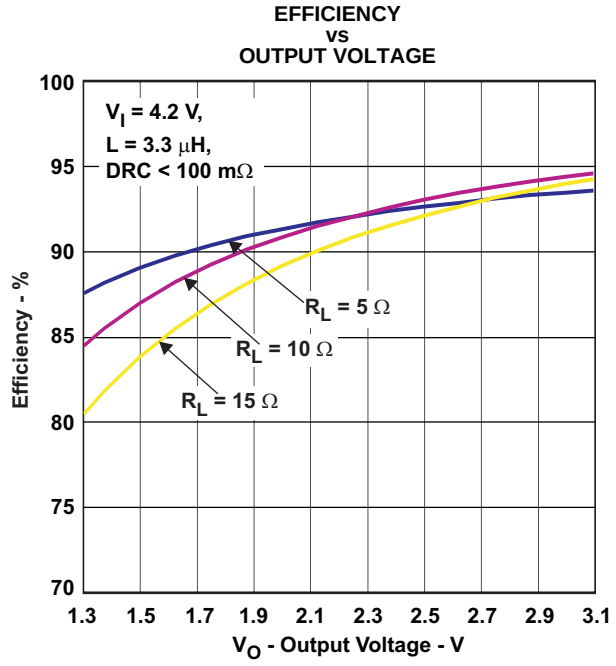

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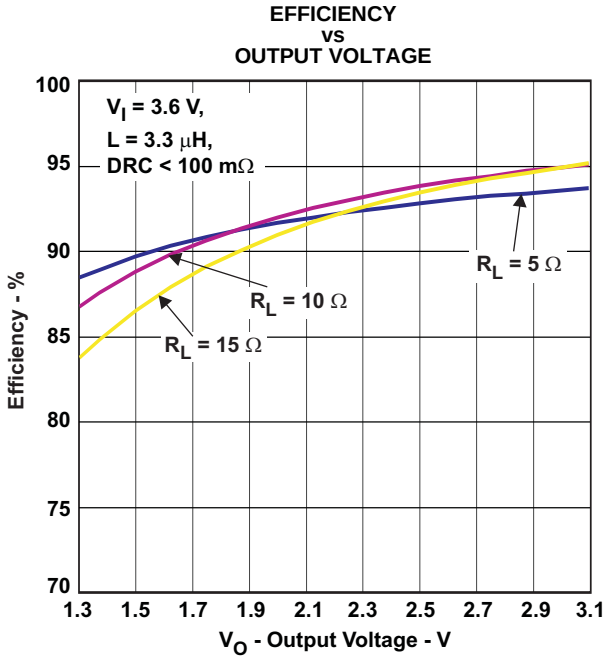

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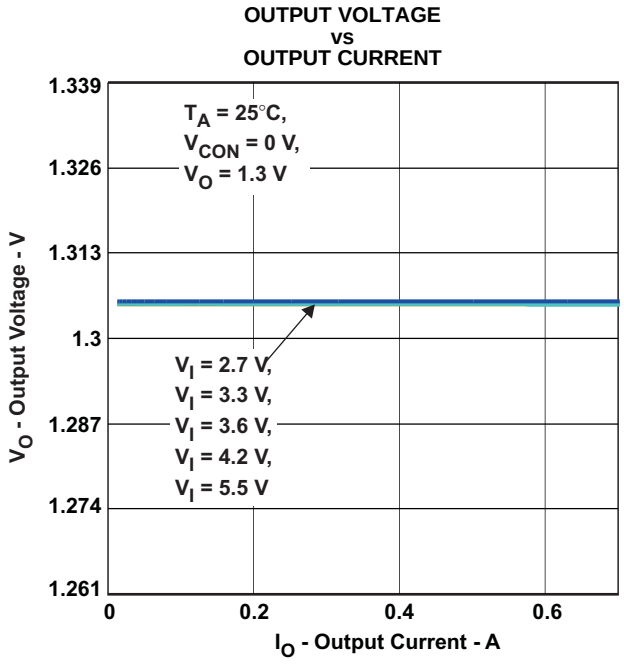

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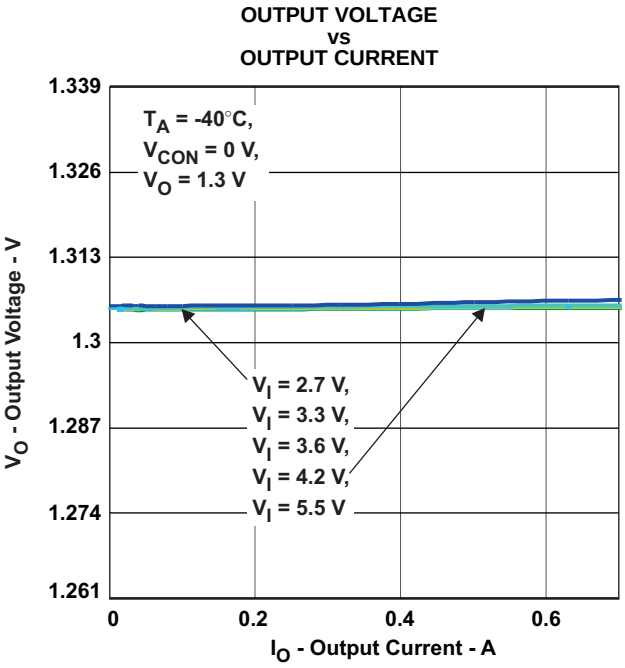

Figure 12.

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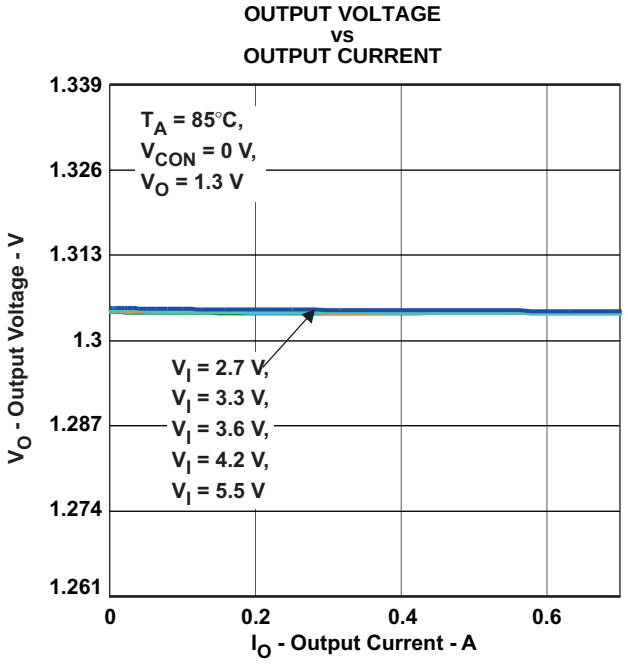

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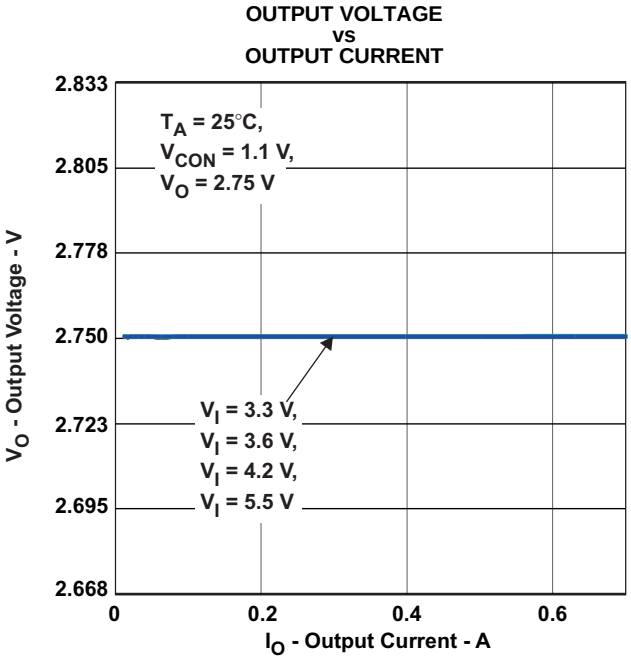

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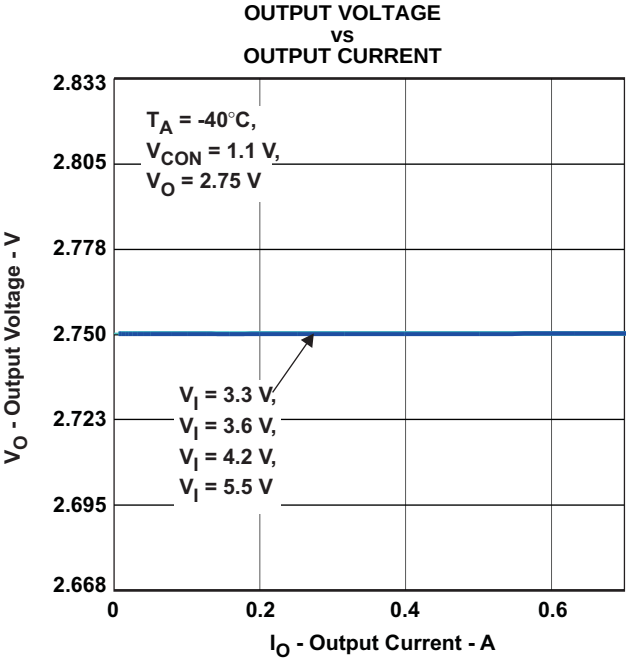
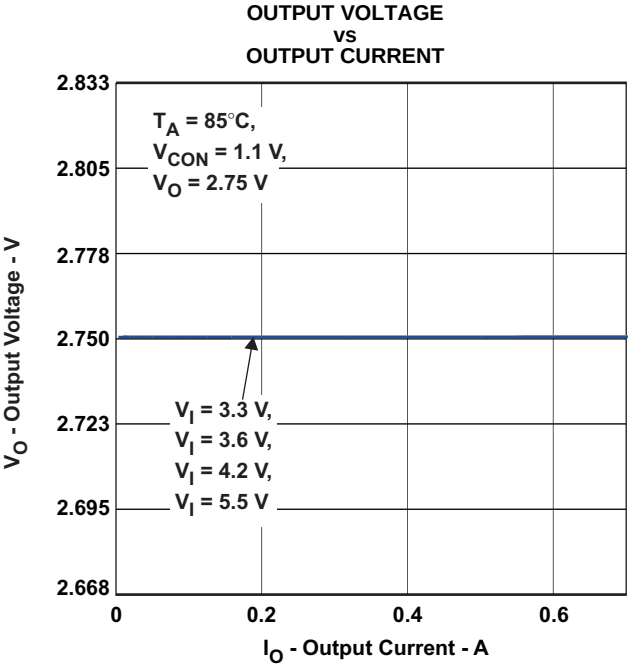


Figure 15.



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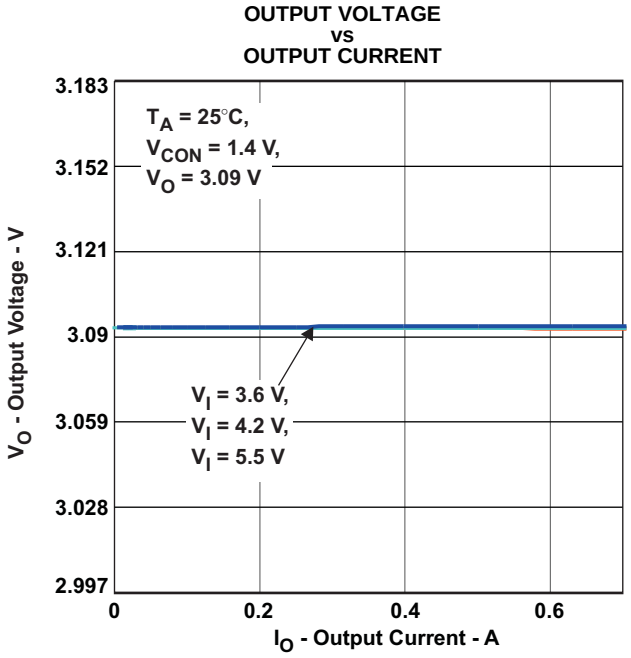

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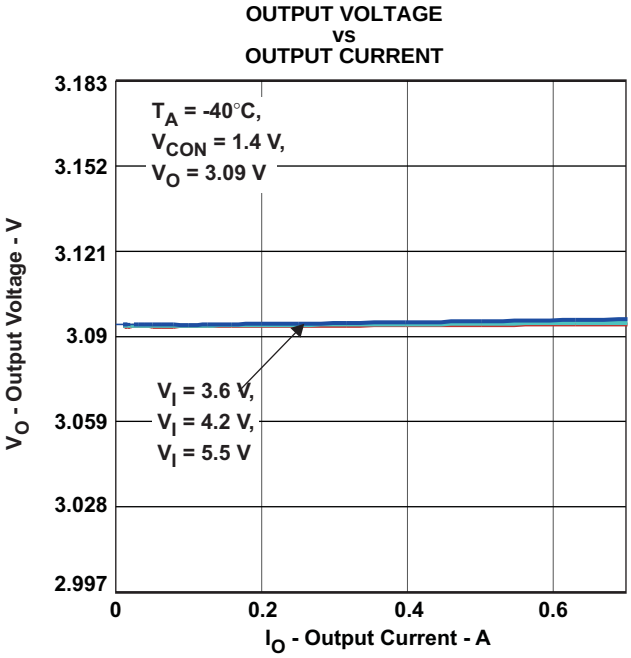

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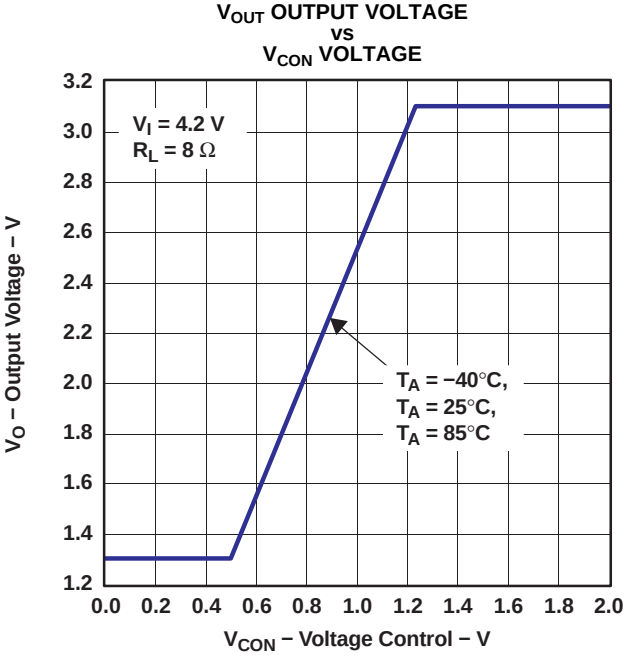

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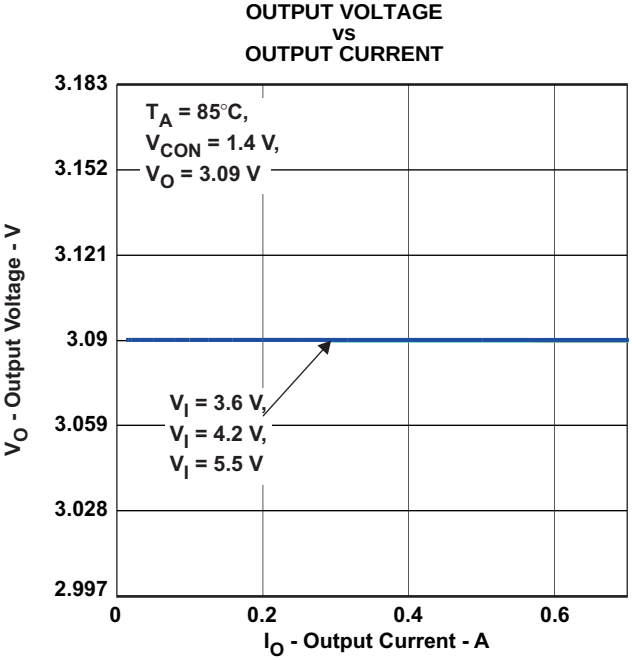

Figure 20.

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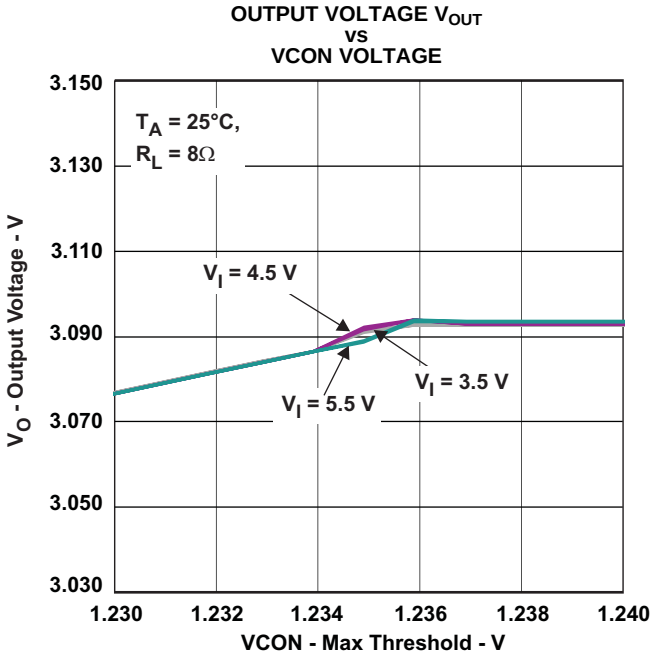

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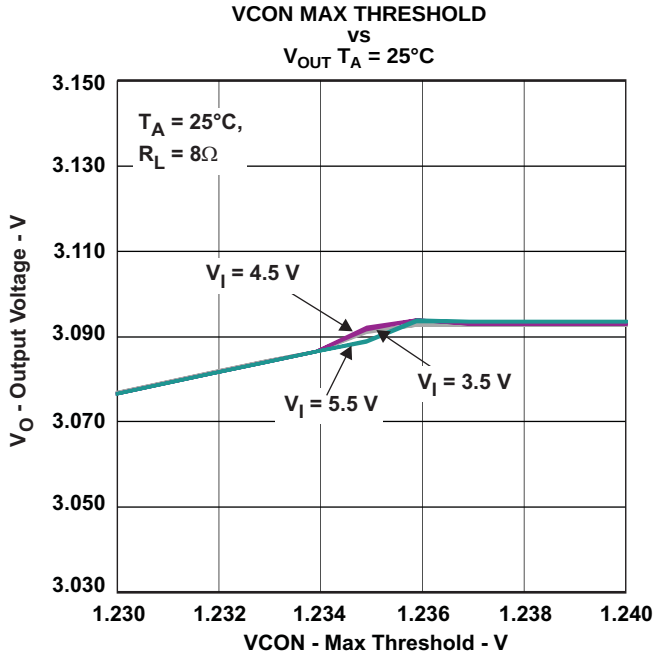

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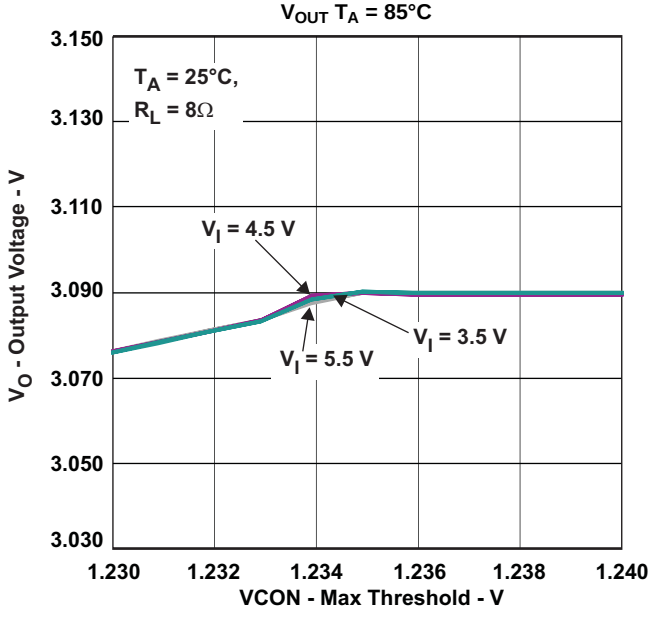

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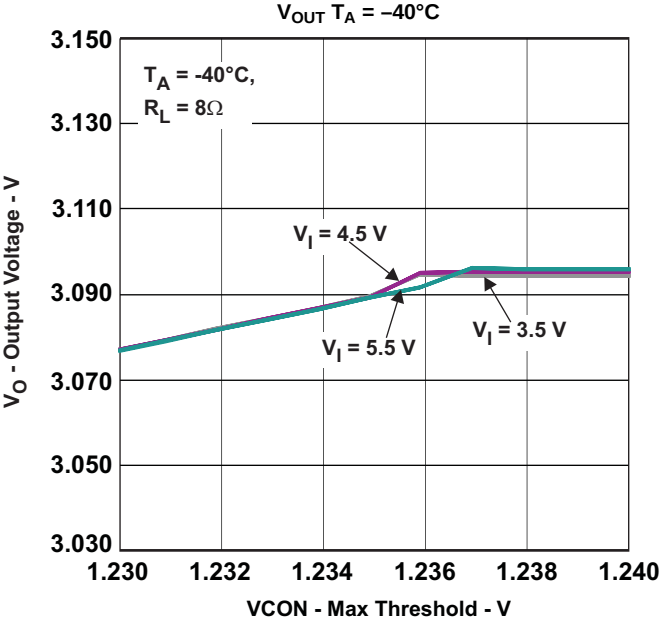

Figure 24.

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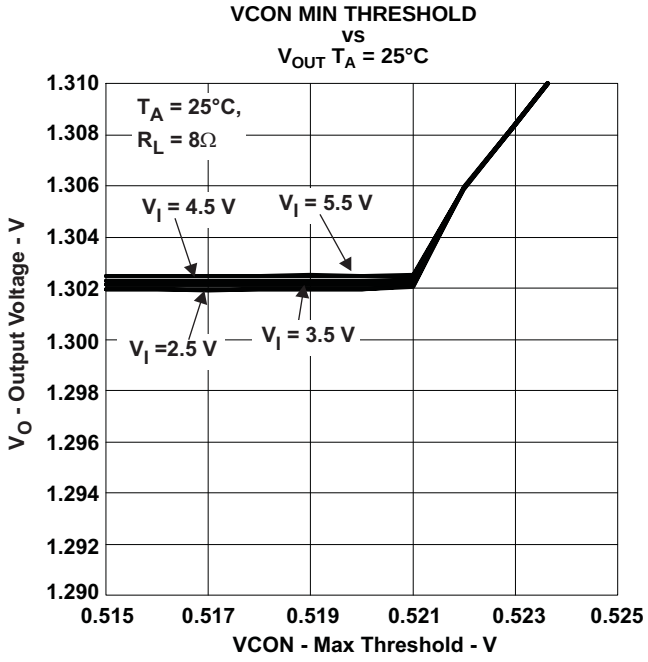

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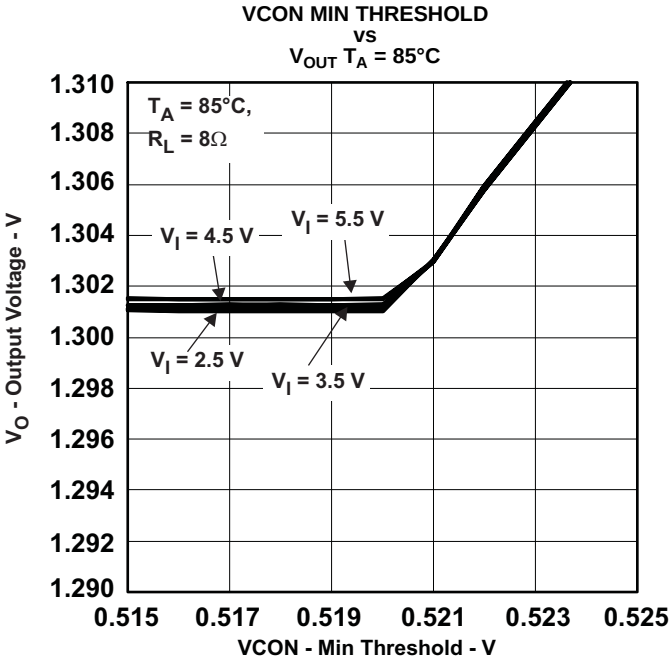

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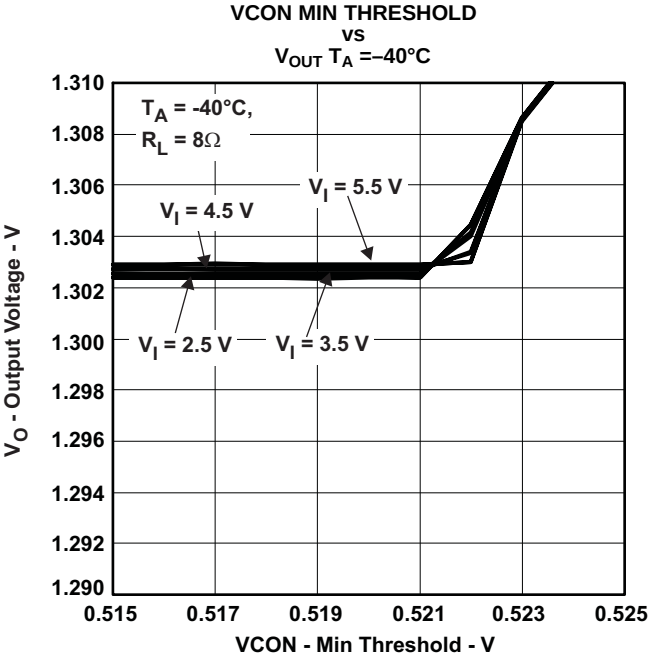

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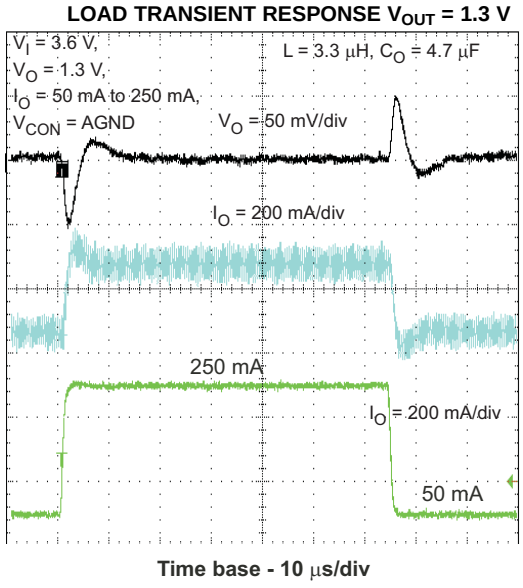

Figure 28.

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LOAD TRANSIENT RESPONSE V_{OUT} = 3.09

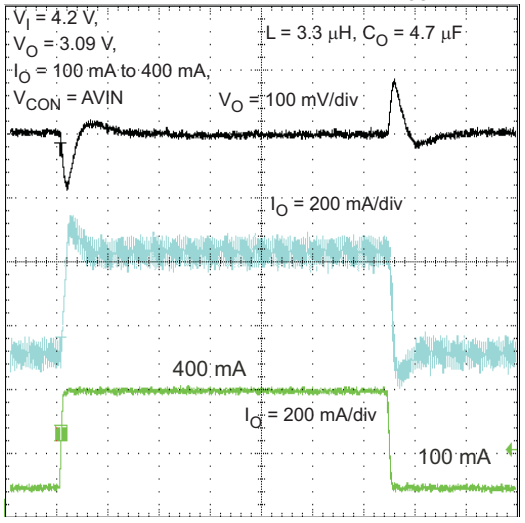

Figure 29.

LOAD TRANSIENT RESPONSE V_{OUT} = 3.09 V

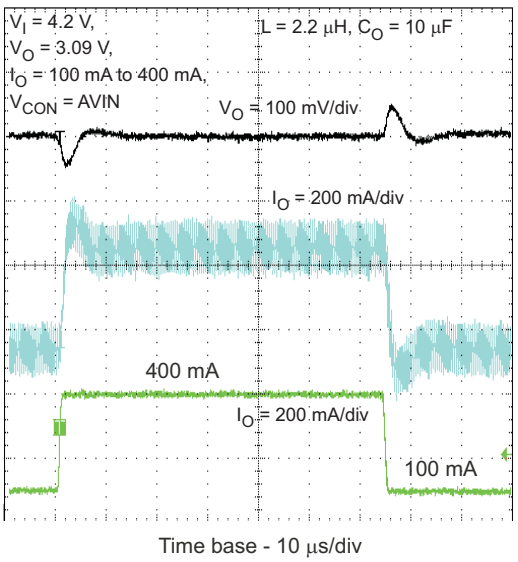

Figure 30.

LOAD TRANSIENT RESPONSE V_{OUT} = 3.09 V

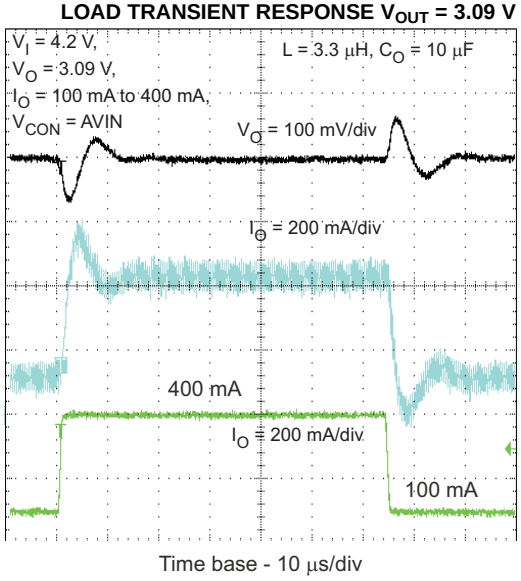

Figure 31.

PWM MODE OPERATION V_{OUT} = 1.3 V

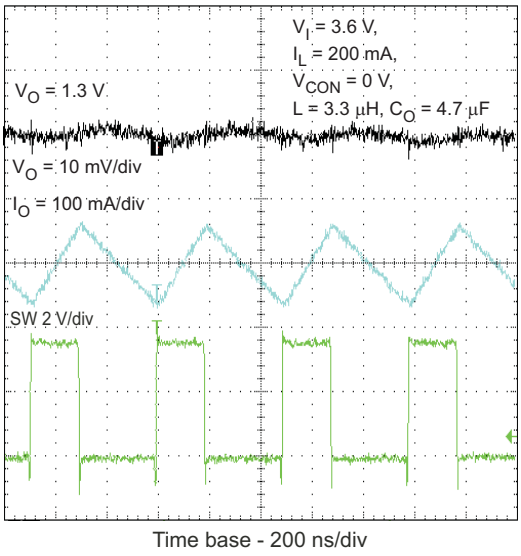

Figure 32.

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PWM MODE OPERATION V_{OUT} = 3.09 V

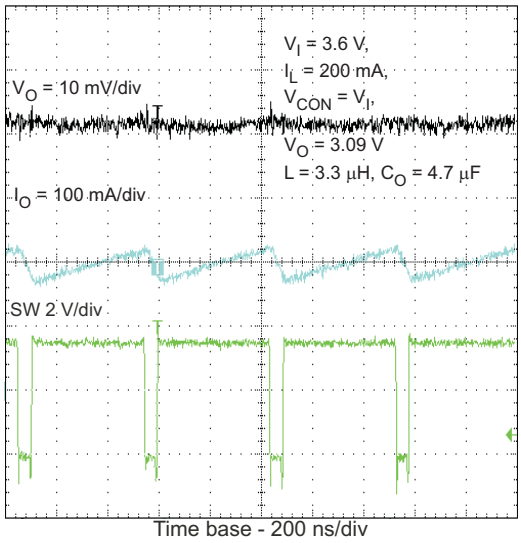

Figure 33.

OUTPUT VOLTAGE RIPPLE AT HIGH DUTY CYCLE OPERATION

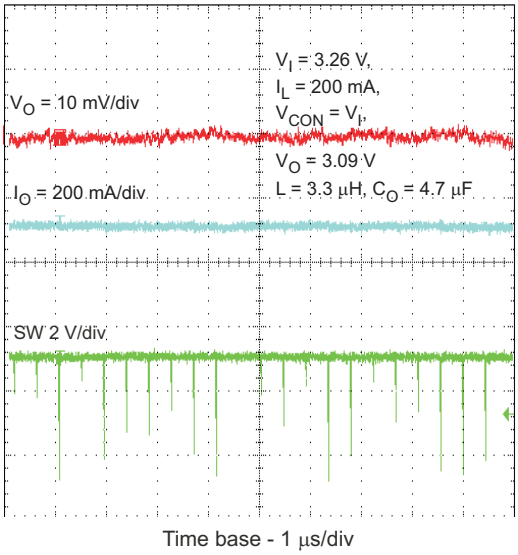

Figure 34.

VCON VOLTAGE RESPONSE

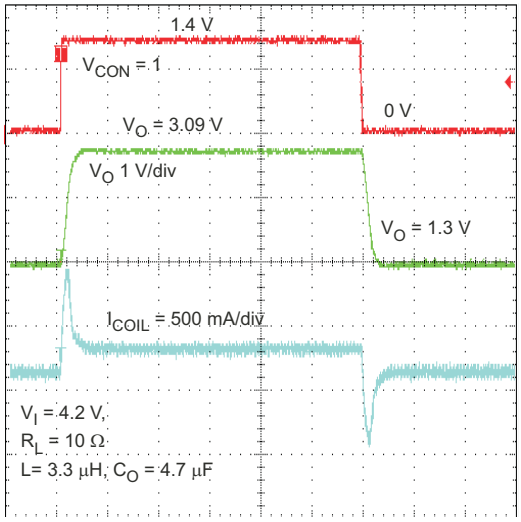

Figure 35.

VCON OUTPUT VOLTAGE RESPONSE AND SYNCHRONOUS APPLIED LOAD TRANSIENT

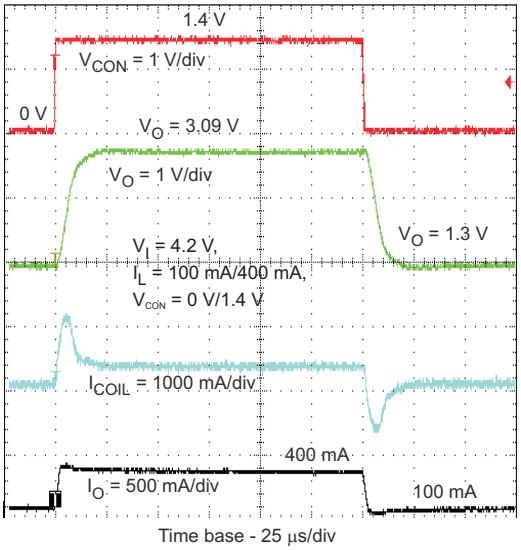

Figure 36.

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STARTUP V_{OUT} 1.3 V

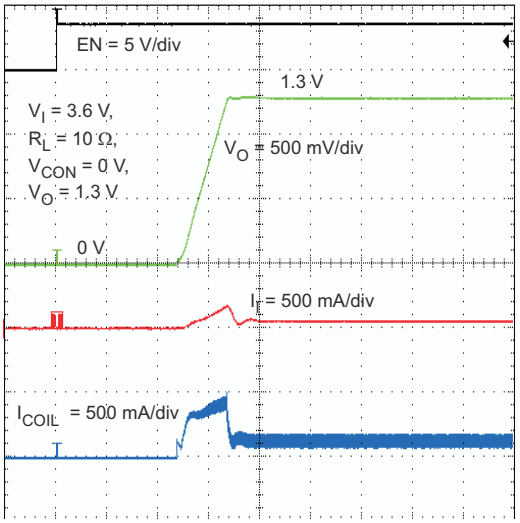

Figure 37.

STARTUP V_{OUT} 3.09 V

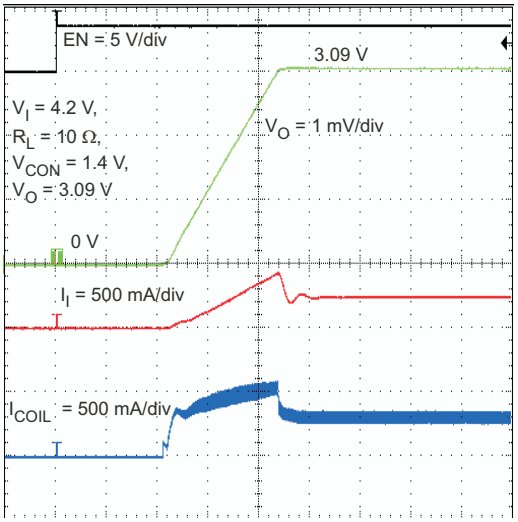

Figure 38.

LINE TRANSIENT RESPONSE

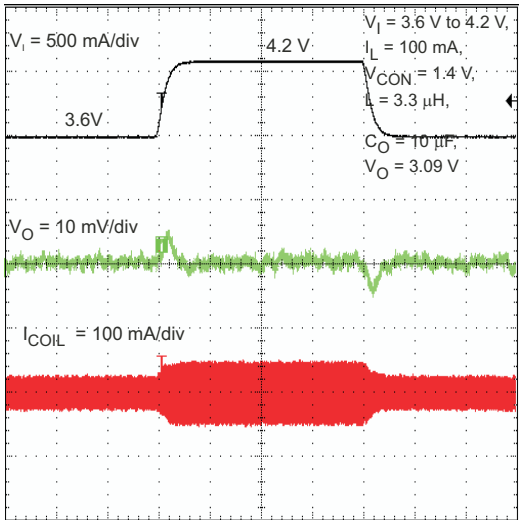

Figure 39.

APPLICATION INFORMATION

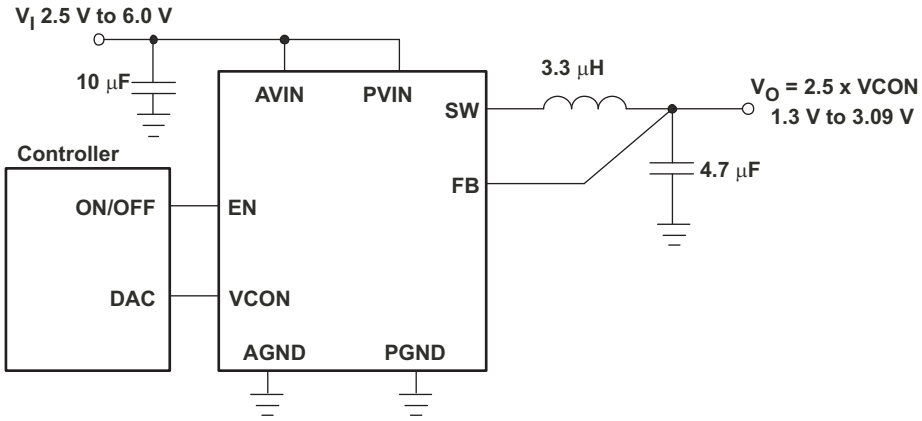

Figure 40. TPS62700 Application Circuit

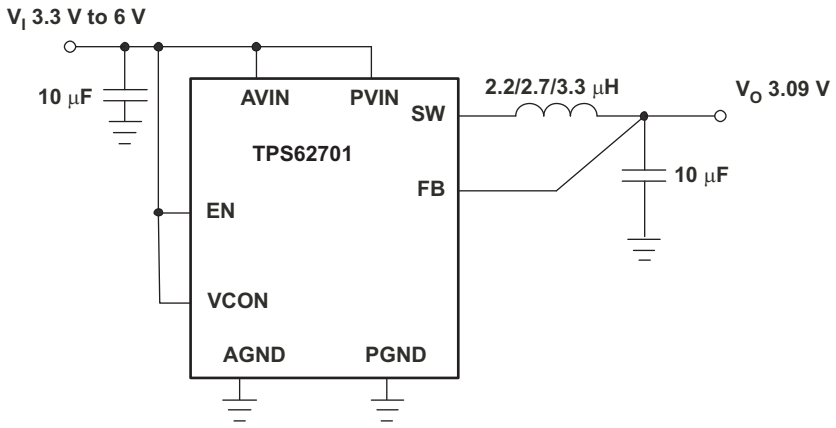

Figure 41. TPS62701 With Fixed V_{OUT} 3.09 V

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OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must have adequate ratings for dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

Equation 2 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum peak inductor current as calculated with Equation 3. This is recommended because during heavy load transients, the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{I \times f} \quad (2)$$

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{\Delta I_L}{2} \quad (3)$$

Where

f = Switching Frequency (2.0 MHz typical)
L = Inductor Value
ΔI_L = Peak to Peak inductor ripple current
I_{L_MAX} = Maximum Inductor current

A good approach is to select the inductor current and inductance rating for the maximum switch current limit of the TPS6270x.

Accepting larger values of ripple current allows the use of lower inductance values, but results in higher output-voltage ripple, greater core losses, and lower output-current capability.

The total losses of the inductor have a strong impact on the efficiency of the DC/DC conversion and consist of both the losses in the dc resistance (R_L) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic-field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 1. List Of Inductors

DIMENSIONS (mm)	INDUCTOR Series	SUPPLIER
2,5 × 2,0 × 1,2	KSLI-252012AG	Hitachi Metals
2,5 × 2,0 × 1,2	MIPSA2520	FDK
2,5 x 2,0 x 1,2	LQM2HPN	Murata
2,8 × 2,6 × 1,4	VLF3014AT	TDK
3,9 × 3,9 × 1,7	LPS4018	Coilcraft

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Output Capacitor Selection

The advanced, fast-response, voltage-mode control scheme of the TPS6270x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output-voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode, and the RMS ripple current is calculated as:

$$I_{RMSCout} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (4)$$

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{out} \times f} + ESR \right) \quad (5)$$

Input Capacitor Selection

Because of the nature of the buck converter due to its pulsating input current, a low-ESR input capacitor is required for best input-voltage filtering, and to minimize interference with other circuits caused by high input-voltage spikes. For most applications, a 10-µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input-voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

List Of Capacitors

Size	Capacitance µF	TYPE	SUPPLIER
0603	4.7	GRM188R60J475K	Murata
0603	10	GRM188R60J106M	Murata

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LAYOUT CONSIDERATIONS

As for all switching power supplies, the PCB layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to achieve the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues, as well as EMI problems. It is critical to provide a low-inductance, low-impedance ground path. Therefore, use wide, short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins PVIN and PGND. The inductor and output capacitor should be placed close to SW and PGND.

The FB line should be connected directly to the output capacitor and routed away from noisy components and traces (e.g., SW line).

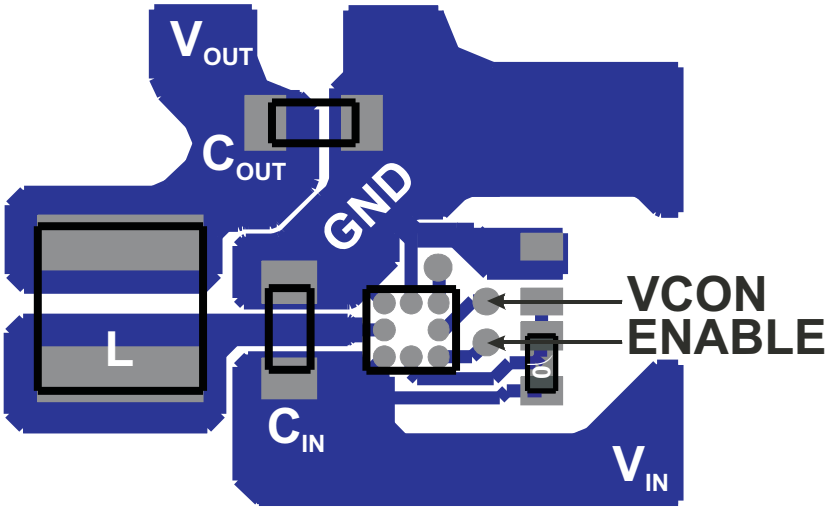
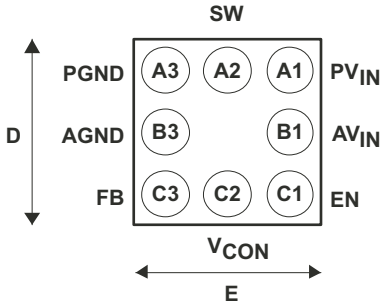


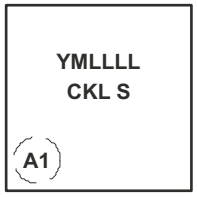
Figure 42. Suggested Board Layout

PACKAGE SUMMARY

CHIP SCALE PACKAGE
(BOTTOM VIEW)



CHIP SCALE PACKAGE
(TOP VIEW)



Code:
- YM: 2 digit year/month date code
- LLLL: lot trace code
- S: assembly site code
- CKL: TPS62700 device code

PACKAGE DIMENSIONS

Dimension D	Dimension E2
1,64 mm ± 0,03mm	1,5 mm ± 0,03

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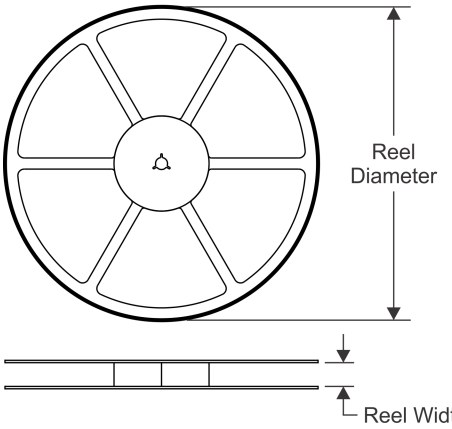
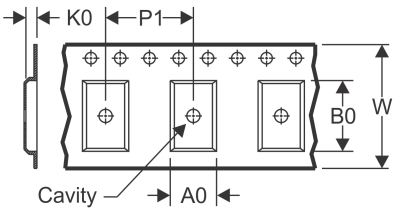
TAPE AND REEL INFORMATION

REEL DIMENSIONS

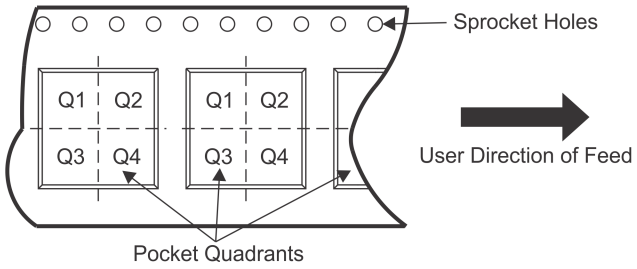


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

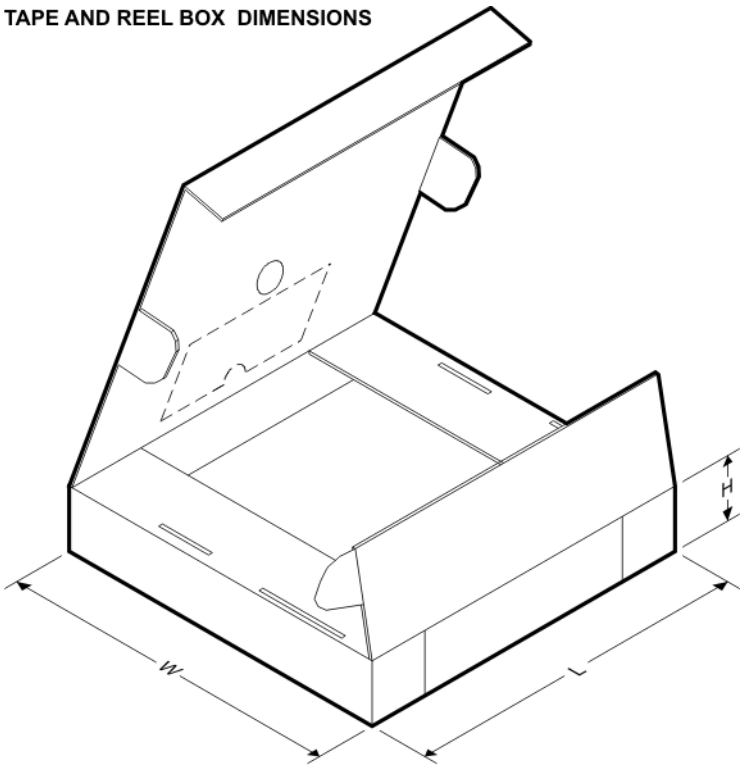
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62700YZFR	DSBGA	YZF	8	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1
TPS62701YZFR	DSBGA	YZF	8	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1

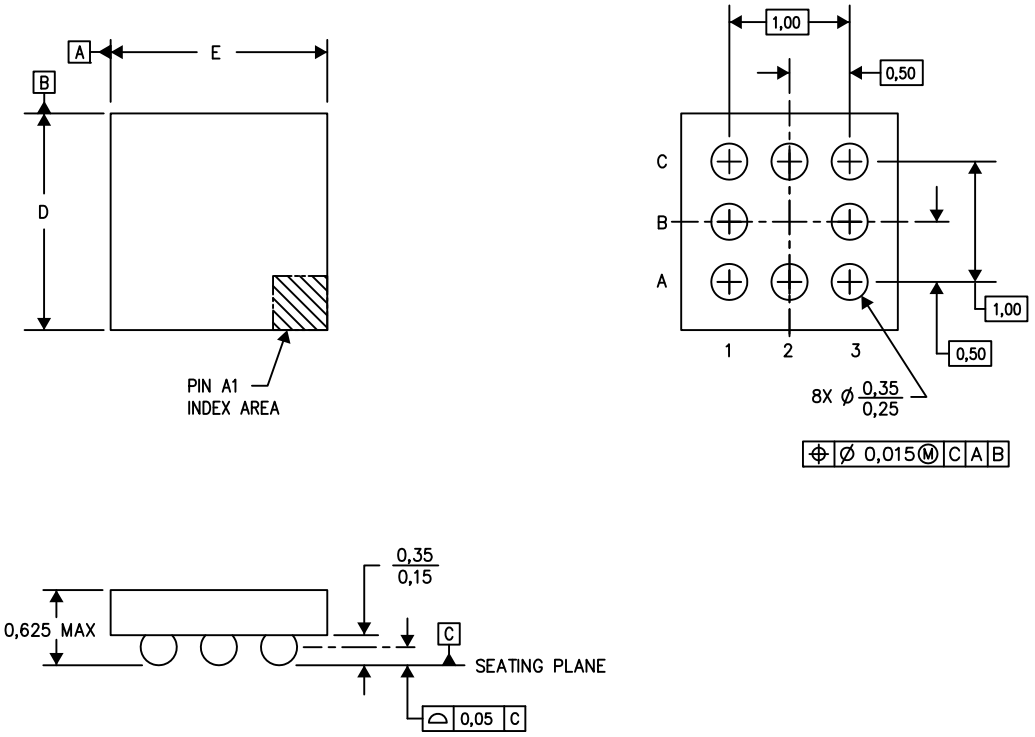
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62700YZFR	DSBGA	YZF	8	3000	182.0	182.0	20.0
TPS62701YZFR	DSBGA	YZF	8	3000	182.0	182.0	20.0

YZF (S–XBGA–N8) DIE–SIZE BALL GRID ARRAY



4205058–3/P 07/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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