# 具有施密特触发输入、三态输出和直通引脚排列的 SN74HCS541 八路缓冲器和线路驱动器

## 1 特性

- 采用可湿侧面 QFN (WBQB) 封装
- 宽工作电压范围：2V 至 6V
- 施密特触发输入可实现慢速或高噪声输入信号
- 低功耗
  - $I_{CC}$ 典型值为 100nA
  - 输入泄漏电流典型值为 ±100nA
- 电压为 6V 时，输出驱动为 ±7.8mA
- 工作环境温度范围：–40°C 至 +125°C，$T_A$

## 2 应用

- 启用或禁用数字信号
- 消除慢速或高噪声输入信号
- 在控制器复位期间保持信号
- 对开关进行去抖

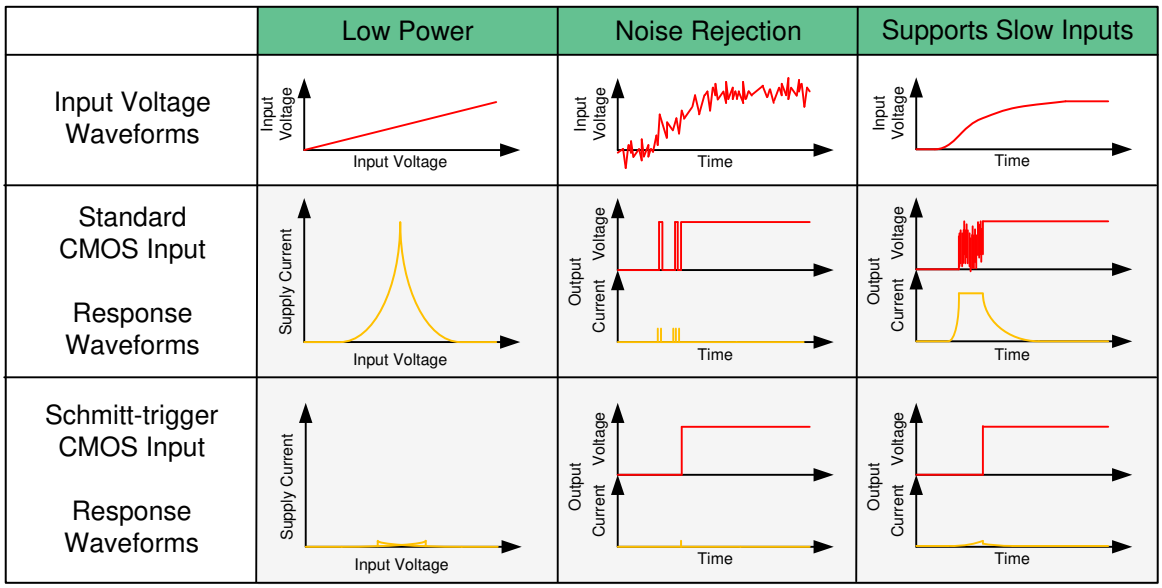
## 3 说明

SN74HCS541 包含三态输出和施密特触发输入的八路缓冲器。低电平有效输出能够使引脚（$\overline{OE1}$、$\overline{OE2}$）控制所有八个通道，并配置为必须为低电平以使输出有效。

器件信息

| 器件型号 | 封装(1) | 封装尺寸（标称值） |
|---|---|---|
| SN74HCS541RKS | VQFN (20) | 4.50mm x 2.50mm |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。




施密特触发输入的优势

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| DATE | REVISION | NOTES |
|---|---|---|
| October 2021 | * | Initial Release |


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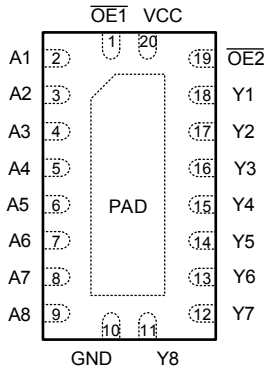
## 5 Pin Configuration and Functions




**RKS Package**
**20-Pin VQFN**
**Top View**

### Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $\overline{OE1}$ | 1 | Input | Output enable input 1, active low |
| A1 | 2 | Input | Input for channel 1 |
| A2 | 3 | Input | Input for channel 2 |
| A3 | 4 | Input | Input for channel 3 |
| A4 | 5 | Input | Input for channel 4 |
| A5 | 6 | Input | Input for channel 5 |
| A6 | 7 | Input | Input for channel 6 |
| A7 | 8 | Input | Input for channel 7 |
| A8 | 9 | Input | Input for channel 8 |
| GND | 10 | — | Ground |
| Y8 | 11 | Output | Output for channel 8 |
| Y7 | 12 | Output | Output for channel 7 |
| Y6 | 13 | Output | Output for channel 6 |
| Y5 | 14 | Output | Output for channel 5 |
| Y4 | 15 | Output | Output for channel 4 |
| Y3 | 16 | Output | Output for channel 3 |
| Y2 | 17 | Output | Output for channel 2 |
| Y1 | 18 | Output | Output for channel 1 |
| $\overline{OE2}$ | 19 | Input | Output enable input 2, active low |
| $V_{CC}$ | 20 | — | Postive supply |
| Thermal Pad | | — | The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply. |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | – 0.5 | 7 | V |
| $I_{IK}$ | Input clamp current[2] | $V_I$ < -0.5 V or $V_I$ > $V_{CC}$ + 0.5 V | | ±20 | mA |
| $I_{OK}$ | Output clamp current[2] | $V_O$ < -0.5 V or $V_O$ > $V_{CC}$ + 0.5 V | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±35 | mA |
| $I_{CC}$ | Continuous current through $V_{CC}$ or GND | | | ±70 | mA |
| $T_J$ | Junction temperature[3] | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | – 65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Guaranteed by design.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±4000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2] | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2 | 5 | 6 | V |
| $V_I$ | Input voltage | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | | $V_{CC}$ | V |
| $T_A$ | Ambient temperature | – 55 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | SN74HCS541 RKS (VQFN) 20 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 83.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 82.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 57.4 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 14.5 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 56.4 | °C/W |


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| THERMAL METRIC[1] | | SN74HCS541 RKS (VQFN) 20 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 40.0 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{T+}$ | Positive switching threshold | | | 2 V | 0.7 | | 1.5 | V |
| | | | | 4.5 V | 1.7 | | 3.15 | |
| | | | | 6 V | 2.1 | | 4.2 | |
| $V_{T-}$ | Negative switching threshold | | | 2 V | 0.3 | | 1 | V |
| | | | | 4.5 V | 0.9 | | 2.2 | |
| | | | | 6 V | 1.2 | | 3 | |
| $\Delta V_T$ | Hysteresis ($V_{T+}$ - $V_{T-}$) | | | 2 V | 0.2 | | 1 | V |
| | | | | 4.5 V | 0.4 | | 1.4 | |
| | | | | 6 V | 0.6 | | 1.6 | |
| $V_{OH}$ | High-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -20 µA | 2 V to 6 V | $V_{CC}$ – 0.1 | $V_{CC}$ – 0.002 | | V |
| | | | $I_{OH}$ = -6 mA | 4.5 V | 4 | 4.3 | | |
| | | | $I_{OH}$ = -7.8 mA | 6 V | 5.4 | 5.75 | | |
| $V_{OL}$ | Low-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | 2 V to 6 V | | 0.002 | 0.1 | V |
| | | | $I_{OL}$ = 6 mA | 4.5 V | | 0.18 | 0.3 | |
| | | | $I_{OL}$ = 7.8 mA | 6 V | | 0.22 | 0.33 | |
| $I_I$ | Input leakage current | $V_I = V_{CC}$ or 0 | | 6 V | | ±100 | ±1000 | nA |
| $I_{OZ}$ | Off-state (high-impedance state) output current | $V_O = V_{CC}$ or 0 | | 6 V | | ±0.01 | ±2 | µA |
| $I_{CC}$ | Supply current | $V_I = V_{CC}$ or 0, $I_O$ = 0 | | 6 V | | 0.1 | 2 | µA |
| $C_i$ | Input capacitance | | | 2 V to 6 V | | | 5 | pF |

## 6.6 Switching Characteristics

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See Parameter Measurement Information. $C_L$ = 50 pF.

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay | A | Y | 2 V | | 13 | 45 | ns |
| | | | | 4.5 V | | 7 | 18 | |
| | | | | 6 V | | 6 | 16 | |
| $t_{en}$ | Enable time | $\overline{OE}$ | Y | 2 V | | 15 | 44 | ns |
| | | | | 4.5 V | | 7 | 22 | |
| | | | | 6 V | | 6 | 18 | |
| $t_{dis}$ | Disable time | $\overline{OE}$ | Y | 2 V | | 12 | 30 | ns |
| | | | | 4.5 V | | 9 | 20 | |
| | | | | 6 V | | 8 | 19 | |
| $t_t$ | Transition-time | | Any | 2 V | | 9 | 16 | ns |
| | | | | 4.5 V | | 5 | 9 | |
| | | | | 6 V | | 4 | 8 | |

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## 6.7 Operating Characteristics

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per gate | No load | | 20 | | pF |


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## 6.8 Typical Characteristics

$T_A$ = 25°C

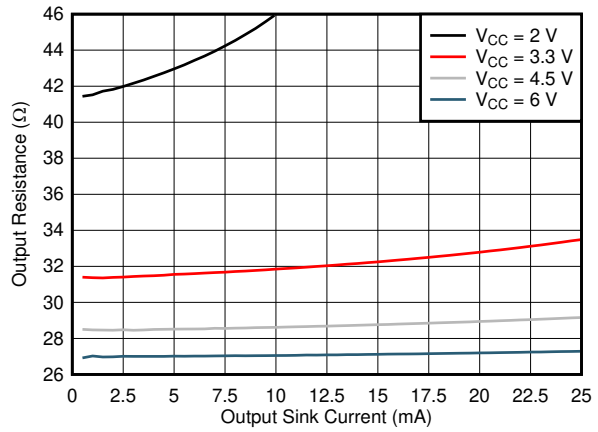



**图 6-1. Output Driver Resistance in LOW State**

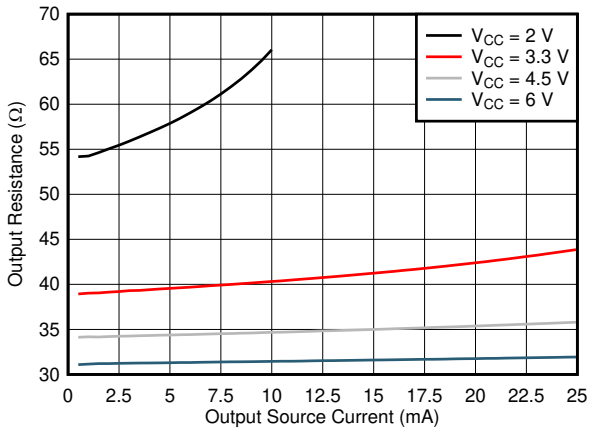



**图 6-2. Output Driver Resistance in HIGH State**

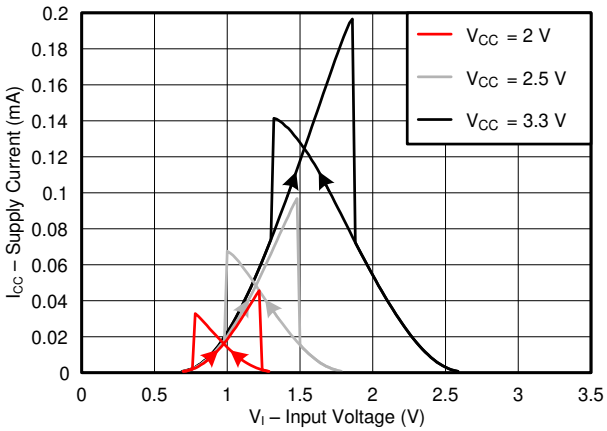



**图 6-3. Supply Current Across Input Voltage, 2-, 2.5-, and 3.3-V Supply**

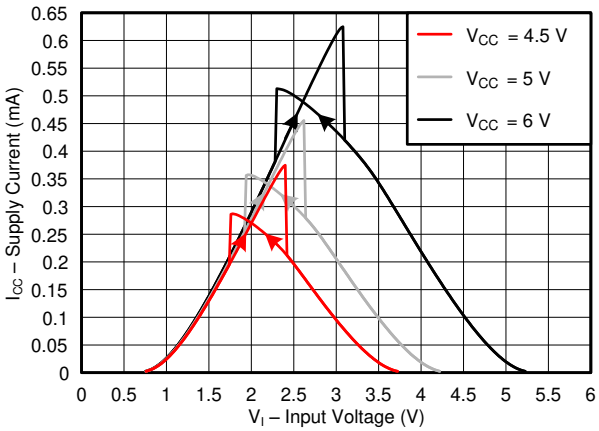


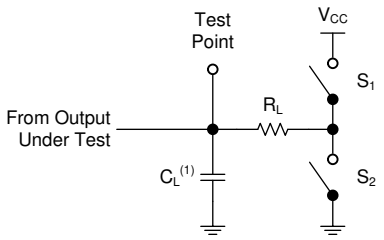

**图 6-4. Supply Current Across Input Voltage, 4.5-, 5-, and 6-V Supply**

## 7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_t$ < 2.5 ns.

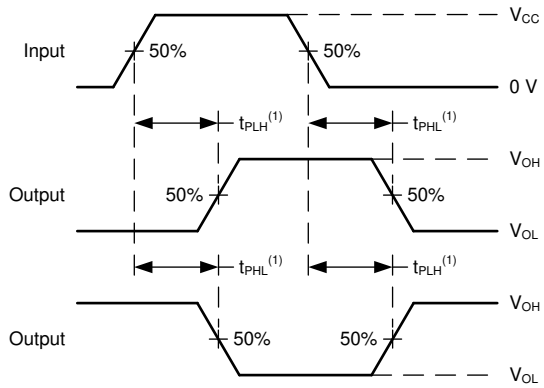
For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.




(1) $C_L$ includes probe and test-fixture capacitance.

**图 7-1. Load Circuit for 3-State Outputs**




(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**图 7-2. Voltage Waveforms Propagation Delays**

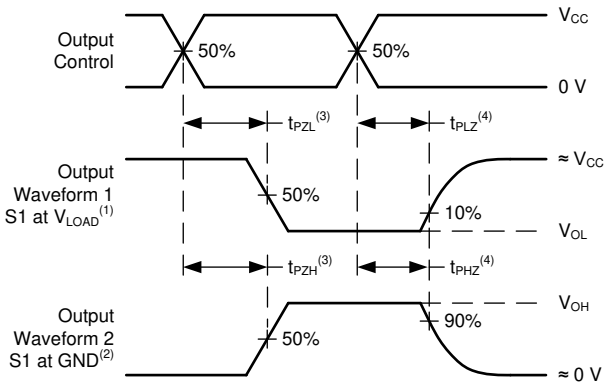
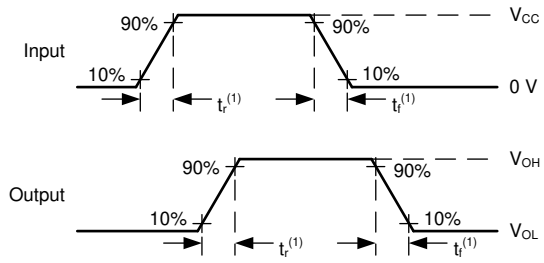



**图 7-3. Voltage Waveforms Propagation Delays**




(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

**图 7-4. Voltage Waveforms, Input and Output Transition Times**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# 8 Detailed Description

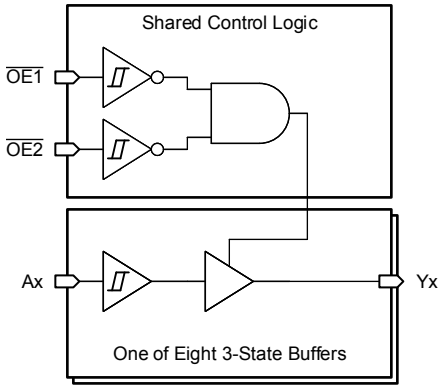
## 8.1 Overview

The SN74HCS541 contains eight buffers with 3-state outputs and Schmitt-trigger inputs. The active low output enable pins ($\overline{OE1}$, $\overline{OE2}$) control all eight channels, and are configured such that both must be low for the outputs to be active.

When the outputs are enabled, the outputs are actively driving low or high.

When the outputs are disabled, the outputs are set into the high-impedance state.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-State outputs. The three states that these outputs can be in are driving high, driving low, and high impedance. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10 kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

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### 8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by $\Delta V_T$ in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

### 8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Electrical Placement of Clamping Diodes for Each Input and Output.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

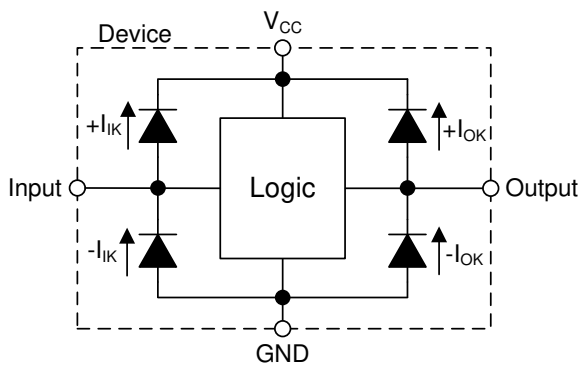


**图 8-1. Electrical Placement of Clamping Diodes for Each Input and Output**

## 8.4 Device Functional Modes

**表 8-1. Function Table**

| INPUTS(1) | | | OUTPUT(2) |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

(1) L = input low, H = input high, X = don't care
(2) L = output low, H = output high, Z = high impedance


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# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74HCS541 can be used to drive signals over relatively long traces or transmission lines. In order to reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver, a series damping resistor placed in series with the transmitter’s output can be used. The plot in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

## 9.2 Typical Application

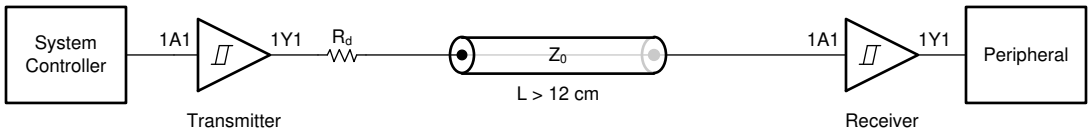


**图 9-1. Typical application block diagram**

### 9.2.1 Design Requirements

#### *9.2.1.1 Power Considerations*

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS541 plus the maximum static supply current, $I_{CC}$, listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS541 plus the maximum supply current, $I_{CC}$, listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS541 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

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The SN74HCS541 can drive a load with total resistance described by $R_L \geqslant V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and Cpd Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### *9.2.1.2 Input Considerations*

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS541, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74HCS541 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than $V_{CC}$ or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

#### *9.2.1.3 Output Considerations*

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.


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### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS541 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation.

### 9.2.3 Application Curve

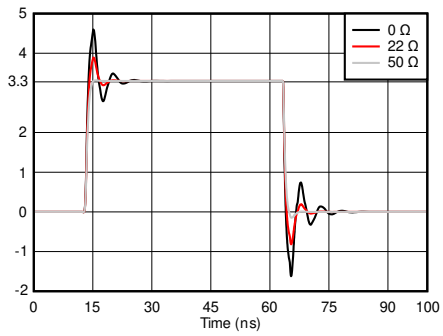


**图 9-2. Simulated signal integrity at the reciever with different damping resistor ($R_d$) values**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

### 11.2 Layout Example

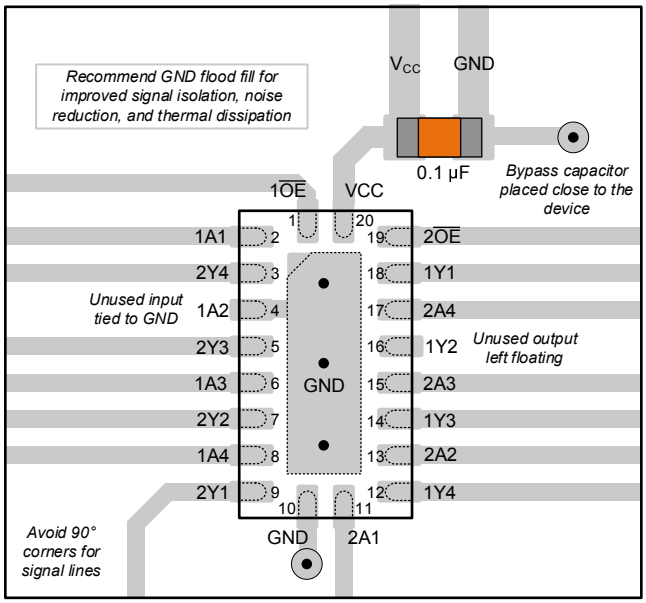


**图 11-1. Example layout for the SN74HCS541 in the RKS Package**


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# 12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *HCMOS Design Considerations* application report (SCLA007)
- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application report (SDYA009)
- Texas Instruments, *Designing With Logic* application report

## 12.2 接收文档更新通知

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## 12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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## 12.4 Trademarks

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## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 术语表

| | |
|---|---|
| TI 术语表 | 本术语表列出并解释了术语、首字母缩略词和定义。 |

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HCS541RKSR | ACTIVE | VQFN | RKS | 20 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HCS541 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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# GENERIC PACKAGE VIEW

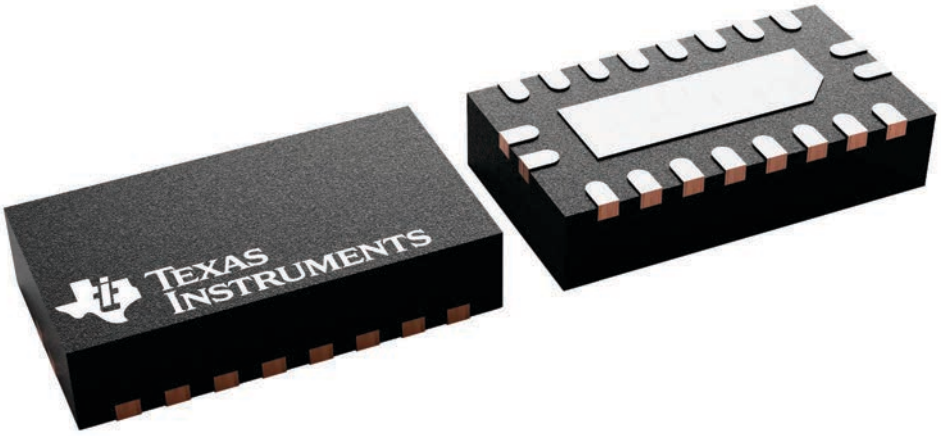
## RKS 20

## VQFN - 1 mm max height

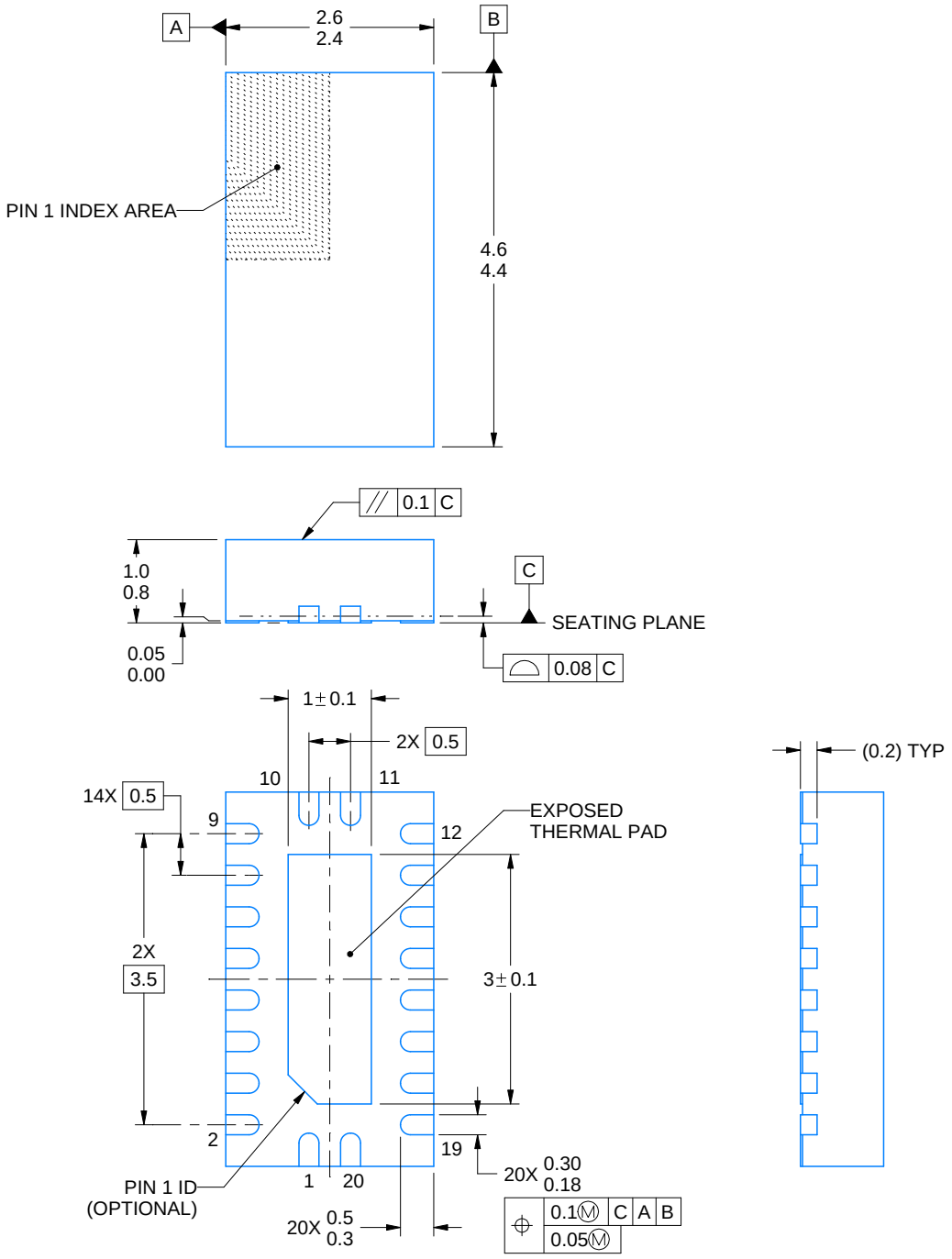
**2.5 x 4.5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



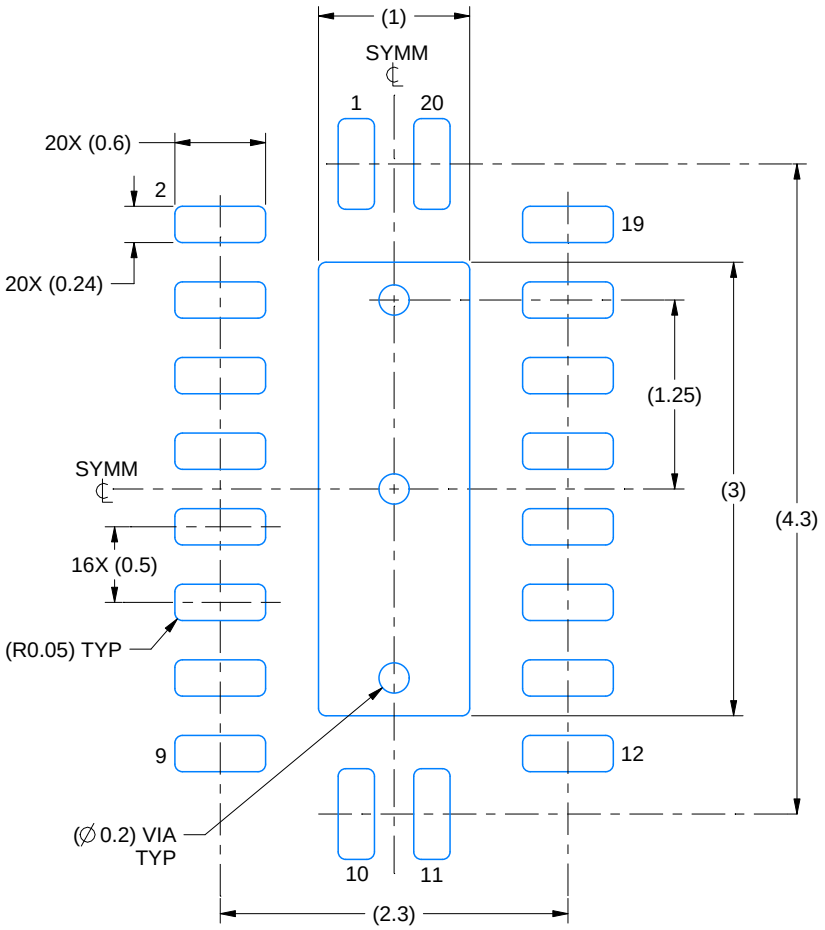

4226872/A



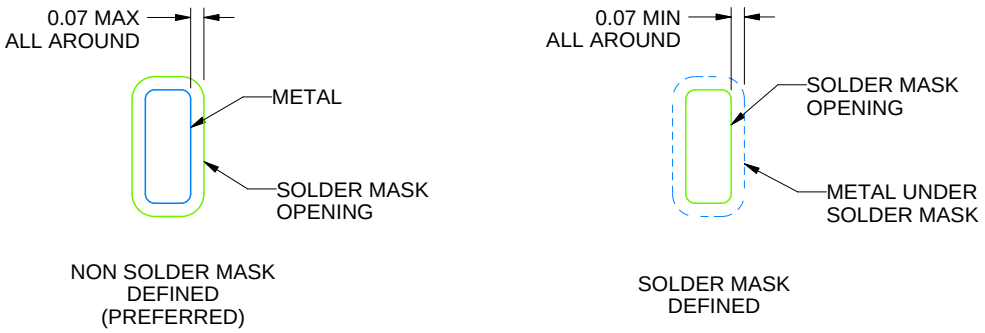

4222490/B 02/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X




SOLDER MASK DETAILS

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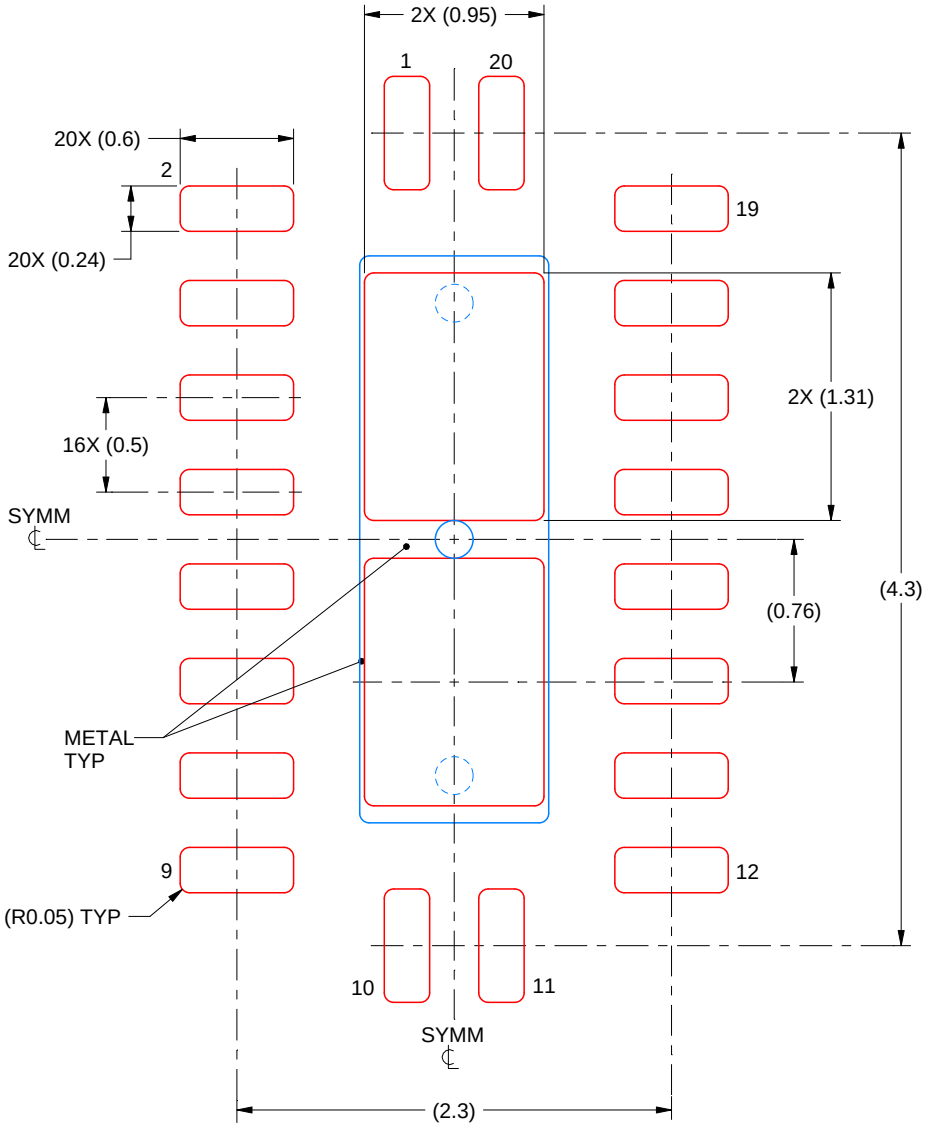
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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