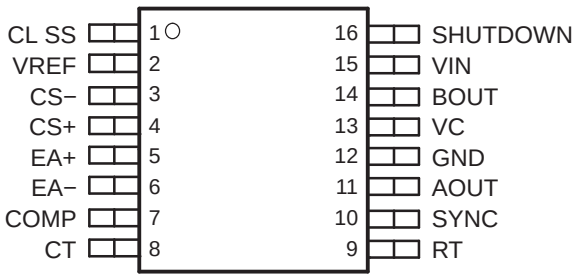
# IMPROVED CURRENT-MODE PWM CONTROLLER

**Check for Samples: UC2856-Q1**

## FEATURES

- **Qualified for Automotive Applications**
- **Pin-for-Pin Compatible With the UC2846**
- **65-ns Typical Delay From Shutdown to Outputs and 50-ns Typical Delay From Sync to Outputs**
- **Improved Current Sense Amplifier With Reduced Noise Sensitivity**
- **Differential Current Sense With 3-V Common-Mode Range**
- **Trimmed Oscillator Discharge Current for Accurate Deadband Control**
- **Accurate 1-V Shutdown Threshold**
- **High Current Dual Totem Pole Outputs (1.5-A Peak)**
- **TTL Compatible Oscillator SYNC Pin Thresholds**
- **ESD Protection**
  - **4-kV Human-Body Model (HBM)**
  - **500-V Charged-Device Model (CDM)**

**DW PACKAGE**
**(TOP VIEW)**

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## DESCRIPTION

The UC2856 is a high performance version of the popular UC2846 series of current mode controllers, and is intended for both design upgrades and new applications where speed and accuracy are important. All input to output delays have been minimized, and the current sense output is slew rate limited to reduce noise sensitivity. Fast 1.5-A peak output stages have been added to allow rapid switching of power FETs.

A low impedance TTL compatible sync output has been implemented with a 3-state function when used as a sync input.

Internal chip grounding has been improved to minimize internal noise caused when driving large capacitive loads. This, in conjunction with the improved differential current-sense amplifier, results in enhanced noise immunity.

Other features include a trimmed oscillator current (8%) for accurate frequency and dead-time control, a 1-V 5% shutdown threshold, and 4-kV minimum ESD protection (HBM) on all pins.

**ORDERING INFORMATION(1)**

| $T_A$ | PACKAGE(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 125°C | SOP – DW | Reel of 2000 | UC2856QDWRQ1 | UC2856Q1 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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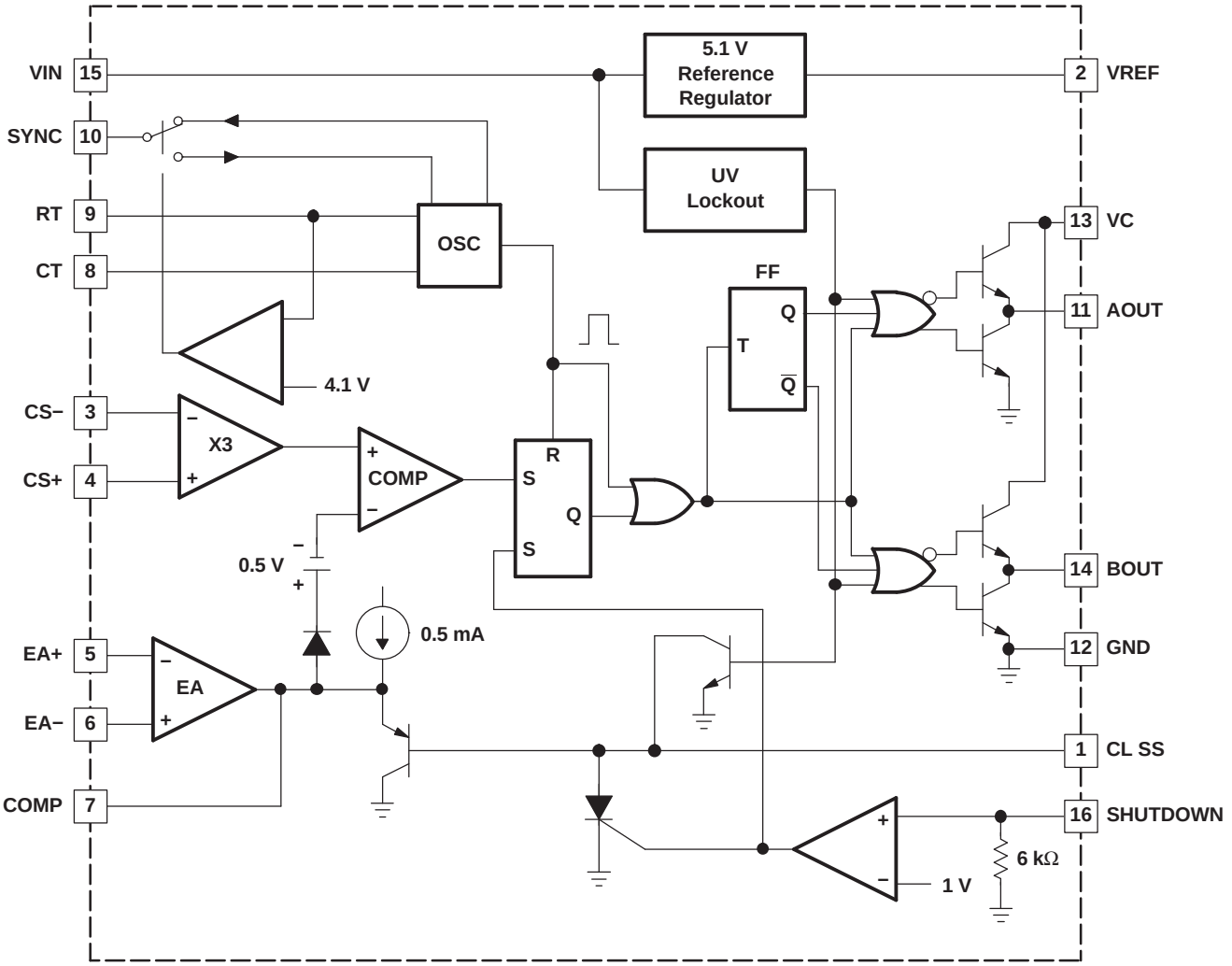
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## BLOCK DIAGRAM

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## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | | UNIT |
|---|---|---|---|
| | Supply voltage | | 40 V |
| | Collector supply voltage | | 40 V |
| $I_O$ | Output current (sink or source) | DC | 0.5 A |
| | | Pulse (0.5 ms) | 2 A |
| | Error amplifier input voltage | | –0.3 V to VIN |
| | Shutdown input voltage | | –0.3 V to 10 V |
| | Current sense input voltage | | –0.3 V to 3 V |
| | SYNC output current | | ±10 mA |
| | Error amplifier output current | | –5 mA |
| | Soft start sink current | | 50 mA |
| | Oscillator charging current | | 5 mA |
| | Power dissipation | $T_A$ = 25°C | 1 W |
| | | $T_C$ = 25°C | 2 W |
| $T_J$ | Operating junction temperature range | | –55°C to 150°C |
| $T_{stg}$ | Storage temperature range | | –65°C to 150°C |
| ESD | Electrostatic discharge protection | Human-Body Model (HBM) | 4000 V |
| | | Charged-Device Model (CDM) | 500 V |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Unless otherwise indicated, voltages are reference to ground and currents are positive into and negative out of the specified terminals.

## ELECTRICAL CHARACTERISTICS

$T_A$ = –40°C to 125°C, VIN = 15 V, RT = 10 kΩ, CT = 1 nF, and $T_A = T_J$ (unless otherwise stated)(1)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Reference Section** | | | | | | |
| Output voltage | $I_O$ = 1 mA, | $T_J$ = 25°C | 5.05 | 5.1 | 5.15 | V |
| Line regulation voltage | VIN = 8 V to 40 V | | | | 20 | mV |
| Load regulation voltage | $I_O$ = –1 mA to –10 mA | | | | 15 | mV |
| Total output variation | Over line, load, and temperature | | 5 | | 5.2 | V |
| Output noise voltage | f = 10 Hz to 10 kHz, | $T_J$ = 25°C | | 50 | | µV |
| Long term stability | 1000 hours, (2) | $T_J$ = 25°C | | 5 | 25 | mV |
| Short circuit current | VREF = 0 V | | –25 | –45 | –65 | mA |
| **Oscillator Section** | | | | | | |
| Initial accuracy | $T_J$ = 25°C | | 180 | 200 | 220 | kHz |
| | $T_J$ = Full range | | 170 | | 230 | |
| Voltage stability | VIN = 8 V to 40 V | | | | 2 | % |
| Discharge current | VCT = 2 V, | $T_J$ = 25°C | 7.5 | 8 | 8.8 | mA |
| | VCT = 2 V | | 6.7 | 8 | 8.8 | |
| Sync output high level voltage | $I_O$ = –1 mA | | 2.4 | 3.6 | | V |
| Sync output low level voltage | $I_O$ = 1 mA | | | 0.2 | 0.4 | V |
| Sync input high level voltage | CT = 0 V, RT = VREF | | 2 | 1.5 | | V |
| Sync input low level voltage | CT = 0 V, RT = VREF | | | 1.5 | 0.8 | V |
| Sync input current | CT = 0 V, RT = VREF, $V_{SYNC}$ = 5 V | | | 1 | 10 | µA |
| Sync delay to outputs | CT = 0 V RT = VREF, $V_{SYNC}$ = 0.8 V to 2 V | | | 50 | 100 | ns |

(1) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.
(2) This parameter, although specified over the recommended operating conditions, is not 100% tested in production.

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## ELECTRICAL CHARACTERISTICS (continued)

$T_A$ = –40°C to 125°C, VIN = 15 V, RT = 10 kΩ, CT = 1 nF, and $T_A = T_J$ (unless otherwise stated)(1)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Error Amplifier Section** | | | | | | |
| Input offset voltage | $V_{CM}$ = 2 V | | | | 5 | mV |
| Input bias current | | | | | –1 | µA |
| Input offset current | | | | | 500 | nA |
| Common mode range | VIN = 8 V to 40 V | | 0 | | VIN–2 | V |
| Open loop gain | $V_O$ = 1.2 V to 3 V | | 80 | 100 | | dB |
| Unity gain bandwidth | $T_J$ = 25°C | | 1 | 1.5 | | MHz |
| CMRR | $V_{CM}$ = 0 V to 38 V, | VIN = 40 V | 75 | 100 | | dB |
| PSRR | VIN = 8 V to 40 V | | 80 | 100 | | dB |
| Output sink current | $V_{ID}$ = –15 mV | $V_{COMP}$ = 1.2 V | 5 | 10 | | mA |
| Output source current | $V_{ID}$ = 15 mV | $V_{COMP}$ = 2.5 V | –0.4 | –0.5 | | mA |
| High-level output voltage | $V_{ID}$ = 50 mV, | $R_L$ (COMP) = 15 kΩ | 4.3 | 4.6 | 4.9 | V |
| Low-level output voltage | $V_{ID}$ = –50 mV, | $R_L$ (COMP) = 15 kΩ | | 0.7 | 1 | V |
| **Current Sense Amplifier Section** | | | | | | |
| Amplifier gain | $V_{CS–}$ = 0 V, | CL SS Open(3) (4) | 2.5 | 2.75 | 3 | V/V |
| Maximum differential input signal ($V_{CS+} – V_{CS–}$) | CL SS Open 3, | $R_L$ (COMP) = 15 kΩ | 1.1 | 1.2 | | V |
| Input offset voltage | $V_{CL\ SS}$ = 0.5 V | COMP open(3) | | 5 | 35 | mV |
| CMRR | $V_{CM}$ = 0 V to 3 V | | 60 | | | dB |
| PSRR | VIN = 8 V to 40 V | | 60 | | | dB |
| Input bias current | $V_{CL\ SS}$ = 0.5 V, | COMP open(3) | –1 | | 1 | µA |
| Input offset current | $V_{CL\ SS}$ = 0.5 V, | COMP open(3) | –1 | | 1 | µA |
| Input common mode range | | | 0 | | 3 | V |
| Delay to outputs | $V_{EA+}$ = VREF, EA– = 0 V, CS+ – CS– = 0 V to 1.5 V | | | 120 | 250 | ns |
| **Current Limit Adjust Section** | | | | | | |
| Current limit offset | $V_{CS–}$ = 0 V, $V_{CS+}$ = 0 V, | COMP open(3) | 0.4 | 0.5 | 0.6 | V |
| Input bias current | $V_{EA+}$ = VREF, | $V_{EA–}$ = 0 V | | –10 | –30 | µA |
| **SHUTDOWN Terminal Section** | | | | | | |
| Threshold voltage | | | 0.95 | 1.00 | 1.05 | V |
| Input voltage range | | | 0 | | 5 | V |
| Minimum latching current ($I_{CL\ SS}$) | | | (5)3 | 1.5 | | mA |
| Maximum non-latching current ($I_{CL\ SS}$) | | | | (6)1.5 | 0.8 | mA |
| Delay to outputs | $V_{SHUTDOWN}$ = 0 V to 1.3 V | | | 65 | 110 | ns |

(3) Parameter measured at trip point of latch with VEA+ = VREF, VEA– = 0 V.

(4) Amplifier gain defined as: $G = \frac{\Delta V_{COMP}}{\Delta V_{CS+}}$; $\Delta V_{CS} - = 0\ V\ 1\ V$.

(5) Current into CL SS assured to latch circuit into shutdown state.

(6) Current into CL SS assured not to latch circuit into shutdown state.


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## ELECTRICAL CHARACTERISTICS (continued)

$T_A$ = –40°C to 125°C, VIN = 15 V, RT = 10 kΩ, CT = 1 nF, and $T_A = T_J$ (unless otherwise stated)[1]

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Output Section** | | | | | |
| Collector-emitter voltage | | 40 | | | V |
| Off-state bias current | VC = 40 V | | | 250 | µA |
| Output low level voltage | $I_{OUT}$ = 20 mA | | 0.1 | 0.5 | V |
| | $I_{OUT}$ = 200 mA | | 0.5 | 2.6 | |
| Output high level voltage | $I_{OUT}$ = –20 mA | 12.5 | 13.2 | | V |
| | $I_{OUT}$ = –200 mA | 12 | 13.1 | | |
| Rise time | C1 = 1 nF | | 40 | 80 | ns |
| Fall time | C1 = 1 nF | | 40 | 80 | ns |
| UVLO low saturation | VIN = 0 V, $I_{OUT}$ = 20 mA | | 0.8 | 1.5 | V |
| **PWM Section** | | | | | |
| Maximum duty cycle | | 45 | 47 | 50 | % |
| Minimum duty cycle | | | | 0 | % |
| **Undervoltage Lockout Section** | | | | | |
| Startup threshold | | | 7.7 | 8 | V |
| Threshold hysteresis | | | 0.7 | | V |
| **Total Standby Current** | | | | | |
| Supply current | | | 18 | 23 | mA |

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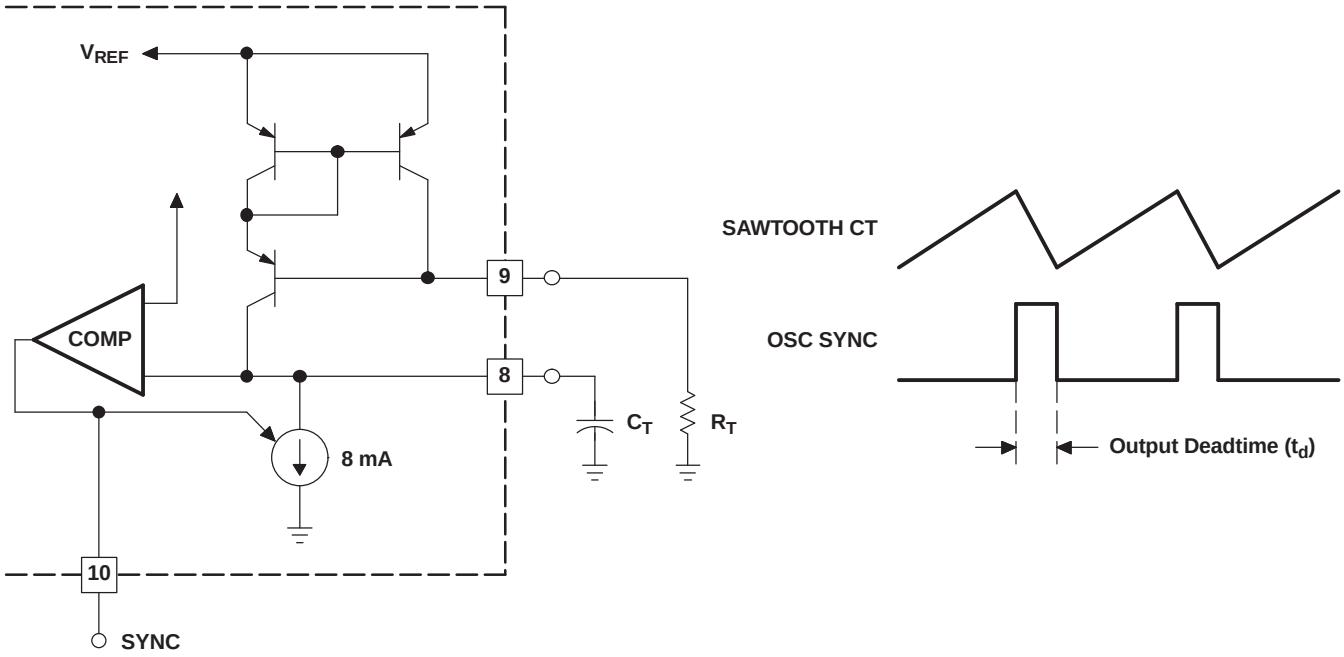
## APPLICATION AND OPERATION INFORMATION




NOTE: Output deadtime is determined by the size of the external capacitor, $C_T$, according to the formula: $Td = \frac{2C_T}{8\ mA - \frac{3.6}{R_T}}$

For large values of $R_T$: $Td = 250\ C_T$

Oscillator frequency is approximated by the formula: $f_T = \frac{2}{R_T \times C_T}$

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**Figure 1. Oscillator Circuit**

NOTE: Error Amplifier can source up to 0.5 mA.

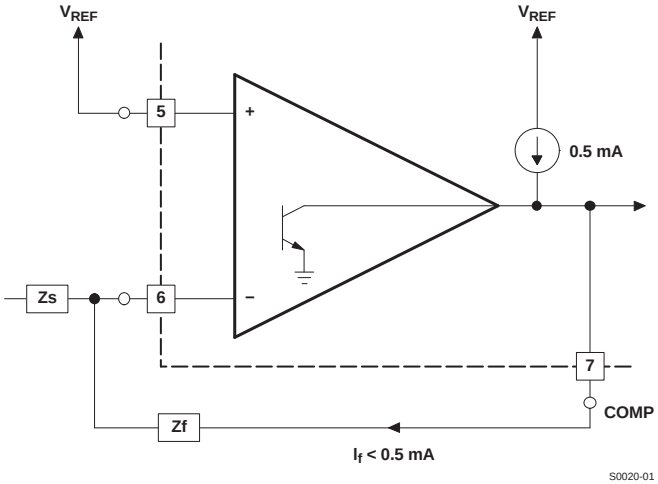


**Figure 2. Error Amplifier Output Configuration**

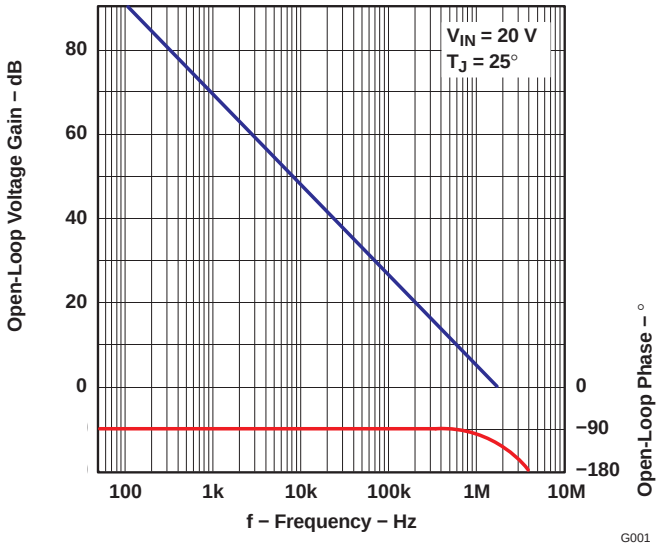


**Figure 3. Error Amplifier Gain and Phase vs Frequency**


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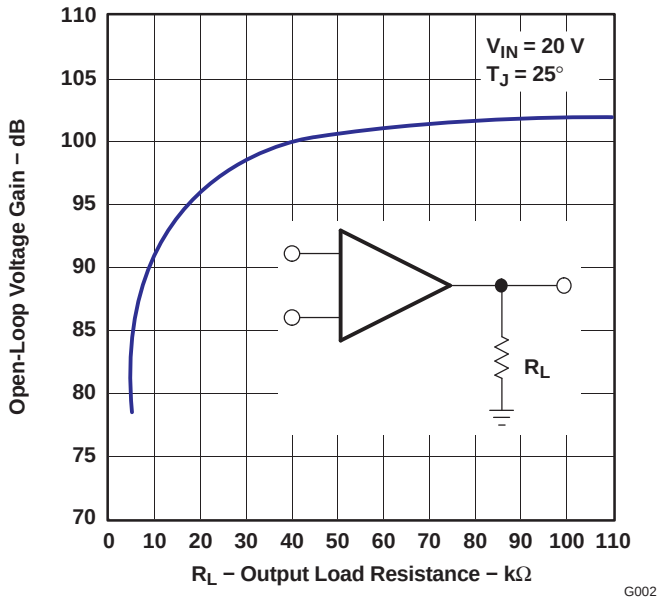
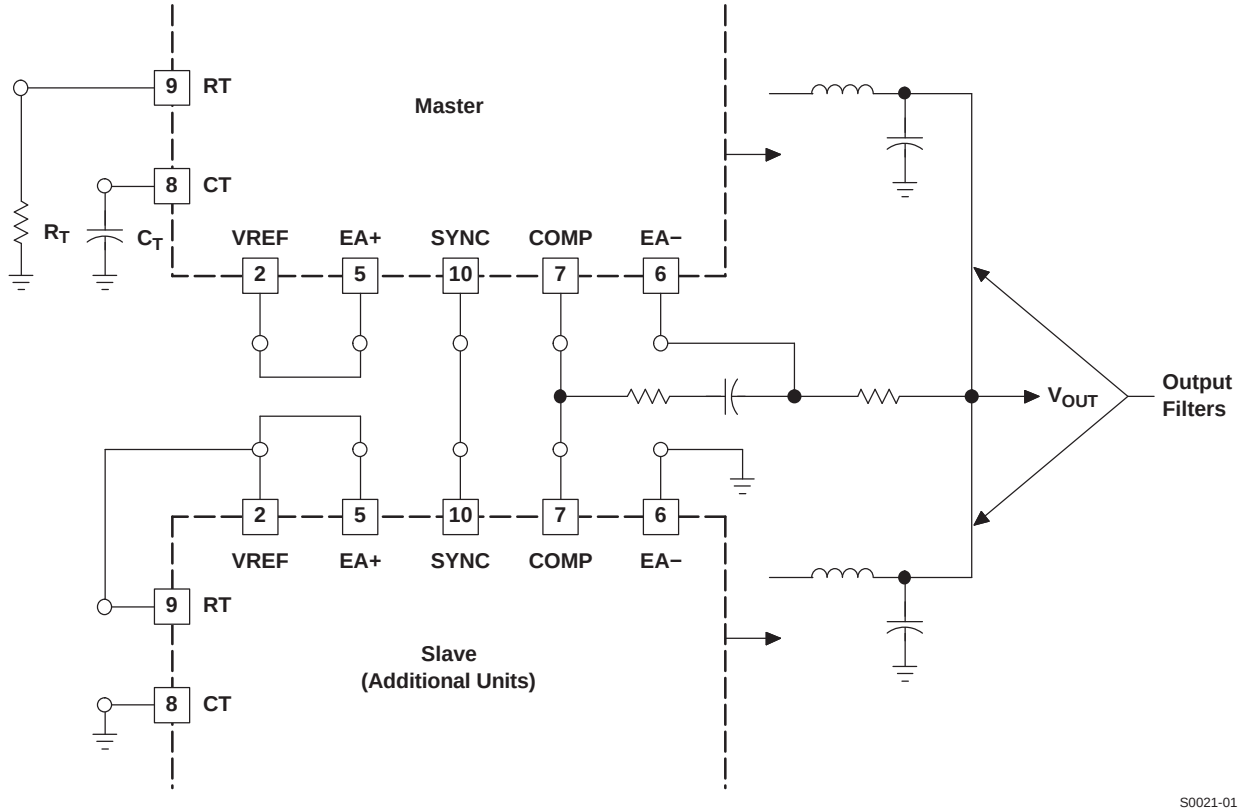



**Figure 4. Error Amplifier Open-Loop DC Gain vs Load Resistance**




NOTE: Slaving allows parallel operation of two or more units with equal current sharing.

**Figure 5. Parallel Operation**

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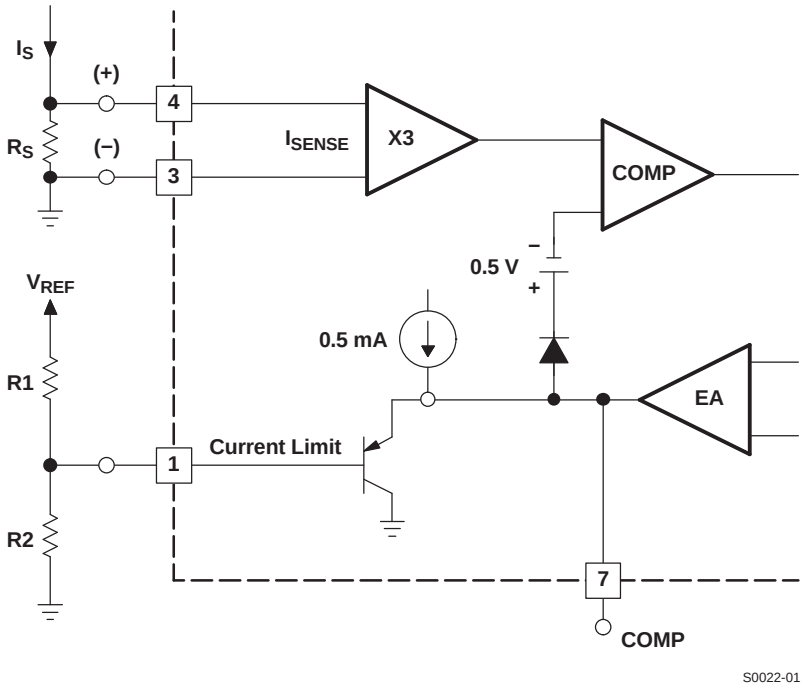


NOTE: Peak current ($I_S$) is determined by the formula: $$I_S = \frac{\left(R2 \times \frac{V_{REF}}{R1+R2}\right) - 0.5}{3R_S}$$

**Figure 6. Pulse by Pulse Current Limiting**


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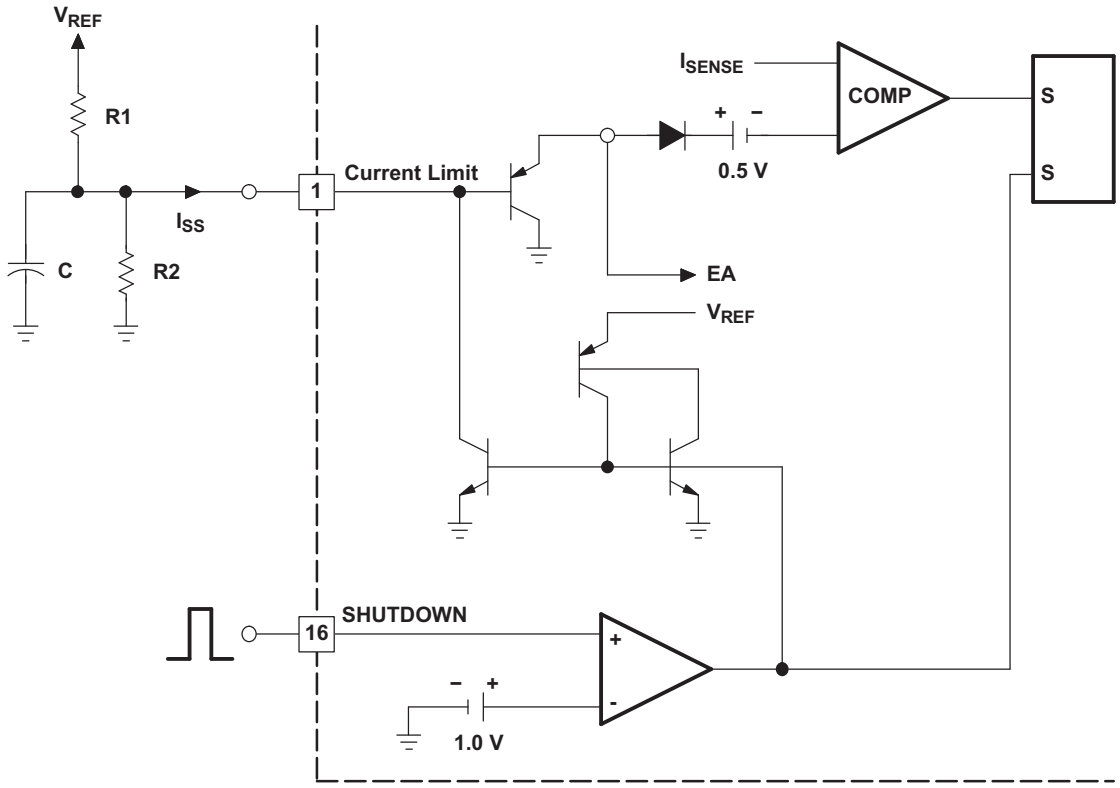


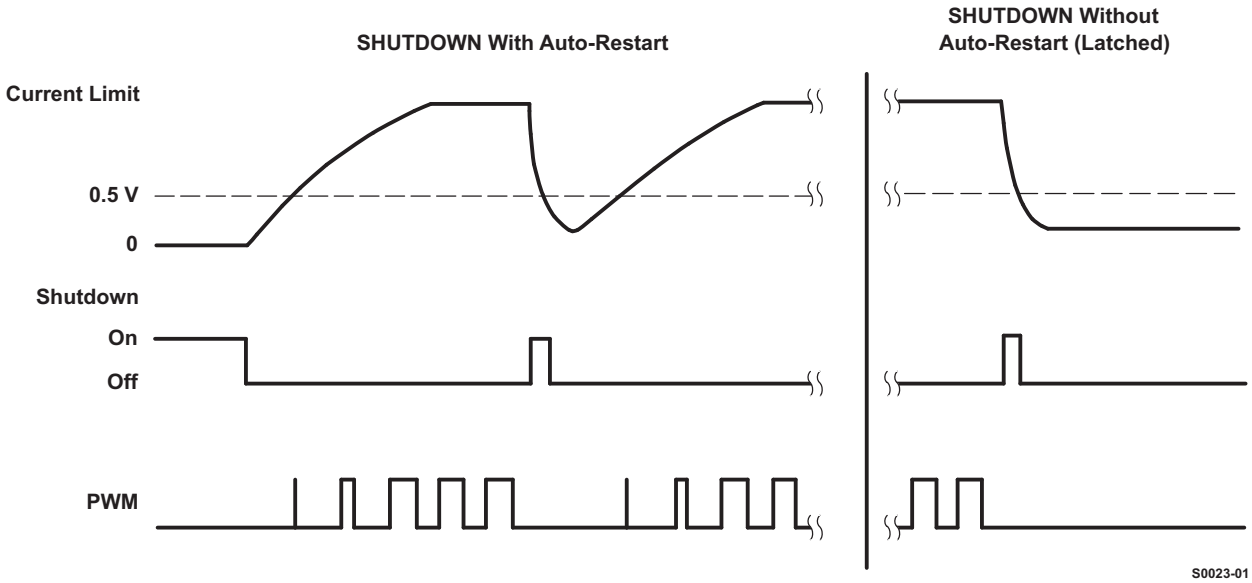


NOTE: If $V_{REF}$ / R1 < 0.8 mA, the shutdown latch commutates when $I_{SS}$ = 0.8 mA, and a restart cycle is initiated. If $V_{REF}$ / R1 > 3 mA, the device latches off until power is cycled.

**Figure 7. Shutdown**

## REVISION HISTORY

**Changes from Original (June 2008) to Revision A** **Page**

- Changed the Input bias current Min Value From: - To: -1 and the Max Value From: -1 To: 1 ..... 4
- Changed the Input offset current Min Value From: - To: -1 ..... 4

**Changes from Revision A (October 2010) to Revision B** **Page**

- Changed the polarity of the comparitor connected to pin 16 in Figure 7 ..... 9


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UC2856QDWRQ1 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | UC2856Q1 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF UC2856-Q1 :**

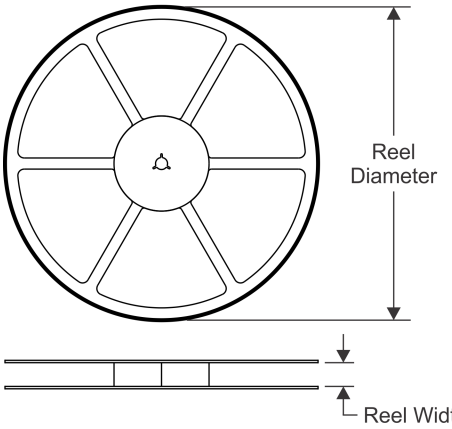
- Catalog: UC2856
- Military: UC2856M

NOTE: Qualified Version Definitions:

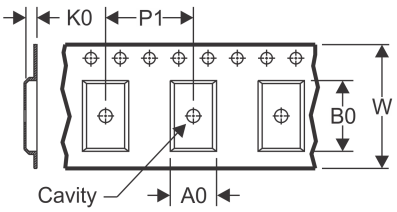
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

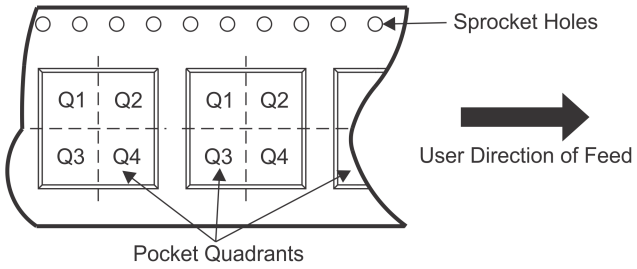



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

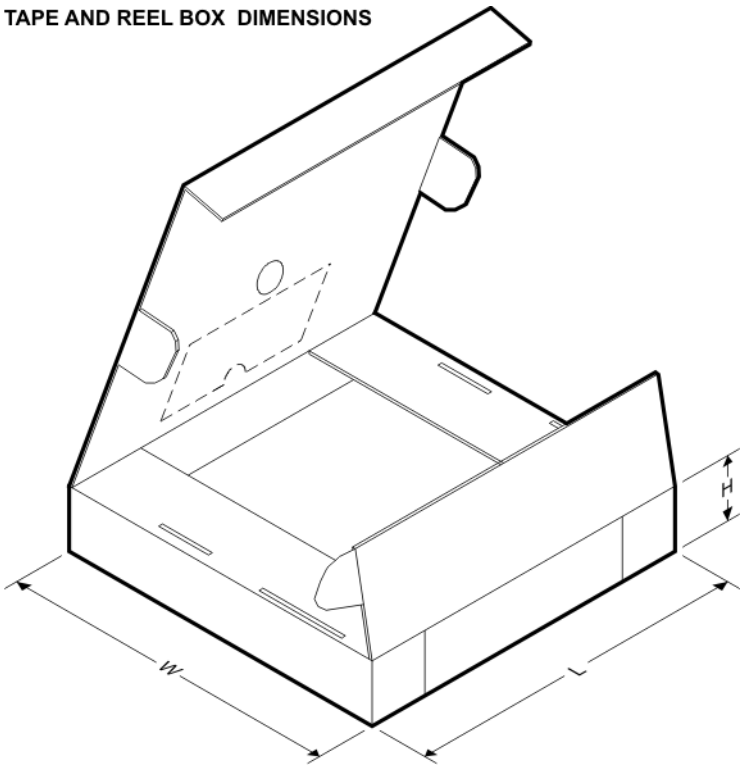
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UC2856QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UC2856QDWRQ1 | SOIC | DW | 16 | 2000 | 853.0 | 449.0 | 35.0 |

# GENERIC PACKAGE VIEW

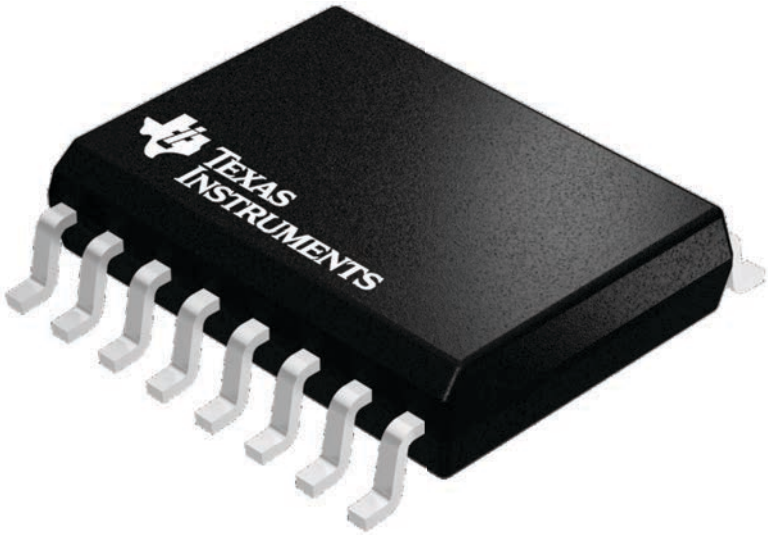
## DW 16

## SOIC - 2.65 mm max height

**7.5 x 10.3, 1.27 mm pitch**

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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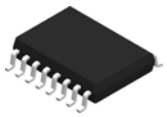
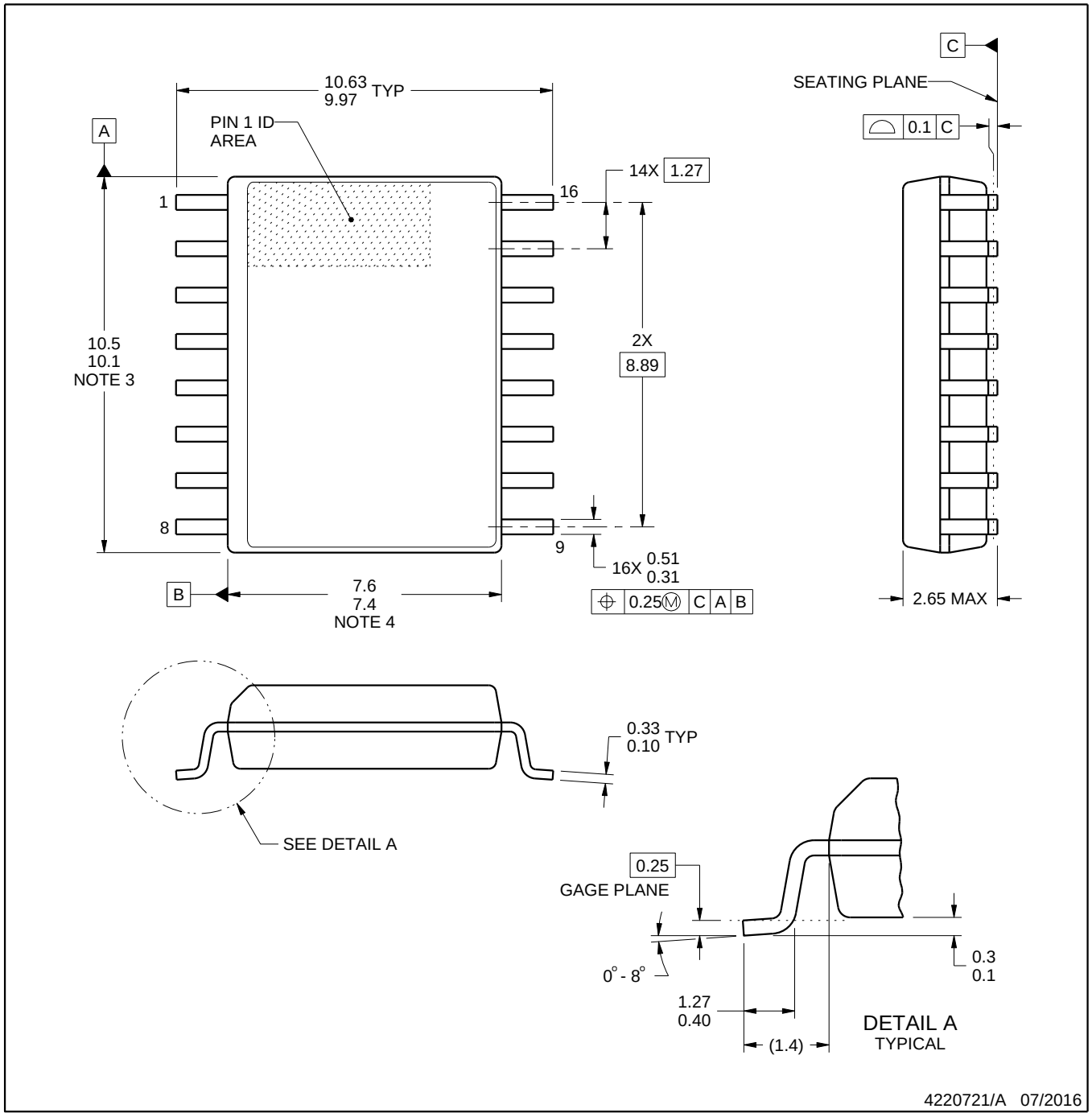


# PACKAGE OUTLINE

## DW0016A

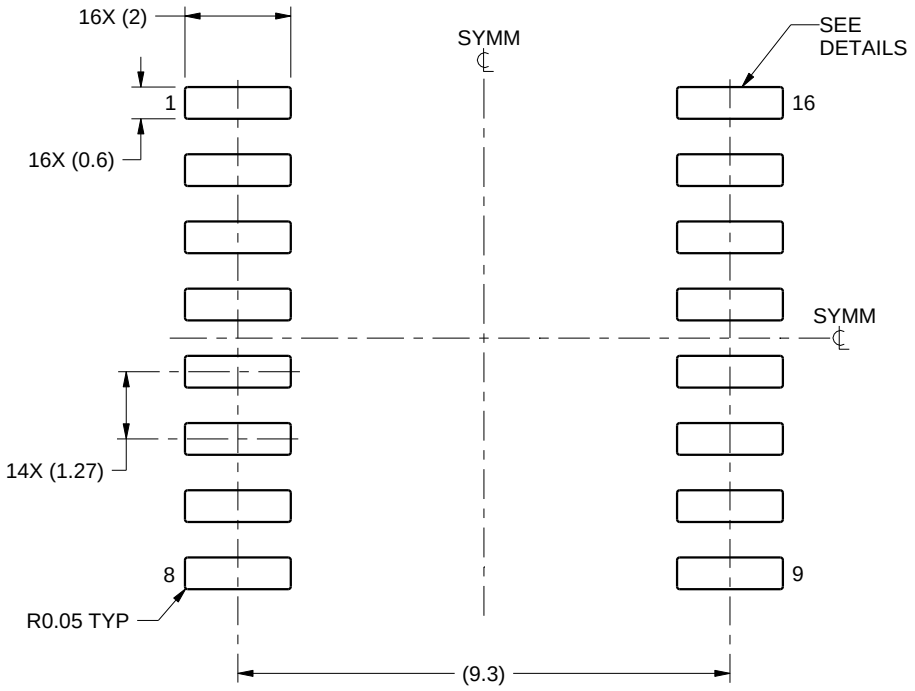
## SOIC - 2.65 mm max height

SOIC

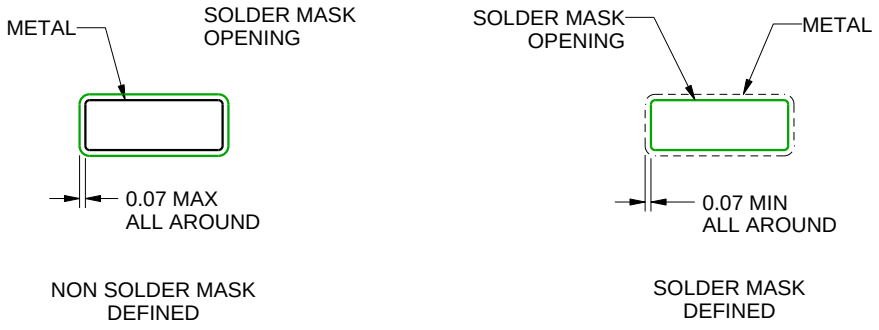



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:7X

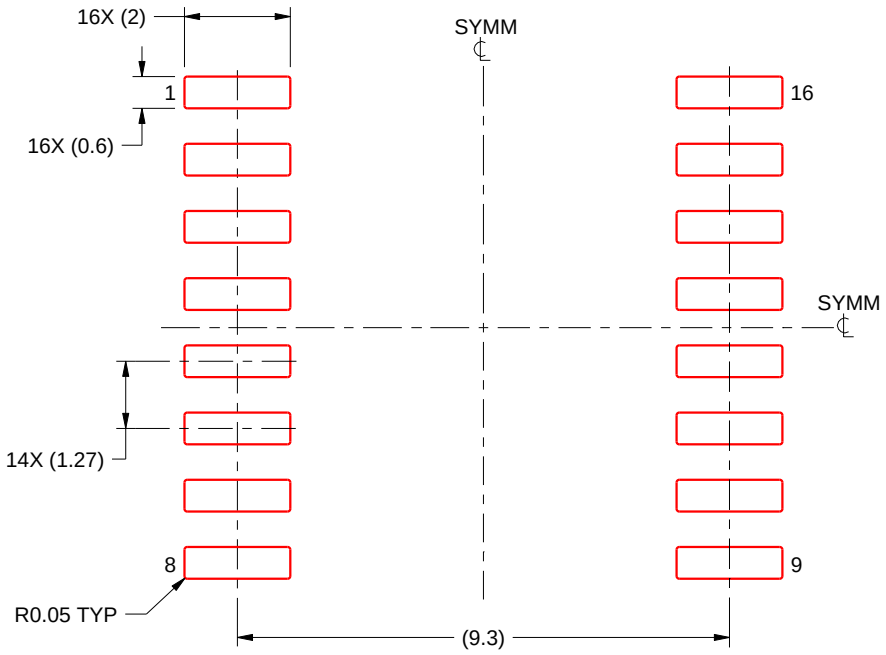



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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