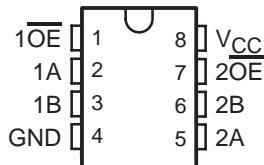


- **Undershoot Protection for Off-Isolation on A and B Ports Up To -2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance ( $r_{on}$ ) Characteristics ( $r_{on} = 3 \Omega$  Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{io(OFF)} = 5 \text{ pF}$  Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption ( $I_{CC} = 3 \mu\text{A}$  Max)**
- **$V_{CC}$  Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **$I_{off}$  Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- **Supports Both Digital and Analog Applications: USB Interface, Bus Isolation, Low-Distortion Signal Gating**

**D OR PW PACKAGE  
(TOP VIEW)**



### description/ordering information

The SN74CBT3306C is a high-speed TTL-compatible FET bus switch with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3306C provides protection for undershoot up to -2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3306C is organized as two 1-bit bus switches with separate output-enable ( $1\overline{OE}$ ,  $2\overline{OE}$ ) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When  $\overline{OE}$  is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 1-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING		
$-40^\circ\text{C}$ to $85^\circ\text{C}$			Tube	SN74CBT3306CD		
			Tape and reel	SN74CBT3306CDR		
TSSOP – PW		Tube	SN74CBT3306CPW			
		Tape and reel	SN74CBT3306CPWR			

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## description/ordering information (continued)

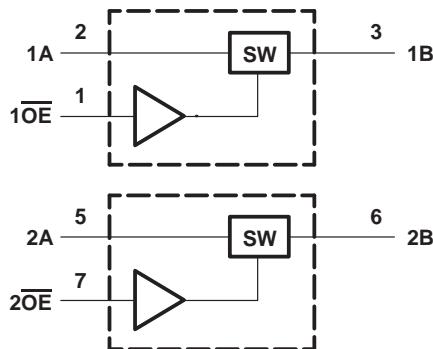
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

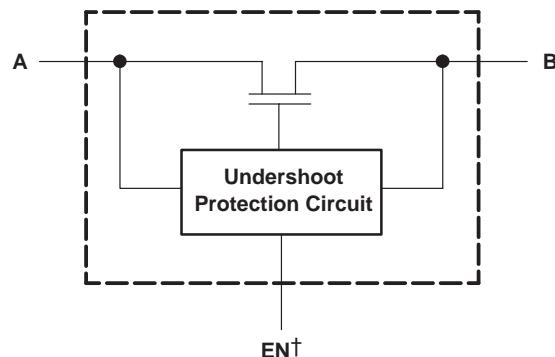
FUNCTION TABLE  
(each bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

## logic diagram (positive logic)



## simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.

1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3.  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
4.  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
5. The package thermal impedance is calculated in accordance with JESD 51-7.

### **recommended operating conditions (see Note 6)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4	5.5	V
$V_{IH}$	High-level control input voltage	2	5.5	V
$V_{IL}$	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 6: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN74CBT3306C****DUAL FET BUS SWITCH****5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION**

SCDS127A – SEPTEMBER 2003 – REVISED OCTOBER 2003

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{IK}$	Control inputs	$V_{CC} = 4.5$ V, $I_{IN} = -18$ mA				-1.8		V
$V_{IKU}$	Data inputs	$V_{CC} = 5$ V, $0$ mA > $I_I \geq -50$ mA, $V_{IN} = V_{CC}$ or GND, Switch OFF				-2		V
$I_{IN}$	Control inputs	$V_{CC} = 5.5$ V, $V_{IN} = V_{CC}$ or GND				$\pm 1$		$\mu A$
$I_{OZ}^{\ddagger}$		$V_{CC} = 5.5$ V, $V_O = 0$ to $5.5$ V, $V_I = 0$ , $V_{IN} = V_{CC}$ or GND				$\pm 10$		$\mu A$
$I_{off}$		$V_{CC} = 0$ , $V_O = 0$ to $5.5$ V, $V_I = 0$				10		$\mu A$
$I_{CC}$		$V_{CC} = 5.5$ V, $I_{I/O} = 0$ , $V_{IN} = V_{CC}$ or GND, Switch ON or OFF				3		$\mu A$
$\Delta I_{CC}^{\$}$	Control inputs	$V_{CC} = 5.5$ V, One input at $3.4$ V, Other inputs at $V_{CC}$ or GND				2.5		mA
$C_{in}$	Control inputs	$V_{IN} = 3$ V or 0				3.5		pF
$C_{io(OFF)}$		$V_{I/O} = 3$ V or 0, Switch OFF, $V_{IN} = V_{CC}$ or GND				5		pF
$C_{io(ON)}$		$V_{I/O} = 3$ V or 0, Switch ON, $V_{IN} = V_{CC}$ or GND				12.5		pF
$r_{on}^{\parallel}$	$V_{CC} = 4$ V, TYP at $V_{CC} = 4$ V		$V_I = 2.4$ V,	$I_O = -15$ mA		8	12	$\Omega$
	$V_{CC} = 4.5$ V		$V_I = 0$	$I_O = 64$ mA		3	6	
				$I_O = 30$ mA		3	6	
			$V_I = 2.4$ V,	$I_O = -15$ mA		5	10	

 $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.† All typical values are at  $V_{CC} = 5$  V (unless otherwise noted),  $T_A = 25^\circ C$ .‡ For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.§ This is the increase in supply current for each input that is at the specified voltage level, rather than  $V_{CC}$  or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4$ V		$V_{CC} = 5$ V $\pm 0.5$ V		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^{\#}$	A or B	B or A	0.24		0.15		ns
$t_{en}$	$\overline{OE}$	A or B	4.6		1.5	4.2	ns
$t_{dis}$	$\overline{OE}$	A or B	4.3		1.5	4.3	ns

# The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

**undershoot characteristics (see Figures 1 and 2)**

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{OUTU}$	$V_{CC} = 5.5$ V, Switch OFF, $V_{IN} = V_{CC}$ or GND	2	$V_{OH} - 0.3$		V

† All typical values are at  $V_{CC} = 5$  V (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

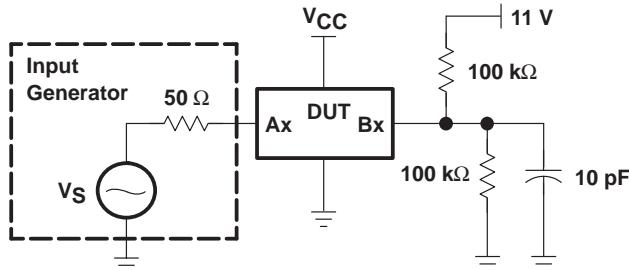


Figure 1. Device Test Setup

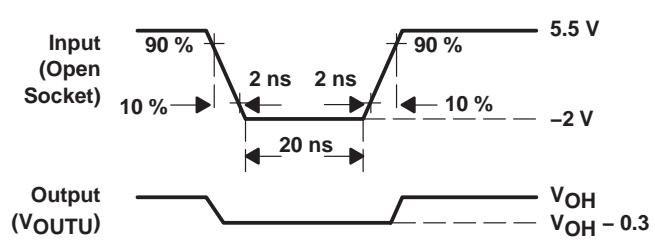
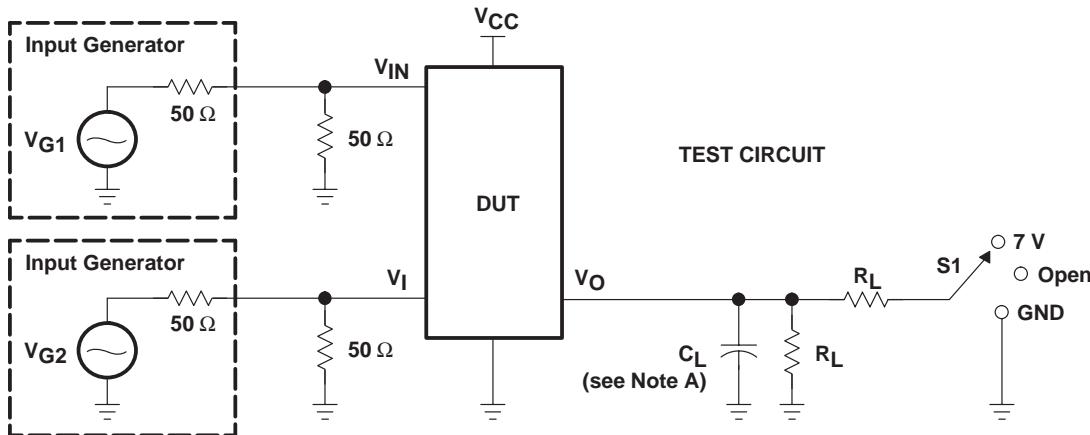
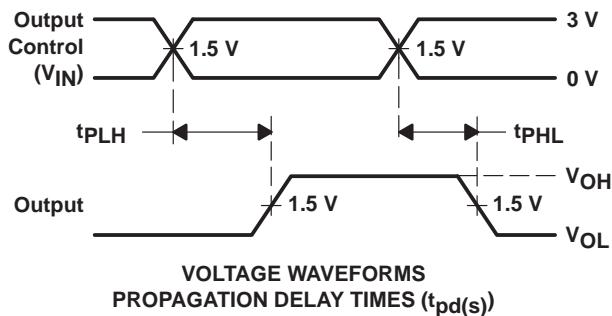
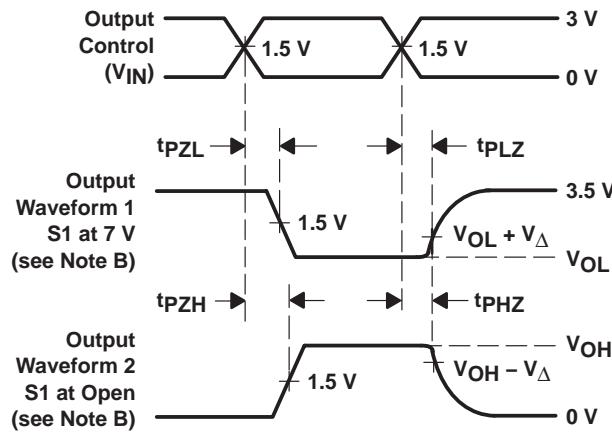


Figure 2. Transient Input Voltage ( $V_I$ ) and Output Voltage ( $V_{OUTU}$ ) Waveforms (Switch OFF)

## PARAMETER MEASUREMENT INFORMATION



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>pd(s)</sub>	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V <sub>CC</sub> or GND V <sub>CC</sub> or GND	50 pF 50 pF	
t <sub>PLZ/tPZL</sub>	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t <sub>PHZ/tPZH</sub>	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V <sub>CC</sub> V <sub>CC</sub>	50 pF 50 pF	0.3 V 0.3 V

VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES (t<sub>pd(s)</sub>)VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

NOTES:

- C<sub>L</sub> includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
- The outputs are measured one at a time with one transition per measurement.
- t<sub>PZL</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd(s)</sub>. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT3306CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU306C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74CBT3306CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU306C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74CBT3306CPW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU306C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74CBT3306CPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	CU306C	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## PACKAGE OPTION ADDENDUM

10-Dec-2020

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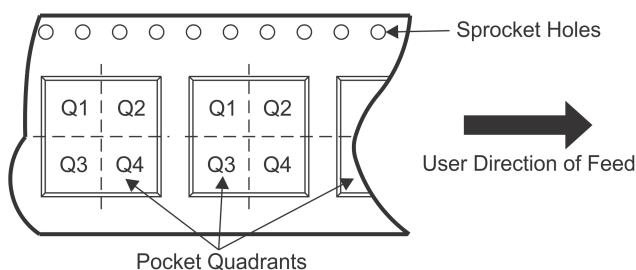
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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


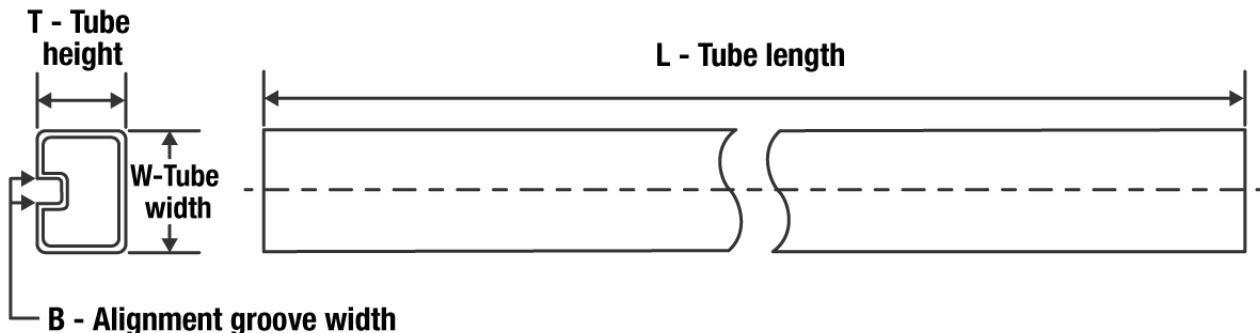
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3306CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBT3306CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SN74CBT3306CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

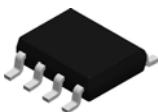

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3306CDR	SOIC	D	8	2500	340.5	336.1	25.0
SN74CBT3306CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
SN74CBT3306CPWR	TSSOP	PW	8	2000	364.0	364.0	27.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBT3306CD	D	SOIC	8	75	507	8	3940	4.32
SN74CBT3306CPW	PW	TSSOP	8	150	530	10.2	3600	3.5

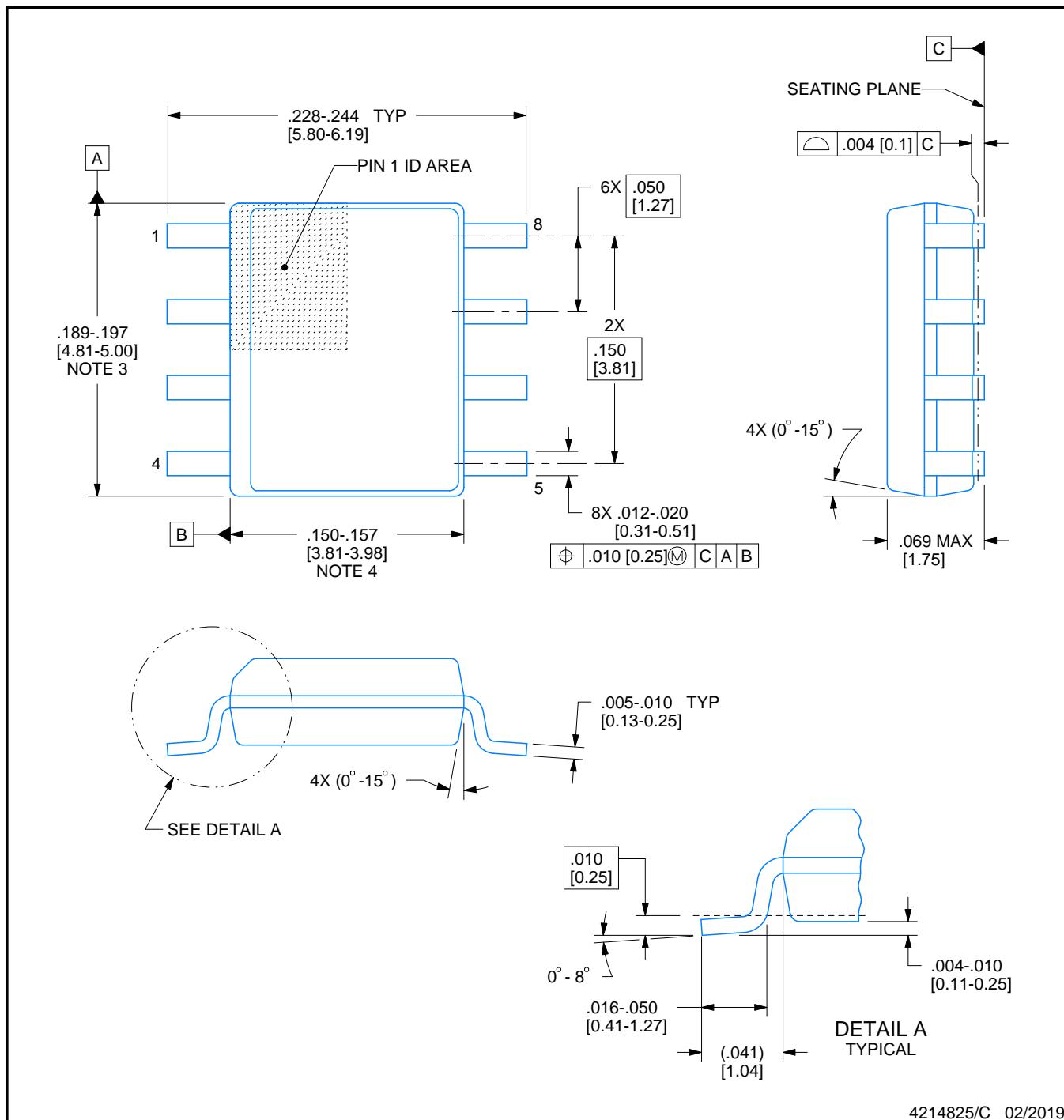


# PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

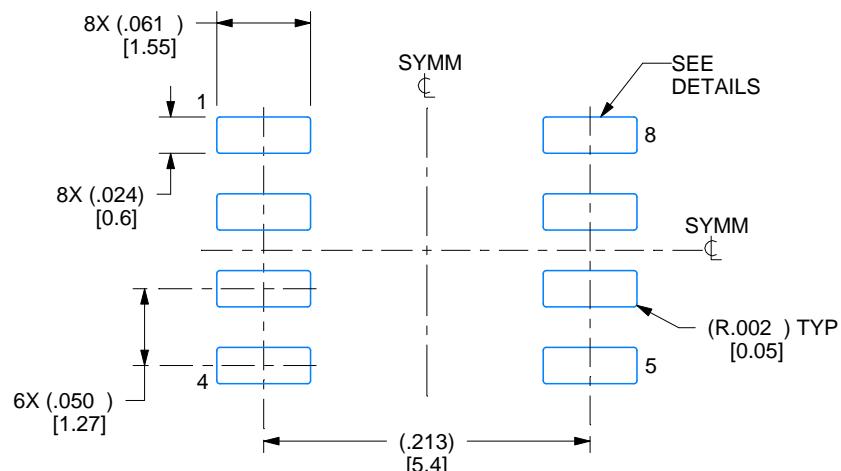
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

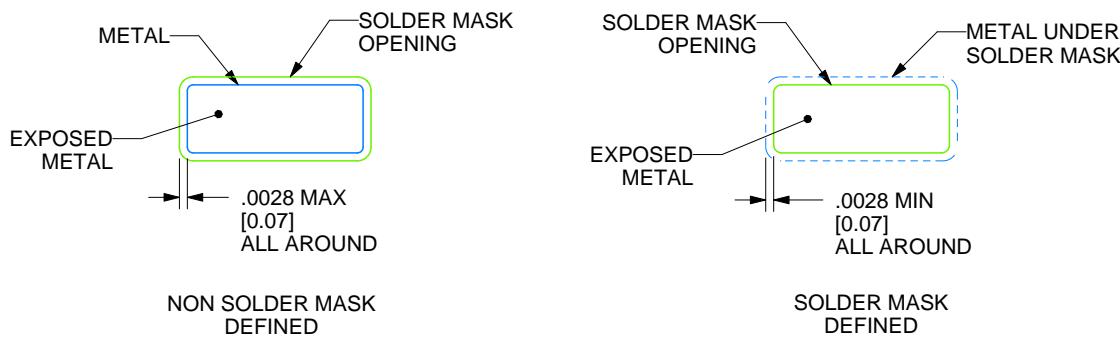
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

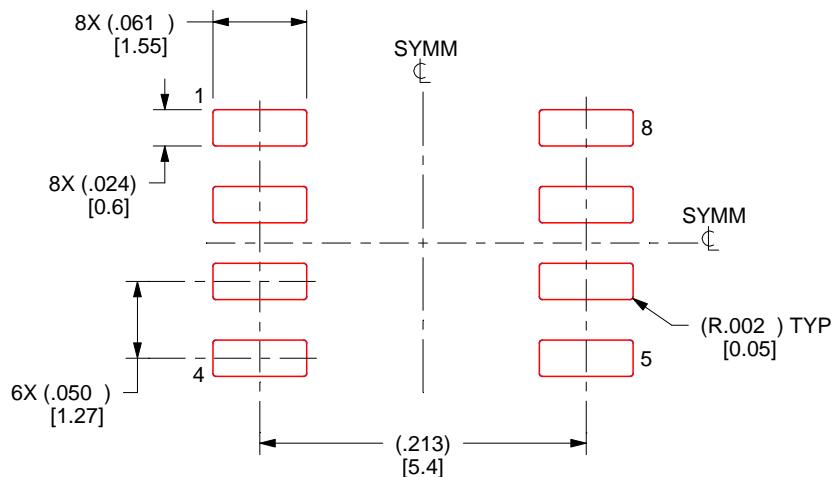
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

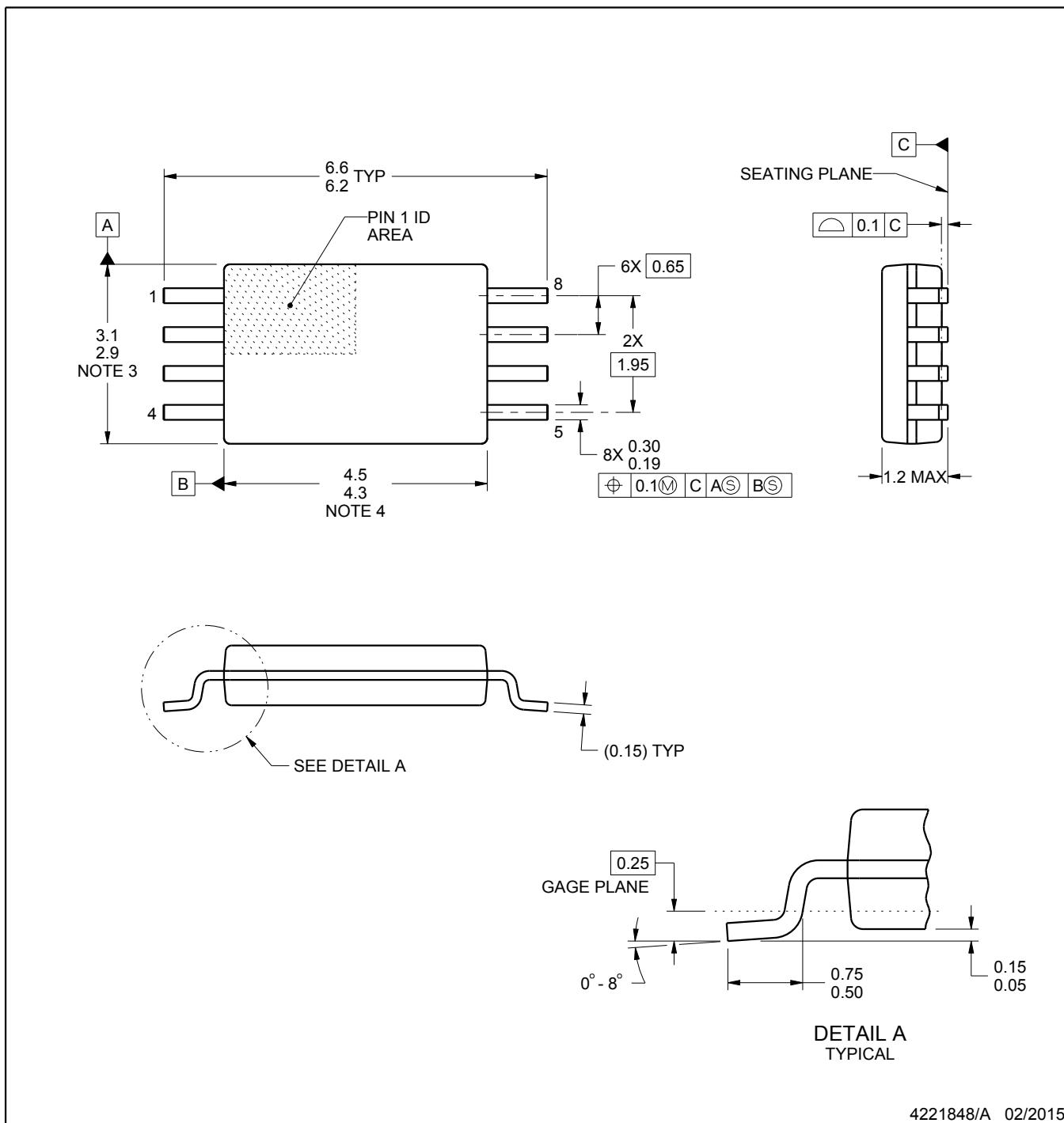
# PACKAGE OUTLINE

PW0008A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

## NOTES:

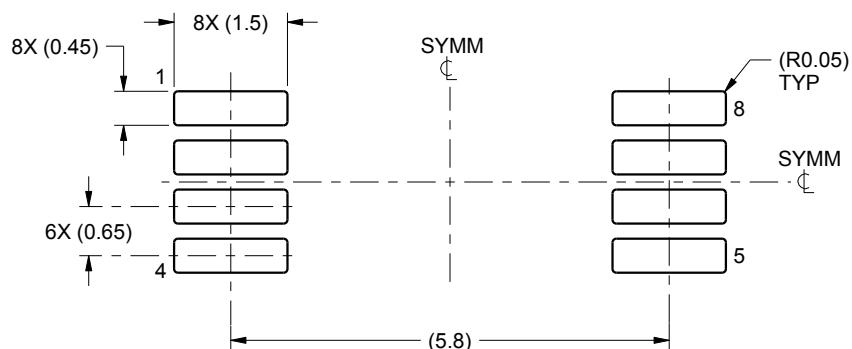
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

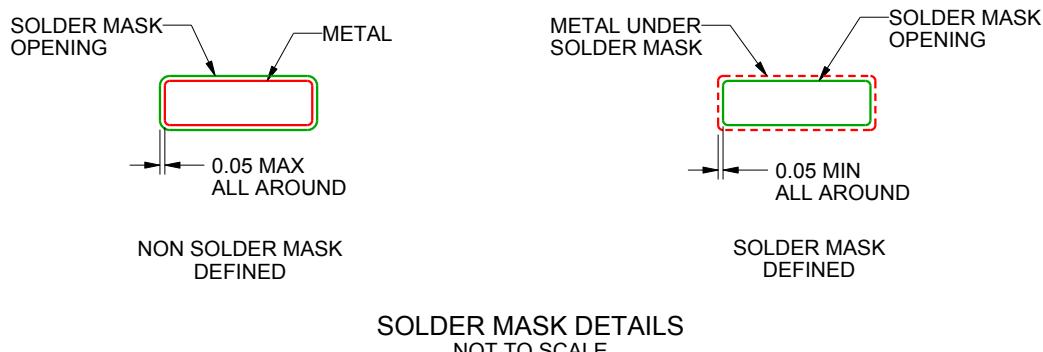
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



4221848/A 02/2015

NOTES: (continued)

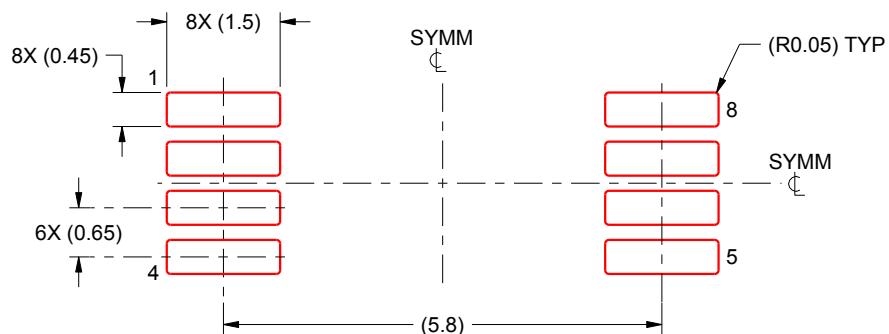
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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