具有中断输出和配置寄存器的 PCA9555 远程 16 位 I²C 和 SMBus I/O 扩展器

1 特性

- 1 µA 低待机电流消耗（最大值）
- I²C 至并行端口扩展器
- 开漏电路低电平有效中断输出
- 可耐受 5V 电压的 I/O 端口
- 兼容大多数微控制器
- 400kHz 快速 I²C 总线
- 针对多达 8 个器件使用的 3 个硬件地址引脚寻址
- 极性反转寄存器
- 具有最大高电流驱动能力的锁存输出，可用于直接驱动 LED
- 锁断性能超过 100mA，符合 JESD 78 II 类规范
- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求
  - 2000V 人体放电模型 (A114-A)
  - 200V 机器放电模型 (A115-A)
  - 1000V 带电器件模型 (C101)

2 应用

- 服务器
- 路由器（电信交换设备）
- 个人计算机
- 个人电子产品
- 工业自动化设备
- 采用 GPIO 受限处理器的产品

3 说明

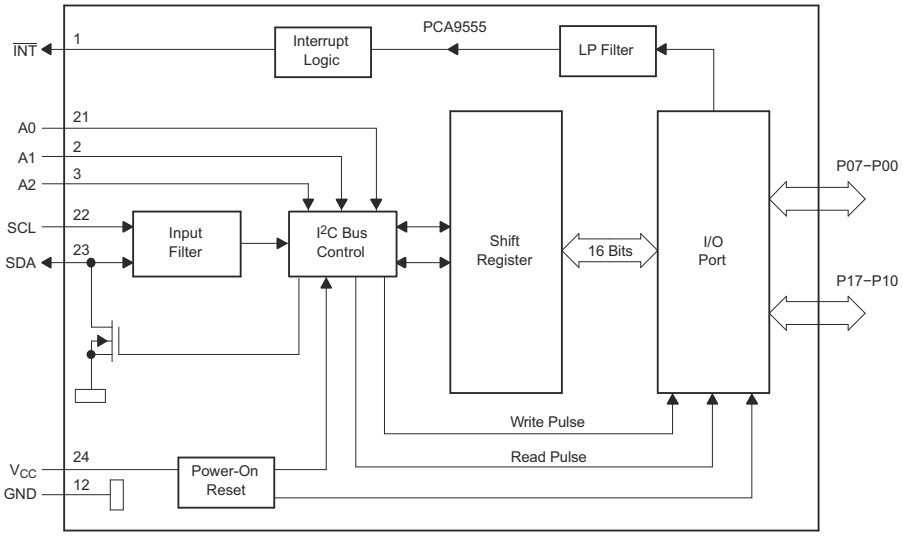
这个用于两线双向总线 (I2C) 的 16 位扩展器设计用于在 2.3V 至 5.5V VCC 之间运行。通过 I²C 接口 [串行时钟 (SCL)，串行数据 (SDA)]，它为大多数微控制器系列产品提供通用远程 I/O 扩展。

PCA9555 由两个 8 位配置（输入或输出可选）、输入端口、输出端口和极性反转（高电平有效或低电平有效运行）寄存器组成。在加电时，I/O 被配置为输入。系统主控制器可以通过写入 I/O 配置位将 I/O 启用为输入或输出。每个输入或输出的数据均保存在相应的输入或输出寄存器中。输入端口寄存器的极性可借助极性反转寄存器进行转换。所有寄存器都可由系统主控器读取。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
PCA9555	SSOP (24) DB	8.20mm × 5.30mm
	SSOP (24) DBQ	8.65mm × 3.90mm
	TVSOP (24) DGV	5.00mm x 4.40mm
	SOIC (24) DW	15.4mm x 7.50mm
	SSOP (24) PW	7.80mm x 4.40mm
	VQFN (24) RGE	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



方框图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

Changes from Revision I (April 2019) to Revision J (March 2021) — **Page**

- Changed the V_{IH} High-level input voltage (SDL, SDA) Max value From: 5.5 V To: V_{CC} in the *Recommended Operating Conditions* ... 5
- Changed the values for the DB, PW, and RGE packages in the *Thermal Information* table ... 6
- Changed the V_{PORR} row in the *Electrical Characteristics* ... 7
- Added the V_{PORF} row in the *Electrical Characteristics* ... 7
- Changed the I_{CC} Standby mode (High Inputs) values in the *Electrical Characteristics* ... 7
- Changed the C_i SCL Max value From: 7 pF To: 8 pF in the *Electrical Characteristics* ... 7
- Changed the C_{io} SDA Max value From: 7 pF To: 9.5 pF in the *Electrical Characteristics* ... 7
- Changed the *Typical characteristic* graphs ... 9
- Changed the *Power Supply Recommendations* ... 27

Changes from Revision H (April 2019) to Revision I (April 2019) — **Page**

- Changed the *I^2C Interface Timing Requirements* table ... 7

Changes from Revision G (March 2018) to Revision H (April 2019) — **Page**

- 更改了*器件信息*表 ... 1
- Added the DW package to the *Thermal Information* table ... 6

Changes from Revision F (June 2014) to Revision G (March 2018) — **Page**

- 添加了应用 列表 ... 1
- Removed the Thermal Information from the *Absolute Maximum Ratings* ... 5
- Added Storage temperature range to the *Absolute Maximum Ratings* ... 5
- Changed the Handling Ratings table to the *ESD Ratings* table ... 5
- Added the *Thermal Information* table ... 6
- Added the *Design Requirements* section ... 25
- Added the *Application Curves* section ... 26
- Added the *Layout* section ... 29

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Changes from Revision E (May 2008) to Revision F (June 2014) **Page**

- Added Interrupt Errata section....16

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5 Pin Configuration and Functions

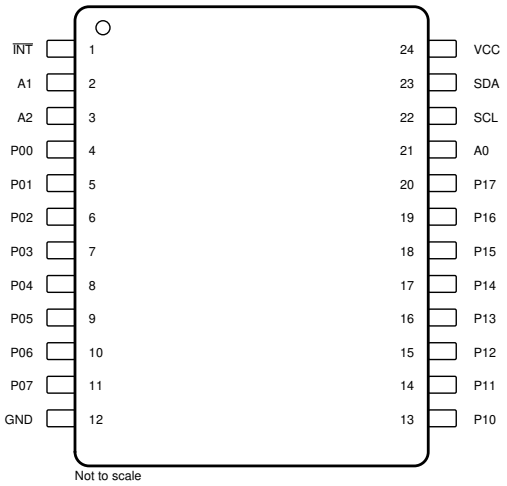


图 5-1. DB, DBQ, DGV, DW or PW Package, 24 Pin (SOP), (Top View)

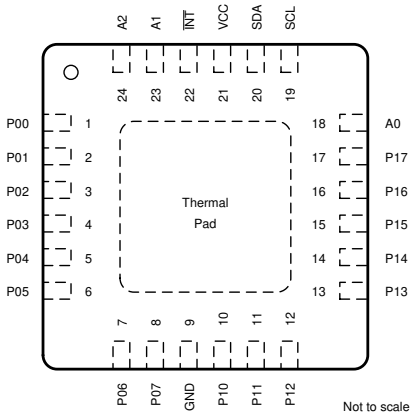


图 5-2. RGE Package, 24 Pin (QFN), (Top View)

表 5-1. Pin Functions

PIN			DESCRIPTION
NAME	SSOP (DB), QSOP (DBQ), TSSOP (PW), AND TVSOP (DGV)	QFN (RGE)	
$\overline{INT}$	1	22	Interrupt output. Connect to V_{CC} through a pullup resistor.
A1	2	23	Address input 1. Connect directly to V_{CC} or ground.
A2	3	24	Address input 2. Connect directly to V_{CC} or ground.
P00	4	1	P-port input/output. Push-pull design structure.
P01	5	2	P-port input/output. Push-pull design structure.
P02	6	3	P-port input/output. Push-pull design structure.
P03	7	4	P-port input/output. Push-pull design structure.
P04	8	5	P-port input/output. Push-pull design structure.
P05	9	6	P-port input/output. Push-pull design structure.
P06	10	7	P-port input/output. Push-pull design structure.
P07	11	8	P-port input/output. Push-pull design structure.
GND	12	9	Ground
P10	13	10	P-port input/output. Push-pull design structure.
P11	14	11	P-port input/output. Push-pull design structure.
P12	15	12	P-port input/output. Push-pull design structure.
P13	16	13	P-port input/output. Push-pull design structure.
P14	17	14	P-port input/output. Push-pull design structure.
P15	18	15	P-port input/output. Push-pull design structure.
P16	19	16	P-port input/output. Push-pull design structure.
P17	20	17	P-port input/output. Push-pull design structure.
A0	21	18	Address input 0. Connect directly to V_{CC} or ground.
SCL	22	19	Serial clock bus. Connect to V_{CC} through a pullup resistor.
SDA	23	20	Serial data bus. Connect to V_{CC} through a pullup resistor.
V_{CC}	24	21	Supply voltage

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		– 0.5	6	V
V_I	Input voltage range(2)		– 0.5	6	V
V_O	Output voltage range(2)		– 0.5	6	V
I_{IK}	Input clamp current	V_I < 0		– 20	mA
I_{OK}	Output clamp current	V_O < 0		– 20	mA
I_{IOK}	Input/output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous output high current	V_O = 0 to V_{CC}		– 50	mA
I_{CC}	Continuous current through GND			– 250	mA
	Continuous current through V_{CC}			160	
T_{stg}	Storage temperature range		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CC}	V_{CC} (1)	V
		A2 – A0, P07 – P00, P17 – P10	0.7 × V_{CC}	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	– 0.5	0.3 × V_{CC}	V
		A2 – A0, P07 – P00, P17 – P10	– 0.5	0.3 × V_{CC}	
I_{OH}	High-level output current	P07 – P00, P17 – P10		– 10	mA
I_{OL}	Low-level output current	P07 – P00, P17 – P10		25	mA
T_A	Operating free-air temperature		– 40	85	°C

(1) For voltages applied above V_{CC}, an increase in ICC will result.

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6.4 Thermal Information

THERMAL METRIC(1)		PCA9555						UNIT
		DB (SSOP)	DBQ (QSOP)	DGV (TVSOP)	DW (SOIC)	PW (TSSOP)	RGE (QFN)	
		24 PINS	24 PINS	24 PINS	24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.9	81.8	105.4	66.7	108.8	48.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.5	39.3	36.7	36.7	54	58.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.4	36.0	50.8	36.7	62.8	27.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.9	7.6	2.4	13.1	11.1	3.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.1	35.6	50.3	62.3	62.3	27.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	15.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage		I_I = – 18 mA	2.3 V to 5.5 V	– 1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising		V_I = V_{CC} or GND, I_O = 0			1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling		V_I = V_{CC} or GND, I_O = 0		0.75	1		V
V_{OH}	P-port high-level output voltage(2)		I_{OH} = – 8 mA	2.3 V	1.8			V
				3 V	2.6			
				4.75 V	4.1			
			I_{OH} = – 10 mA	2.3 V	1.7			
				3 V	2.5			
				4.75 V	4			
I_{OL}	SDA		V_{OL} = 0.4 V	2.3 V to 5.5 V	3			mA
	P port(3)		V_{OL} = 0.5 V		8	20		
			V_{OL} = 0.7 V		10	24		
	$\overline{INT}$		V_{OL} = 0.4 V		3			
I_I	SCL, SDA		V_I = V_{CC} or GND	2.3 V to 5.5 V			±1	μA
	A2 – A0						±1	
I_{IH}	P port		V_I = V_{CC}	2.3 V to 5.5 V			1	μA
I_{IL}	P port		V_I = GND	2.3 V to 5.5 V			– 100	μA
I_{CC}	Operating mode		V_I = V_{CC} or GND, I_O = 0, I/O = inputs, f_{SCL} = 400 kHz, No load	5.5 V		100	200	μA
				3.6 V		30	75	
				2.7 V		20	50	
	Standby mode	Low inputs	V_I = GND, I_O = 0, I/O = inputs, f_{SCL} = 0 kHz, No load	5.5 V		1.1	1.5	mA
				3.6 V		0.7	1.3	
				2.7 V		0.5	1	
		High inputs	V_I = V_{CC}, I_O = 0, I/O = inputs, f_{SCL} = 0 kHz, No load	5.5 V		2.5	3.5	μA
				3.6 V		1	1.8	
				2.7 V		0.7	1.6	
ΔI_{CC}	Additional current in standby mode		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			1.5	mA
C_I	SCL		V_I = V_{CC} or GND	2.3 V to 5.5 V		3	8	pF
C_{io}	SDA		V_{IO} = V_{CC} or GND	2.3 V to 5.5 V		3	9.5	pF
	P port					3.7	9.5	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.
(2) Each I/O must be externally limited to a maximum of 25 mA, and each octal (P07 – P00 and P17 – P10) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
(3) The total current sourced by all I/Os must be limited to 160 mA (80 mA for P07 – P00 and 80 mA for P17 – P10).

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

		MIN	MAX	UNIT
I²C BUS—STANDARD MODE				
f_{scl}	I²C clock frequency	0	100	kHz
t_{sch}	I²C clock high time	4		μs
t_{scl}	I²C clock low time	4.7		μs
t_{sp}	I²C spike time		50	ns
t_{sds}	I²C serial-data setup time	250		ns
t_{sdh}	I²C serial-data hold time	0		ns

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6.6 I²C Interface Timing Requirements (continued)

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

			MIN	MAX	UNIT
t_{icr}	I²C input rise time			1000	ns
t_{icf}	I²C input fall time			300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	ns
t_{buf}	I²C bus free time between stop and start		4.7		µs
t_{sts}	I²C start or repeated start condition setup		4.7		µs
t_{sth}	I²C start or repeated start condition hold		4		µs
t_{sps}	I²C stop condition setup		4		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45	µs
C_b (1)	I²C bus capacitive load			400	pF
I²C BUS—FAST MODE					
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		20	300	ns
t_{icf}	I²C input fall time		20 × (V_{CC} / 5.5 V)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus	20 × (V_{CC} / 5.5 V)	300	ns
t_{buf}	I²C bus free time between stop and start		1.3		µs
t_{sts}	I²C start or repeated start condition setup		0.6		µs
t_{sth}	I²C start or repeated start condition hold		0.6		µs
t_{sps}	I²C stop condition setup		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.9	µs
C_b (1)	I²C bus capacitive load			400	pF

(1) C_b = total capacitance of one bus line in pF.

6.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leqslant 100$ pF (unless otherwise noted) (see 图 7-1 and 图 7-2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4	µs
t_{pv}	Output data valid	SCL	P port		200	ns
t_{ps}	Input data setup time	P port	SCL	150		ns
t_{ph}	Input data hold time	P port	SCL	1		µs

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6.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

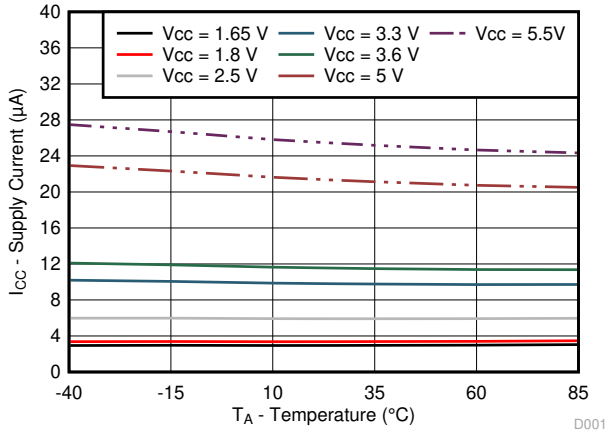


图 6-1. Supply Current vs Temperature for Different Supply Voltage (V_{CC})

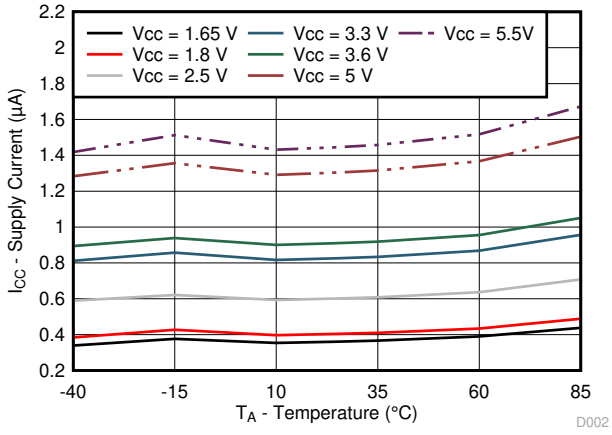


图 6-2. Standby Supply Current vs Temperature for Different Supply Voltage (V_{CC})

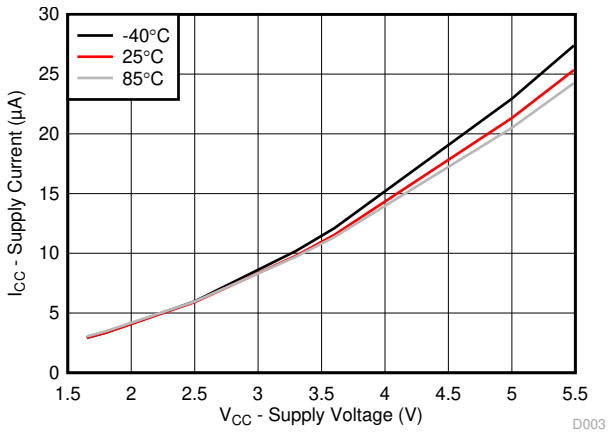


图 6-3. Supply Current vs Supply Voltage for Different Temperature (T_A)

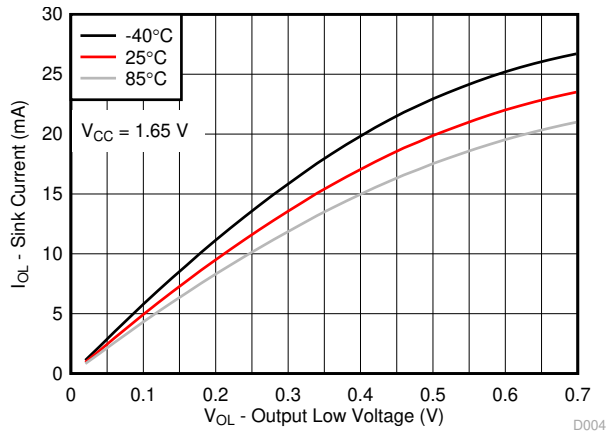


图 6-4. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.65 V

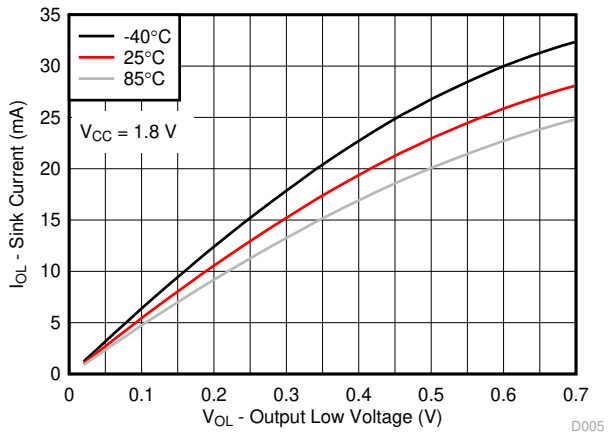


图 6-5. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.8 V

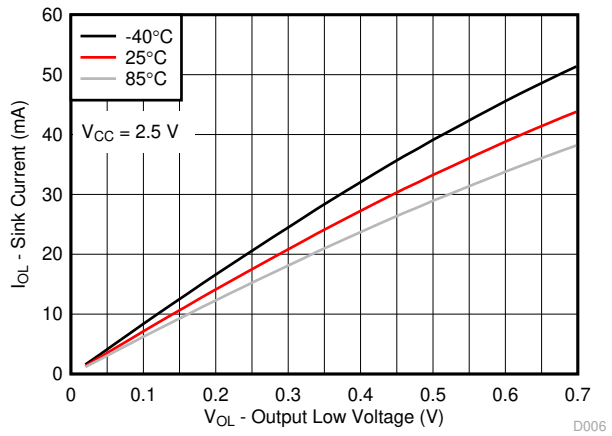


图 6-6. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 2.5 V

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6.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

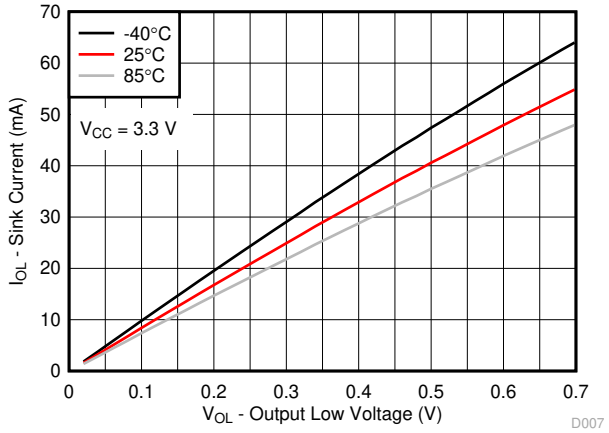


图 6-7. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 3.3 V

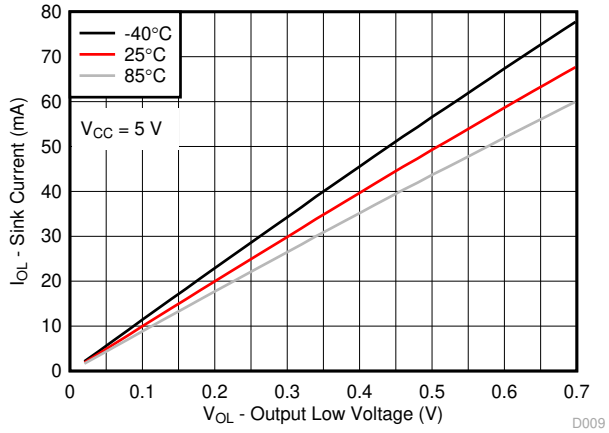


图 6-8. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 5 V

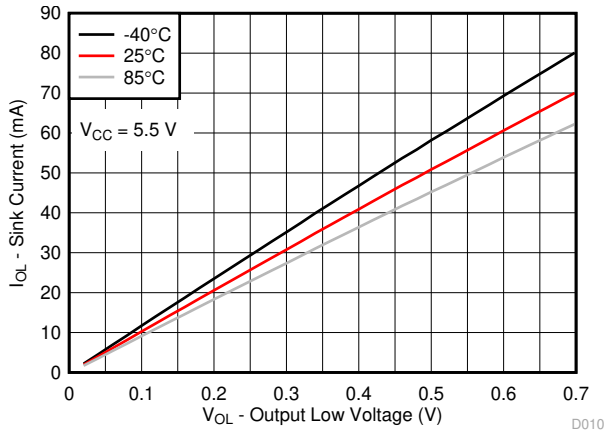


图 6-9. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 5.5 V

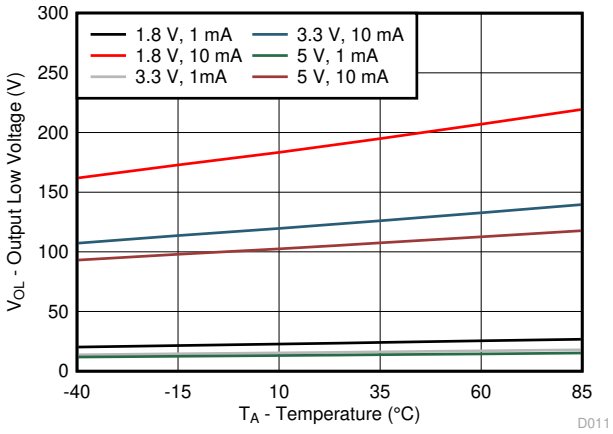


图 6-10. I/O Low Voltage vs Temperature for Different V_{CC} and I_{OL}

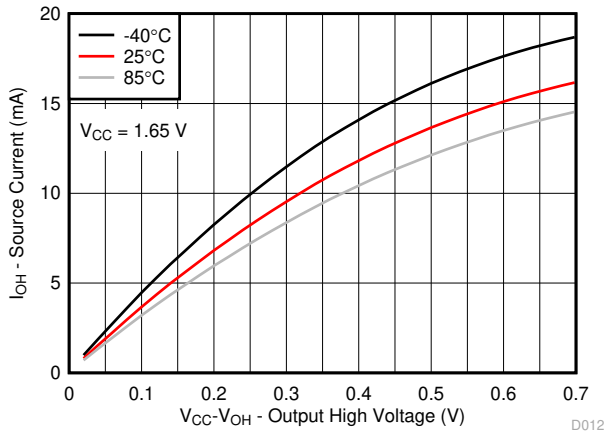


图 6-11. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.65 V

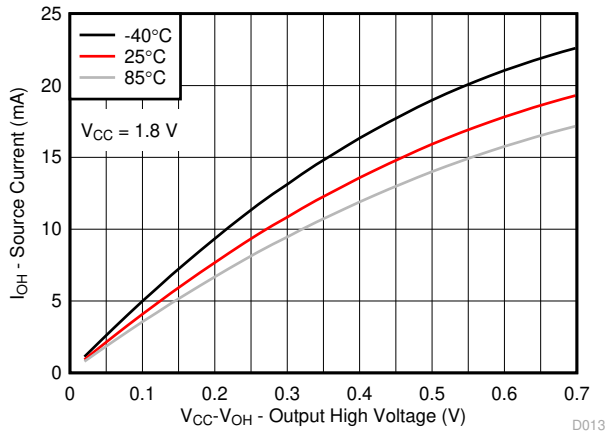


图 6-12. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.8 V

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6.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

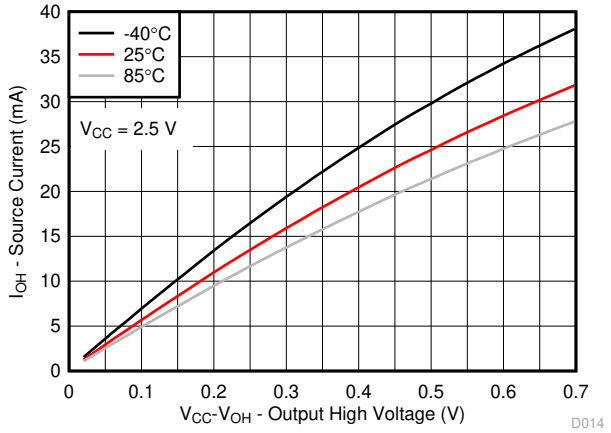


图 6-13. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 2.5 V

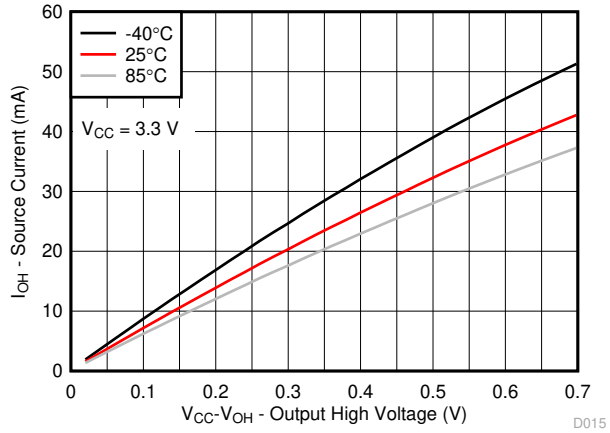


图 6-14. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 3.3 V

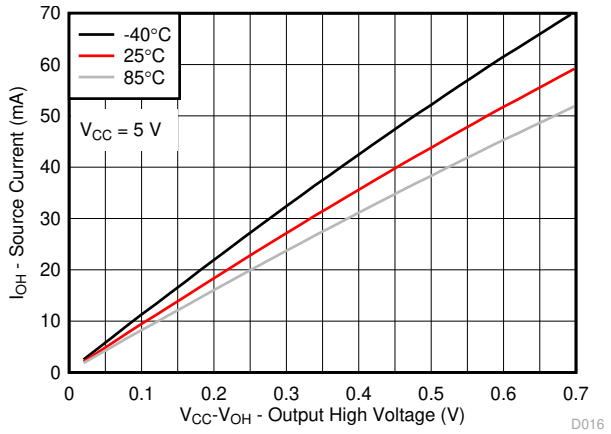


图 6-15. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 5 V

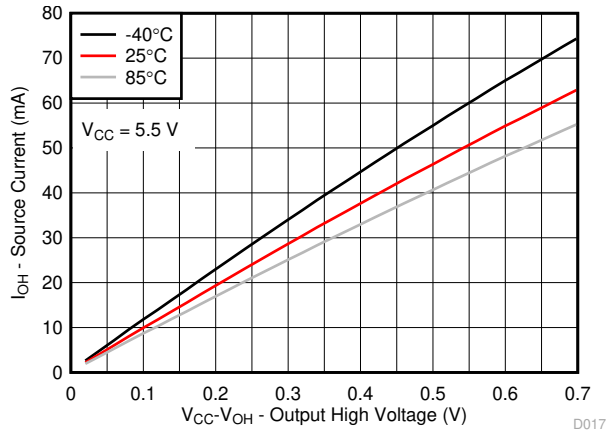


图 6-16. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 5.5 V

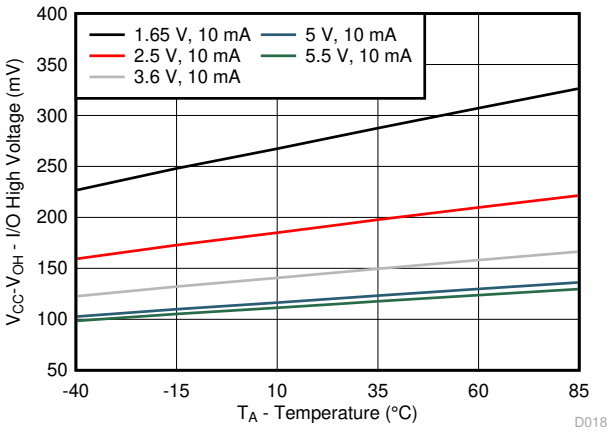


图 6-17. V_{CC} – V_{OH} Voltage vs Temperature for Different V_{CC}

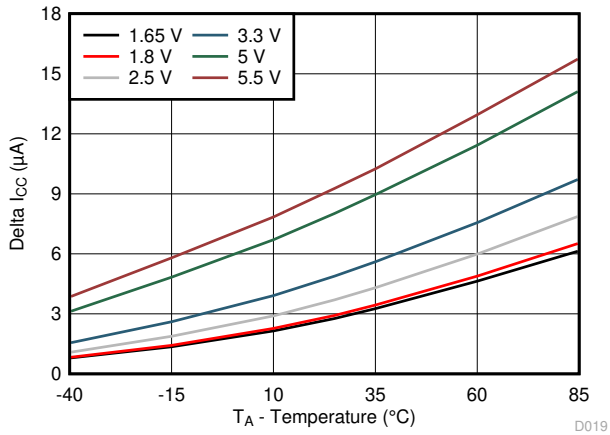
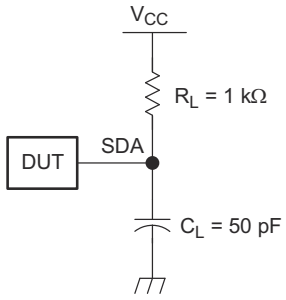


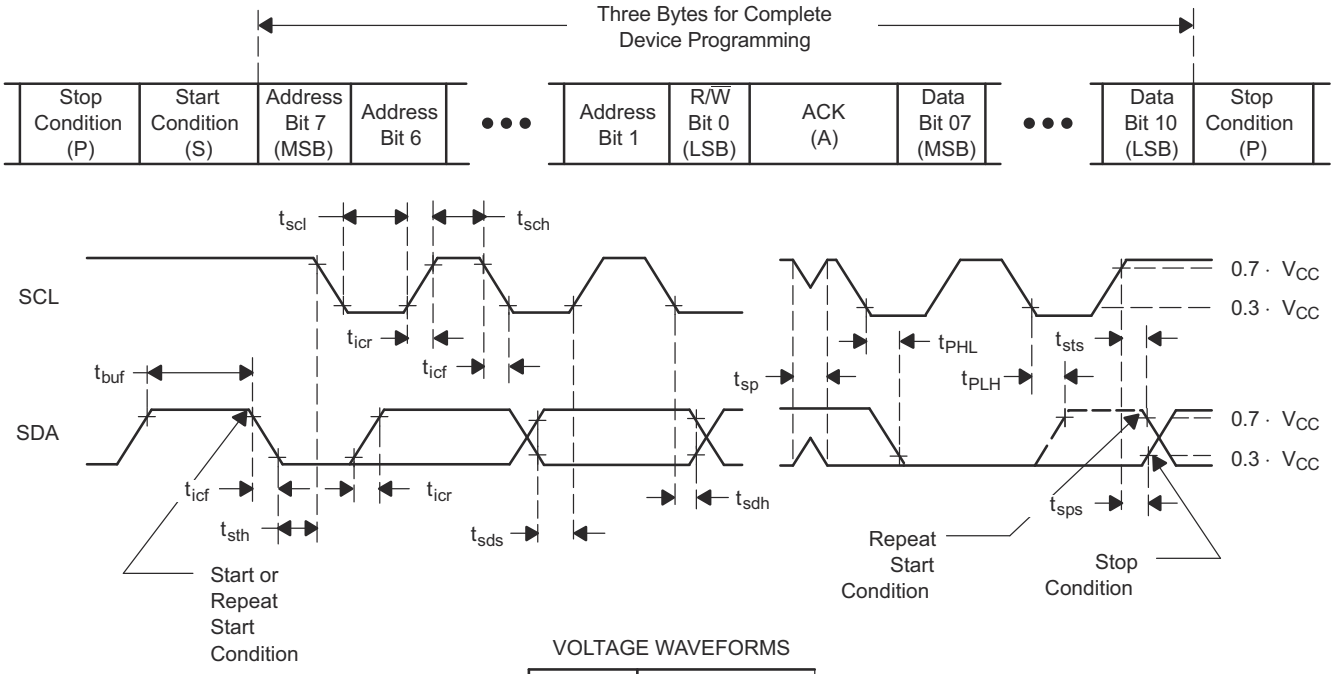
图 6-18. Δ I_{CC} vs Temperature for Different V_{CC} (V_I = V_{CC} – 0.6 V)

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7 Parameter Measurement Information



SDA LOAD CONFIGURA TION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I²C address
2, 3	P-port data

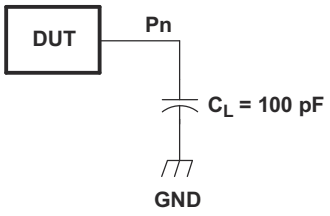
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ⩽ 10 MHz, Z_O = 50 Ω, t_r/t_f ⩽ 30 ns.

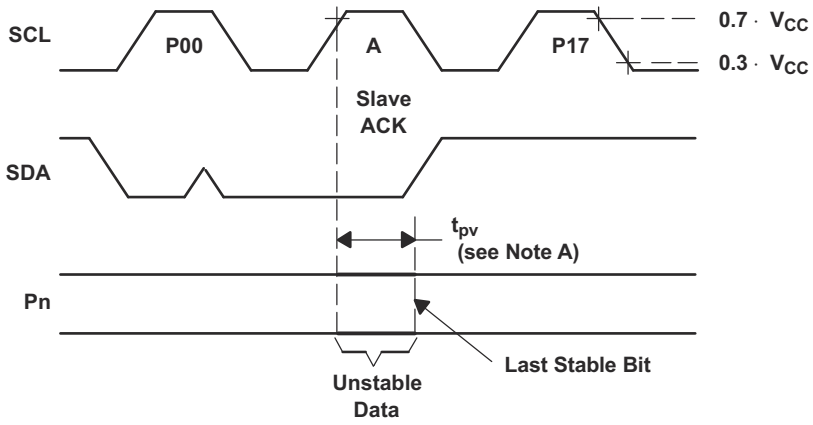
C. All parameters and waveforms are not applicable to all devices.

图 7-1. I²C Interface Load Circuit And Voltage Waveforms

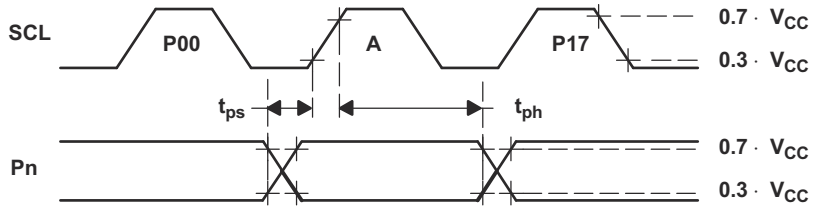
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P-PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)



READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.
B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ⩽ 10 MHz, Z_O = 50 Ω, t_r/t_f ⩽ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

图 7-2. P-Port Load Circuit And Voltage Waveforms

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8 Detailed Description

8.1 Overview

The system master can reset the PCA9555 in the event of a timeout or other improper operation by utilizing the power-on reset feature, which puts the registers in their default state and initializes the I^2C/SMBus state machine.

The PCA9555 open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{INT}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the PCA9555 can remain a simple slave device.

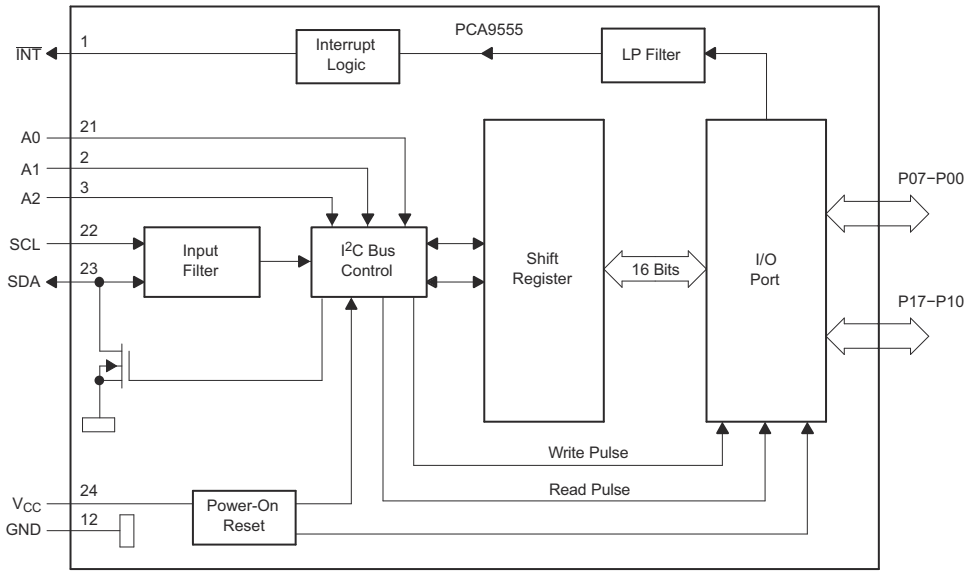
The device outputs (latched) have high-current drive capability for directly driving LEDs.

Although pin-to-pin and I^2C-address is compatible with the PCF8575, software changes are required due to the enhancements.

The PCA9555 is identical to the PCA9535, except for the inclusion of the internal I/O pullup resistor, which pulls the I/O to a default high when configured as an input and undriven.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I^2C address and allow up to eight devices to share the same I^2C bus or SMBus. The fixed I^2C address of the PCA9555 is the same as the PCF8575, PCF8575C, and PCF8574, allowing up to eight of these devices in any combination to share the same I^2C bus or SMBus.

8.2 Functional Block Diagram

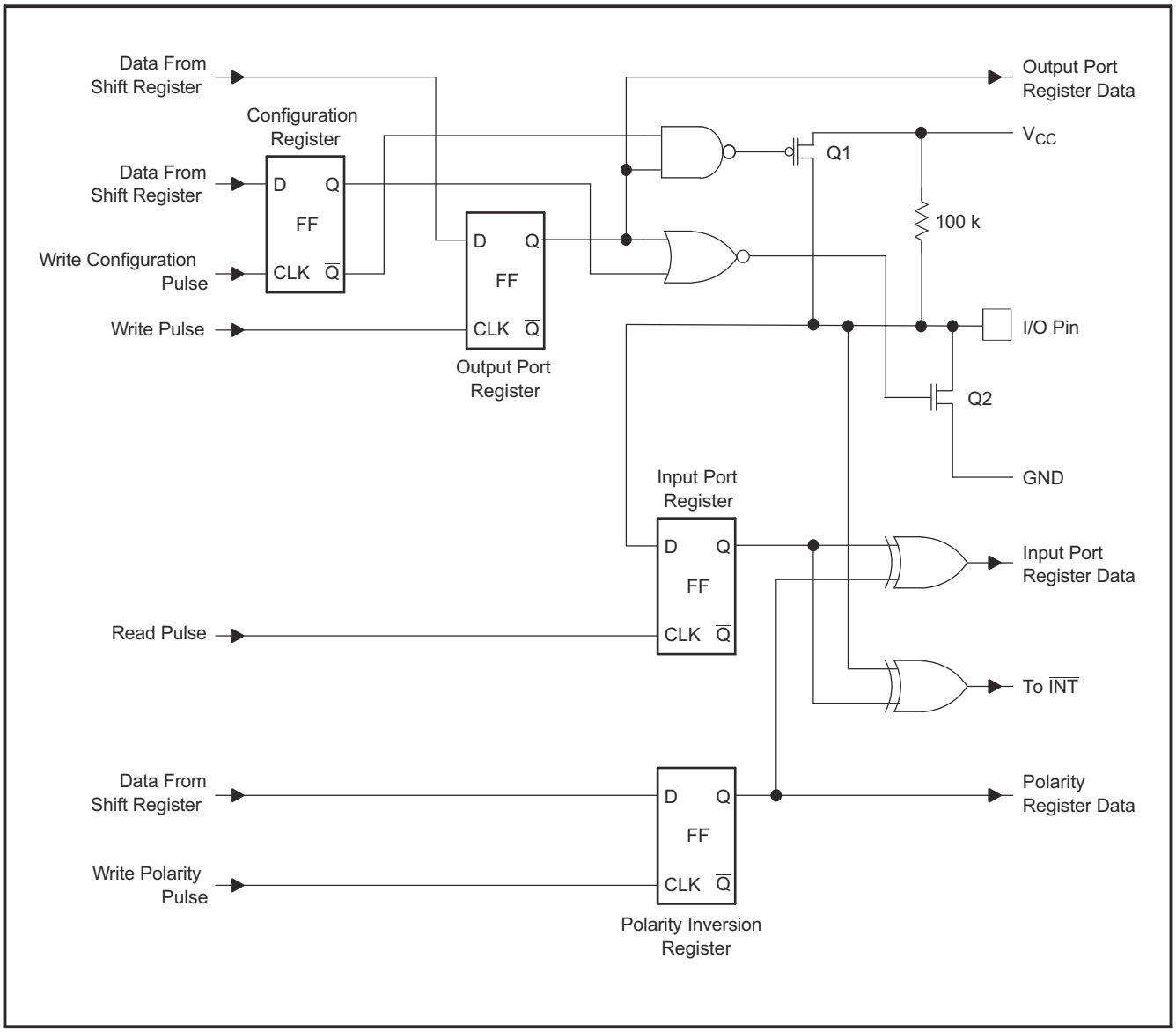


A. Pin numbers shown are for DB, DBQ, DGV, DW, and PW packages.

B. All I/Os are set to inputs at reset.

图 8-1. Logic Diagram

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A. At power-on reset, all registers return to default values.

图 8-2. Simplified Schematic Of P-Port I/Os

8.3 Device Features

8.3.1 Power-On Reset (POR)

When power (from 0 V) is applied to V_{CC}, an internal power-on reset circuit holds the PCA9555 in a reset condition until V_{CC} has reached V_{POR}. At that time, the reset condition is released, and the PCA9555 registers and I^2C-SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle.

8.3.2 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 (in 图 8-2) are off, creating a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output Port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

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8.4 Device Functional Modes

8.4.1 Interrupt ($\overline{INT}$) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$. Writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register. Because each 8-pin port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1 or vice versa.

The $\overline{INT}$ output has an open-drain structure and requires pullup resistor to V_{CC}.

8.4.1.1 Interrupt Errata

8.4.1.1.1 INT Description

The INT will be improperly de-asserted if the following two conditions occur:

1. The last I^2C command byte (register pointer) written to the device was 00h.

Note

This generally means the last operation with the device was a Read of the input register. However, the command byte may have been written with 00h without ever going on to read the input register. After reading from the device, if no other command byte written, it will remain 00h.

2. Any other slave device on the I^2C bus acknowledges an address byte with the R/W bit set high

8.4.1.1.2 System Impact

Can cause improper interrupt handling as the Master will see the interrupt as being cleared.

8.4.1.1.3 System Workaround

Minor software change: User must change command byte to something besides 00h after a Read operation to the PCA9555 device or before reading from another slave device.

Note

Software change will be compatible with other versions (competition and TI redesigns) of this device.

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8.5 Programming

8.5.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see 图 8-3). After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address.

After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0 – A2) of the slave device must not be changed between the Start and Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see 图 8-4).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see 图 8-3).

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see 图 8-5). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

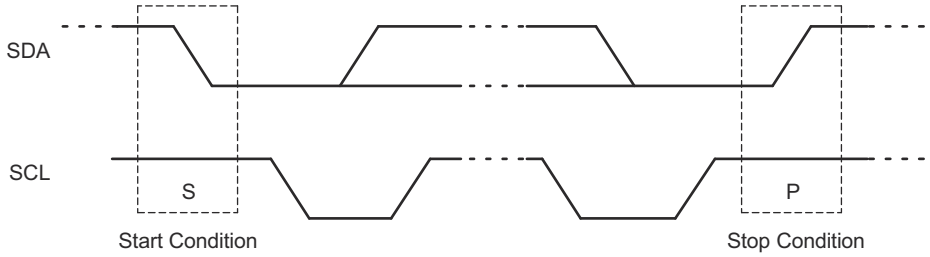


图 8-3. Definition Of Start And Stop Conditions

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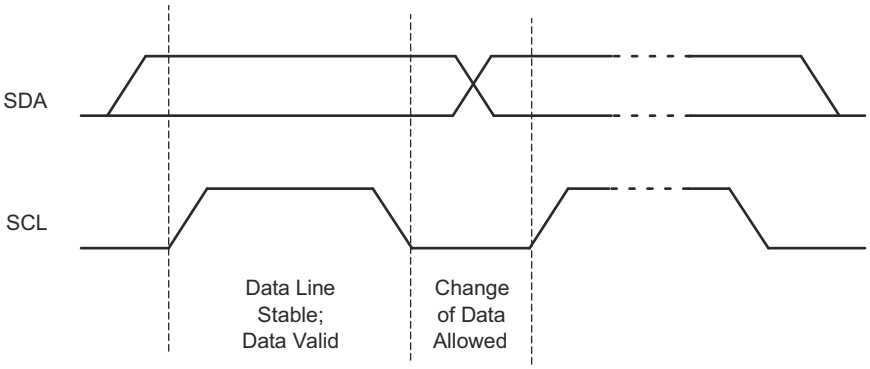


图 8-4. Bit Transfer

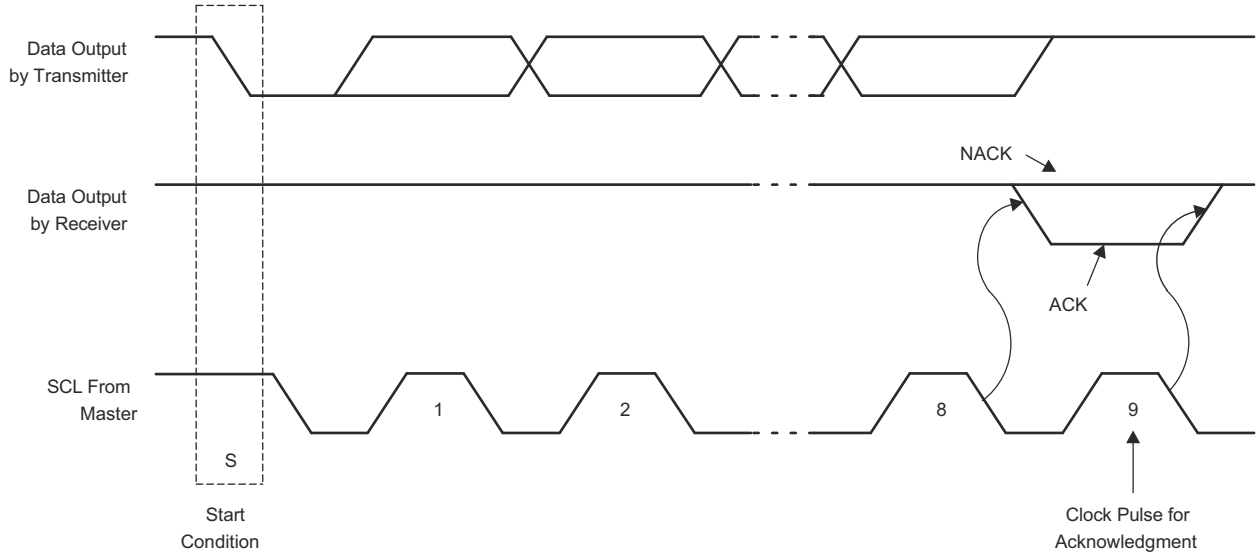


图 8-5. Acknowledgment On I²C Bus

8.5.2 Register Map

表 8-1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	L	H	L	L	A2	A1	A0	R/ $\overline{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

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8.5.2.1 Device Address

图 8-6 shows the address byte of the PCA9555.

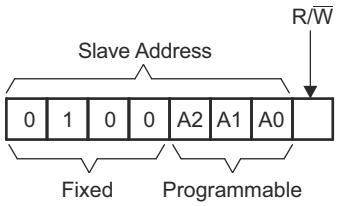


图 8-6. PCA9555 Address

表 8-2. Address Reference

INPUTS			I²C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 20 (hexadecimal)
L	L	H	33 (decimal), 21 (hexadecimal)
L	H	L	34 (decimal), 22 (hexadecimal)
L	H	H	35 (decimal), 23 (hexadecimal)
H	L	L	36 (decimal), 24 (hexadecimal)
H	L	H	37 (decimal), 25 (hexadecimal)
H	H	L	38 (decimal), 26 (hexadecimal)
H	H	H	39 (decimal), 27 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

8.5.2.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9555. Three bits of this data byte state the operation (read or write) and the internal register (input, output, polarity inversion, or configuration) that will be affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

图 8-7. Control Register Bits

7	6	5	4	3	2	1	0
0	0	0	0	0	B2	B1	B0

表 8-3. Command Byte

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
0	0	0	0x00	Input Port 0	Read byte	xxxx xxxx
0	0	1	0x01	Input Port 1	Read byte	xxxx xxxx
0	1	0	0x02	Output Port 0	Read/write byte	1111 1111
0	1	1	0x03	Output Port 1	Read/write byte	1111 1111
1	0	0	0x04	Polarity Inversion Port 0	Read/write byte	0000 0000
1	0	1	0x05	Polarity Inversion Port 1	Read/write byte	0000 0000
1	1	0	0x06	Configuration Port 0	Read/write byte	1111 1111
1	1	1	0x07	Configuration Port 1	Read/write byte	1111 1111

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8.5.2.3 Register Descriptions

The Input Port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the I^2C device that the Input Port register will be accessed next.

表 8-4. Registers 0 And 1 (Input Port Registers)

Bit	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X
Bit	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

The Output Port registers (registers 2 and 3) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

表 8-5. Registers 2 And 3 (Output Port Registers)

Bit	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1
Bit	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

The Polarity Inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained.

表 8-6. Registers 4 And 5 (Polarity Inversion Registers)

Bit	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0
Bit	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

The Configuration registers (registers 6 and 7) configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

表 8-7. Registers 6 And 7 (Configuration Registers)

Bit	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1
Bit	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

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8.5.2.4 Bus Transactions

Data is exchanged between the master and the PCA9555 through write and read commands.

8.5.2.4.1 Writes

Data is transmitted to the PCA9555 by sending the device address and setting the least-significant bit to a logic 0 (see 图 8-6 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte.

The eight registers within the PCA9555 are configured to operate as four register pairs. The four pairs are input ports, output ports, polarity inversion ports, and configuration ports. After sending data to one register, the next data byte is sent to the other register in the pair (see 图 8-8 and 图 8-9). For example, if the first byte is sent to output port (register 3), the next byte is stored in Output Port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

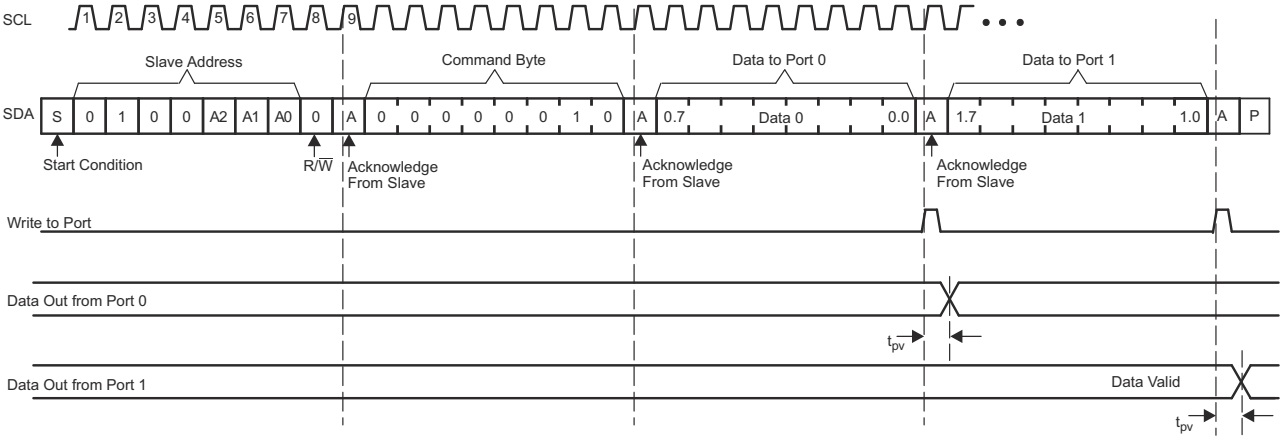


图 8-8. Write To Output Port Registers

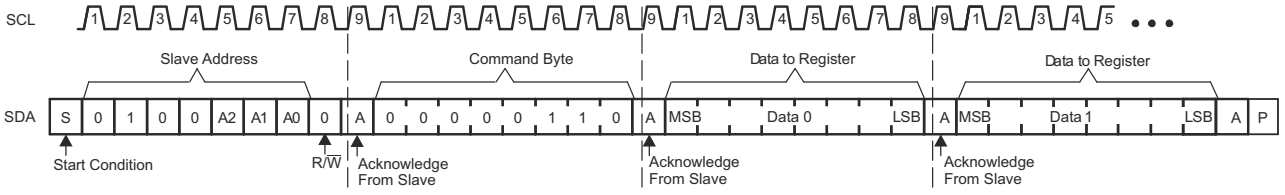


图 8-9. Write To Configuration Registers

8.5.2.4.2 Reads

The bus master first must send the PCA9555 address with the least-significant bit set to a logic 0 (see 图 8-6 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again, but this time, the least-significant bit is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9555 (see 图 8-10 through 图 8-12).

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. For example, if the command byte references Input Port 1 before the restart, and the restart occurs when Input Port 0 is being read, the stored command byte changes to reference Input Port 0. The original command byte is forgotten. If a subsequent restart occurs, Input Port 0 is read first. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.

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Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

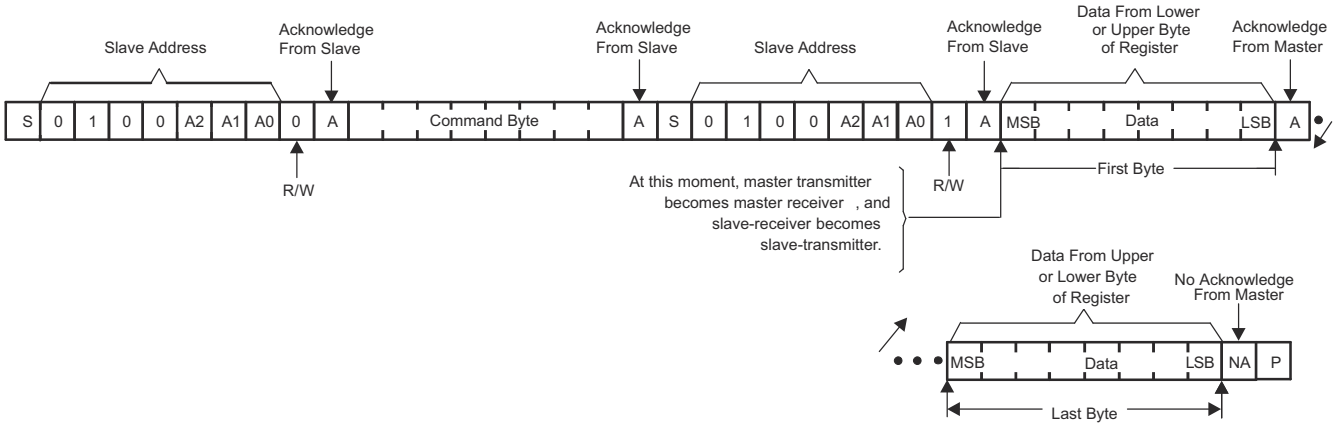
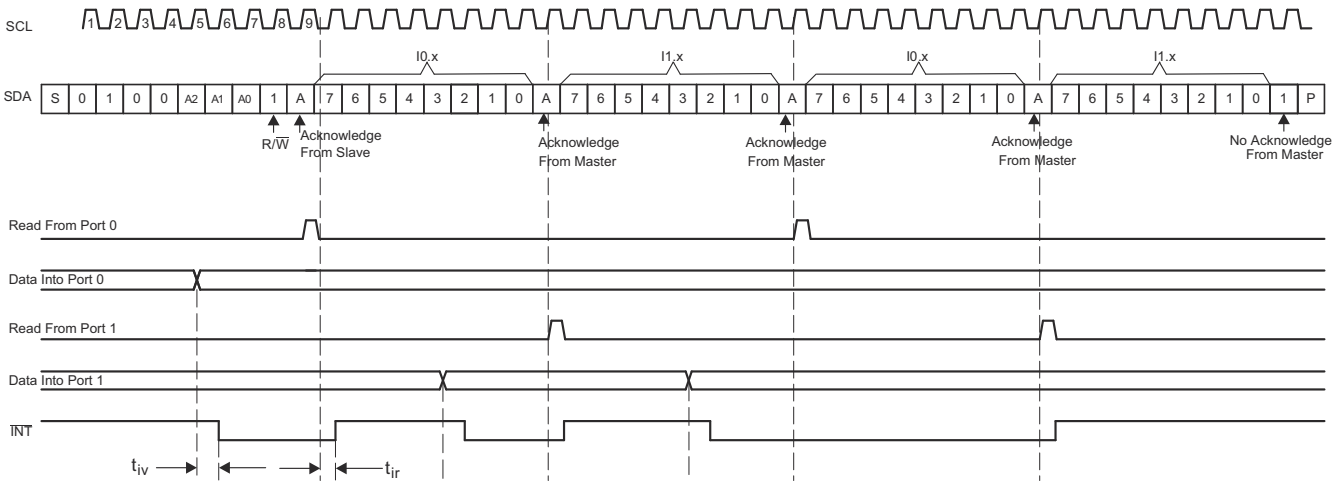


图 8-10. Read From Register

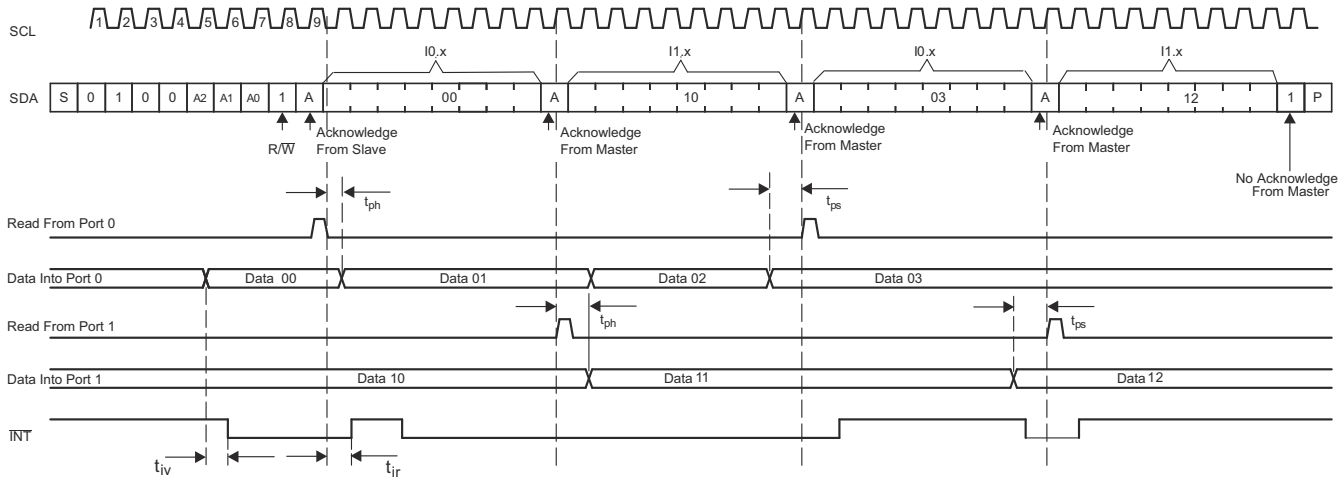


A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see 图 8-10 for these details).

图 8-11. Read Input Port Register, Scenario 1

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A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see 图 8-10 for these details).

图 8-12. Read Input Port Register, Scenario 2

9 Application Information Disclaimer

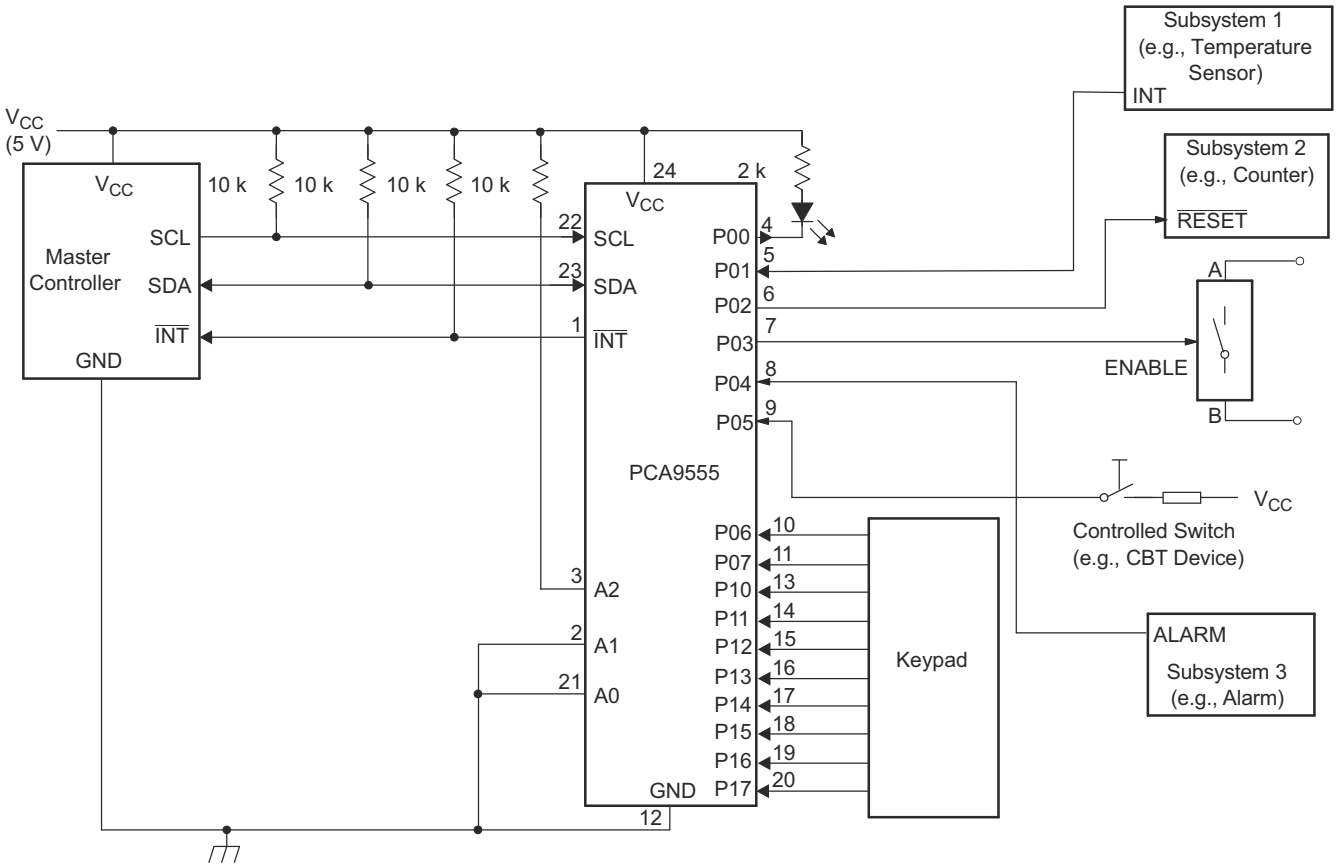
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Typical Application

图 9-1 shows an application in which the PCA9555 can be used.



A. Device address is configured as 0100100 for this example.
B. P00, P02, and P03 are configured as outputs.
C. P01, P04 – P07, and P10 – P17 are configured as inputs.
D. Pin numbers shown are for DB, DBQ, DGV, DW, and PW packages.

图 9-1. Typical Application

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9.1.1.1 Design Requirements

For this design example, use the parameters shown in 表 9-1.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
I^2C and Subsystem Voltage (V_{CC})	5 V
Output current rating, P-port sinking (I_{OL})	25 mA
I^2C bus clock (SCL) speed	400 kHz

9.1.1.2 Design Requirements

9.1.1.2.1 Minimizing I_{CC} When I/O Is Used To Control Led

When an I/O is used to control an LED, normally it is connected to V_{CC} through a resistor as shown in 图 9-1. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in Electrical Characteristics shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}. For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC} when the LED is off to minimize current consumption.

图 9-2 shows a high-value resistor in parallel with the LED. 图 9-3 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply current consumption when the LED is off.

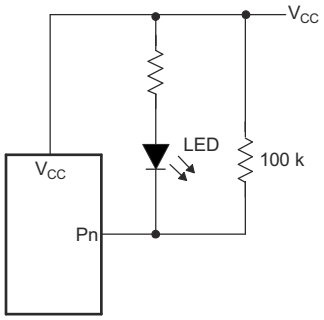


图 9-2. High-Value Resistor In Parallel With Led

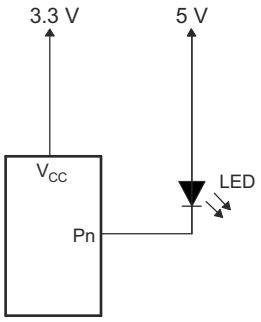
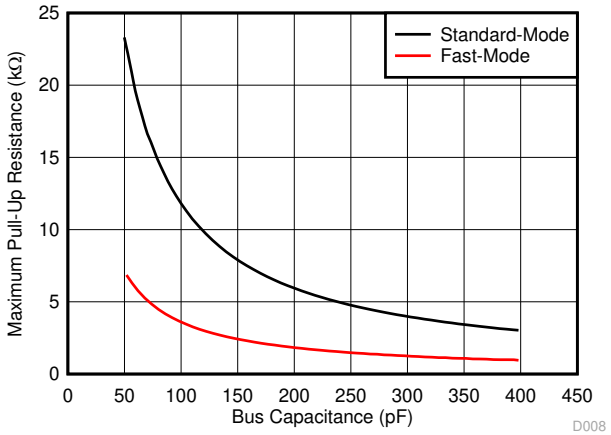


图 9-3. Device Supplied By Lower Voltage

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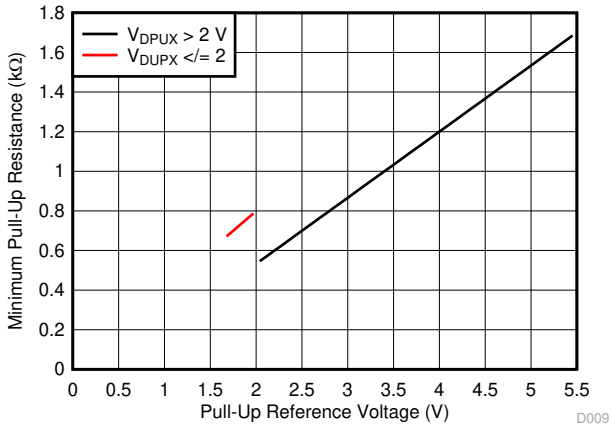
9.1.1.3 Application Curves



Standard-mode: f_{SCL} = 100 kHz, t_r = 1 µs

Fast-mode: f_{SCL} = 400 kHz, t_r = 300 ns

图 9-4. Maximum Pull-Up Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2 × V_{CC}, I_{OL} = 2 mA when V_{CC} ≤ 2 V

V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{CC} > 2 V

图 9-5. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-up Reference Voltage (V_{CC})

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10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCA9555 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in 图 10-1 and 图 10-2.

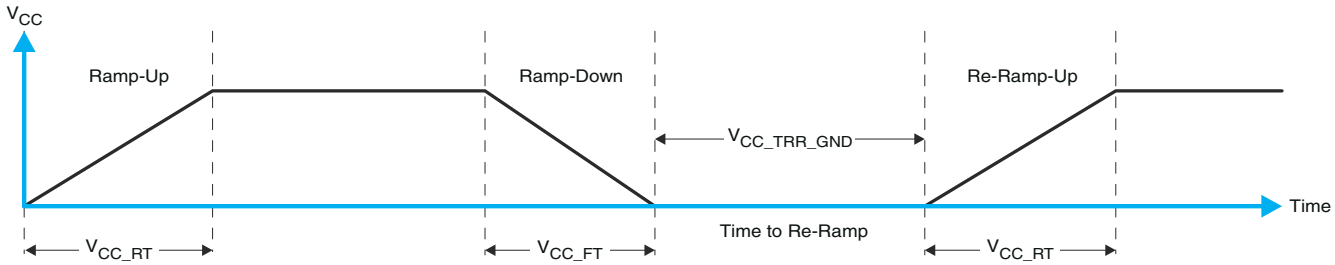


图 10-1. V_{CC} Is Lowered Below 0.2 V Or 0 V And Then Ramped Up To V_{CC}

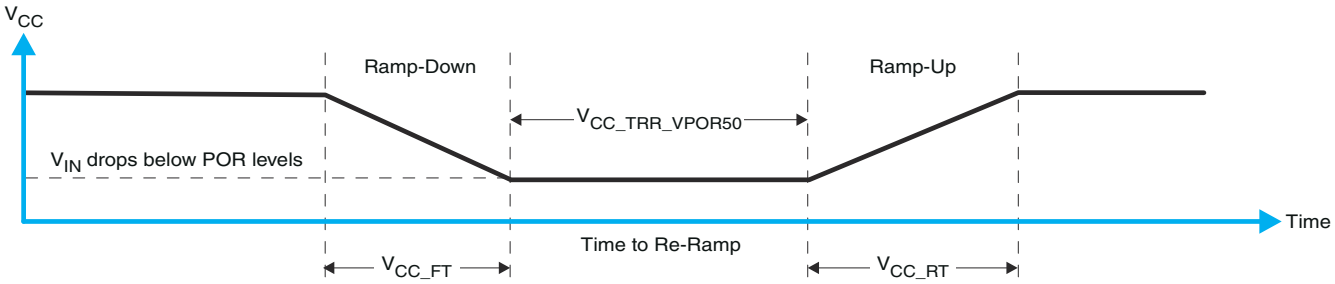


图 10-2. V_{CC} Is Lowered Below The Por Threshold, Then Ramped Back Up To V_{CC}

表 10-1 specifies the performance of the power-on reset feature for PCA9555 for both types of power-on reset.

表 10-1. Recommended Supply Sequencing And Ramp Rates(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See 图 10-1	1		100	ms
V_{CC_RT}	Rise rate	See 图 10-1	0.01		100	ms
$V_{CC_TRR_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See 图 10-1	0.001			ms
$V_{CC_TRR_POR50}$	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	See 图 10-2	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 μs	See 图 10-3			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See 图 10-3				μs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.767		1.144	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}		1.033		1.428	V

(1) T_A = –40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and the device impedance are factors that affect power-on reset performance. 图 10-3 and 表 10-1 provide more information on how to measure these specifications.

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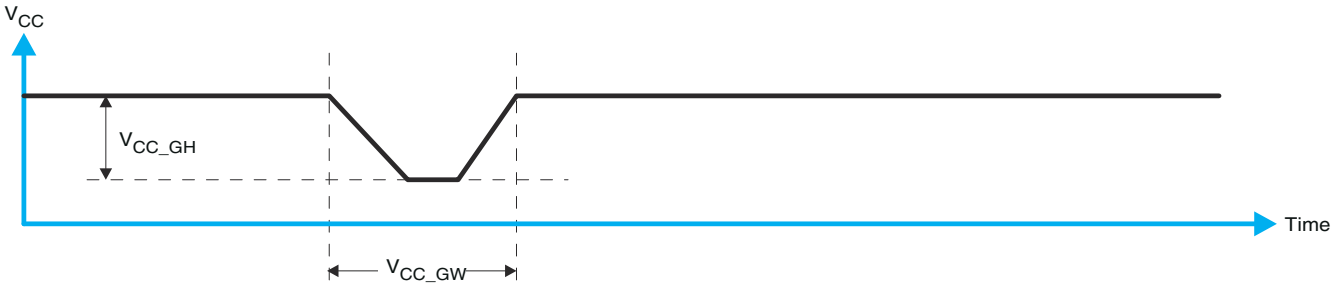


图 10-3. Glitch Width And Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. 图 10-4 and 表 10-1 provide more details on this specification.

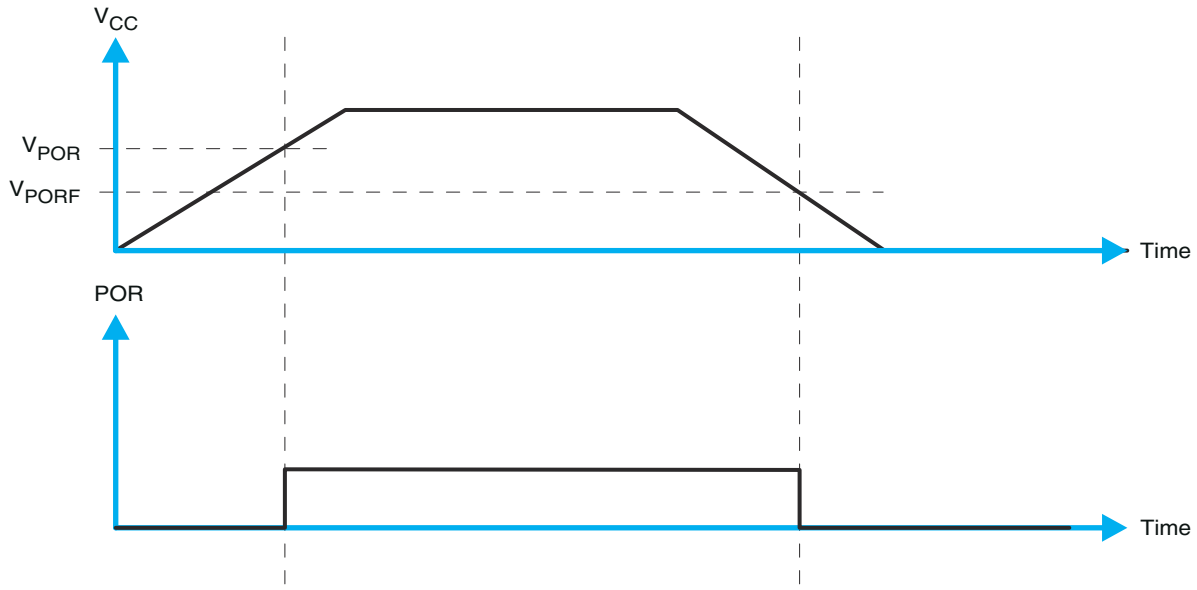


图 10-4. V_{POR}

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11 Layout

11.1 Layout Guidelines

For printed circuit board (PCB) layout of the PCA9555, common PCB layout practices must be followed, but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the V_{CC} pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors must be placed as close to the PCA9555 as possible. These best practices are shown in the 节 *11.2*.

For the layout example provided in the 节 *11.2*, it is possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V_{CC}, or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in the 节 *11.2*.

11.2 Layout Example

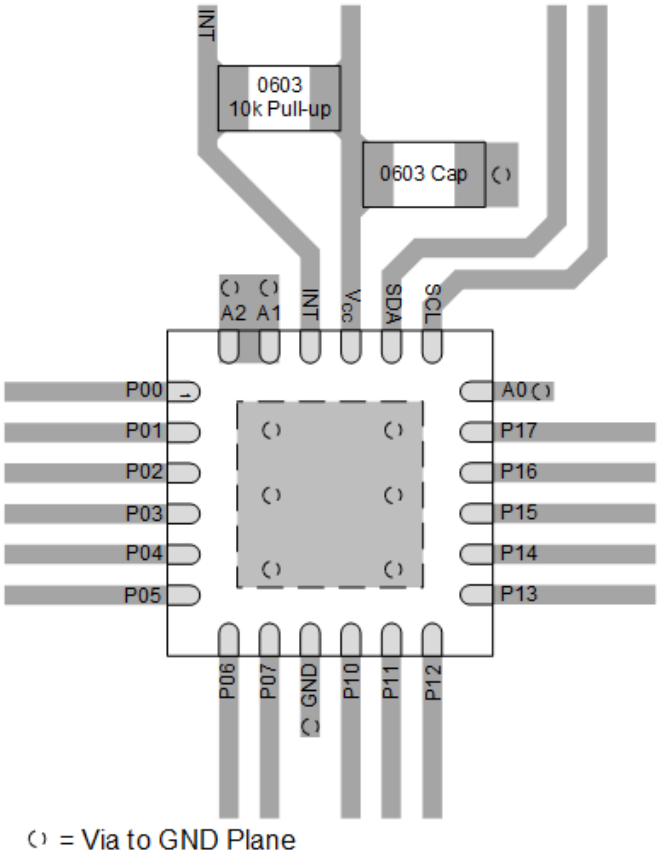


图 11-1. PCA9555 Example Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9555DB	LIFEBUY	SSOP	DB	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	
PCA9555DBQR	ACTIVE	SSOP	DBQ	24	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PCA9555	Samples
PCA9555DBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	Samples
PCA9555DGVR	ACTIVE	TVSOP	DGV	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	Samples
PCA9555DW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9555	Samples
PCA9555DWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9555	Samples
PCA9555DWRG4	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9555	Samples
PCA9555PW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	Samples
PCA9555PWE4	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	Samples
PCA9555PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	Samples
PCA9555PWRG4	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD9555	Samples
PCA9555RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD9555	Samples
PCA9555RGERG4	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD9555	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

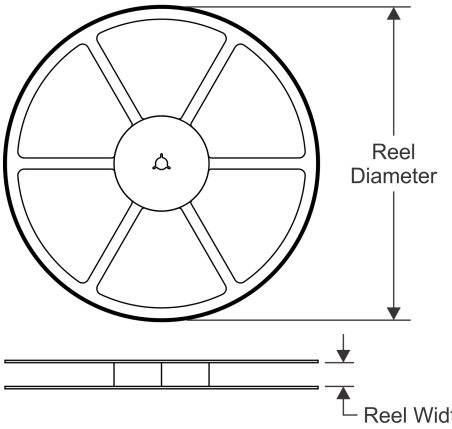
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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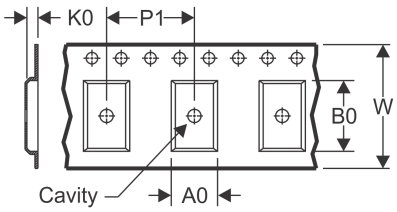
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

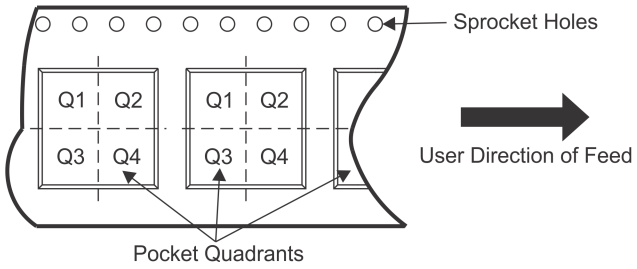


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

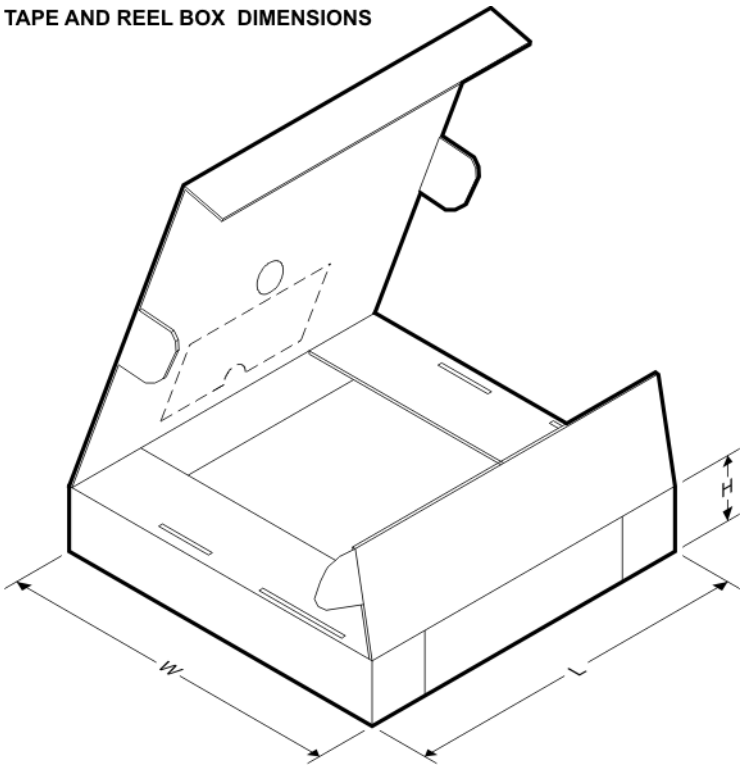
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9555DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
PCA9555DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
PCA9555DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9555DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
PCA9555PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCA9555PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCA9555RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
PCA9555RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

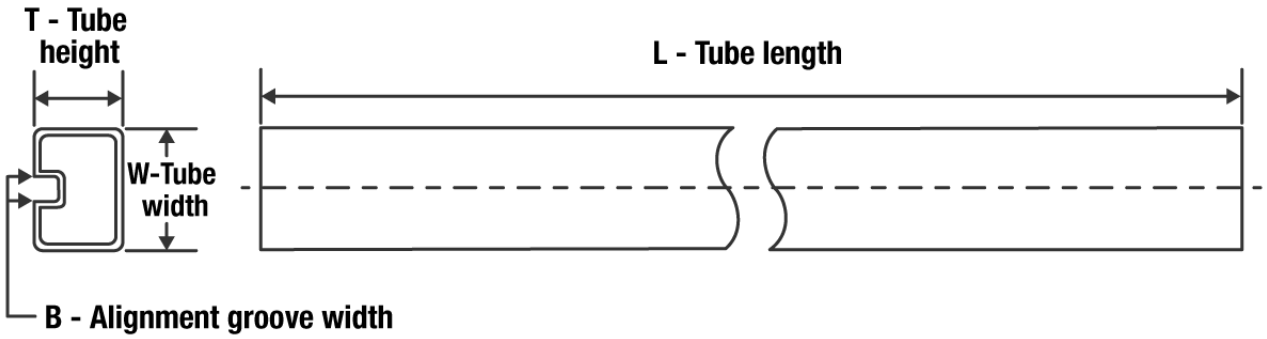
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9555DBQR	SSOP	DBQ	24	2500	853.0	449.0	35.0
PCA9555DBR	SSOP	DB	24	2000	853.0	449.0	35.0
PCA9555DGVR	TVSOP	DGV	24	2000	853.0	449.0	35.0
PCA9555DWR	SOIC	DW	24	2000	350.0	350.0	43.0
PCA9555PWR	TSSOP	PW	24	2000	367.0	367.0	38.0
PCA9555PWR	TSSOP	PW	24	2000	853.0	449.0	35.0
PCA9555RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
PCA9555RGER	VQFN	RGE	24	3000	853.0	449.0	35.0

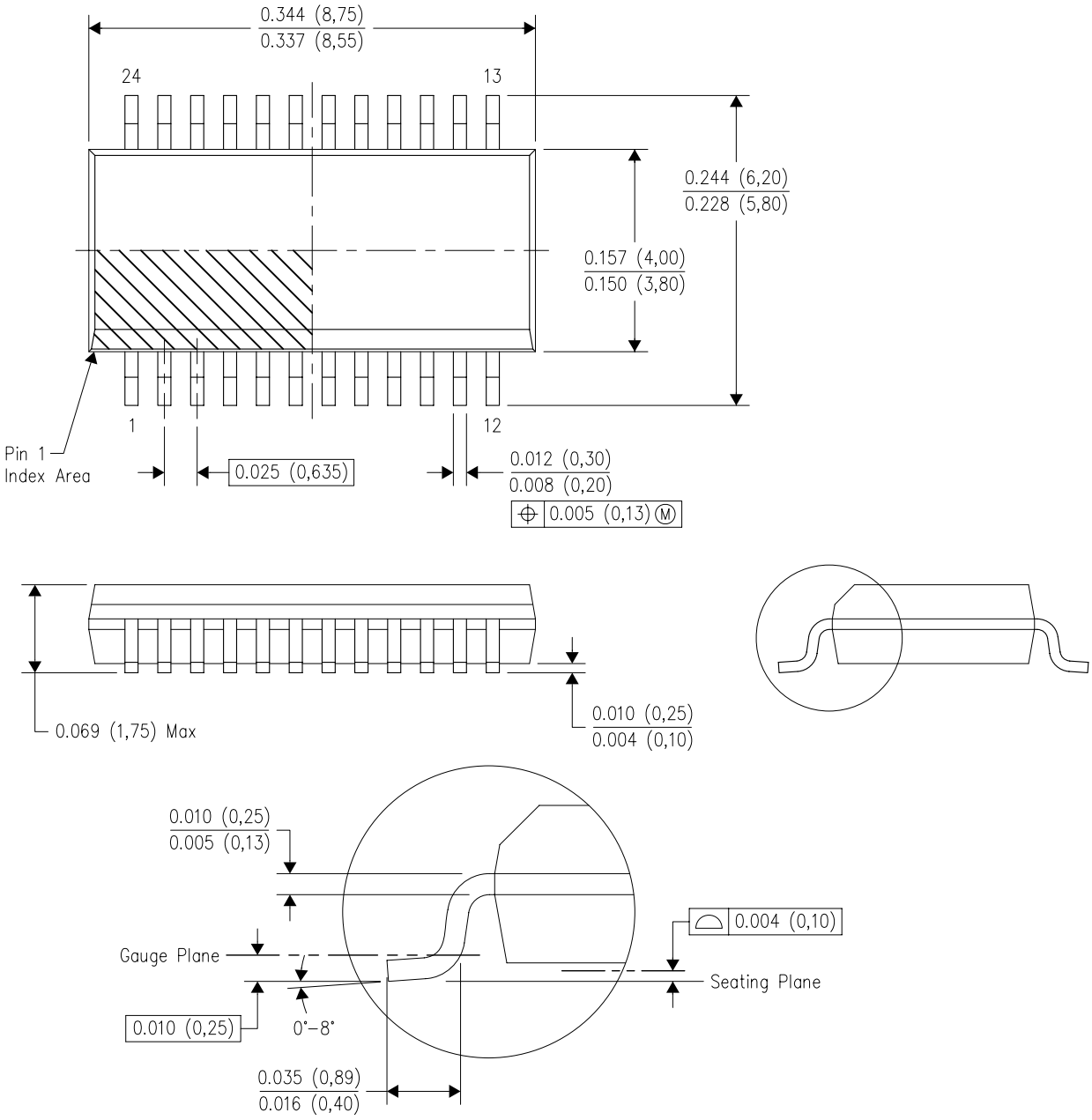
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCA9555DB	DB	SSOP	24	60	530	10.5	4000	4.1
PCA9555DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
PCA9555PW	PW	TSSOP	24	60	530	10.2	3600	3.5
PCA9555PWE4	PW	TSSOP	24	60	530	10.2	3600	3.5

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



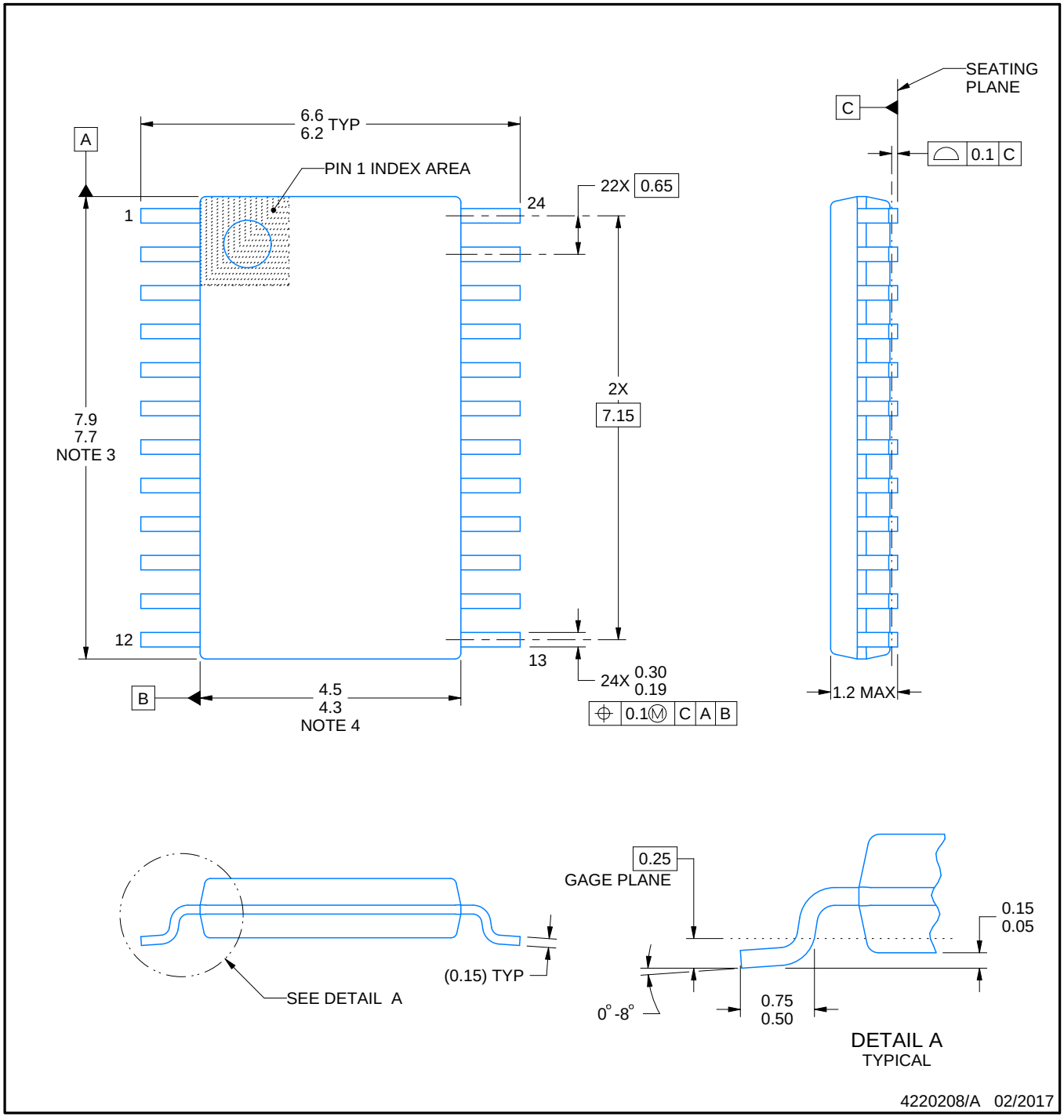
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

PACKAGE OUTLINE

PW0024A

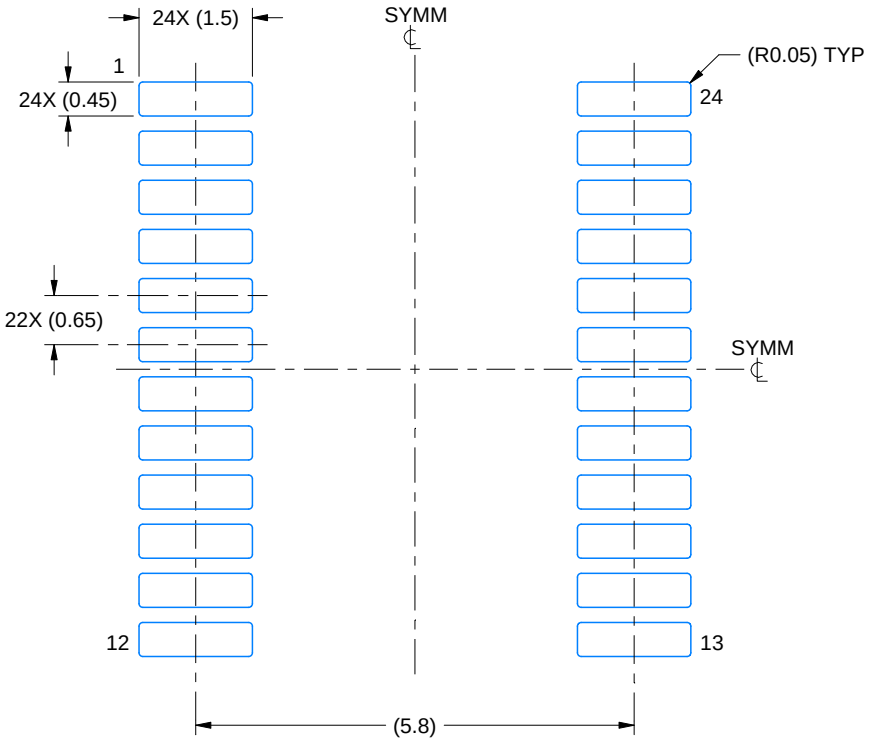
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

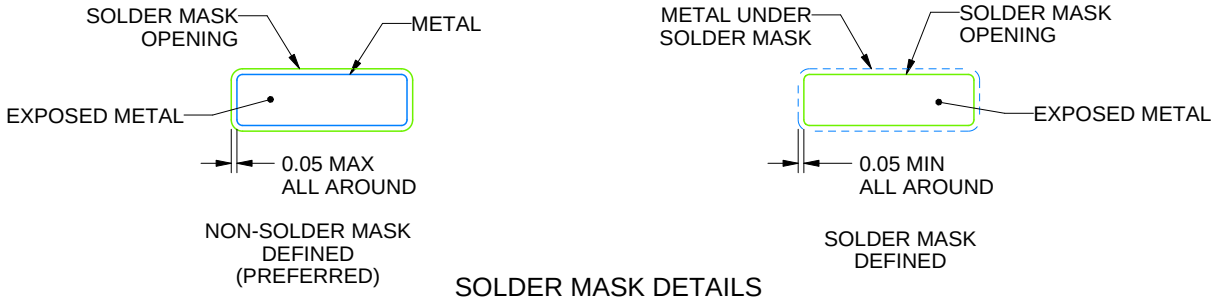


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

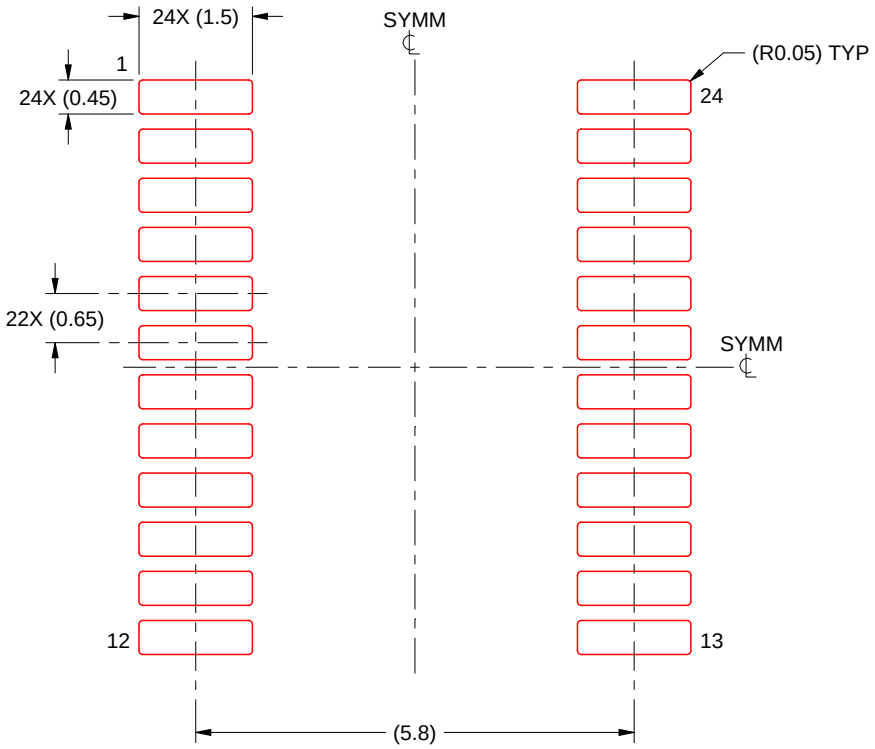


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



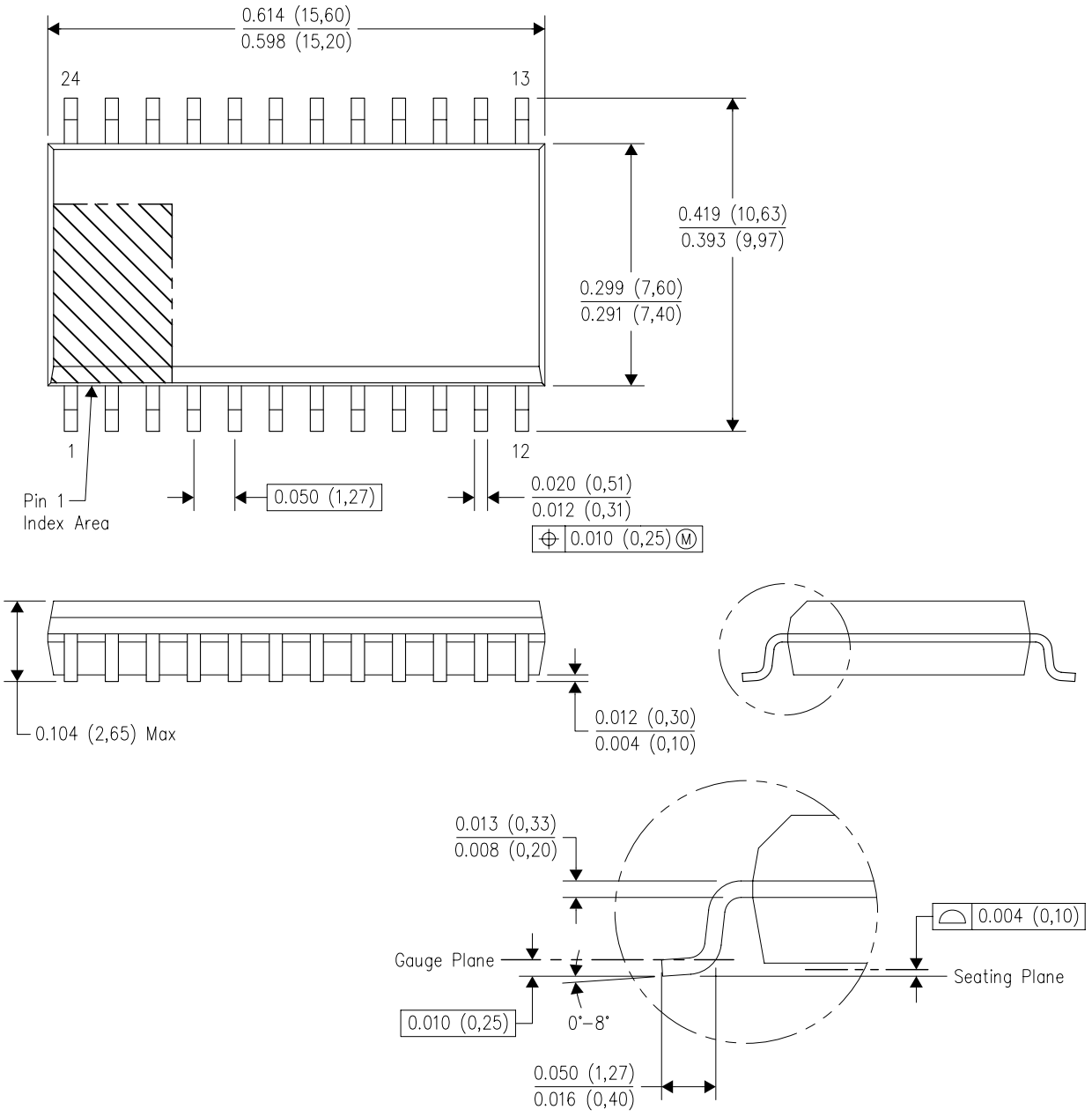
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE

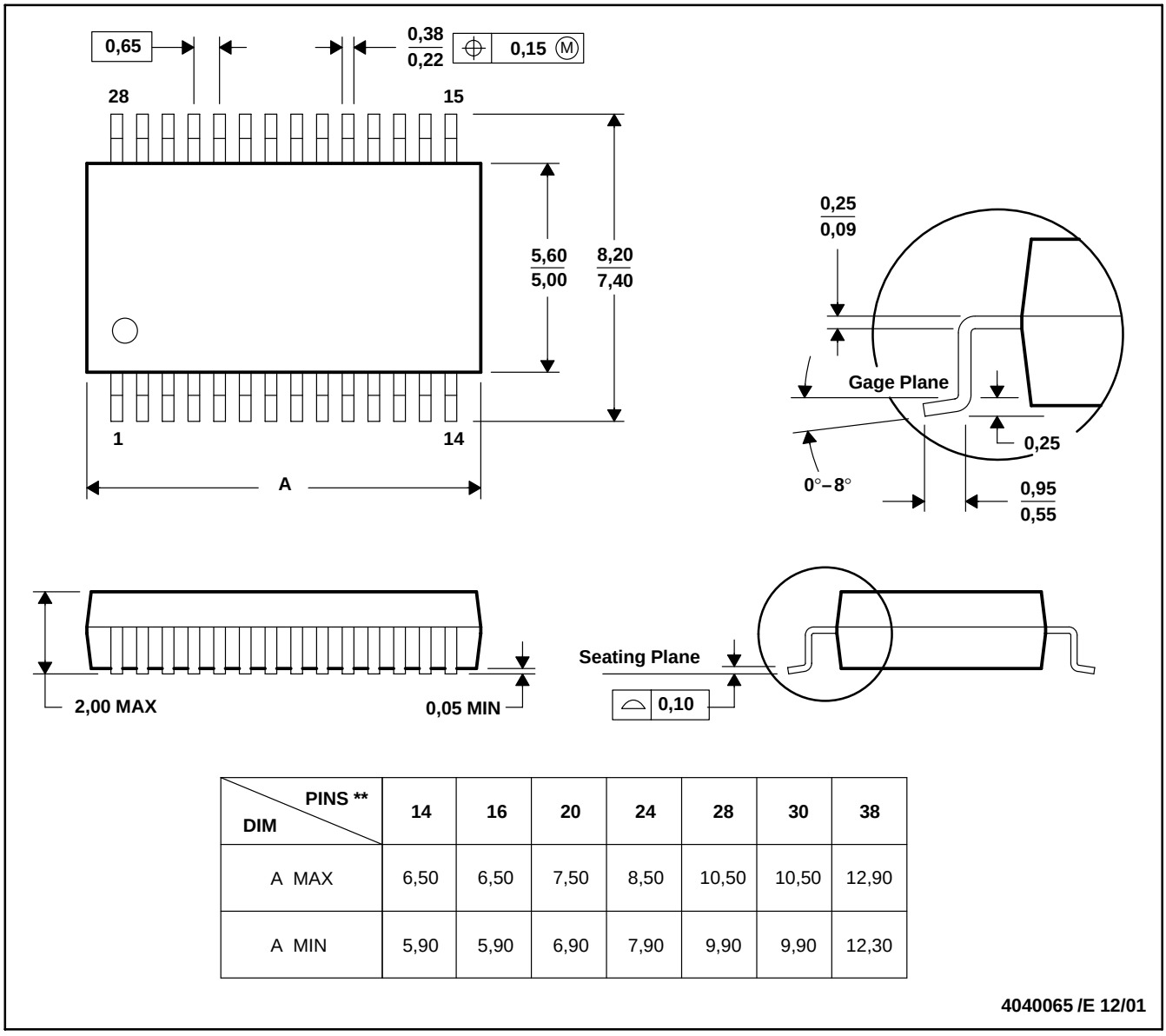


NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

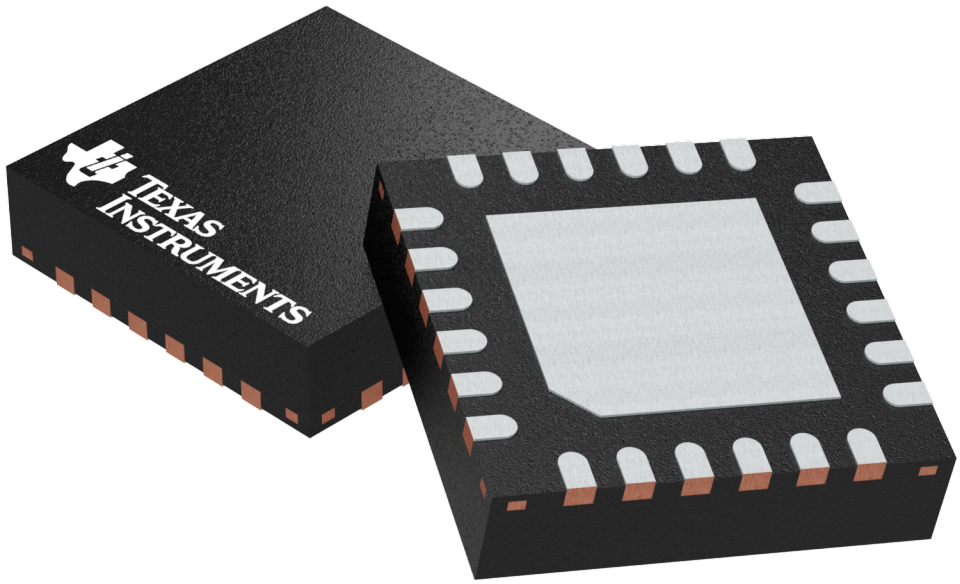
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

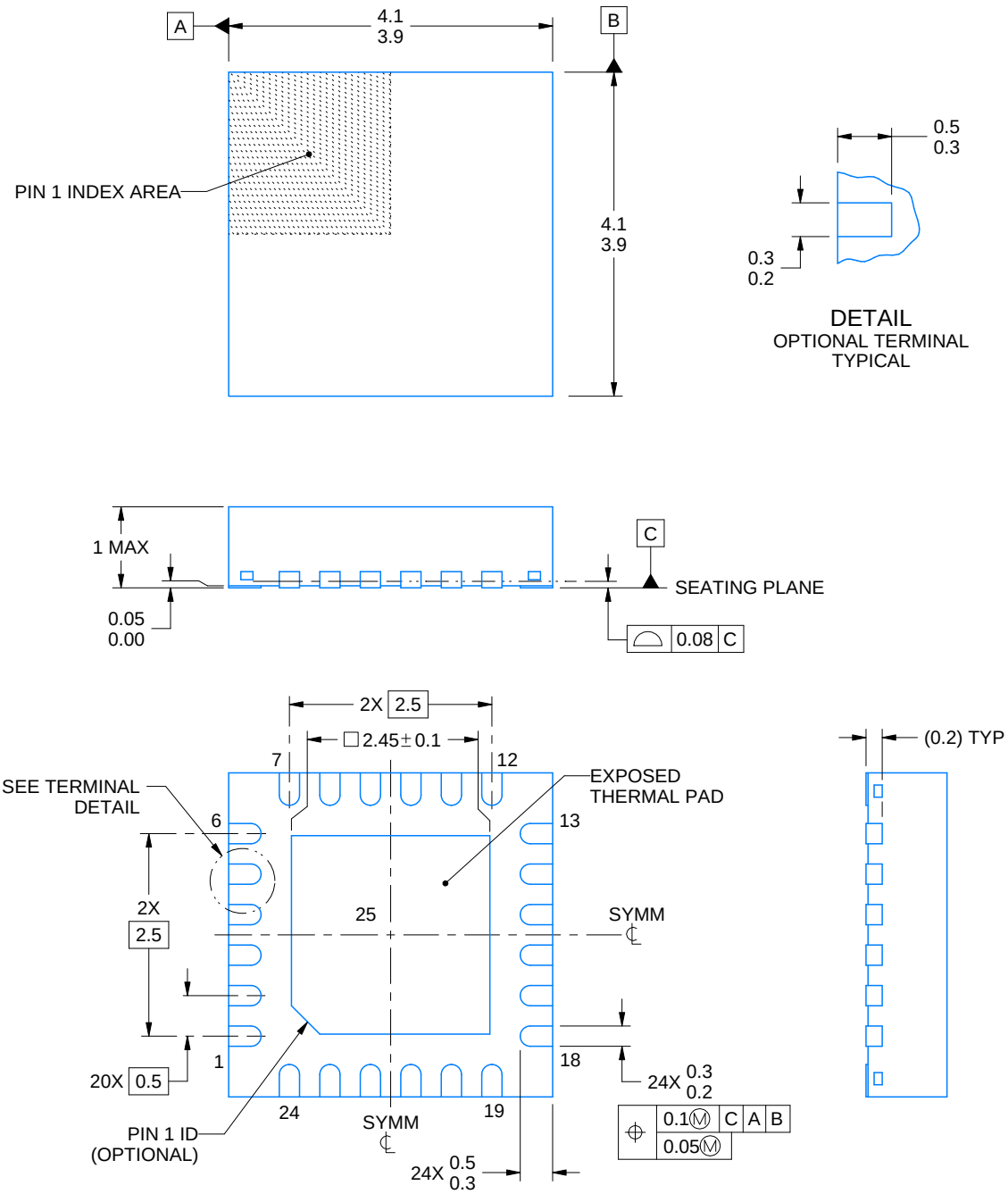
4204104/H

PACKAGE OUTLINE

RGE0024B

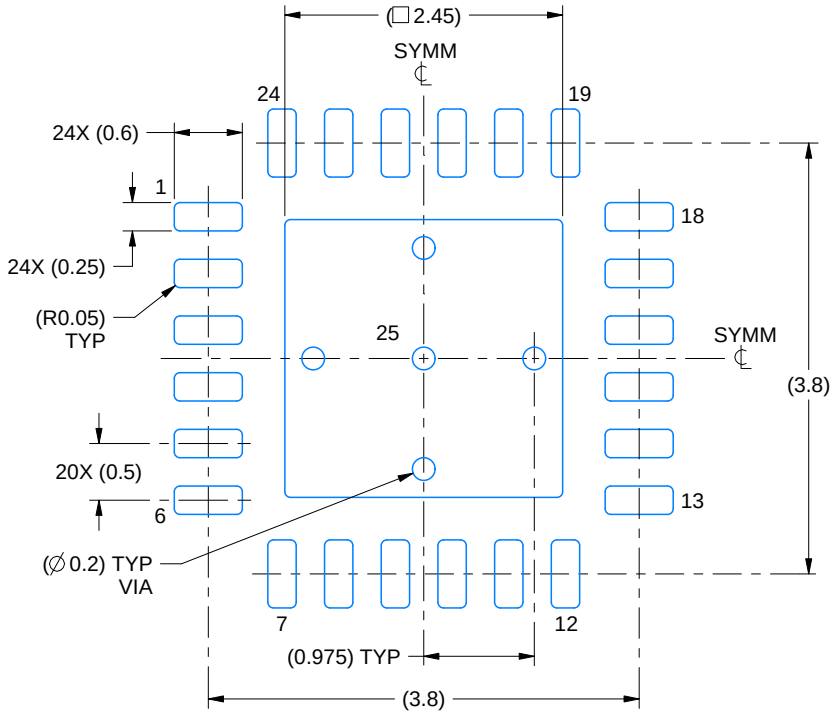
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

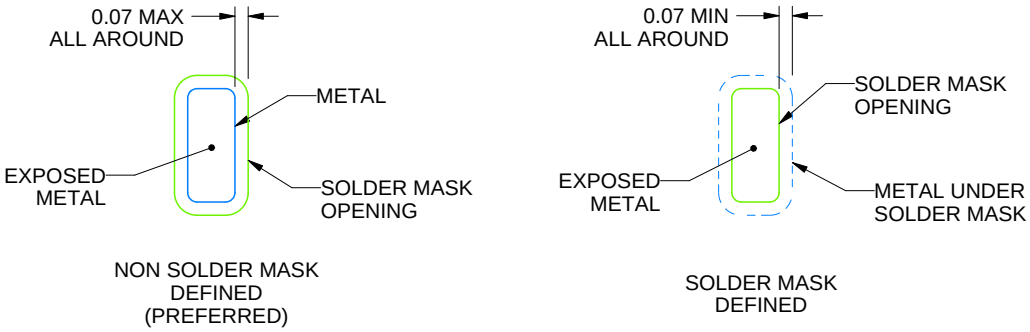


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

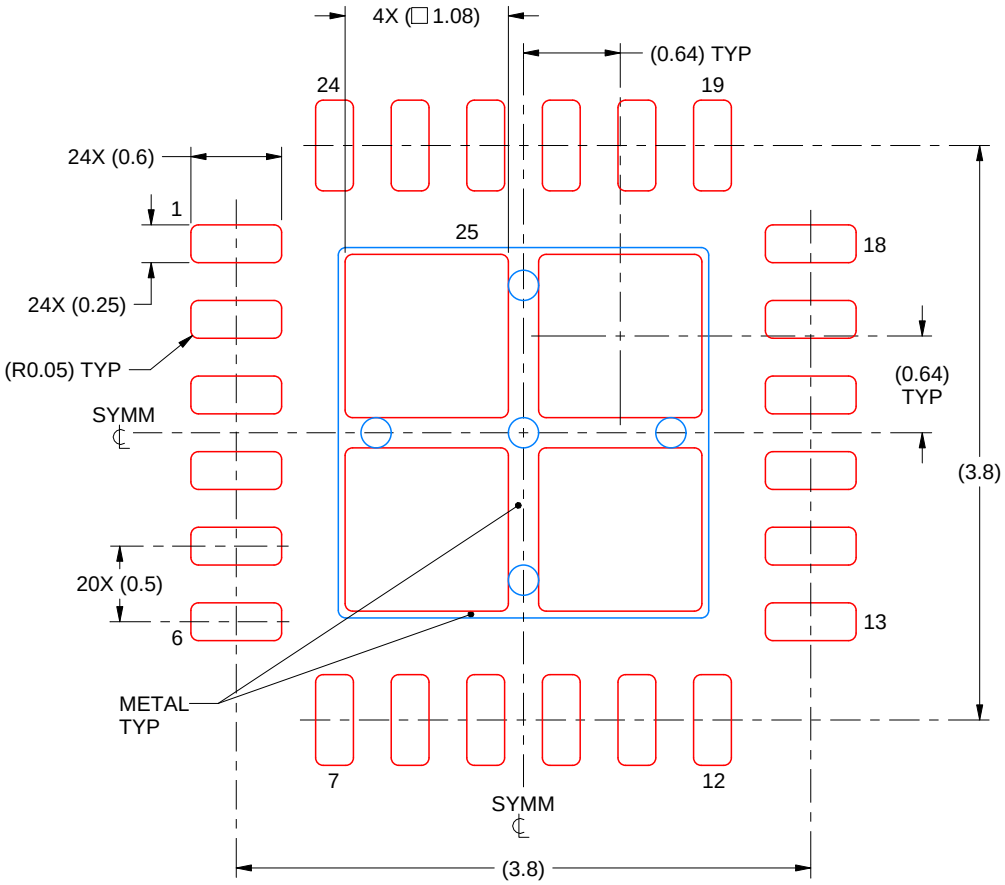


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

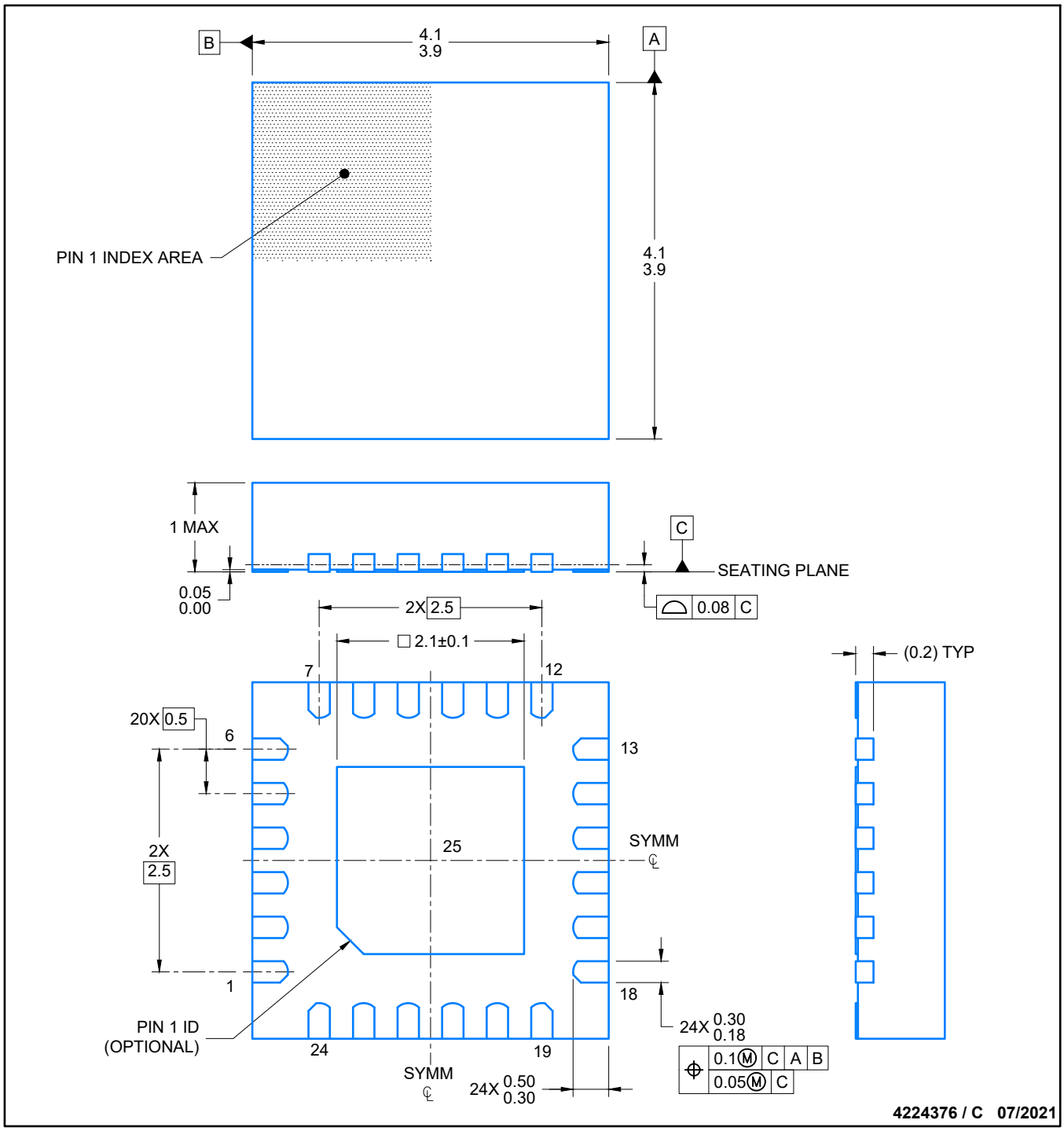
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RGE0024C

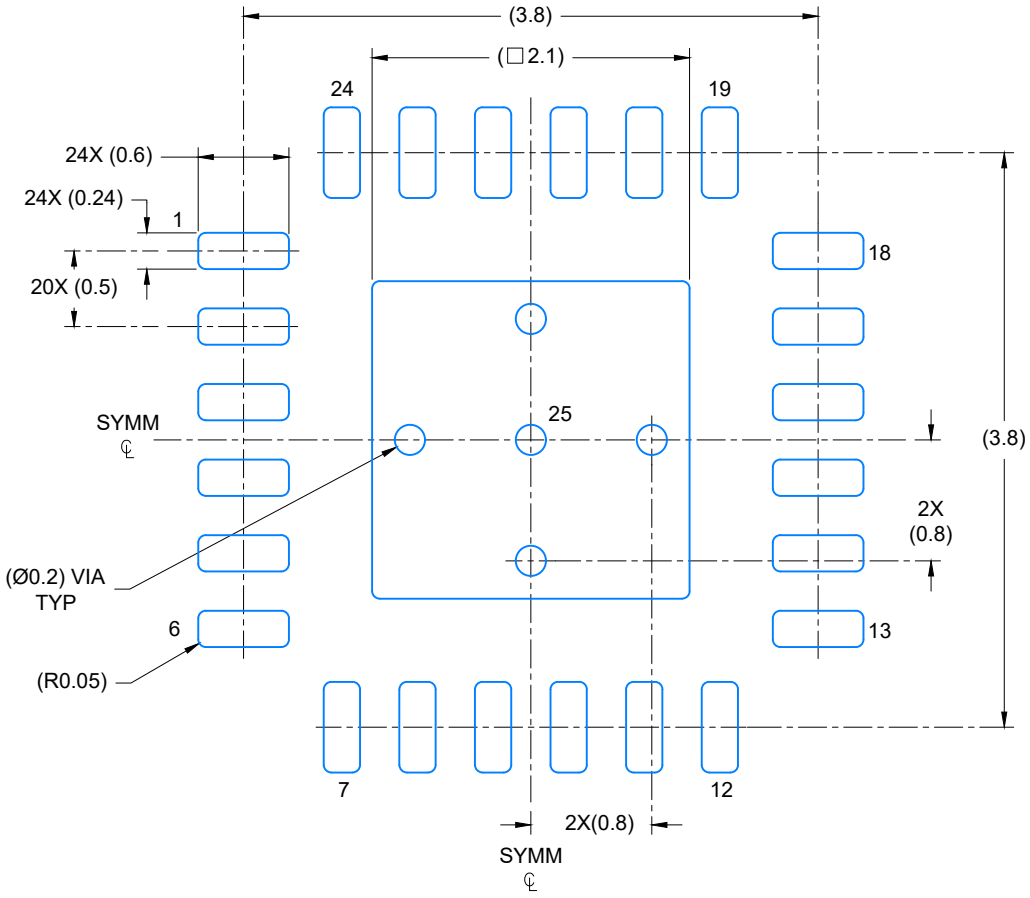
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



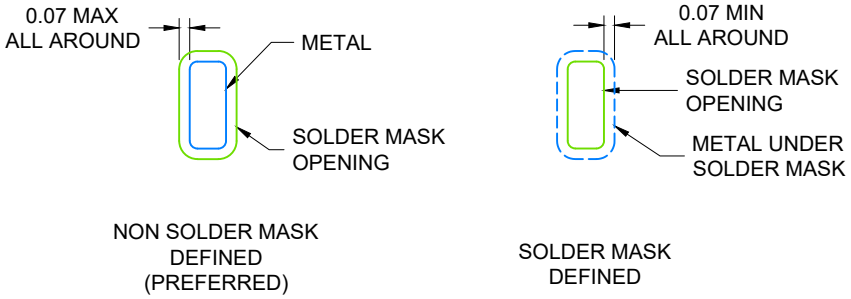
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

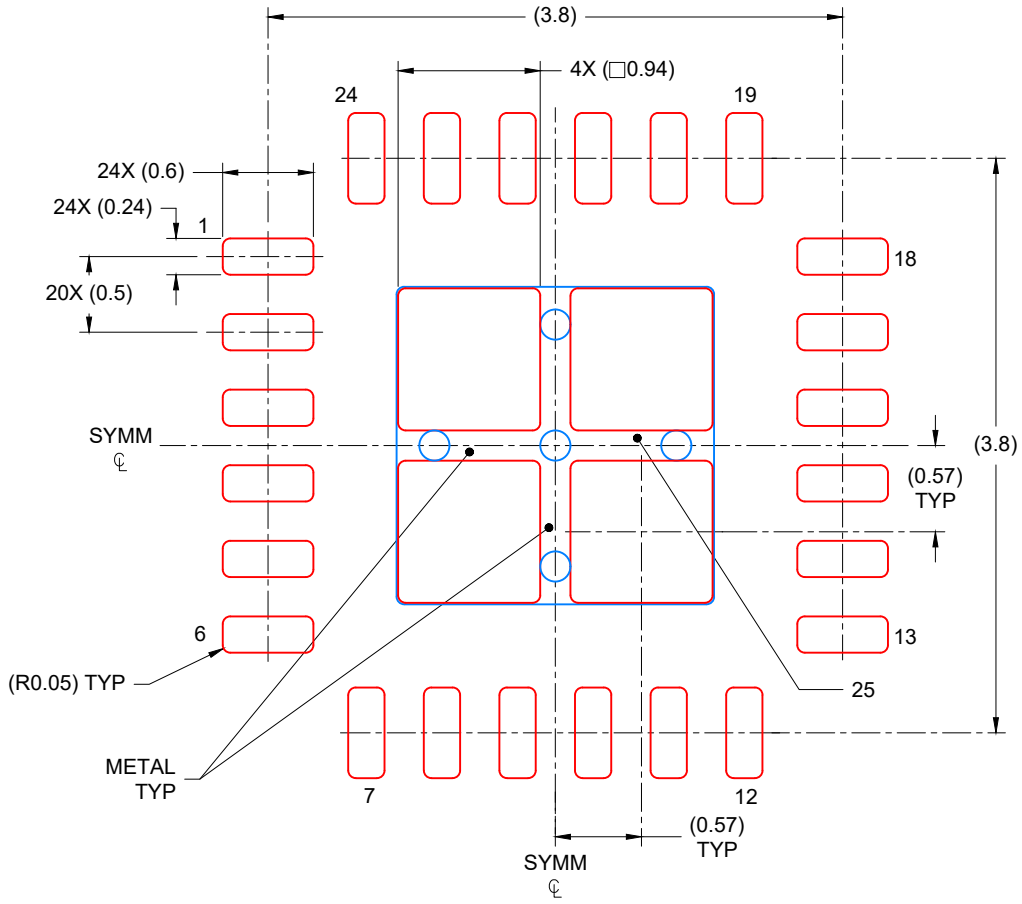


SOLDER MASK DETAILS

4224376 / C 06/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 20X

4224376 / C 06/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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