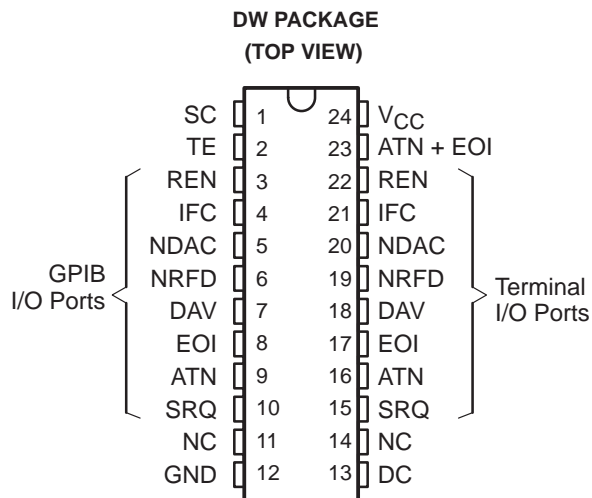


# SN75ALS164 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SLLS022C – JUNE 1986 – REVISED MAY 1998

- **8-Channel Bidirectional Transceiver**
- **Designed to Implement Control Bus Interface**
- **Designed for Multiple-Controller Systems**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low-Power Dissipation . . . 46 mW Max Per Channel**
- **Fast Propagation Times . . . 20 ns Max**
- **High-Impedance pnp Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Bus-Terminating Resistors Provided on Driver Outputs**
- **No Loading of Bus When Device Is Powered Down ( $V_{CC} = 0$ )**
- **Power-Up/Power-Down Protection (Glitch Free)**



NC – No internal connection

**NOT RECOMMENDED FOR NEW DESIGNS**

## description

The SN75ALS164 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, advanced low-power Schottky device designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS164 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS164 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. All outputs are disabled (at the high-impedance state) during  $V_{CC}$  power-up and power-down transitions for glitch-free operation. The direction of data flow through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SN75ALS164 is identical to the SN75ALS162 with the addition of an OR gate to help simplify board layouts in several popular applications. The ATN and EOI signals are ORed to provide the ATN + EOI output, which is a standard totem-pole output.

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage  $V_{CC}$  is 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV minimum for increased noise immunity. All receivers have 3-state outputs that present a high impedance to the terminal when disabled.

The SN75ALS164 is characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1998, Texas Instruments Incorporated

# SN75ALS164 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SLLS022C – JUNE 1986 – REVISED MAY 1998

**CHANNEL IDENTIFICATION TABLE**

NAME	IDENTITY	CLASS
DC TE SC	Direction-Control Talk-Enable System Control	Control
ATN SRQ REN IFC EOI	Attention Service Request Remote Enable Interface Clear End or Identity	Bus Management
ATN+EOI	ATN Logical or EOI	Logic
DAV NDAC NRFD	Data Valid No Data Accepted Not Ready for Data	Data Transfer

## Function Tables

**RECEIVE/TRANSMIT FUNCTION TABLE**

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN† (controlled by DC)	SRQ	REN (controlled by SC)	IFC	EOI	DAV	NDAC	NRFD (controlled by TE)
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side.

Data transfer is noninverting in both directions.

† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI when the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

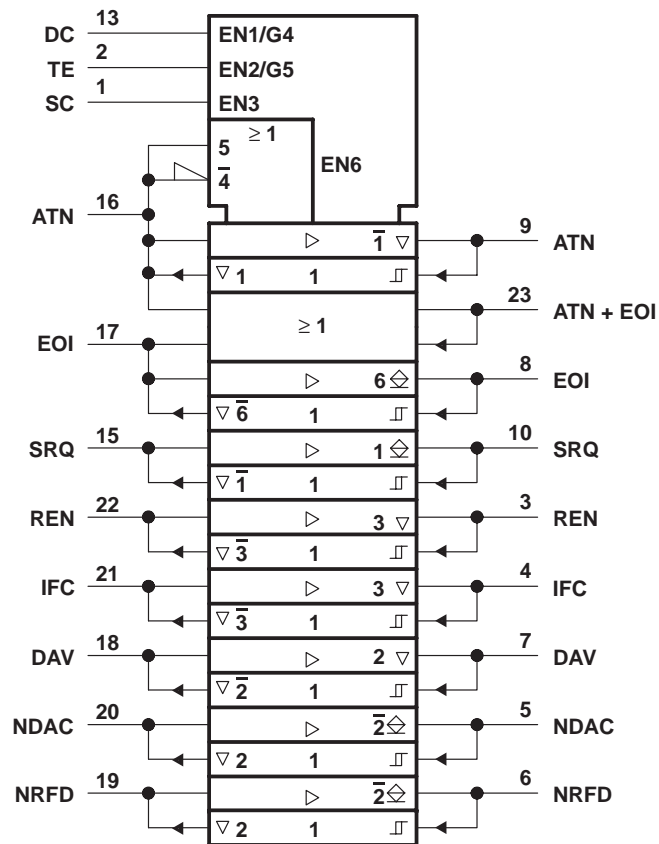
**ATN + EOI FUNCTION TABLE**

INPUTS		OUTPUT ATN + EOI
ATN	EOI	
H	X	H
X	H	H
L	L	L

# SN75ALS164 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SLLS022C – JUNE 1986 – REVISED MAY 1998

**logic symbol†**

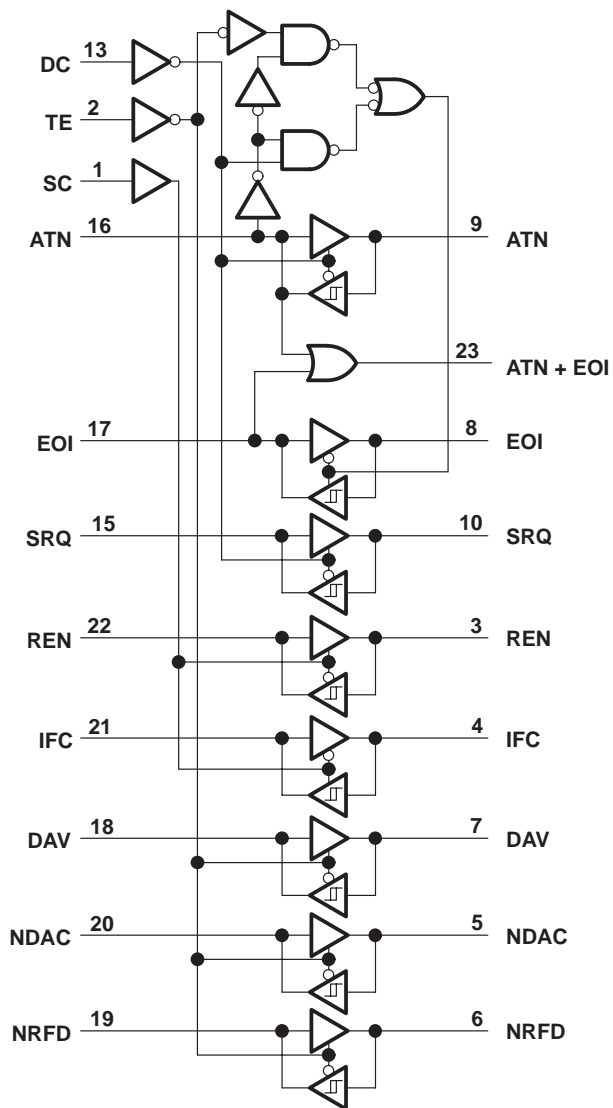


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

▽ Designates 3-state outputs

◇ Designates passive-pullup outputs

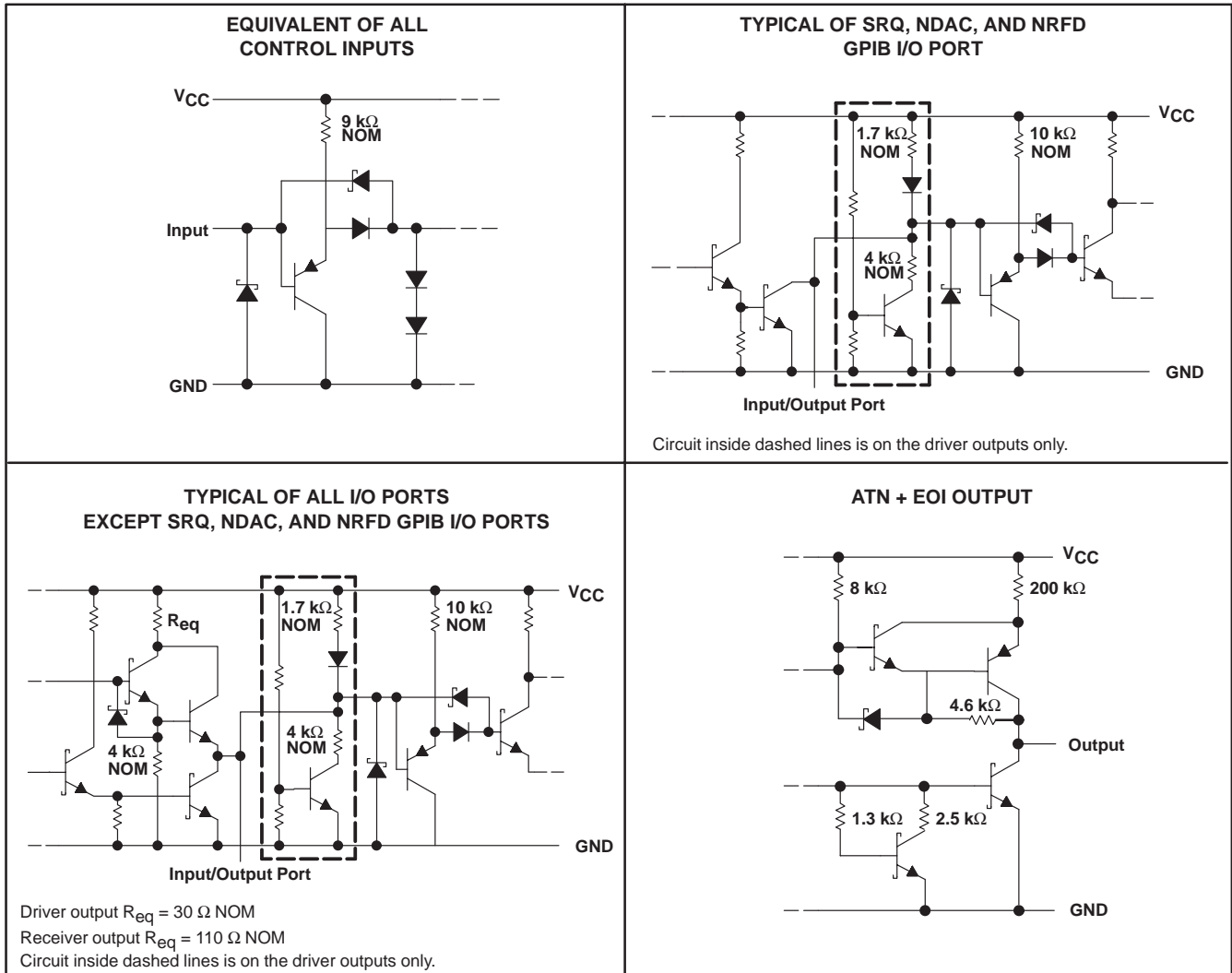
**logic diagram (positive logic)**



# SN75ALS164 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SLLS022C – JUNE 1986 – REVISED MAY 1998

## schematics of inputs and outputs



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Low-level driver output current	100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2)	81°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to network ground terminal.  
2. The package thermal impedance is calculated in accordance with JESD 51.

# SN75ALS164

## OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SLLS022C – JUNE 1986 – REVISED MAY 1998

### recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
High-level input voltage, $V_{IH}$		2			V
Low-level input voltage, $V_{IL}$		0.8			V
High-level output current, $I_{OH}$	Bus ports with 3-state outputs	– 5.2			mA
	Terminal ports	– 800			$\mu$ A
	ATN + EOI	– 400			
Low-level output current, $I_{OL}$	Bus ports	48			mA
	Terminal ports	16			
	ATN + EOI	4			
Operating free-air temperature, $T_A$		0	70		$^{\circ}$ C

### electrical characteristics over recommended supply-voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	Input clamp voltage	$I_I = -18$ mA		– 0.8	– 1.5		V
$V_{hys}$	Hysteresis ( $V_{T+} - V_{T-}$ )	Bus		0.4	0.65		V
$V_{OH}^{\ddagger}$	High-level output voltage	Terminal	$I_{OH} = -800$ $\mu$ A	2.7	3.5		V
		Bus	$I_{OH} = -5.2$ mA	2.5	3.3		
		ATN+EOI	$I_{OH} = -400$ $\mu$ A	2.7			
$V_{OL}$	Low-level output voltage	Terminal	$I_{OL} = 16$ mA		0.3	0.5	V
		Bus	$I_{OL} = 48$ mA		0.35	0.5	
		ATN+EOI	$I_{OL} = 4$ mA			0.4	
$I_I$	Input current at maximum input voltage	Terminal§	$V_I = 5.5$ V		0.2	100	$\mu$ A
		ATN, EOI	$V_I = 5.5$ V			200	
$I_{IH}$	High-level input current	Terminal control	$V_I = 2.7$ V		0.1	20	$\mu$ A
		ATN, EOI	$V_I = 2.7$ V			40	
$I_{IL}$	Low-level input current	Terminal control	$V_I = 0.5$ V		– 10	– 100	$\mu$ A
		ATN, EOI	$V_I = 0.5$ V			– 500	
$V_{I/O}(\text{bus})$	Voltage at bus port	Driver disabled	$I_{I(\text{bus})} = 0$	2.5	3.0	3.7	V
			$I_{I(\text{bus})} = -12$ mA			– 1.5	
$I_{I/O}(\text{bus})$	Current into bus port	Power on	Driver disabled	$V_{I(\text{bus})} = -1.5$ V to 0.4 V	– 1.3		mA
				$V_{I(\text{bus})} = 0.4$ V to 2.5 V	0	– 3.2	
				$V_{I(\text{bus})} = 2.5$ V to 3.7 V		+ 2.5	
				$V_{I(\text{bus})} = 3.7$ V to 5 V	0	2.5	
				$V_{I(\text{bus})} = 5$ V to 5.5 V	0.7	2.5	
		Power off	$V_{CC} = 0$ , $V_{I(\text{bus})} = 0$ to 2.5 V		– 40	$\mu$ A	
$I_{OS}$	Short-circuit output current	Terminal		– 15	– 35	– 75	mA
		Bus		– 25	– 50	– 125	
		ATN + EOI		– 10		– 100	
$I_{CC}$	Supply current	No load, TE, DC, and SC low		55	75		mA
$C_{I/O}(\text{bus})$	Bus-port capacitance	$V_{CC} = 0$ to 5 V, $V_{I/O} = 0$ to 2 V, $f = 1$ MHz		30			pF

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^{\circ}$ C.

‡  $V_{OH}$  applies for 3-state outputs only.

§ Except ATN and EOI terminals.



# SN75ALS164

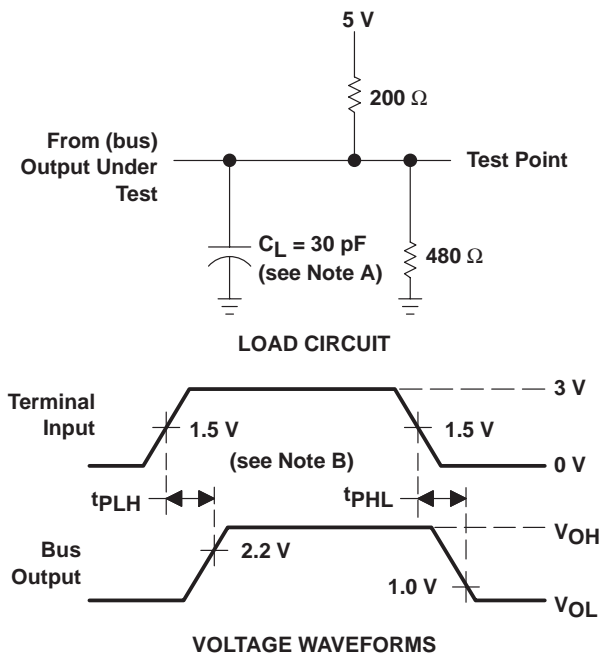
## OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SLLS022C – JUNE 1986 – REVISED MAY 1998

### switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V}$

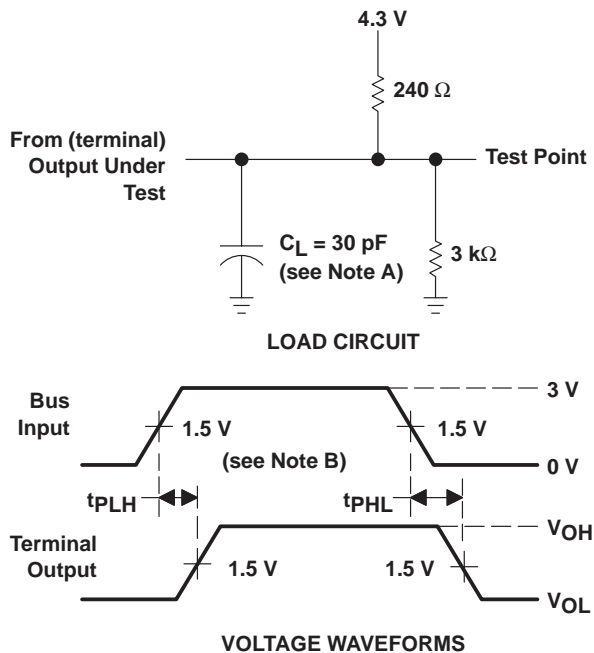
PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	Terminal	Bus	$C_L = 30\text{ pF}$ , See Figure 1		10	20	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output					12	20	
$t_{PLH}$	Propagation delay time, low-to-high-level output	Bus	Terminal	$C_L = 30\text{ pF}$ , See Figure 2		5	10	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output					7	14	
$t_{PLH}$	Propagation delay time, low-to-high-level output	Terminal ATN or Terminal EOI	ATN+EOI	$C_L = 15\text{ pF}$ , See Figure 3		3.5	10	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output	Terminal ATN or Terminal EOI	ATN+EOI	$C_L = 15\text{ pF}$ , See Figure 3		7	15	ns
$t_{PZH}$	Output enable time to high level	TE, DC, or SC	Bus (ATN, EOI, REN, IFC, and DAV)	$C_L = 15\text{ pF}$ , See Figure 4			30	ns
$t_{PHZ}$	Output disable time from high level						20	
$t_{PZL}$	Output enable time to low level						45	
$t_{PLZ}$	Output disable time from low level						20	
$t_{PZH}$	Output enable time to high level	TE, DC, or SC	Terminal	$C_L = 15\text{ pF}$ , See Figure 5			30	ns
$t_{PHZ}$	Output disable time from high level						25	
$t_{PZL}$	Output enable time to low level						30	
$t_{PLZ}$	Output disable time from low level						25	

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .

**Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms**



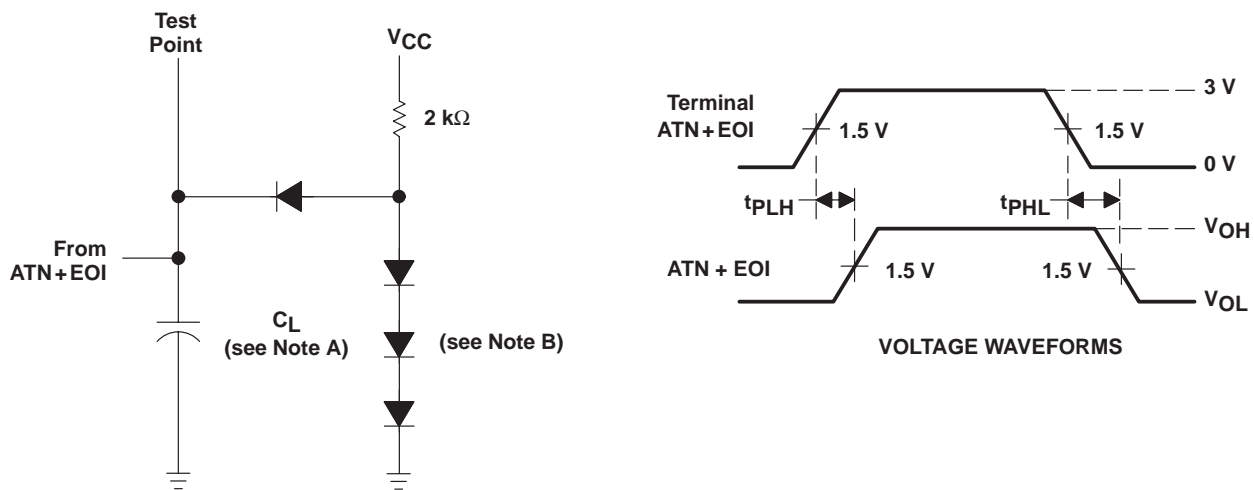
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .

**Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms**

# SN75ALS164 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SLLS022C – JUNE 1986 – REVISED MAY 1998

## PARAMETER MEASUREMENT INFORMATION

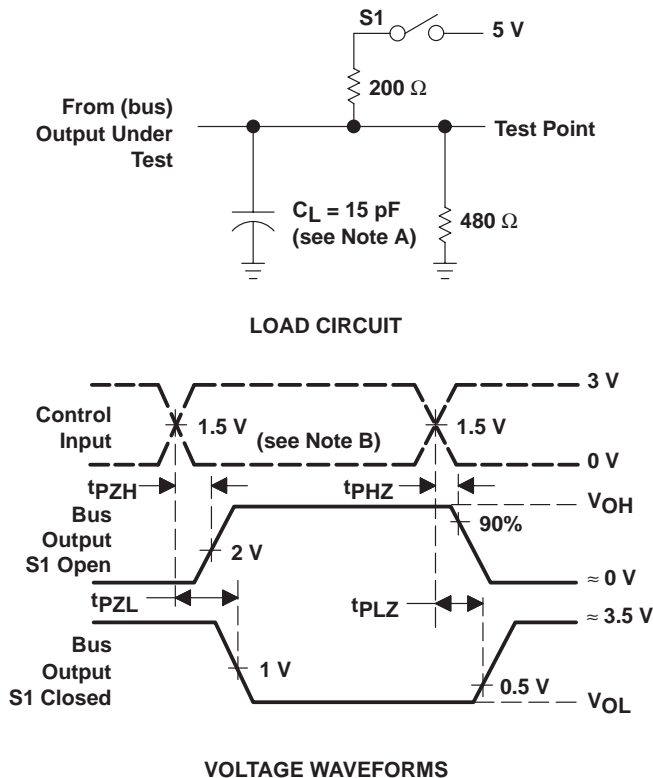


### LOAD CIRCUIT

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All diodes are 1N916 or 1N3064

Figure 3. ATN + EOI Load Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION**



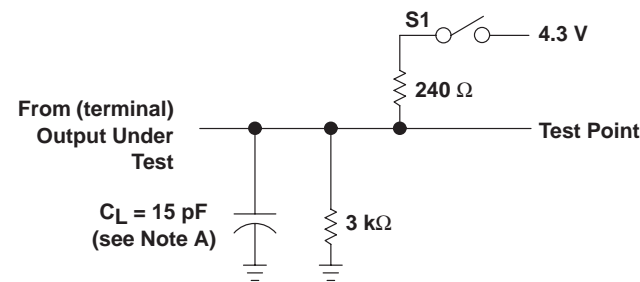
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1 \text{ MHz}$ , 50% duty cycle,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ ,  $Z_O = 50 \Omega$ .

**Figure 4. Bus Load Circuit and Voltage Waveforms**

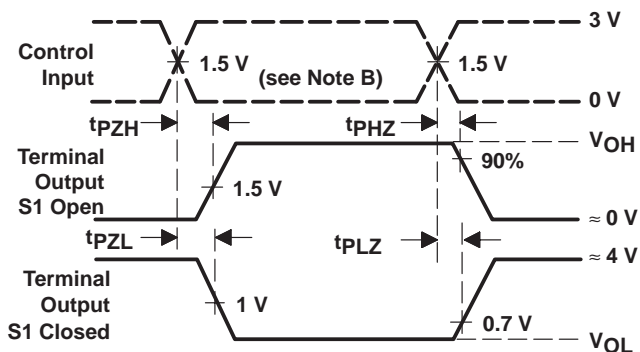
# SN75ALS164 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SLLS022C – JUNE 1986 – REVISED MAY 1998

## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .

Figure 5. Terminal Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

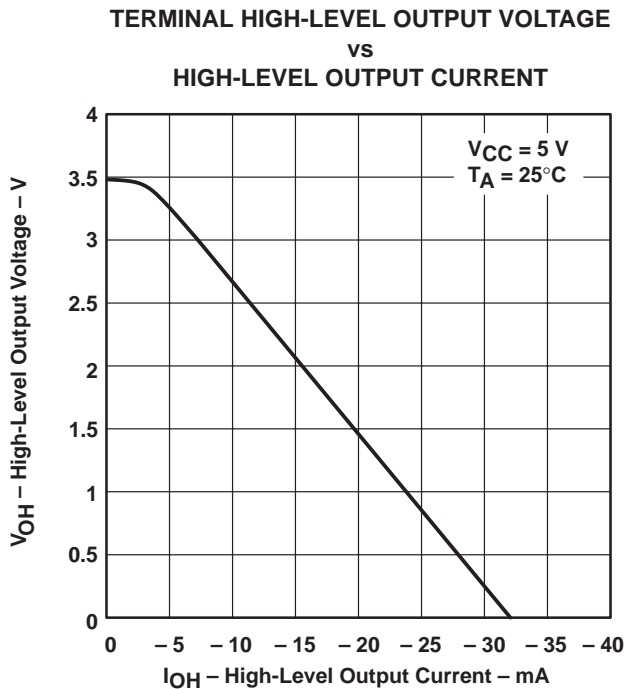


Figure 6

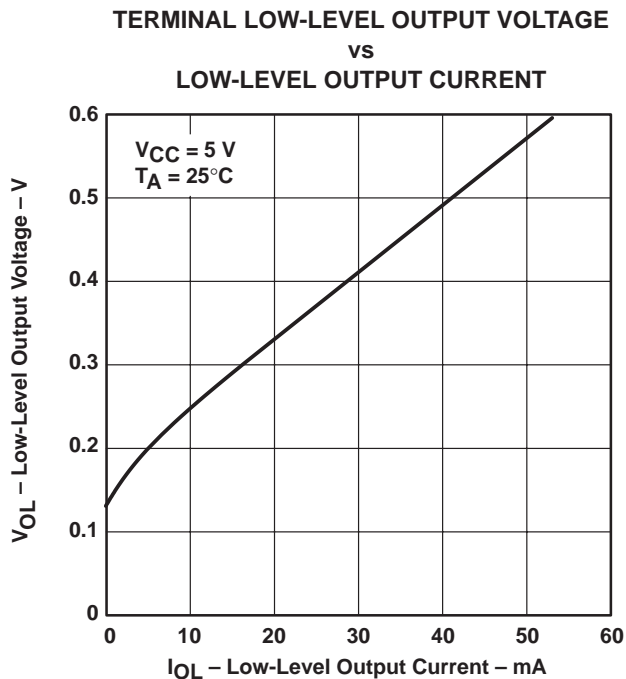


Figure 7

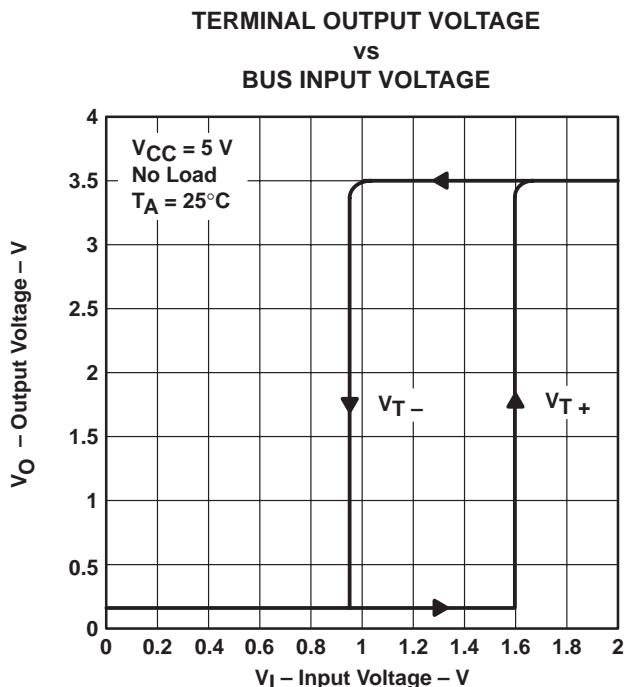
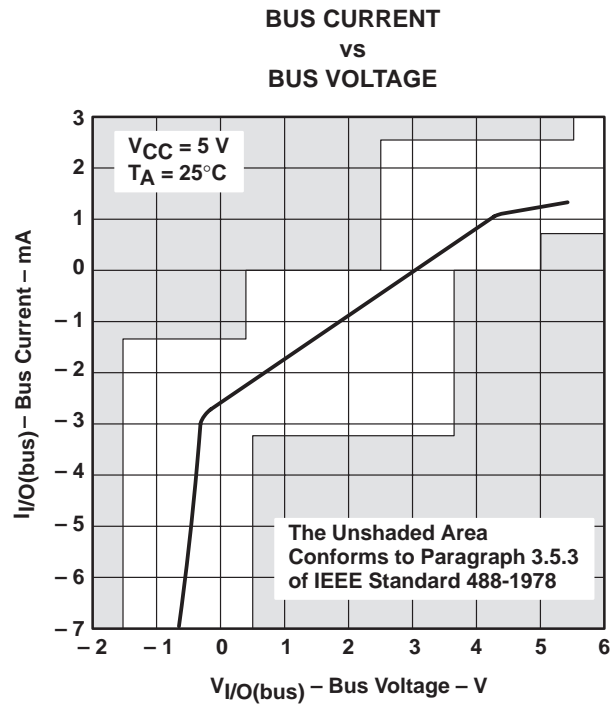
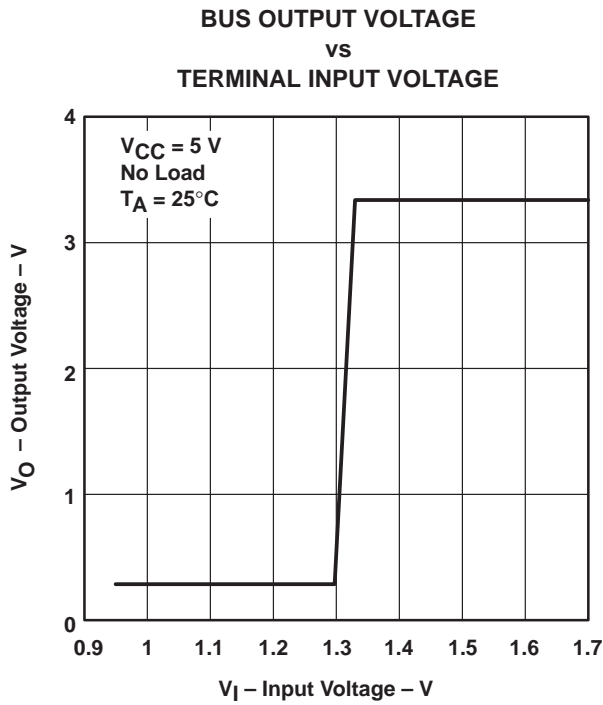
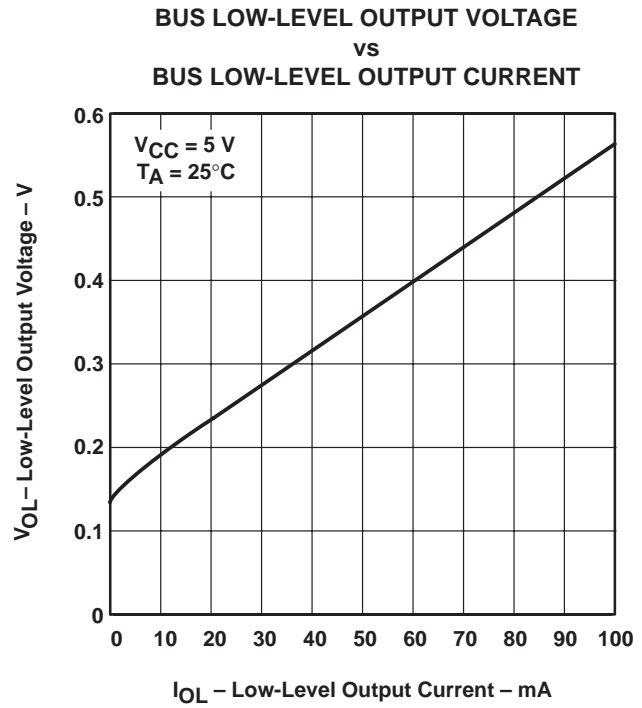
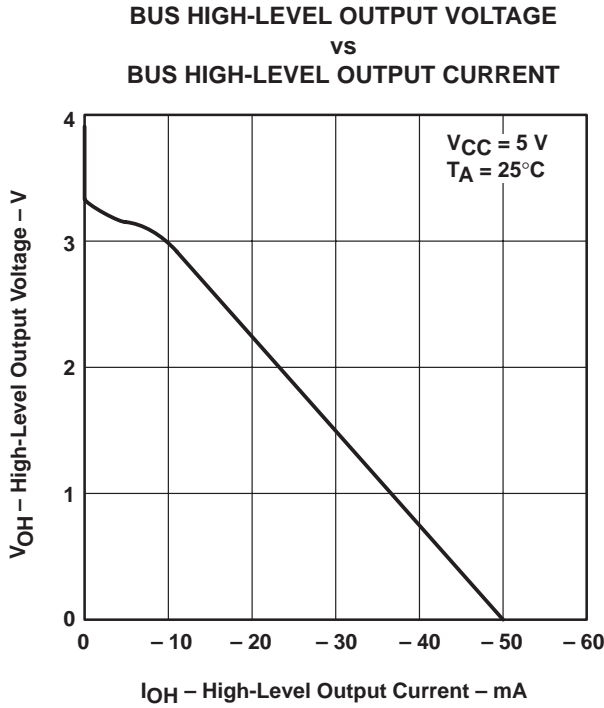


Figure 8

# SN75ALS164 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SLLS022C – JUNE 1986 – REVISED MAY 1998

## TYPICAL CHARACTERISTICS



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS164DW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS164	<a href="#">Samples</a>
SN75ALS164DWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS164	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

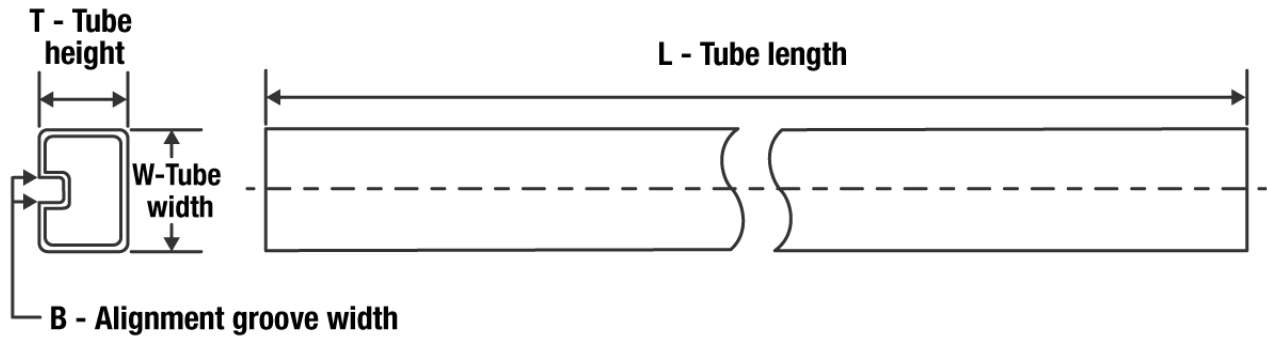

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS164DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS164DWR	SOIC	DW	24	2000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75ALS164DW	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated