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TEXAS INSTRUMENTS

SN74AHCT1G125

SCLS378N –AUGUST 1997–REVISED JANUARY 2016

## SN74AHCT1G125 Single Bus Buffer Gate With 3-State Output

1 Features

- Operating Range of 4.5 V to 5.5 V
- Max t_{pd} of 6 ns at 5 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±8-mA Output Drive at 5 V
- Inputs are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17

2 Applications

- Wireless Infrastructure
- Servers
- Power Infrastructure
- PCs/Notebooks
- Programmable Logic Controllers
- Tests and Measurements
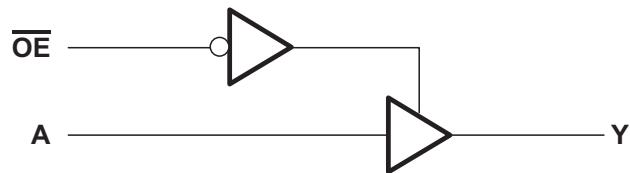
3 Description

The SN74AHCT1G125 device is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, data is passed from the A input to the Y output.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AHCT1G125	SOT-23 (5)	2.90 mm x 1.60 mm
	SC-70 (5)	2.00 mm x 1.30 mm
	SOT-553 (5)	1.65 mm x 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

Table of Contents

5 Revision History

**Changes from Revision M (December 2014) to Revision N**   **Page**

- Added the T_j Junction Temp 150°C to Absolute Maximum Ratings[1] 4
- Changed figure 3 in Functional Block Diagram 8

Changes from Revision L (June 2005) to Revision M   **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Deleted *Ordering Information* table. 1
- Changed MAX operating temperature to 125°C in *Recommended Operating Conditions* table. 4

Product Folder Links: *SN74AHCT1G125*

6 Pin Configuration and Functions

DBV PACKAGE (TOP VIEW)

```
OE   | 1        5 | V_CC
A    | 2          |
GND  | 3        4 | Y
```

DCK PACKAGE (TOP VIEW)

```
OE   | 1     5 | V_CC
A    | 2       |
GND  | 3     4 | Y
```

DRL PACKAGE (TOP VIEW)

```
OE   | 1   5 | V_CC
A    | 2     |
GND  | 3   4 | Y
```
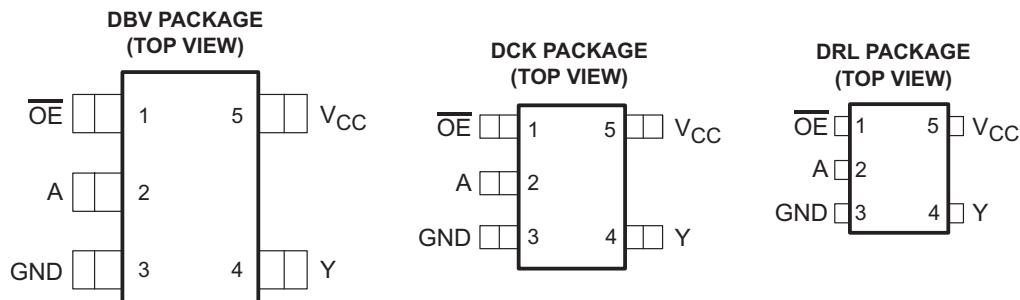
See mechanical drawings for dimensions.

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$\overline{OE}$	I	Output Enable
2	A	I	Input A
3	GND	—	Ground Pin
4	Y	O	Output Y
5	V_{CC}	—	Power Pin

7 Specifications

7.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I	Input voltage range[2]		−0.5	7	V
V_O	Output voltage range[2]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous channel current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		−65	150	°C
T_j	Junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

7.4 Thermal Information

THERMAL METRIC[1]		SN74AHCT1G125			UNIT
		DBV	**DCK**	**DRL**	
		5 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	231.3	287.6	328.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	119.9	97.7	105.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	60.6	65.	150.3	
ψ_{JT}	Junction-to-top characterization parameter	17.8	2.0	6.9	
ψ_{JB}	Junction-to-board characterization parameter	60.1	64.2	148.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	**TYP**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
V_{OH}	I_{OH} = −50 µA	4.5 V	4.4	4.5		4.4		4.4		V
	I_{OH} = −8 mA		3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	µA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			1		10		10	µA
ΔI_{CC}[1]	One input at 3.4 V, Other input at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4	10		10		10	pF
C_o	$V_O = V_{CC}$ or GND	5 V		10						pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

7.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	**TYP**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
t_{PLH}	A	Y	C_L = 15 pF		3.8	5.5	1	6.5	1	7	ns
t_{PHL}					3.8	5.5	1	6.5	1	7	
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		3.6	5.1	1	6	1	6.5	ns
t_{PZL}					3.6	5.1	1	6	1	6.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		4.6	6.8	1	8	1	8.5	ns
t_{PLZ}					4.6	6.8	1	8	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	1	9.5	ns
t_{PHL}					5.3	7.5	1	8.5	1	9.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		5.1	7.1	1	8	1	9	ns
t_{PZL}					5.1	7.1	1	8	1	9	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.1	8.8	1	10	1	11	ns
t_{PLZ}					6.1	8.8	1	10	1	11	

7.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	14	pF

7.8 Typical Characteristics
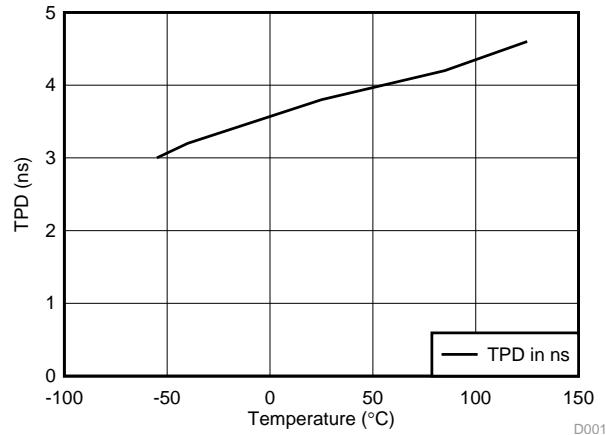
Figure 1. TPD vs Temperature

Product Folder Links: *SN74AHCT1G125*

8 Parameter Measurement Information

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN74AHCT1G125 device is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

9.2 Functional Block Diagram
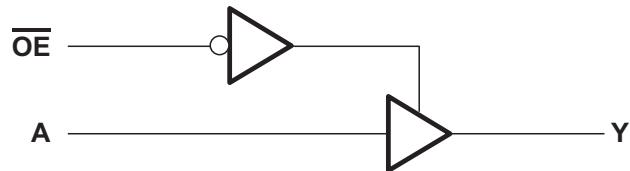
Figure 3. Logic Diagram (Positive Logic)

9.3 Feature Description

- TTL inputs
  - Lowered switching threshold allows up translation 3.3 V to 5 V
- Slow edges reduce output ringing

9.4 Device Functional Modes

Table 1. Function Table

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

Product Folder Links: *SN74AHCT1G125*

10 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74AHCT1G125 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8 V V_{IL} and 2V V_{IH}. This feature makes it Ideal for translating up from 3.3 V to 5 V. Figure 4 shows this type of translation.

10.2 Typical Application
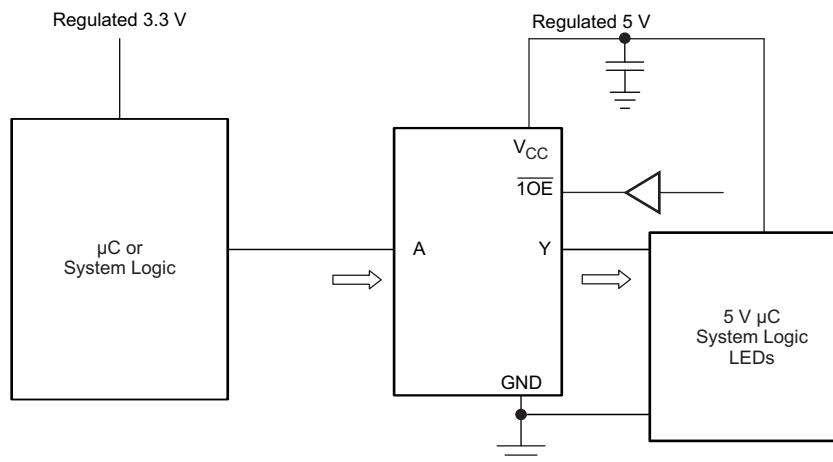
Figure 4. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   – For rise time and fall time specifications, see Δt/ΔV in the *Recommended Operating Conditions* table.
   – For specified High and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
   – Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend Output Conditions
   – Load currents should not exceed 25 mA per output and 50 mA total for the part.
   – Outputs should not be pulled above V_{CC}.

Typical Application (continued)

10.2.3 Application Curves

Tranlsation from 3.3V to 5V

Figure 5. Translation from 3.3 V to 5 V
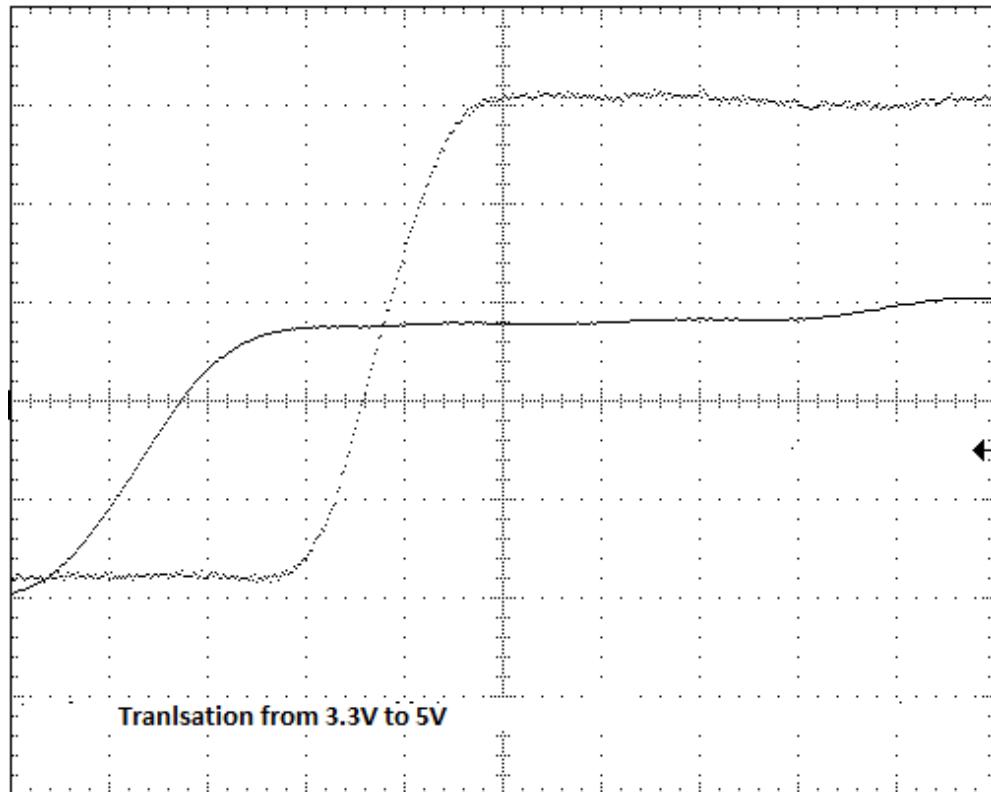
11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

Product Folder Links: *SN74AHCT1G125*

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 6 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

12.2 Layout Example
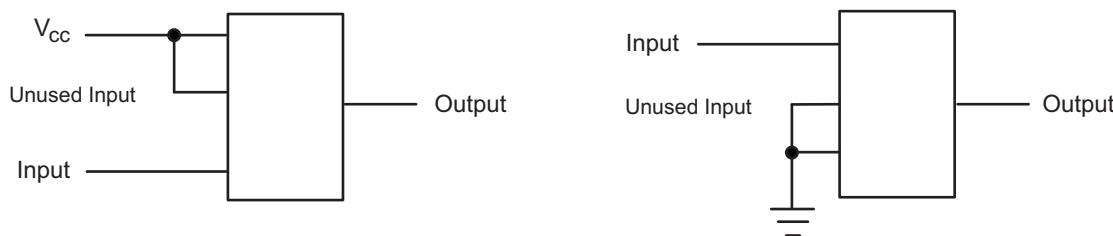
Figure 6. Layout Diagram

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.
    This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AHCT1G125DBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B25G	Samples
74AHCT1G125DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B25G	Samples
74AHCT1G125DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B25G	Samples
74AHCT1G125DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BM3	Samples
74AHCT1G125DCKTE4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BM3	Samples
74AHCT1G125DCKTG4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BM3	Samples
SN74AHCT1G125DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(B253, B25G, B25J, B25L, B25S)	Samples
SN74AHCT1G125DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(B253, B25G, B25J, B25L, B25S)	Samples
SN74AHCT1G125DCK3	ACTIVE	SC70	DCK	5	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 85	BMY	Samples
SN74AHCT1G125DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(BM3, BMG, BMJ, BML, BMS)	Samples
SN74AHCT1G125DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(BM3, BMG, BMJ, BML, BMS)	Samples
SN74AHCT1G125DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(BMB, BMS)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74AHCT1G125 :

- Automotive: SN74AHCT1G125-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS
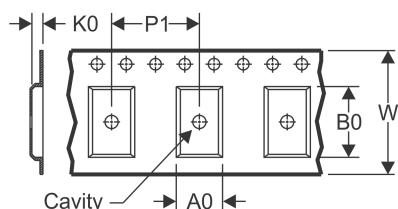
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
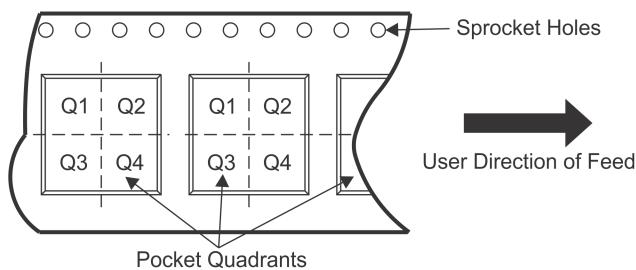
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AHCT1G125DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHCT1G125DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHCT1G125DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
74AHCT1G125DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHCT1G125DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74AHCT1G125DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHCT1G125DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G125DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHCT1G125DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AHCT1G125DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHCT1G125DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHCT1G125DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AHCT1G125DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHCT1G125DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT1G125DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS
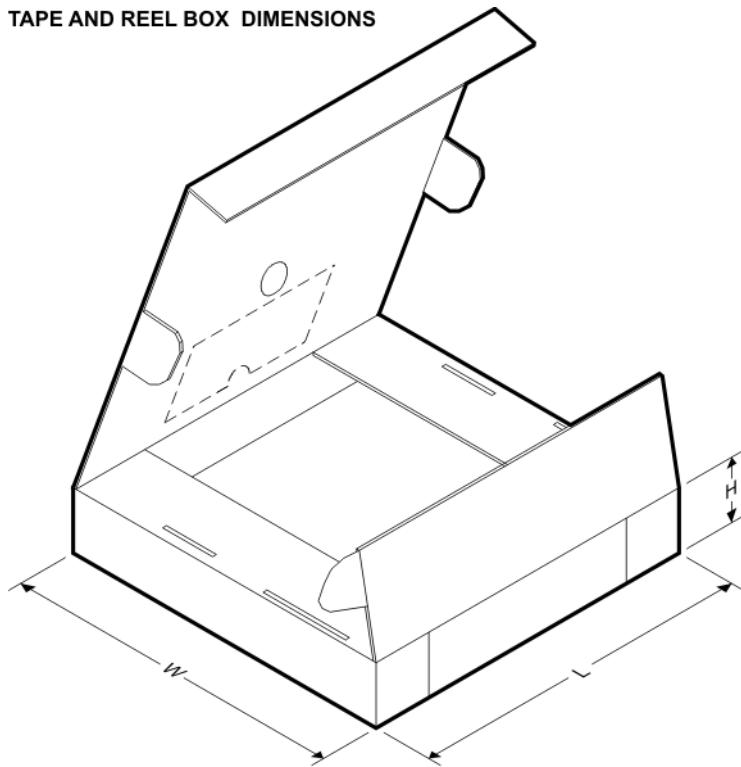
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AHCT1G125DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74AHCT1G125DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
74AHCT1G125DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
74AHCT1G125DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHCT1G125DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHCT1G125DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHCT1G125DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHCT1G125DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AHCT1G125DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AHCT1G125DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHCT1G125DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHCT1G125DCKT	SC70	DCK	5	250	202.0	201.0	28.0

PACKAGE MATERIALS INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT1G125DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHCT1G125DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHCT1G125DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0

4214839/F   06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

DBV0005A

SOT-23 - 1.45 mm max height

PKG

5X (1.1)

1

5X (0.6)

5

SYMM

2

(1.9)

2X (0.95)

3

4

(R0.05) TYP

(2.6)
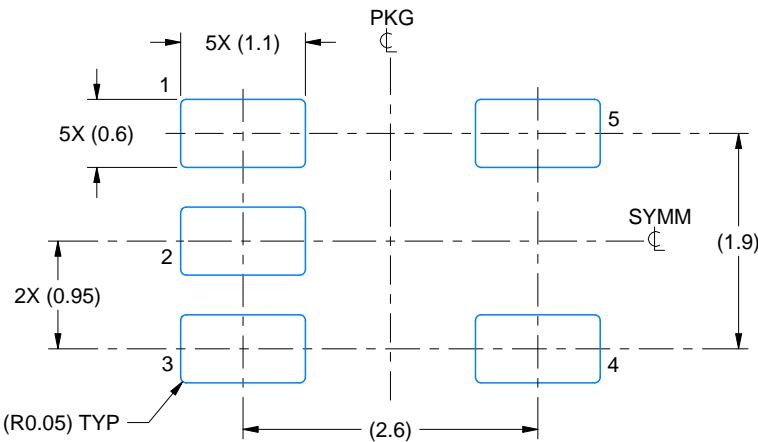
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.07 MAX
ARROUND

0.07 MIN
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED
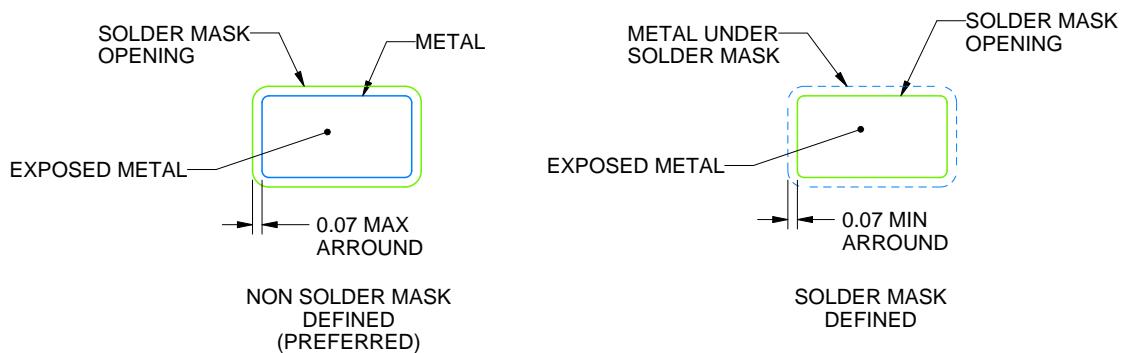
SOLDER MASK DETAILS

4214839/F   06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F   06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DCK (R−PDSO−G5)   PLASTIC SMALL−OUTLINE PACKAGE
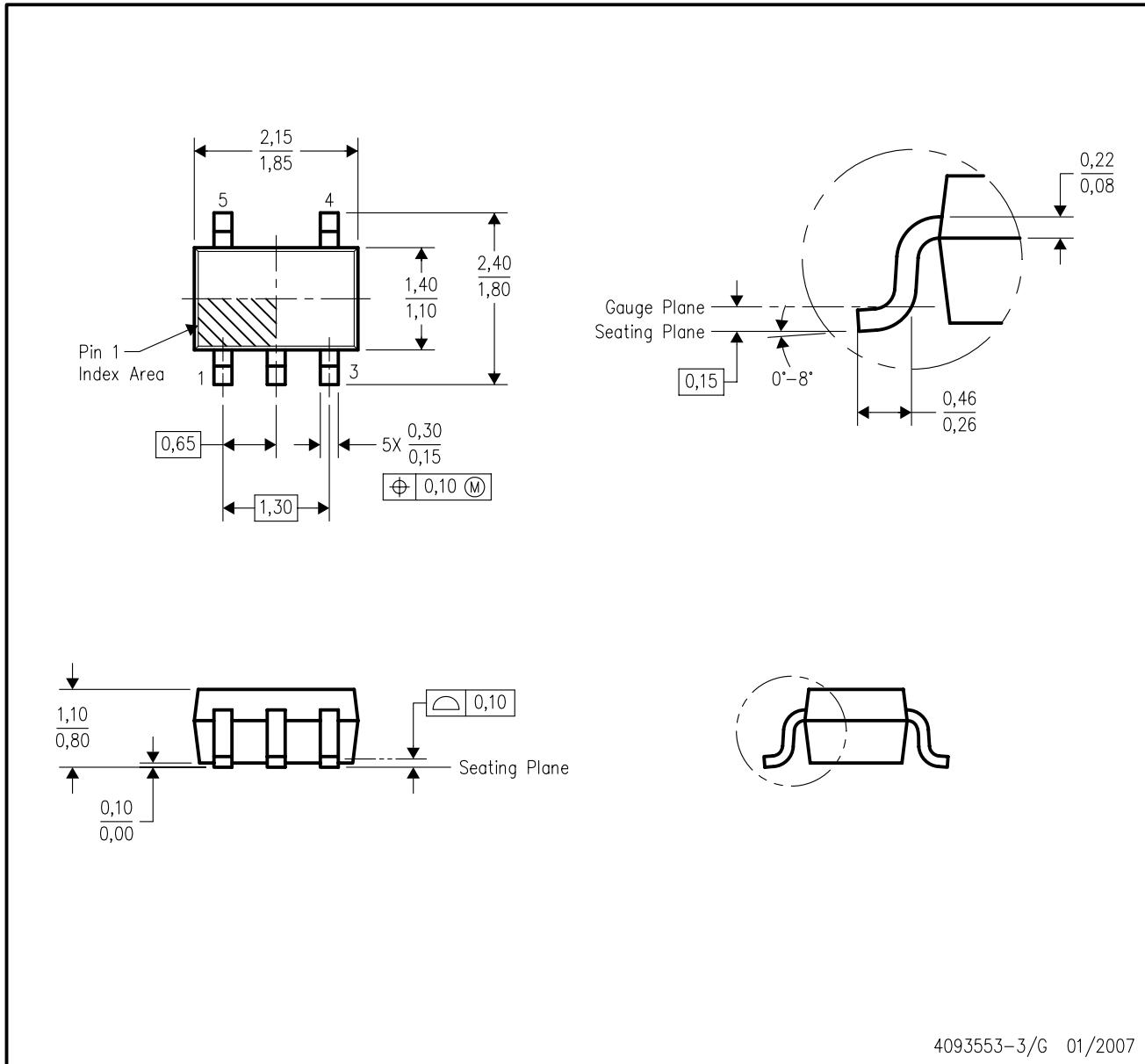
4093553−3/G 01/2007

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Falls within JEDEC MO−203 variation AA.

DCK (R–PDSO–G5)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
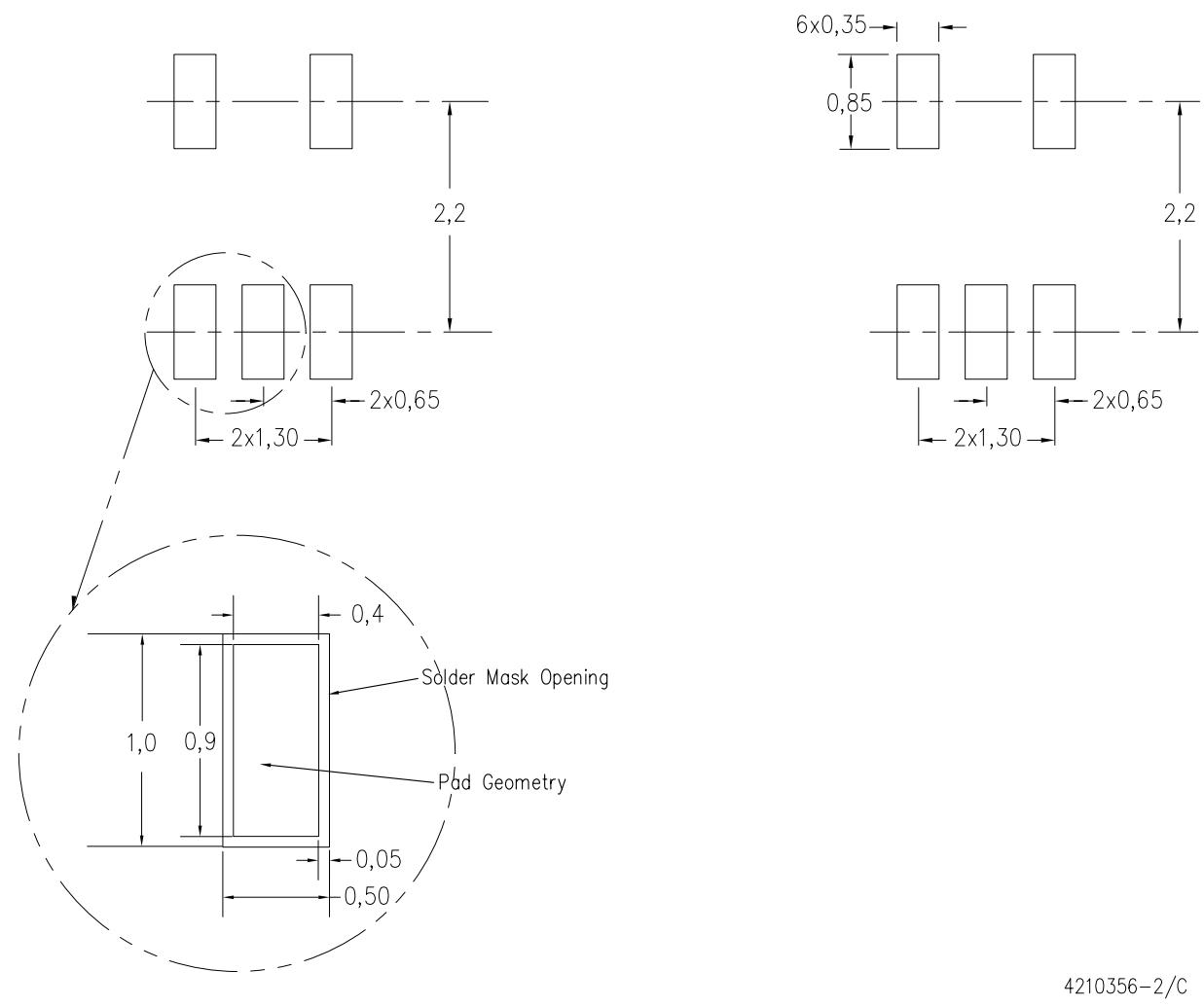
6x0,35

0,85

2,2

2,2

2x0,65

2x0,65

2x1,30

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356–2/C 07/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D.   Publication IPC–7351 is recommended for alternate designs.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
              metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

TEXAS INSTRUMENTS
www.ti.com
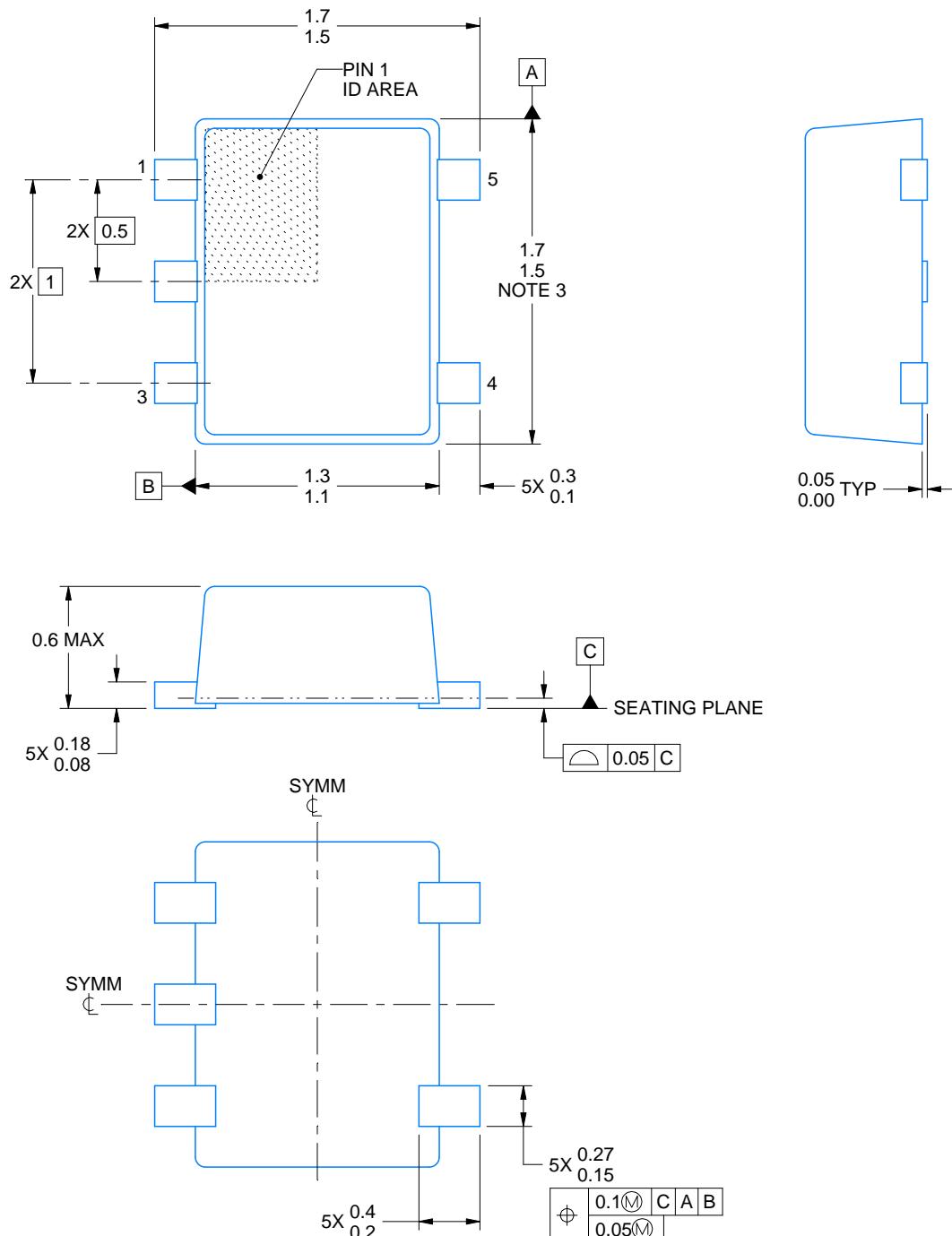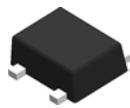
4220753/B   12/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1
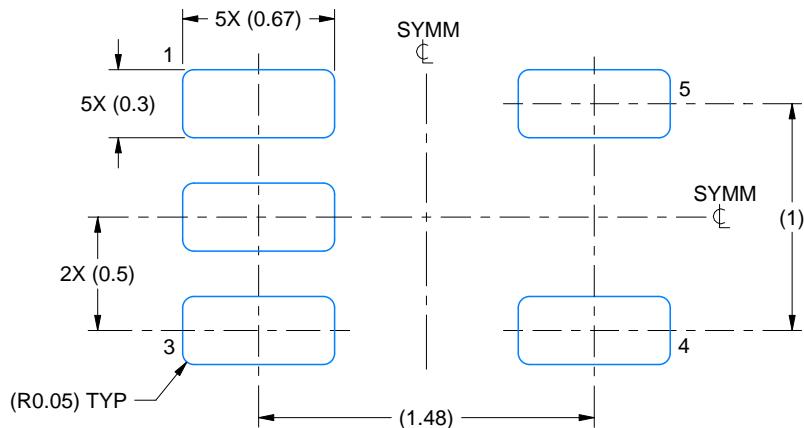
LAND PATTERN EXAMPLE
SCALE:30X
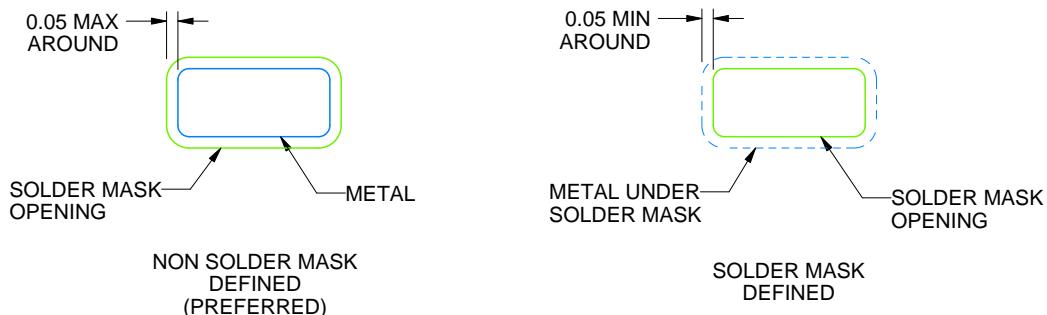
5X (0.67)
5X (0.3)
2X (0.5)
1
SYMM
5
SYMM
(1)
(1.48)
3
4
(R0.05) TYP

SOLDERMASK DETAILS

0.05 MAX AROUND
SOLDER MASK OPENING
METAL
NON SOLDER MASK DEFINED (PREFERRED)

0.05 MIN AROUND
METAL UNDER SOLDER MASK
SOLDER MASK OPENING
SOLDER MASK DEFINED

4220753/B   12/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

TEXAS INSTRUMENTS
www.ti.com
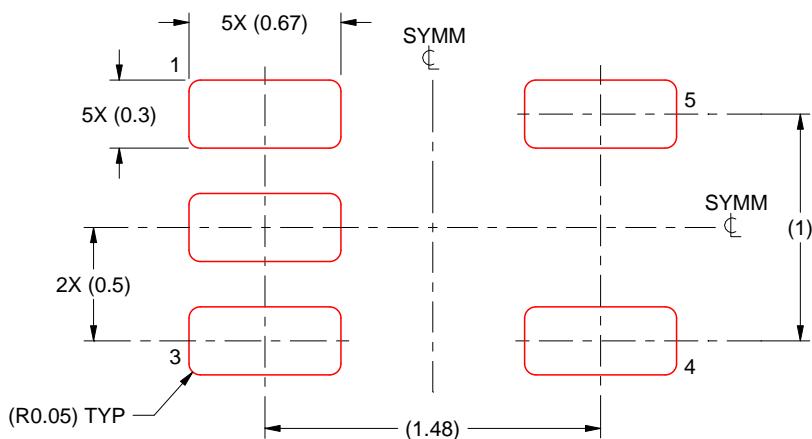
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/B   12/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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