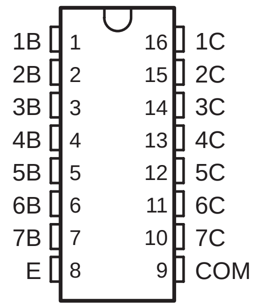
# ULN2004AI
# HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

SLRS055 − APRIL 2004

- **500-mA-Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay-Driver Applications**

**D, N, OR NS PACKAGE**
**(TOP VIEW)**



## description/ordering information

The ULN2004AI is a high-voltage, high-current Darlington transistor array. This device consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher-current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The ULN2004AI has a 10.5-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

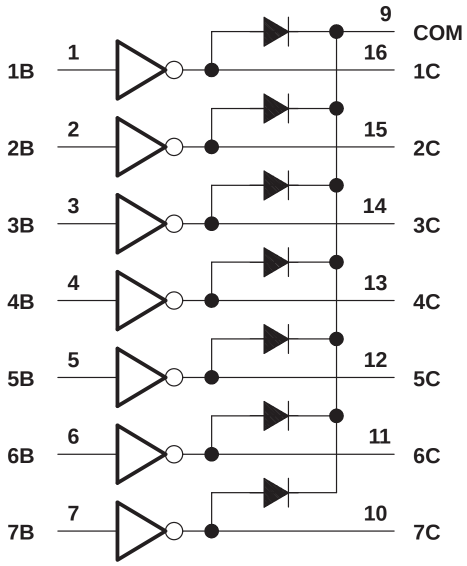
**ORDERING INFORMATION**

| $T_A$ | PACKAGE[†] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 105°C | PDIP (N) | Tube of 25 | ULN2004AIN | ULN2004AIN |
| | SOIC (D) | Tube of 40 | ULN2004AID | ULN2004AI |
| | | Reel of 2500 | ULN2004AIDR | |
| | SOP (NS) | Reel of 2000 | ULN2004AINSR | ULN2004AI |

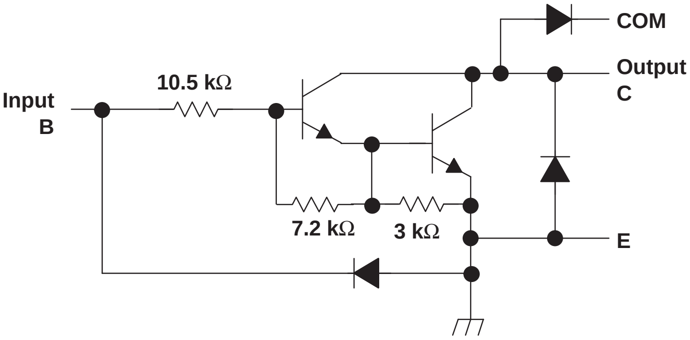
[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

TEXAS INSTRUMENTS

## logic diagram



## schematics (each Darlington pair)



All resistor values shown are nominal.

## absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)[†]

| | | |
|---|---|---|
| Collector-emitter voltage | | 50 V |
| Clamp diode reverse voltage (see Note 1) | | 50 V |
| Input voltage, $V_I$ (see Note 1) | | 30 V |
| Peak collector current (see Notes 2 and 4) | | 500 mA |
| Output clamp current, $I_{OK}$ | | 500 mA |
| Total emitter-terminal current | | −2.5 A |
| Operating free-air temperature range, $T_A$ | | −40°C to 105°C |
| Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3): | D package | 73°C/W |
| | N package | 67°C/W |
| | NS package | 64°C/W |
| Operating virtual junction temperature, $T_J$ | | 150°C |
| Storage temperature range, $T_{stg}$ | | −65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
2. Maximum power dissipation is a function of $T_J$(max), $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## electrical characteristics, $T_A$ = 25°C

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{I(on)}$ | On-state input voltage | 6 | $V_{CE}$ = 2 V | $I_C$ = 125 mA | | | 5 | V |
| | | | | $I_C$ = 200 mA | | | 6 | |
| | | | | $I_C$ = 275 mA | | | 7 | |
| | | | | $I_C$ = 350 mA | | | 8 | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $I_I$ = 250 µA, | $I_C$ = 100 mA | | 0.9 | 1.1 | V |
| | | | $I_I$ = 350 µA, | $I_C$ = 200 mA | | 1 | 1.3 | |
| | | | $I_I$ = 500 µA, | $I_C$ = 350 mA | | 1.2 | 1.6 | |
| $I_{CEX}$ | Collector cutoff current | 1 | $V_{CE}$ = 50 V, | $I_I$ = 0 | | | 50 | µA |
| $V_F$ | Clamp forward voltage | 8 | $I_F$ = 350 mA | | | 1.7 | 2 | V |
| $I_I$ | Input current | 4 | $V_I$ = 5 V | | | 0.35 | 0.5 | mA |
| | | | $V_I$ = 12 V | | | 1 | 1.45 | |
| $I_R$ | Clamp reverse current | 7 | $V_R$ = 50 V | | | | 50 | µA |
| $C_i$ | Input capacitance | | $V_I$ = 0, | f = 1 MHz | | 15 | 25 | pF |

## electrical characteristics, $T_A$ = −40°C to 105°C

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{I(on)}$ | On-state input voltage | 6 | $V_{CE}$ = 2 V | $I_C$ = 125 mA | | | 5 | V |
| | | | | $I_C$ = 200 mA | | | 6 | |
| | | | | $I_C$ = 275 mA | | | 7 | |
| | | | | $I_C$ = 350 mA | | | 8 | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $I_I$ = 250 µA, | $I_C$ = 100 mA | | 0.9 | 1.1 | V |
| | | | $I_I$ = 350 µA, | $I_C$ = 200 mA | | 1 | 1.3 | |
| | | | $I_I$ = 500 µA, | $I_C$ = 350 mA | | 1.2 | 1.6 | |
| $I_{CEX}$ | Collector cutoff current | 1 | $V_{CE}$ = 50 V, | $I_I$ = 0 | | | 50 | µA |
| | | 2 | $V_{CE}$ = 50 V | $I_I$ = 0 | | | 100 | |
| | | | | $V_I$ = 1 V | | | 500 | |
| $V_F$ | Clamp forward voltage | 8 | $I_F$ = 350 mA | | | 1.7 | 2 | V |
| $I_{I(off)}$ | Off-state input current | 3 | $V_{CE}$ = 50 V, | $I_C$ = 500 µA | 50 | 65 | | µA |
| $I_I$ | Input current | 4 | $V_I$ = 5 V | | | 0.35 | 0.5 | mA |
| | | | $V_I$ = 12 V | | | 1 | 1.45 | |
| $I_R$ | Clamp reverse current | 7 | $V_R$ = 50 V | | | | 100 | µA |
| $C_i$ | Input capacitance | | $V_I$ = 0, | f = 1 MHz | | 15 | 25 | pF |

## switching characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | See Figure 8 | | 0.25 | 1 | µs |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | See Figure 8 | | 0.25 | 1 | µs |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 50 V, $I_O$ ≈ 300 mA,<br>See Figure 9 | $V_S$ − 20 | | | mV |

## switching characteristics, $T_A$ = −40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | See Figure 8 | | 1 | 10 | µs |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | See Figure 8 | | 1 | 10 | µs |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 50 V, $I_O$ ≈ 300 mA,<br>See Figure 9 | $V_S$ − 500 | | | mV |

## PARAMETER MEASUREMENT INFORMATION

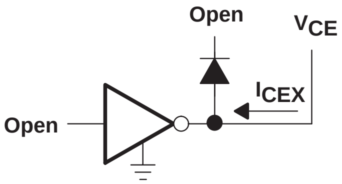


Figure 1. $I_{CEX}$ Test Circuit

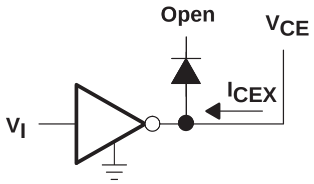


Figure 2. $I_{CEX}$ Test Circuit

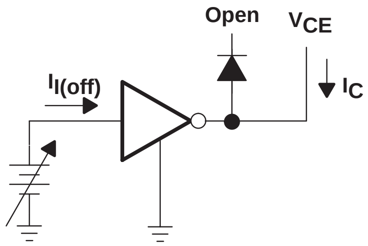


Figure 3. $I_{I(off)}$ Test Circuit

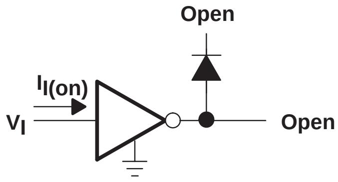
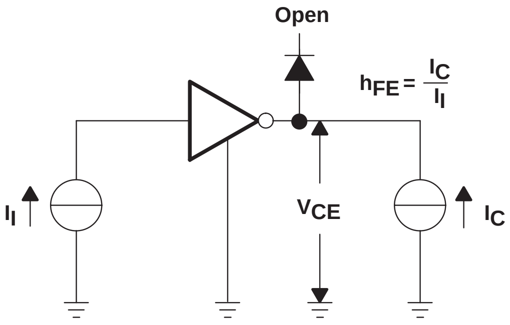


Figure 4. $I_I$ Test Circuit



NOTE: $I_I$ is fixed for measuring $V_{CE(sat)}$, variable for measuring $h_{FE}$.

Figure 5. $h_{FE}$, $V_{CE(sat)}$ Test Circuit

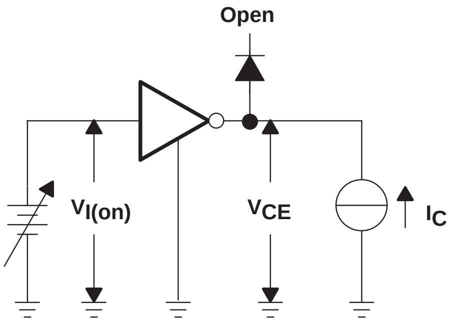


Figure 6. $V_{I(on)}$ Test Circuit

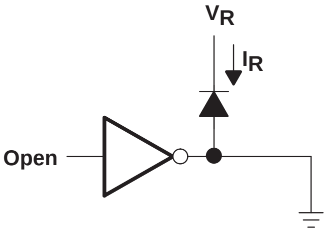


Figure 7. $I_R$ Test Circuit

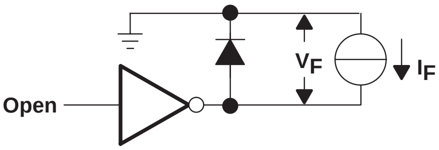


Figure 8. $V_F$ Test Circuit

## PARAMETER MEASUREMENT INFORMATION

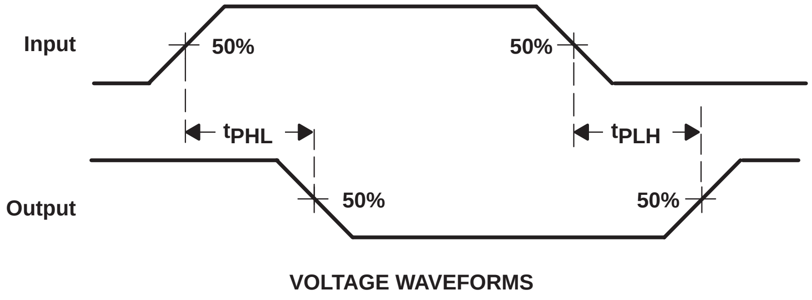
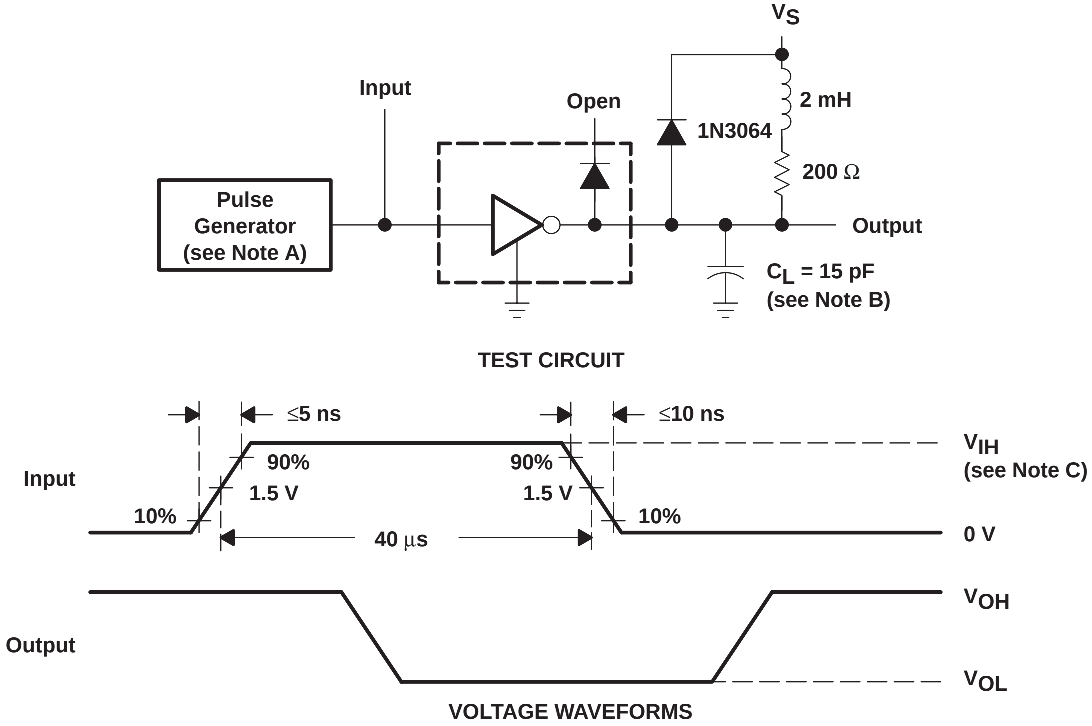


Figure 9. Propagation Delay-Time Waveforms



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.
C. For testing, $V_{IH}$ = 3 V

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

## TYPICAL CHARACTERISTICS

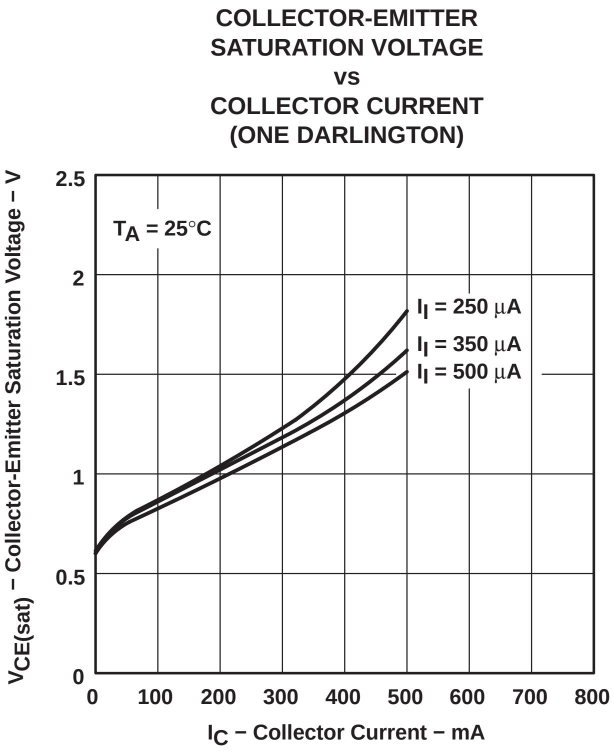


Figure 11

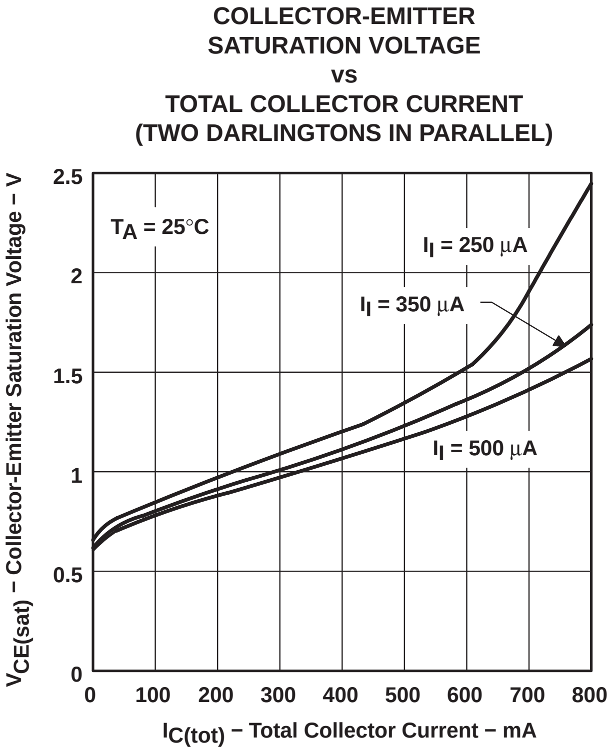


Figure 12

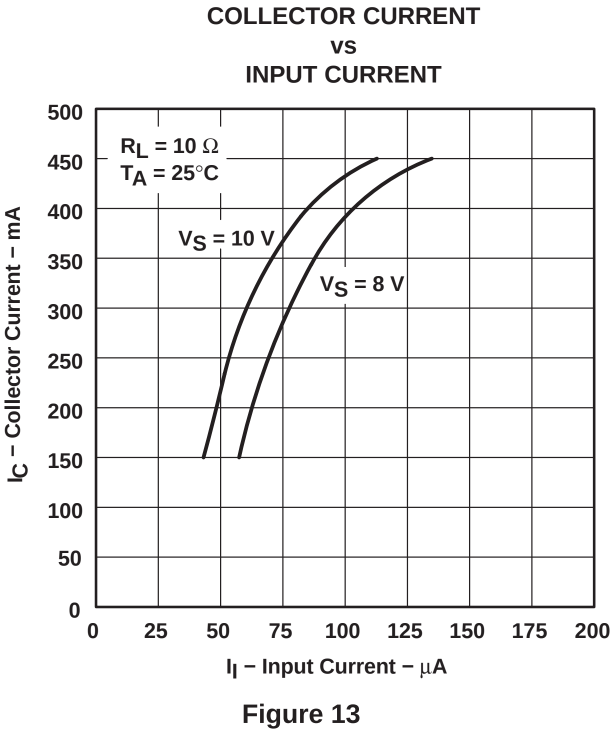


Figure 13

## APPLICATION INFORMATION

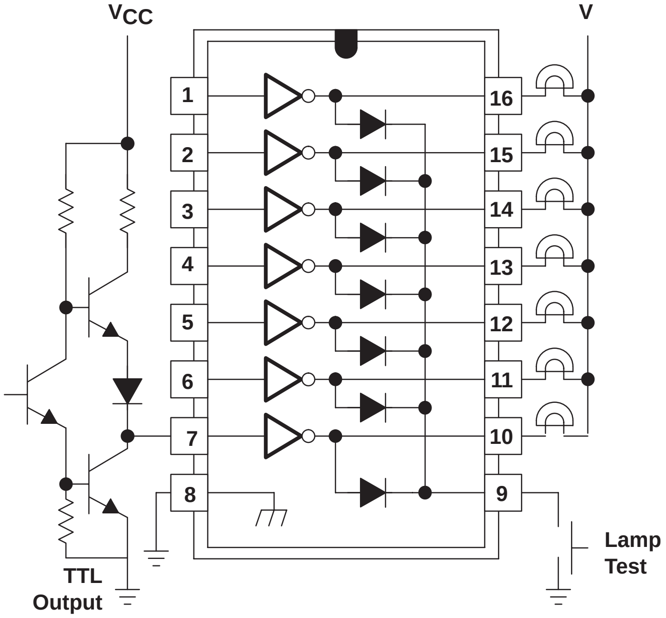


Figure 14. TTL to Load

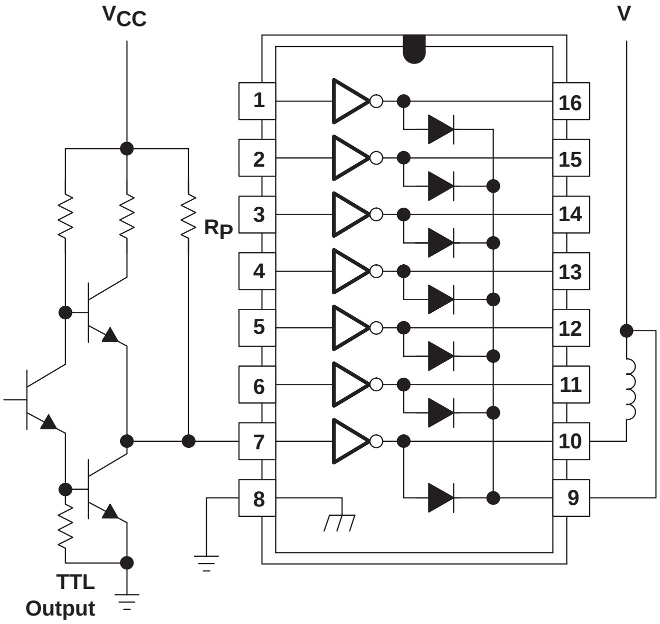


Figure 15. Use of Pullup Resistors to Increase Drive Current

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ULN2004AID | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2004AI | Samples |
| ULN2004AIDR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2004AI | Samples |
| ULN2004AIN | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 105 | ULN2004AIN | Samples |
| ULN2004AINSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2004AI | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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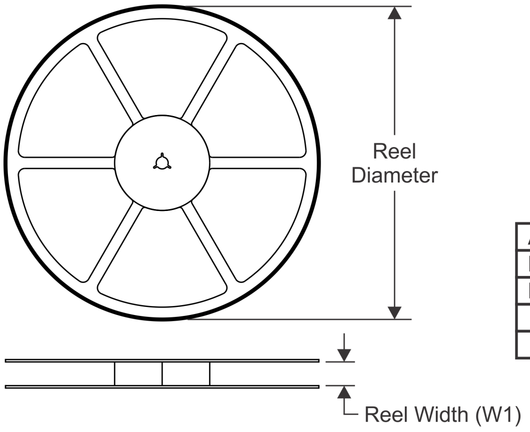
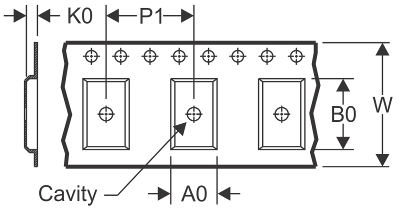
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

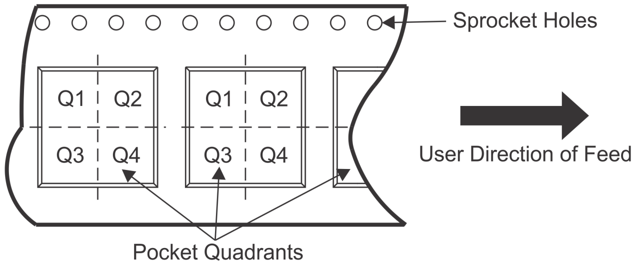


### TAPE DIMENSIONS



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

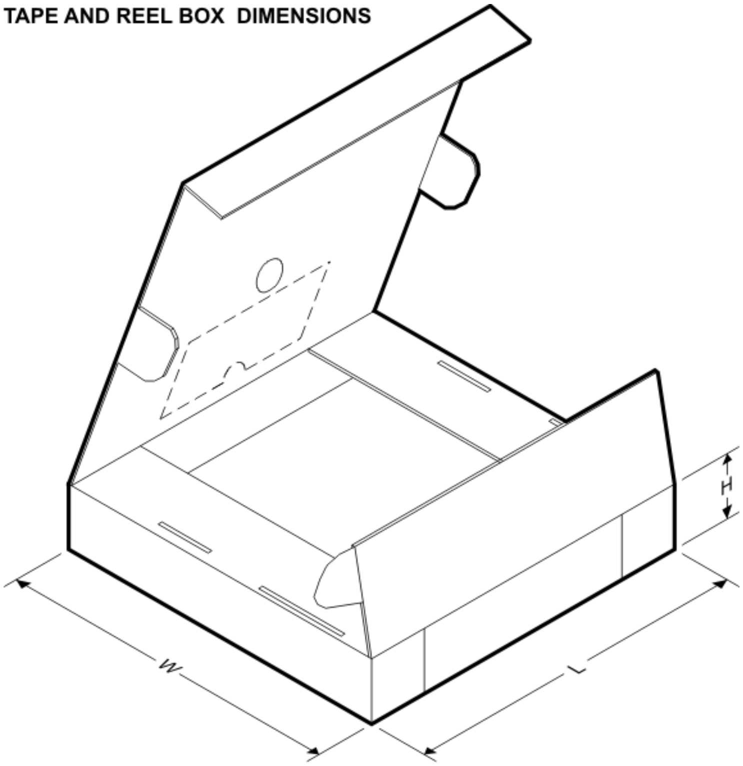
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ULN2004AIDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2004AINSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

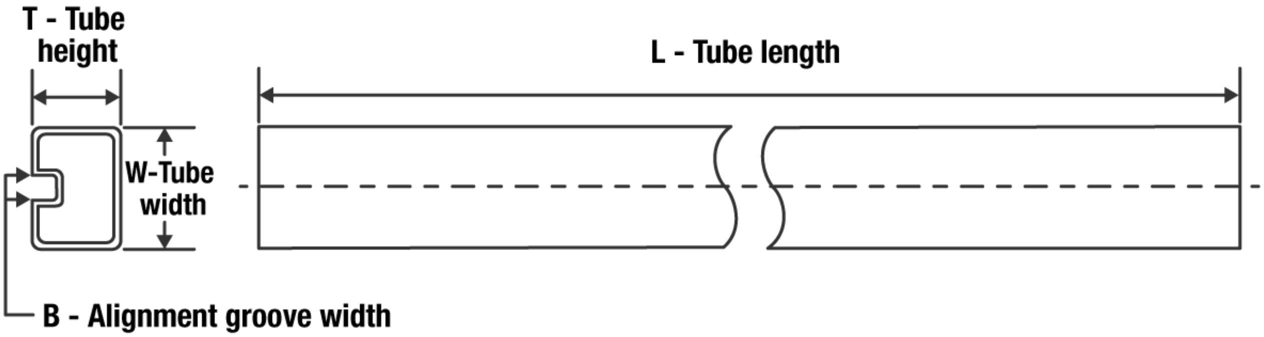
## TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

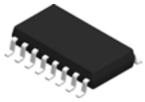
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ULN2004AIDR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| ULN2004AINSR | SO | NS | 16 | 2000 | 853.0 | 449.0 | 35.0 |

## TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| ULN2004AID | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| ULN2004AIN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| ULN2004AIN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

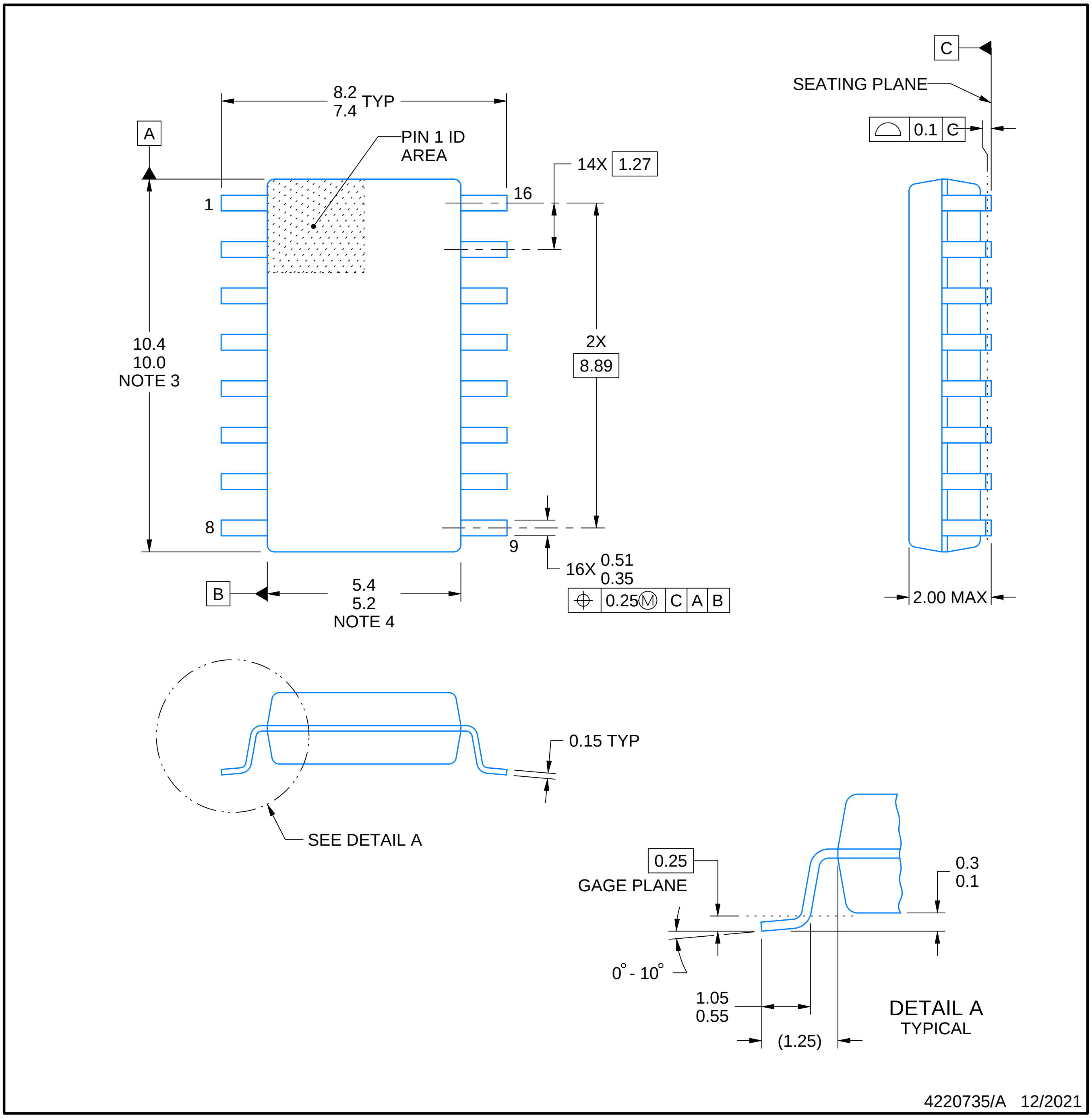


# PACKAGE OUTLINE

# NS0016A

## SOP - 2.00 mm max height

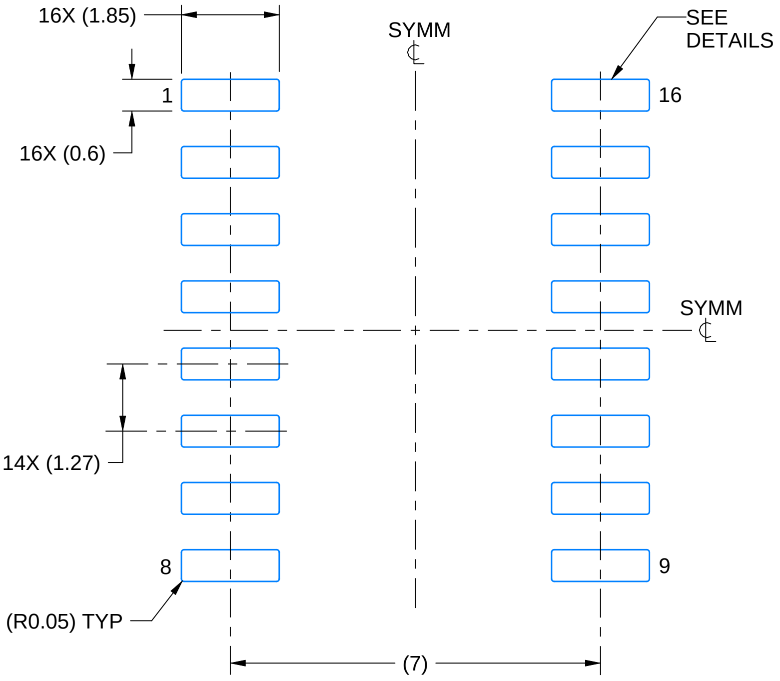
SOP



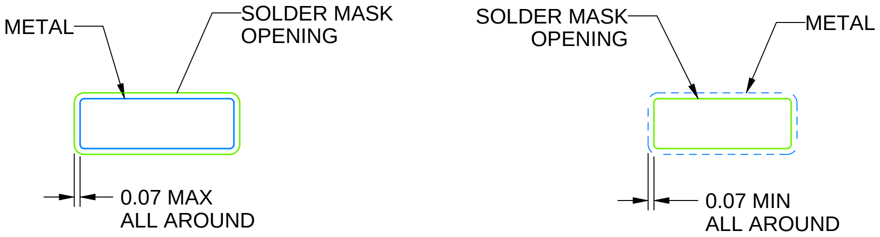
4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK DEFINED

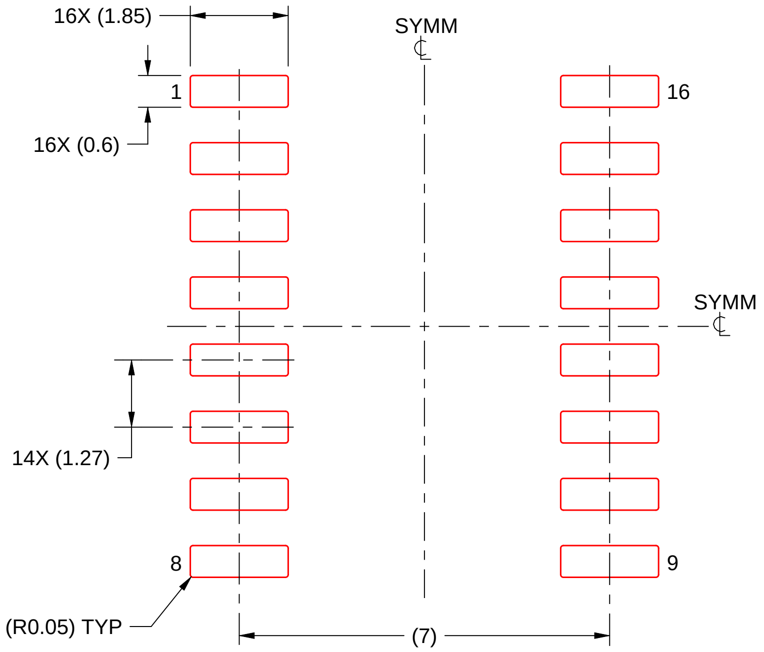
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



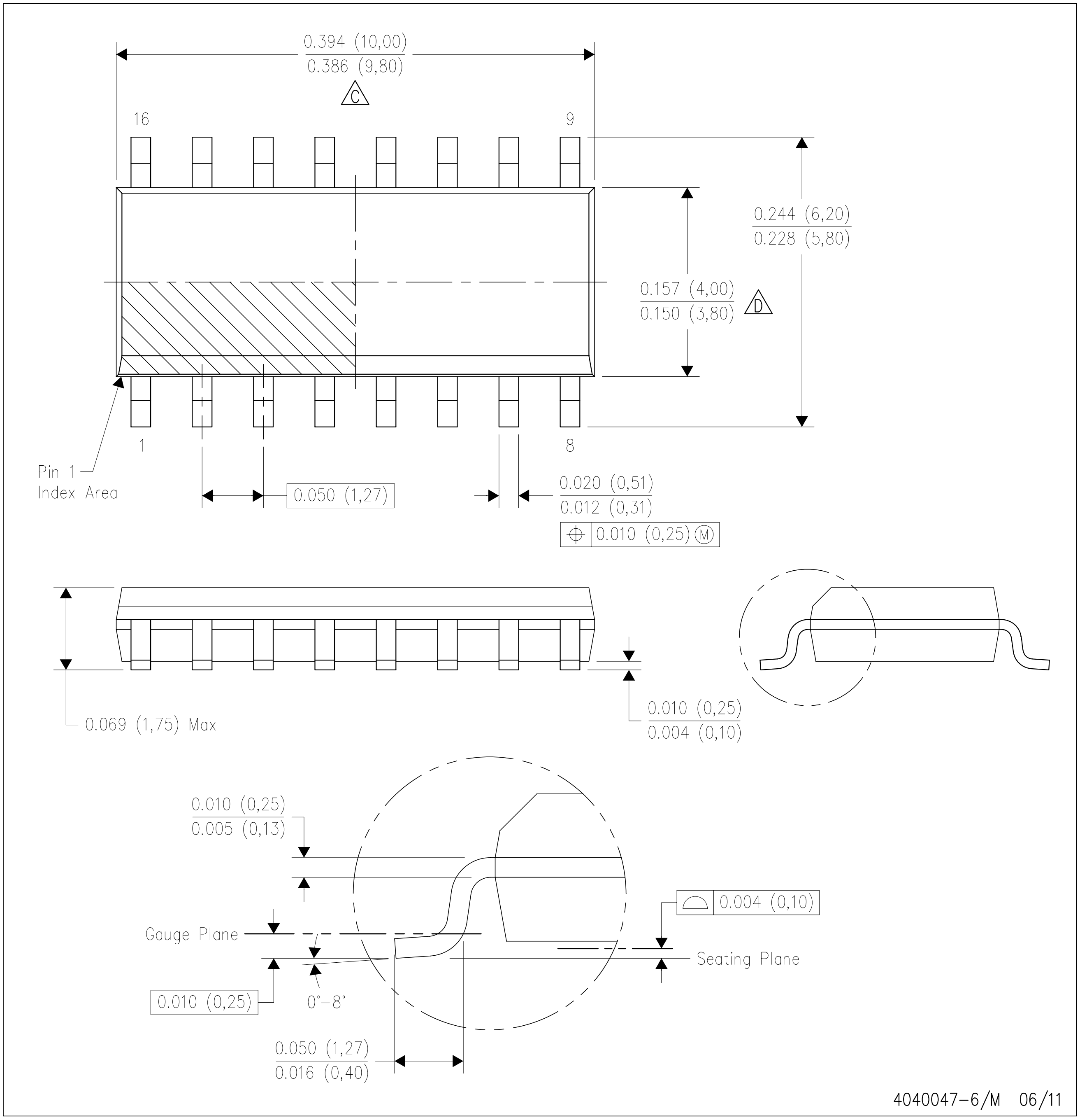
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

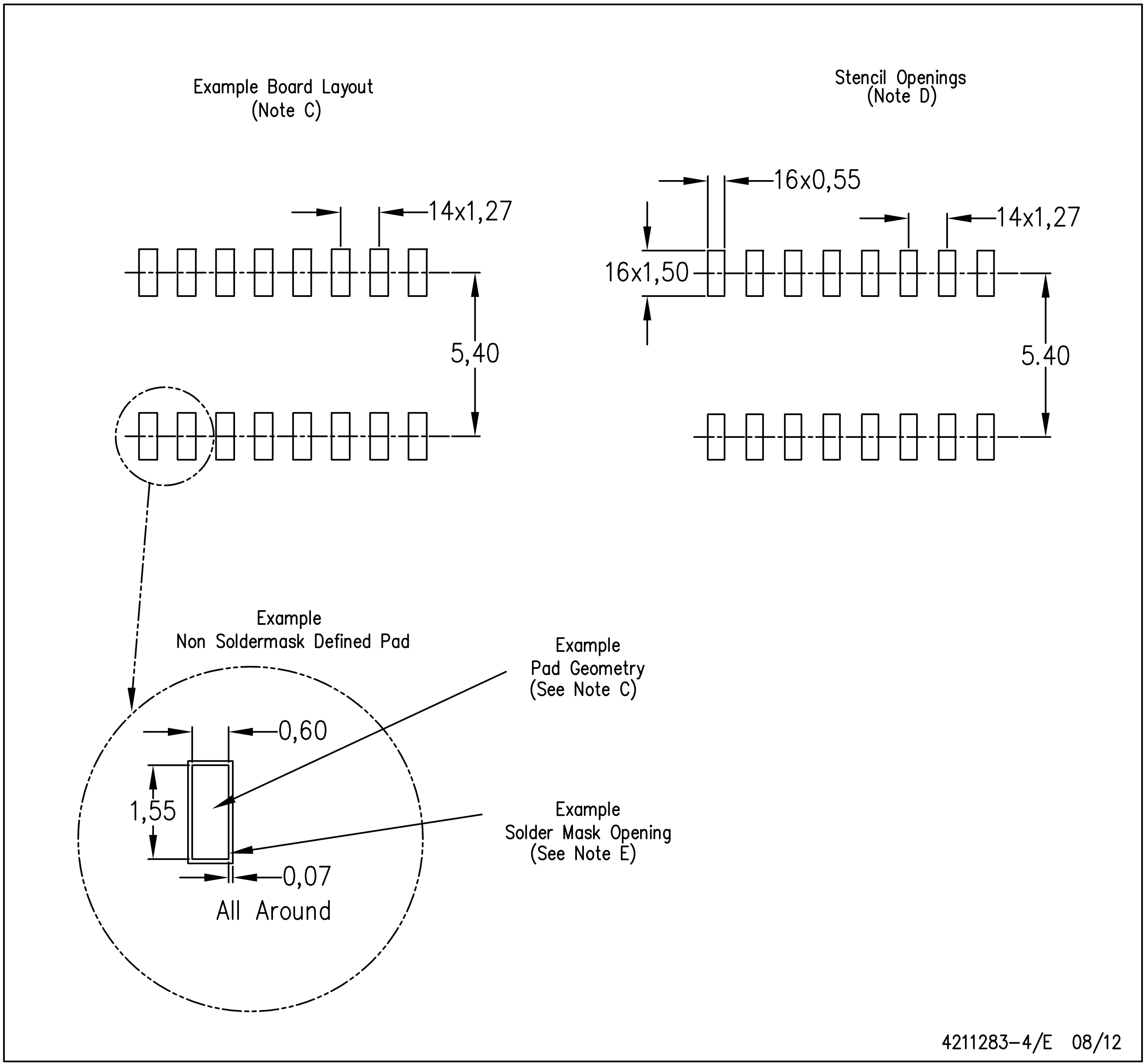
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

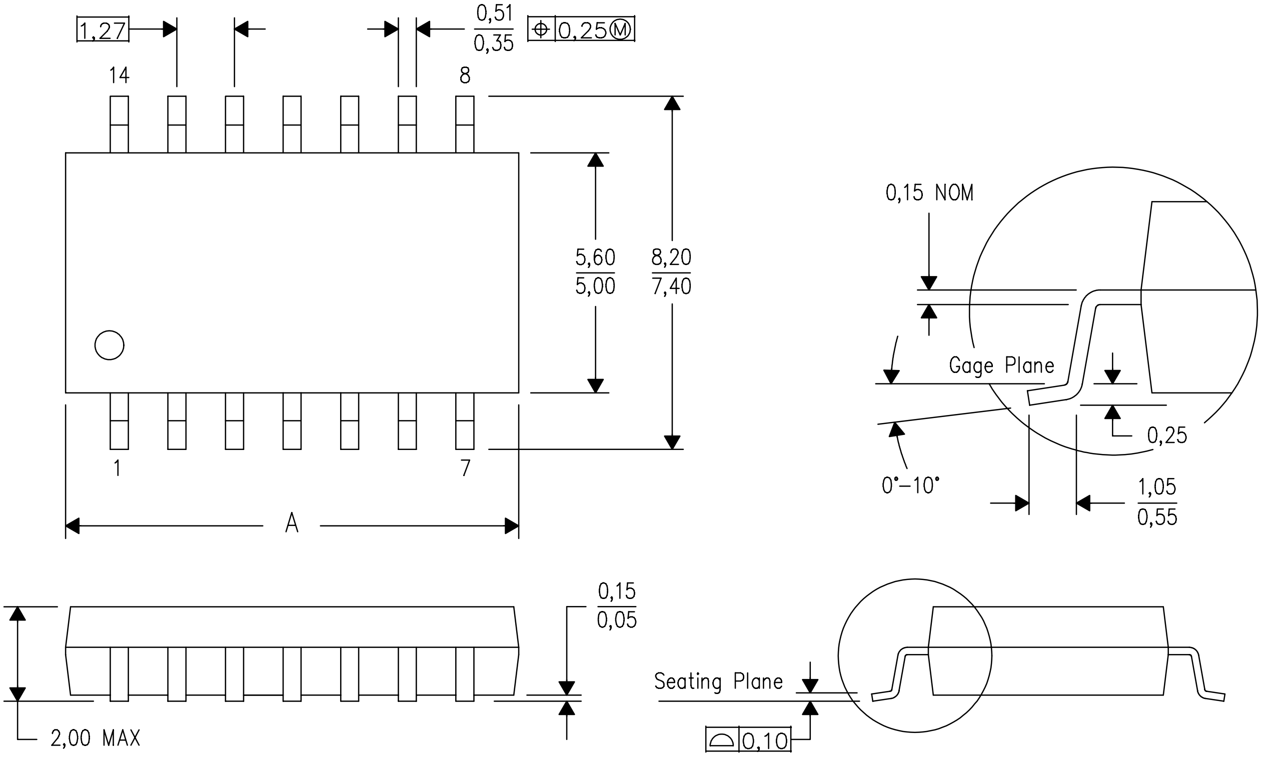


NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



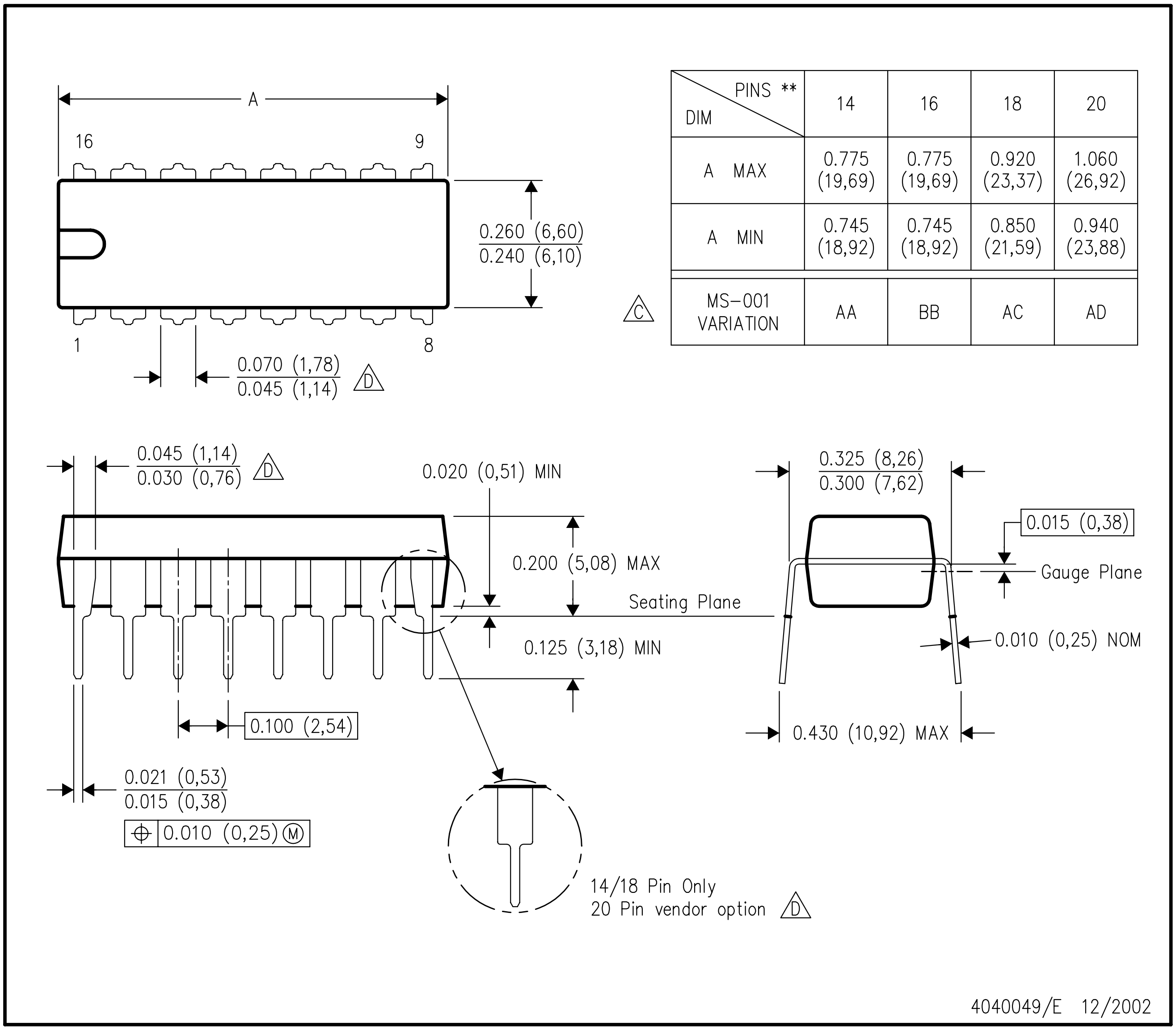
| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS–001 VARIATION | AA | BB | AC | AD |

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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