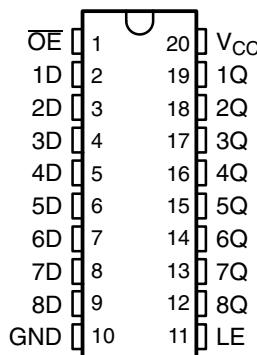


# SN54LV573A, SN74LV573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

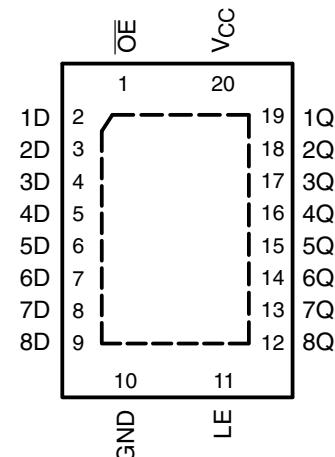
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- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 8 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2.3 V at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

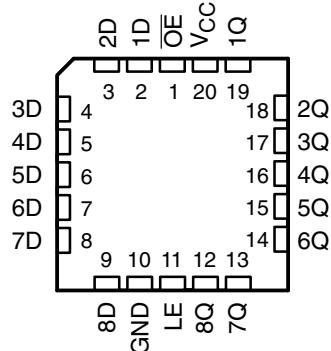
SN54LV573A . . . J OR W PACKAGE  
SN74LV573A . . . DB, DGV, DW, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LV573A . . . RGY PACKAGE  
(TOP VIEW)



SN54LV573A . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV573ARGYR	LV573A
	SOIC – DW	Tube of 25	SN74LV573ADW	LV573A
		Reel of 2000	SN74LV573ADWR	
	SOP – NS	Reel of 2000	SN74LV573ANSR	74LV573A
	SSOP – DB	Reel of 2000	SN74LV573ADBR	LV573A
	TSSOP – PW	Tube of 70	SN74LV573APW	LV573A
		Reel of 2000	SN74LV573APWR	
		Reel of 250	SN74LV573APWT	
-55°C to 125°C	TVSOP – DGV	Reel of 2000	SN74LV573ADGVR	LV573A
	VFBGA – GQN	Reel of 1000	SN74LV573AGQNR	LV573A
	CDIP – J	Tube of 20	SNJ54LV573AJ	SNJ54LV573AJ
	CFP – W	Tube of 85	SNJ54LV573AW	SNJ54LV573AW
	LCCC – FK	Tube of 55	SNJ54LV573AFK	SNJ54LV573AFK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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# SN54LV573A, SN74LV573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## description/ordering information (continued)

The 'LV573A devices are octal transparent D-type latches designed for 2-V to 5.5-V  $V_{CC}$  operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

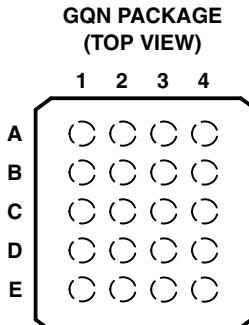
While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



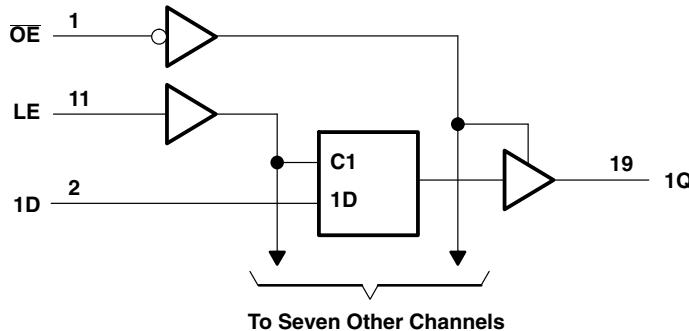
### terminal assignments

	1	2	3	4
A	1D	$\overline{OE}$	$V_{CC}$	1Q
B	3D	3Q	2D	2Q
C	5D	4D	5Q	4Q
D	7D	7Q	6D	6Q
E	GND	8D	LE	8Q

### FUNCTION TABLE (each latch)

INPUTS			OUTPUT Q
OE	LE	D	
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

## logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, FK, J, NS, PW, RGY, and W packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. This value is limited to 5.5 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.  
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

**SN54LV573A, SN74LV573A  
OCTAL TRANSPARENT D-TYPE LATCHES  
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**recommended operating conditions (see Note 5)**

			SN54LV573A		SN74LV573A		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	1.5	V <sub>CC</sub> × 0.7		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> × 0.7			
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> × 0.7			
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> × 0.7			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	0.5	V <sub>CC</sub> × 0.3		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3			
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3			
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3			
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
		3-state	0	5.5	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	–50	–50	–50		μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	–2	–2			
		V <sub>CC</sub> = 3 V to 3.6 V	–8	–8			
		V <sub>CC</sub> = 4.5 V to 5.5 V	–16	–16			
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50	50	50	50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	2	2	2	2	mA
		V <sub>CC</sub> = 3 V to 3.6 V	8	8	8	8	
		V <sub>CC</sub> = 4.5 V to 5.5 V	16	16	16	16	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V	200	200	200	200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V	100	100	100	100	
		V <sub>CC</sub> = 4.5 V to 5.5 V	20	20	20	20	
T <sub>A</sub>	Operating free-air temperature		–55	125	–40	85	°C

NOTE 5: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LV573A			SN74LV573A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	2 V to 5.5 V	V <sub>CC</sub> – 0.1			V <sub>CC</sub> – 0.1			V
	I <sub>OH</sub> = –2 mA	2.3 V	2			2			
	I <sub>OH</sub> = –8 mA	3 V	2.48			2.48			
	I <sub>OH</sub> = –16 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V		0.1		0.1			V
	I <sub>OL</sub> = 2 mA	2.3 V		0.4		0.4			
	I <sub>OL</sub> = 8 mA	3 V		0.44		0.44			
	I <sub>OL</sub> = 16 mA	4.5 V		0.55		0.55			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		±1		±1			μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V		±5		±5			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		20		20			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0		5		5			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		1.8		1.8			pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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**SN54LV573A, SN74LV573A  
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**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER		$T_A = 25^\circ\text{C}$		SN54LV573A		SN74LV573A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	LE high	6.5	6.5	6.5	6.5	6.5	ns
$t_{su}$	Setup time	Data before LE $\downarrow$	5	5	5	5	5	ns
$t_h$	Hold time	Data after LE $\downarrow$	2	2	2	2	2	ns

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER		$T_A = 25^\circ\text{C}$		SN54LV573A		SN74LV573A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	LE high	5	5	5	5	5	ns
$t_{su}$	Setup time	Data before LE $\downarrow$	3.5	3.5	3.5	3.5	3.5	ns
$t_h$	Hold time	Data after LE $\downarrow$	1.5	1.5	1.5	1.5	1.5	ns

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER		$T_A = 25^\circ\text{C}$		SN54LV573A		SN74LV573A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	LE high	5	5	5	5	5	ns
$t_{su}$	Setup time	Data before LE $\downarrow$	3.5	3.5	3.5	3.5	3.5	ns
$t_h$	Hold time	Data after LE $\downarrow$	1.5	1.5	1.5	1.5	1.5	ns

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			UNIT	
				MIN	TYP	MAX		
$t_{pd}$	D	Q	$C_L = 15 \text{ pF}$	8.9*	15.8*	1*	18*	1
	LE	Q		9.6*	16.2*	1*	19*	1
$t_{en}$	OE	Q		9.3*	16.2*	1*	19*	1
$t_{dis}$	$\overline{OE}$	Q		6.7*	12.6*	1*	15*	1
$t_{pd}$	D	Q	$C_L = 50 \text{ pF}$	10.9	18.7	1	21	1
	LE	Q		11.6	19.1	1	23	1
$t_{en}$	$\overline{OE}$	Q		11.4	19	1	22	1
$t_{dis}$	$\overline{OE}$	Q		8.6	17.3	1	19	1
$t_{sk(o)}$					2			2

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV573A		SN74LV573A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	D	Q	$C_L = 15 \text{ pF}$	6.2*	11*	1*	13*	1	13		ns
	LE	Q		6.8*	11.9*	1*	14*	1	14		
$t_{en}$	$\overline{OE}$	Q	$C_L = 50 \text{ pF}$	6.6*	11.5*	1*	13.5*	1	13.5		ns
$t_{dis}$	$\overline{OE}$	Q		4.9*	11*	1*	13*	1	13		
$t_{pd}$	D	Q	$C_L = 50 \text{ pF}$	7.7	14.5	1	16.5	1	16.5		ns
	LE	Q		8.2	15.4	1	17.5	1	17.5		
$t_{en}$	$\overline{OE}$	Q	$C_L = 50 \text{ pF}$	8	15	1	17	1	17		ns
$t_{dis}$	$\overline{OE}$	Q		6.2	14.5	1	16.5	1	16.5		
$t_{sk(o)}$					1.5				1.5		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV573A		SN74LV573A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	D	Q	$C_L = 15 \text{ pF}$	4.3*	6.8*	1*	8*	1	8		ns
	LE	Q		4.7*	7.7*	1*	9*	1	9		
$t_{en}$	$\overline{OE}$	Q	$C_L = 15 \text{ pF}$	4.7*	7.7*	1*	9*	1	9		ns
$t_{dis}$	$\overline{OE}$	Q		3.5*	7.7*	1*	9*	1	9		
$t_{pd}$	D	Q	$C_L = 50 \text{ pF}$	5.3	8.8	1	10	1	10		ns
	LE	Q		5.7	9.7	1	11	1	11		
$t_{en}$	$\overline{OE}$	Q	$C_L = 50 \text{ pF}$	5.7	9.7	1	11	1	11		ns
$t_{dis}$	$\overline{OE}$	Q		4.2	9.7	1	11	1	11		
$t_{sk(o)}$					1				1		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**noise characteristics,  $V_{CC} = 3.3 \text{ V}$ ,  $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 6)**

PARAMETER		SN74LV573A			UNIT	
		MIN	TYP	MAX		
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$			0.6	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$			-0.5	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$			2.9		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99		V

NOTE 6: Characteristics are for surface-mount packages only.

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**operating characteristics,  $T_A = 25^\circ\text{C}$**

PARAMETER			TEST CONDITIONS		$V_{CC}$	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	Outputs enabled	D to Q	$C_L = 50 \text{ pF}$ , $f = 10 \text{ MHz}$		3.3 V	16	pF
		LE to Q			5 V	18	
					3.3 V	18.2	
					5 V	21.3	

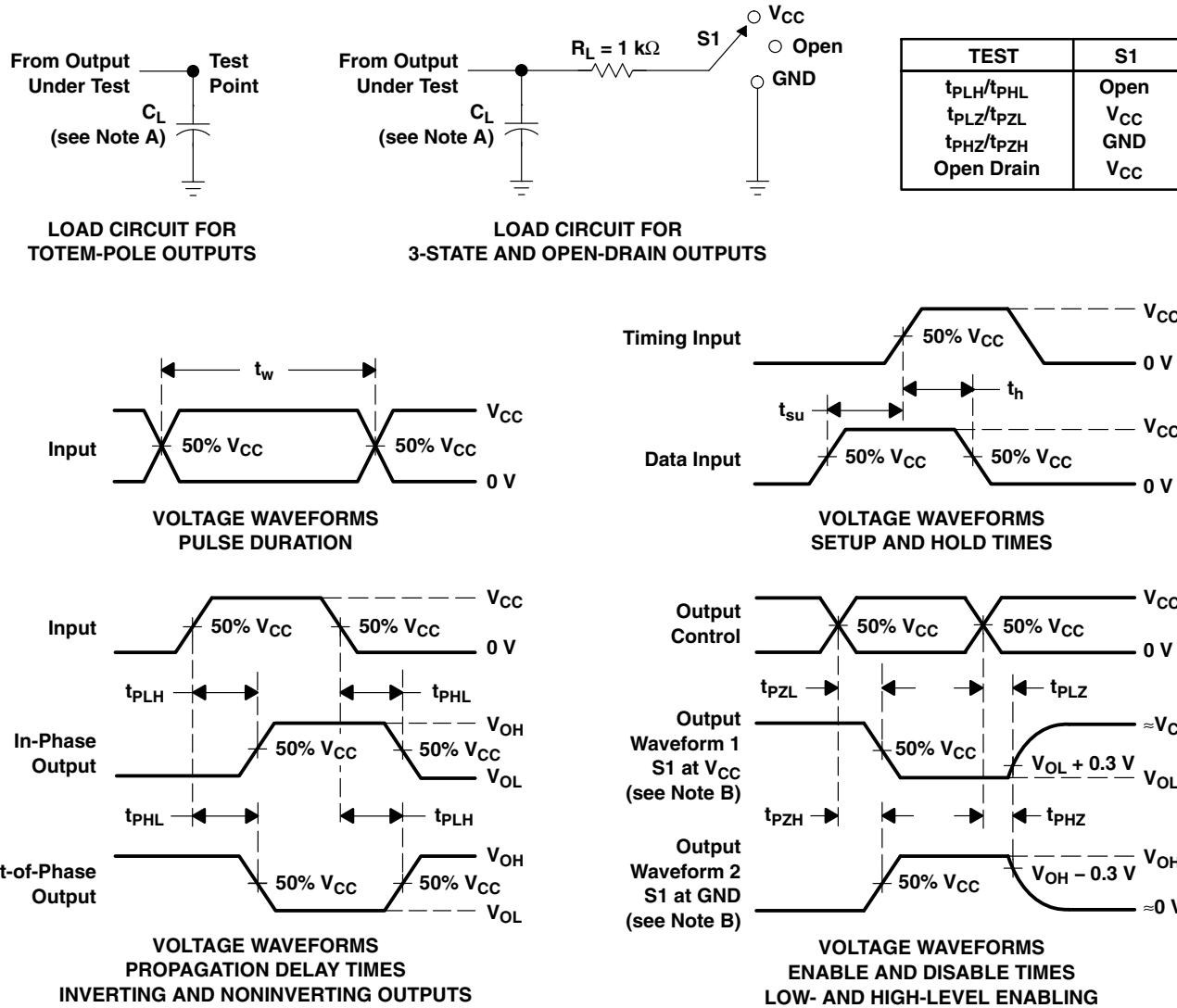


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## PARAMETER MEASUREMENT INFORMATION



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
- The outputs are measured one at a time, with one input transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV573ADBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LV573ADBRG4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LV573ADGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LV573ADW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LV573ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LV573ANSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV573A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LV573APW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LV573APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LV573APWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LV573APWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LV573APWT	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LV573ARGYR	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LV573A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LV573ARGYRG4	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LV573A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

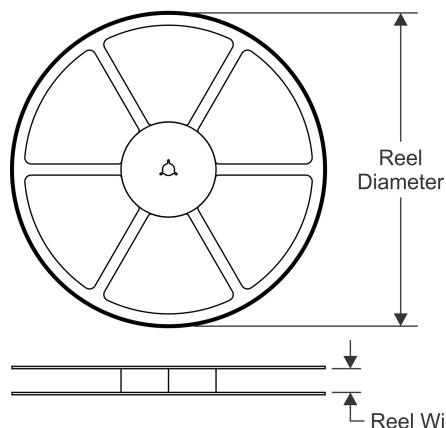
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

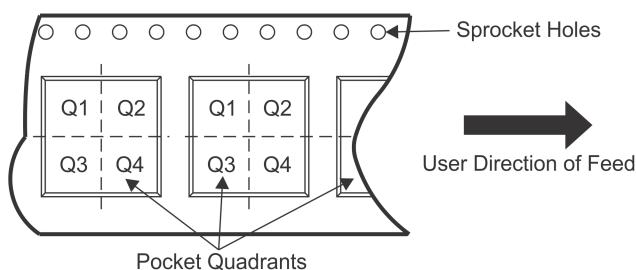
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


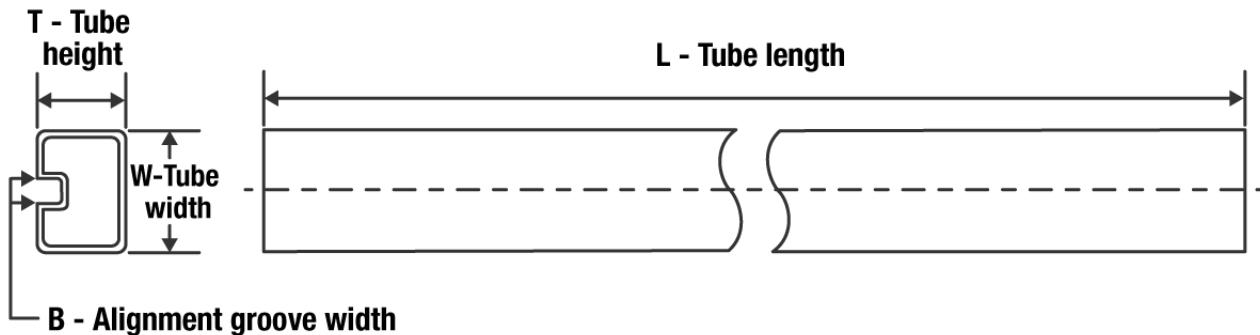
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV573ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV573ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV573ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV573ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV573APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV573APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LV573ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV573ADBR	SSOP	DB	20	2000	853.0	449.0	35.0
SN74LV573ADGVR	TVSOP	DGV	20	2000	853.0	449.0	35.0
SN74LV573ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LV573ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LV573APWR	TSSOP	PW	20	2000	853.0	449.0	35.0
SN74LV573APWT	TSSOP	PW	20	250	853.0	449.0	35.0
SN74LV573ARGYR	VQFN	RGY	20	3000	853.0	449.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LV573ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LV573APW	PW	TSSOP	20	70	530	10.2	3600	3.5

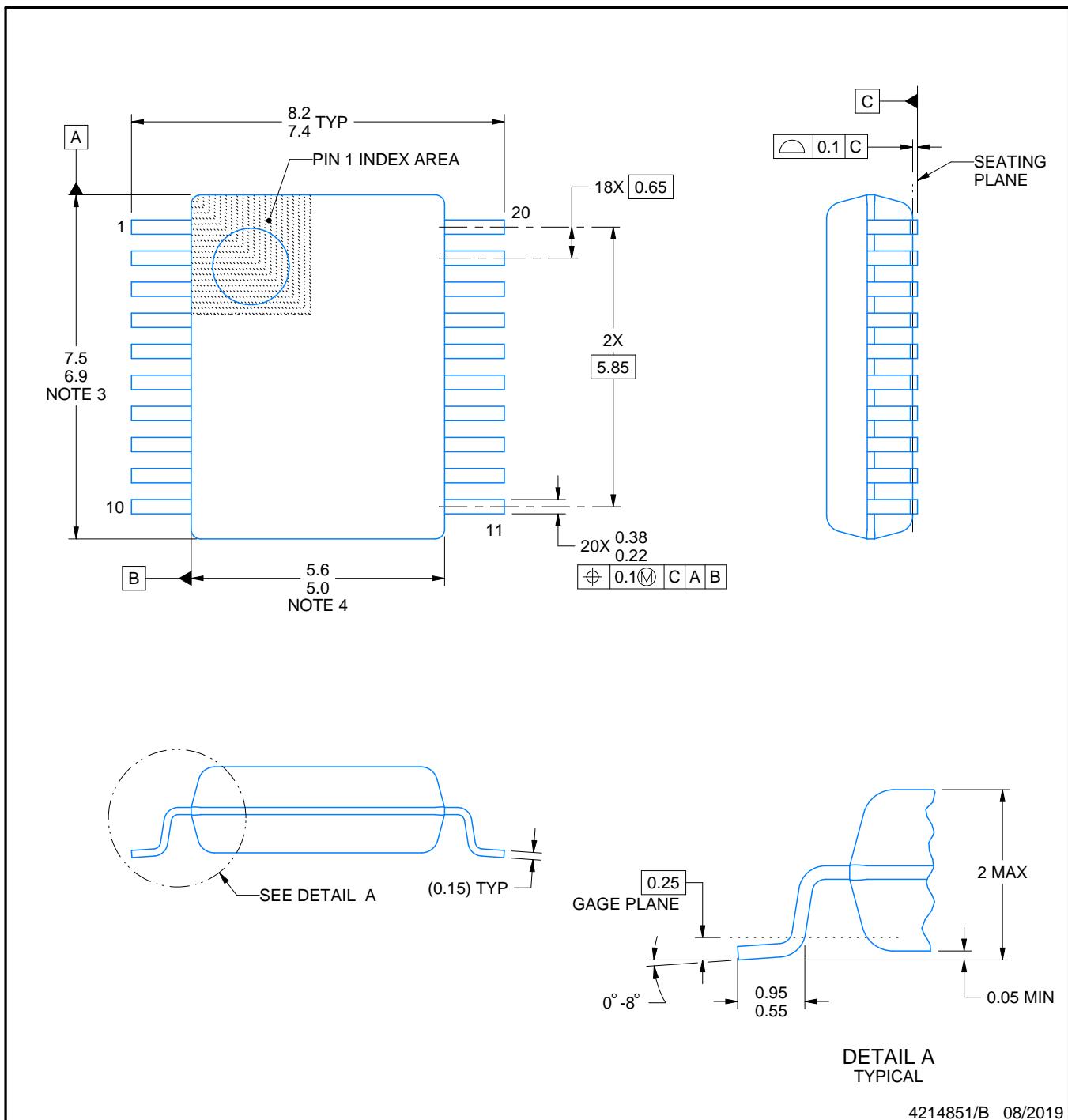
# PACKAGE OUTLINE

DB0020A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

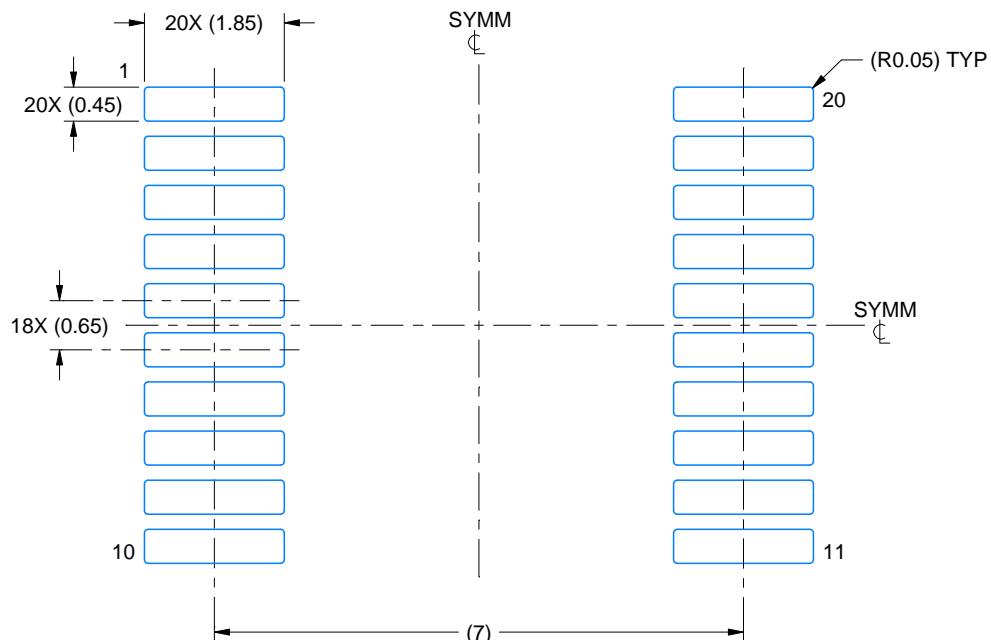
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

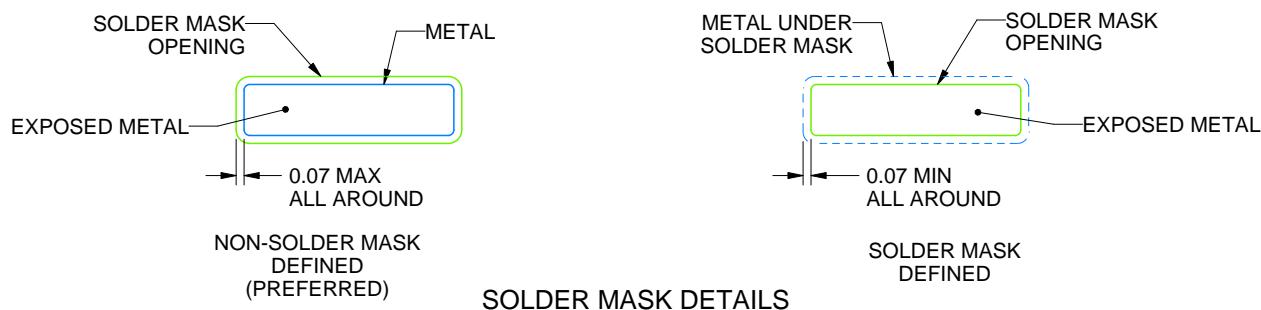
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

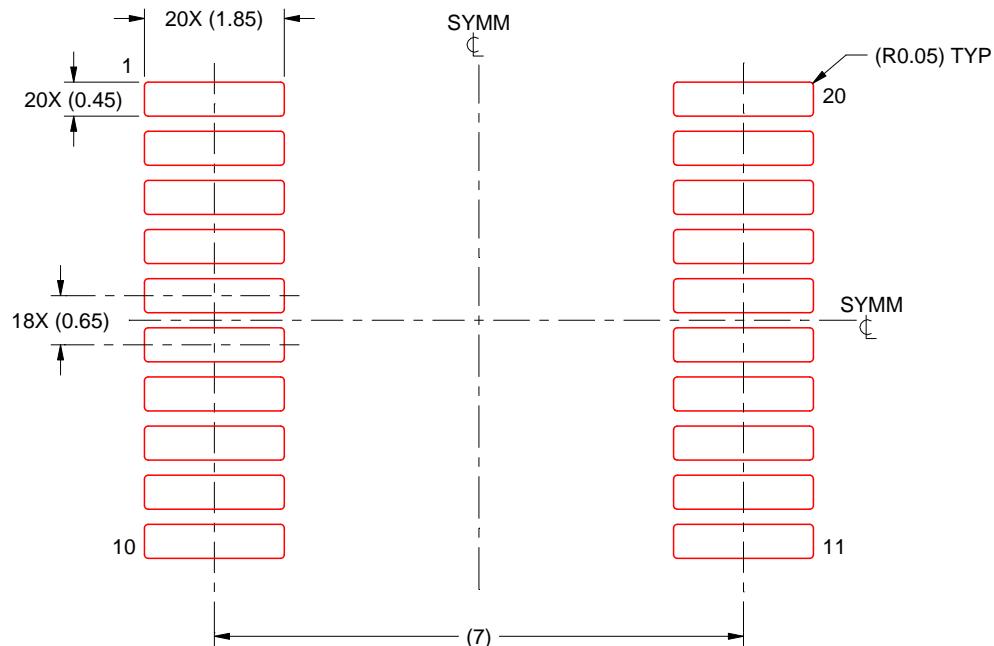
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



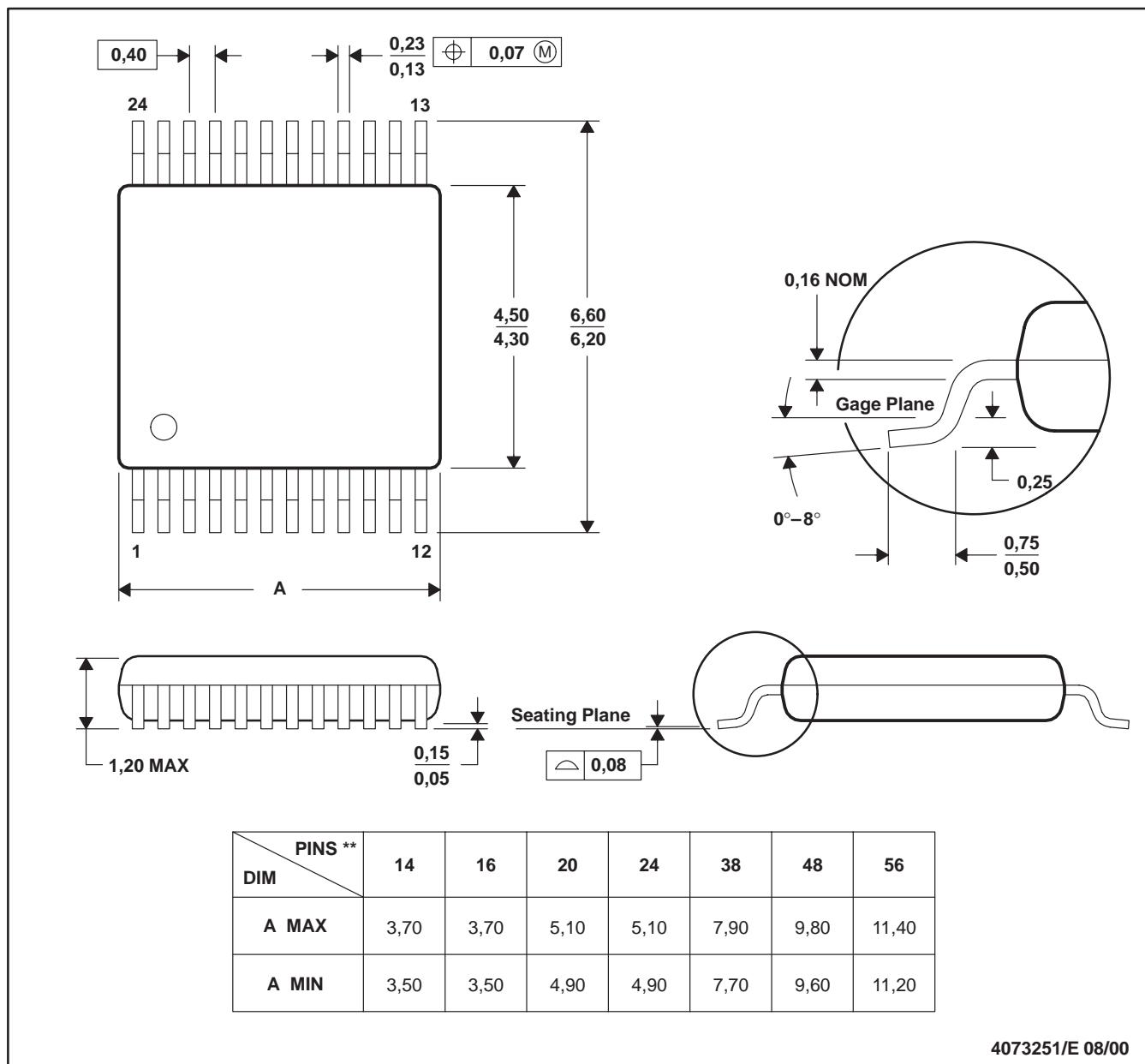
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

# GENERIC PACKAGE VIEW

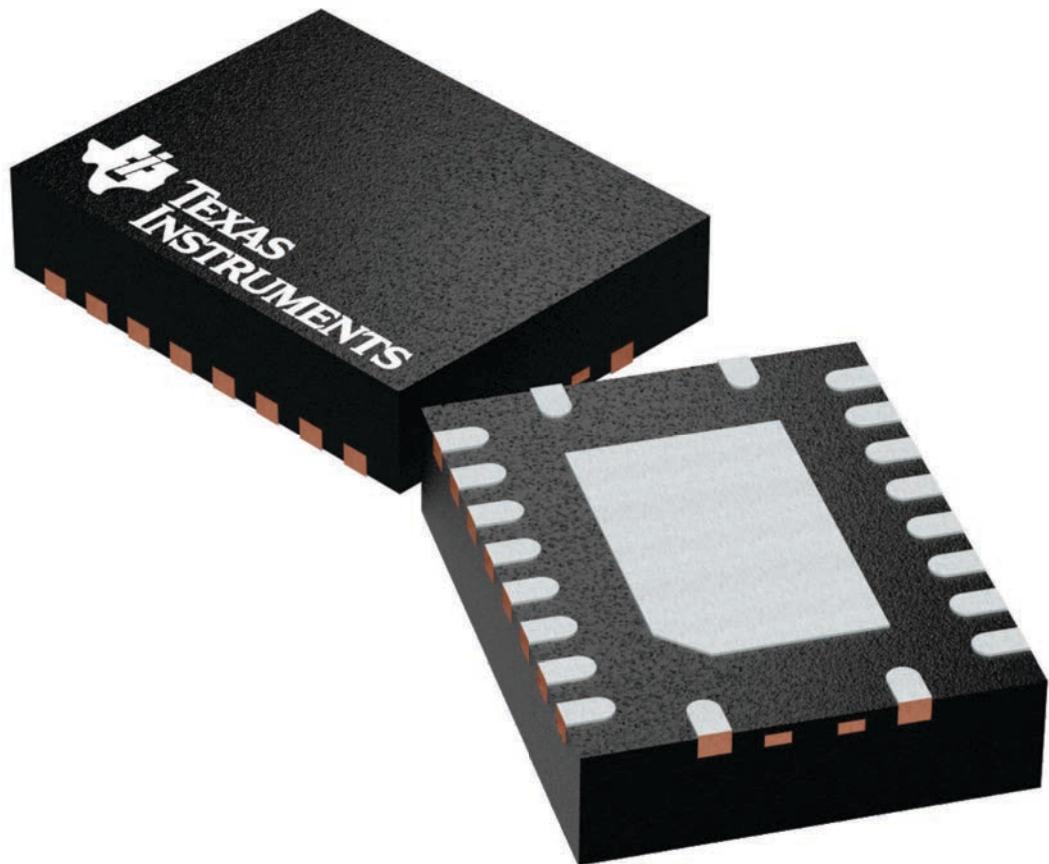
**RGY 20**

**VQFN - 1 mm max height**

**3.5 x 4.5, 0.5 mm pitch**

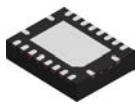
**PLASTIC QUAD FGLATPACK - NO LEAD**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A

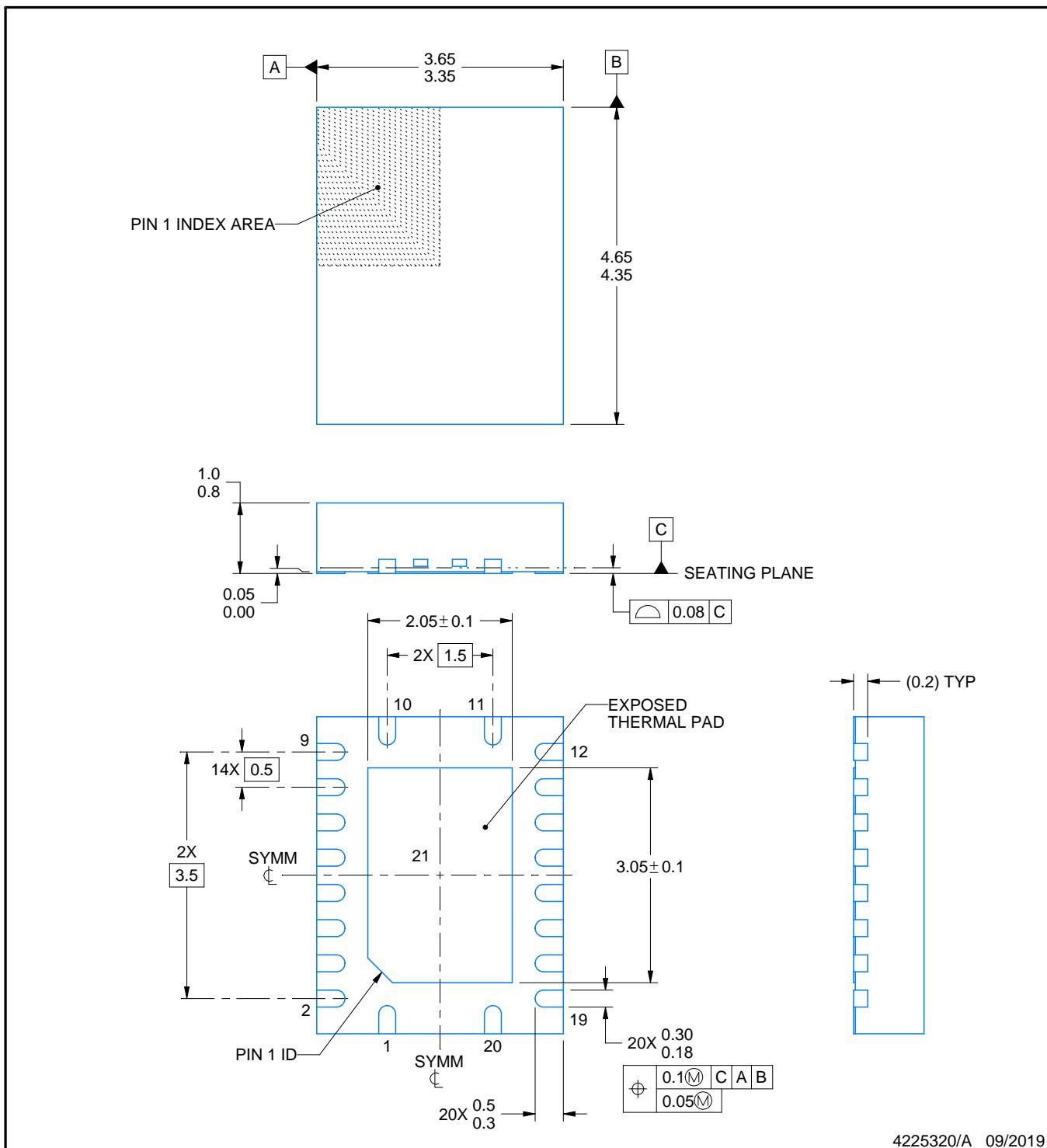
**RGY0020A**



**PACKAGE OUTLINE**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4225320/A 09/2019

**NOTES:**

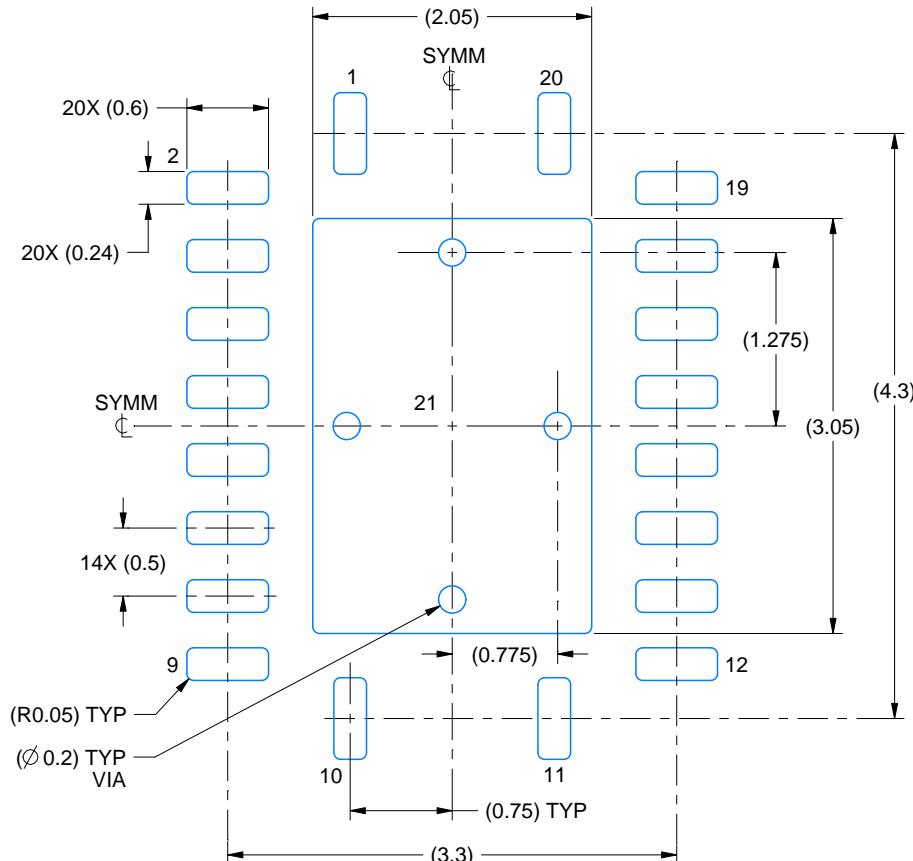
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

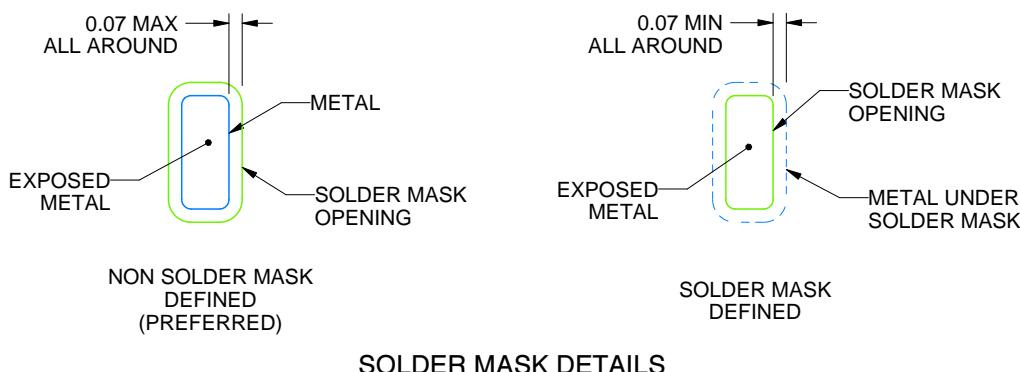
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

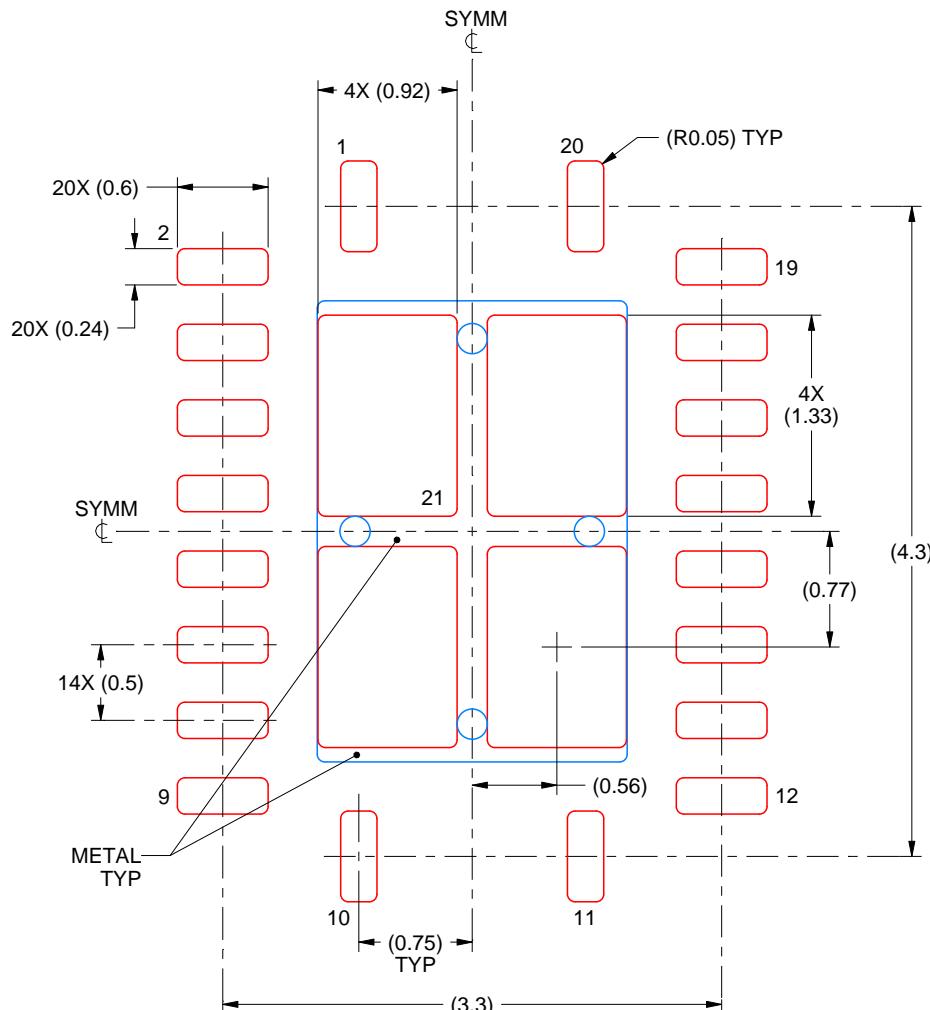
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

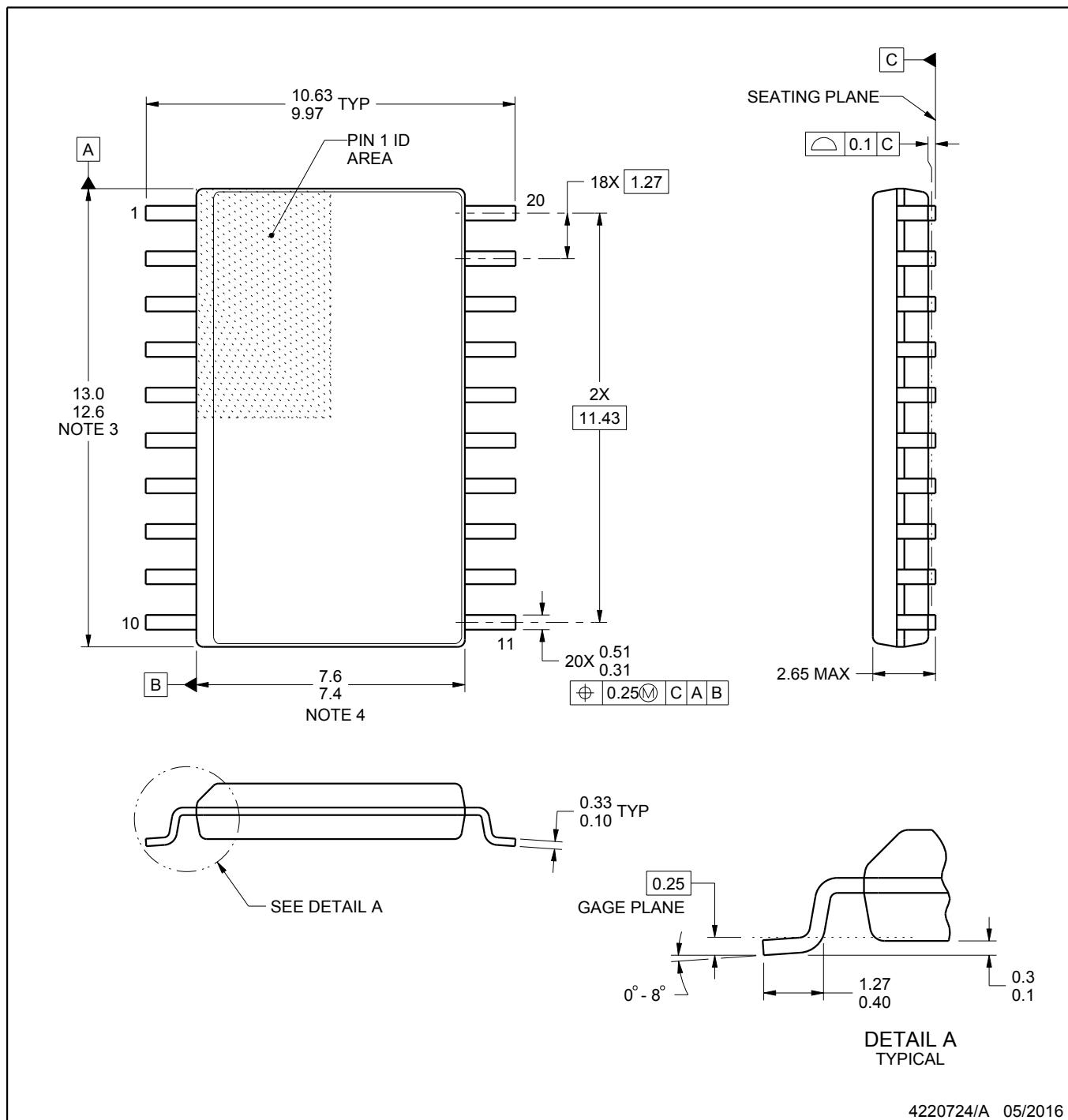


## PACKAGE OUTLINE

**DW0020A**

## **SOIC - 2.65 mm max height**

SOIC



## NOTES:

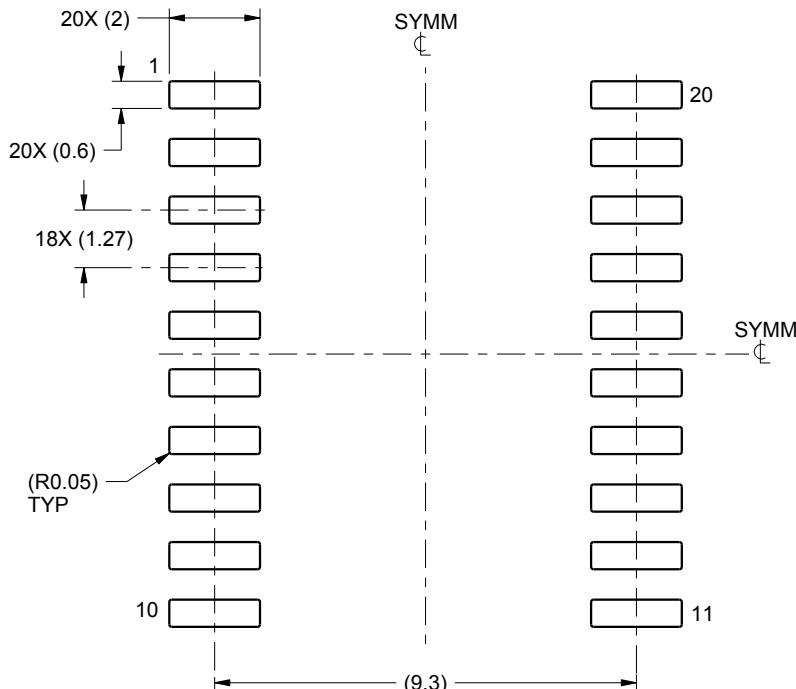
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

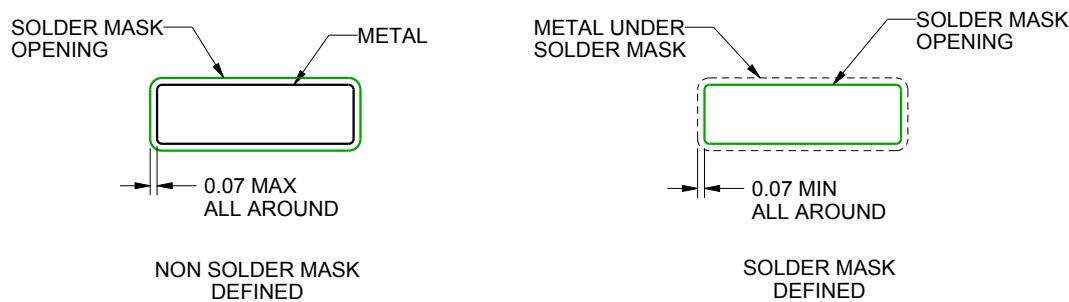
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

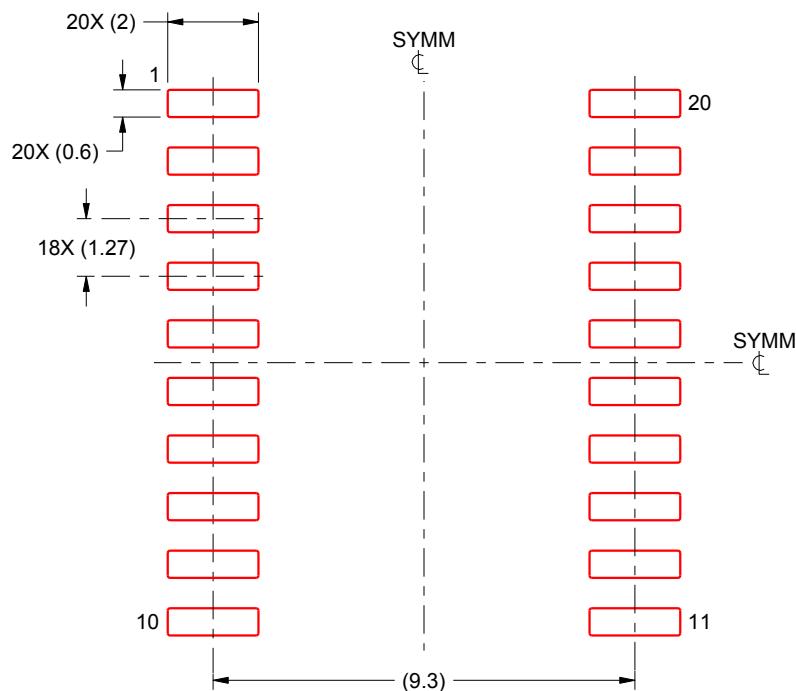
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

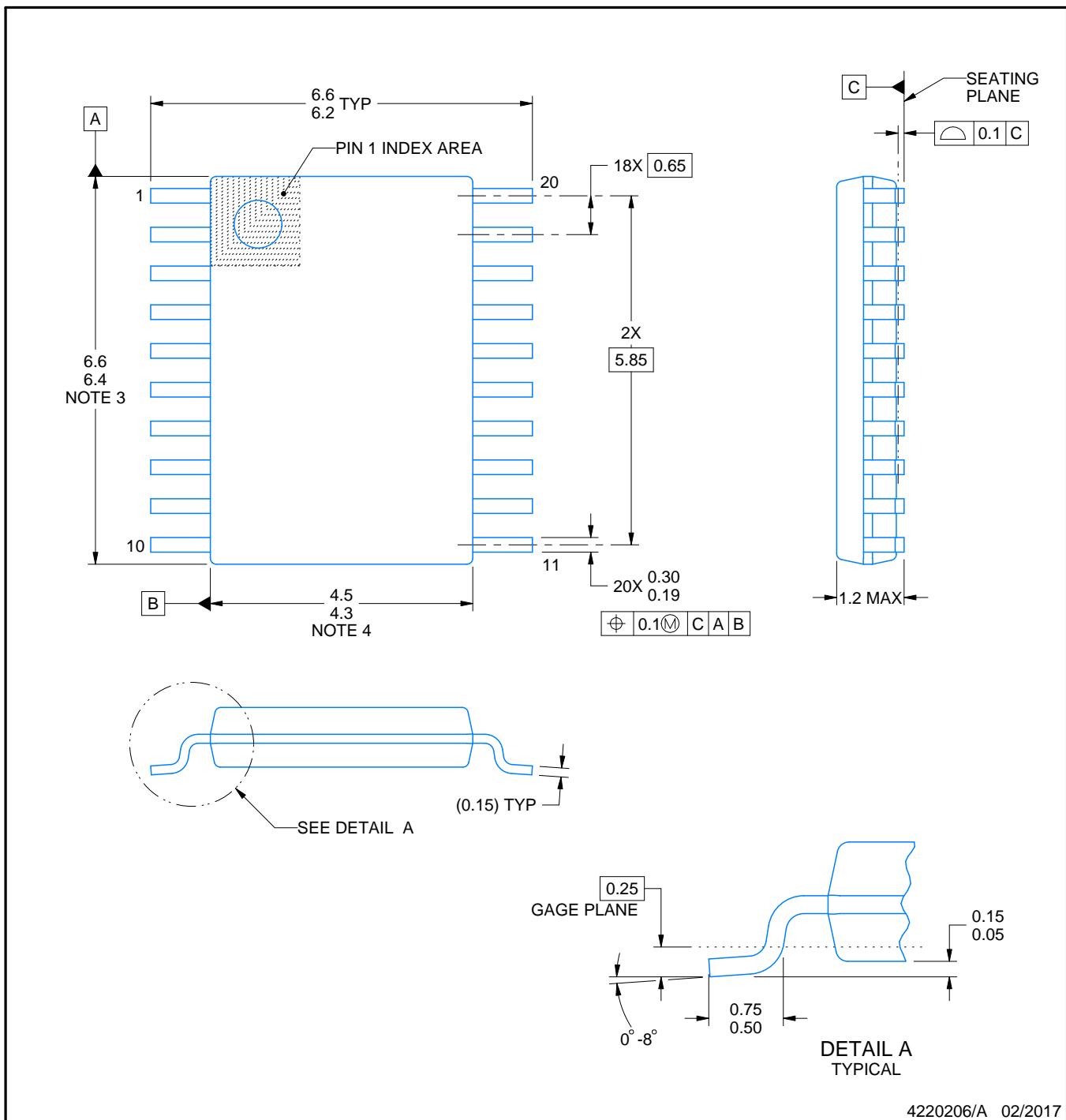
## PACKAGE OUTLINE

**PW0020A**



## **TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



## NOTES:

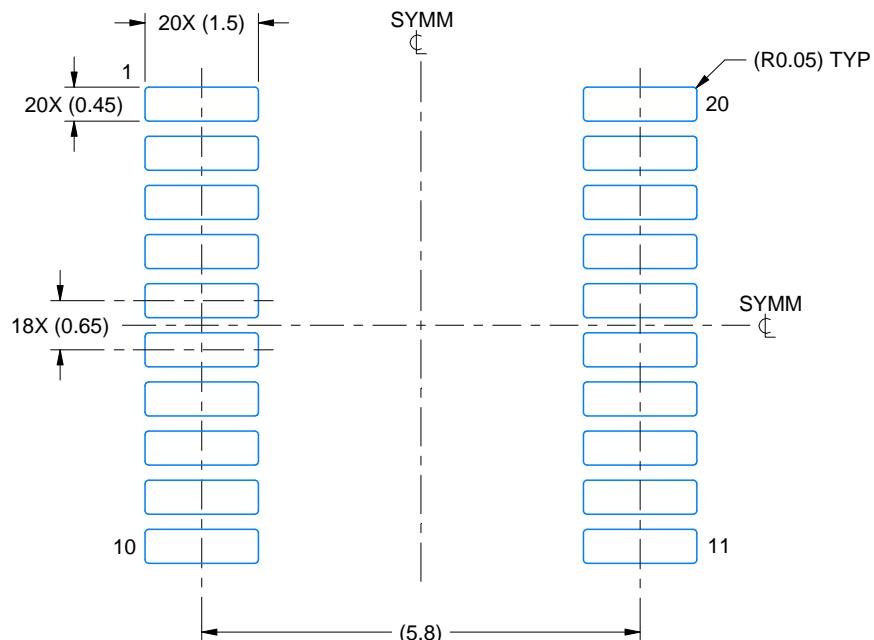
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

## EXAMPLE BOARD LAYOUT

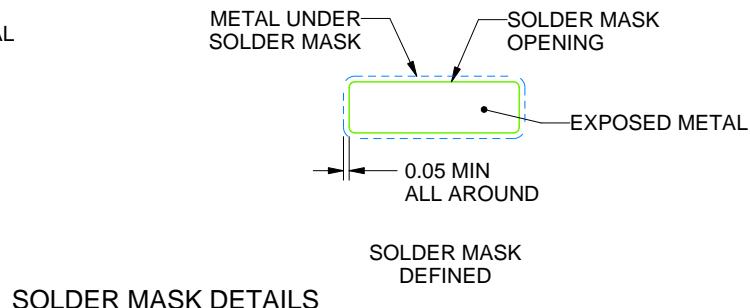
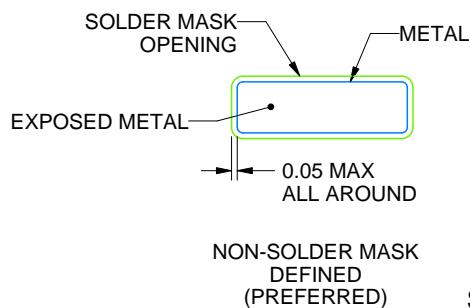
**PW0020A**

## **TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

#### NOTES: (continued)

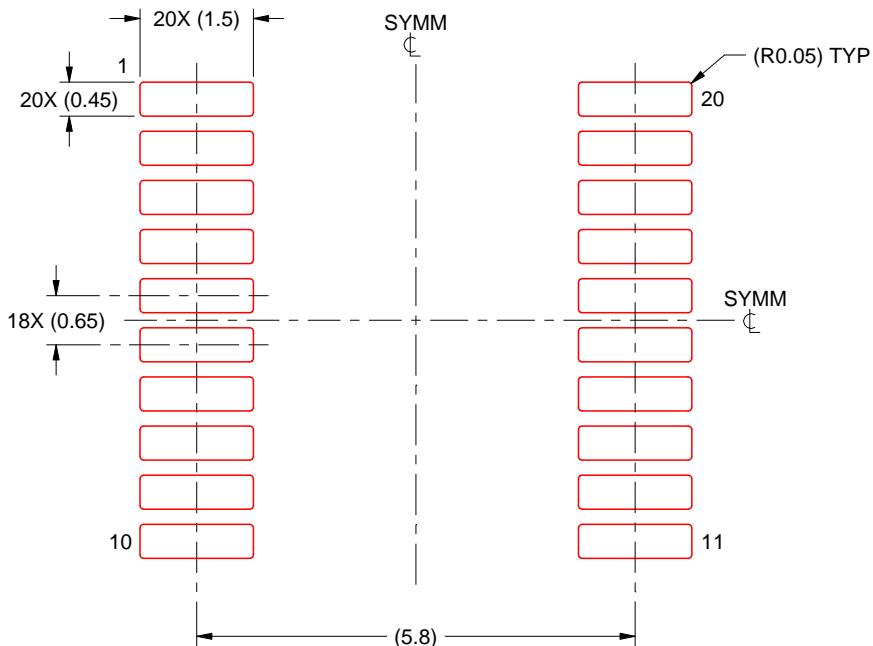
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

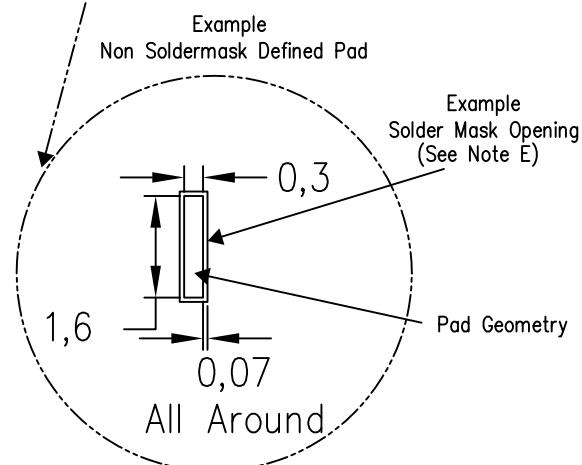
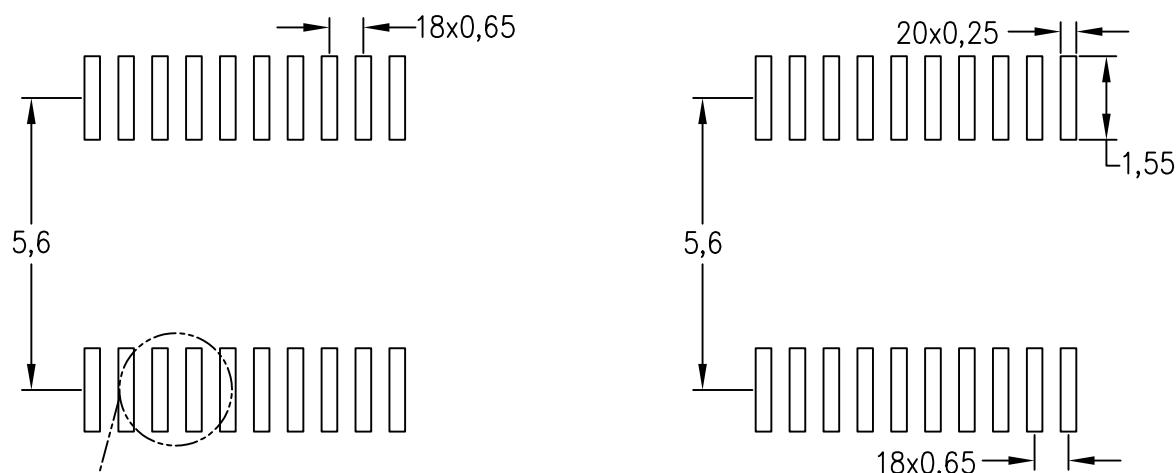
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

## Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).

4211284-5/G 08/15

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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