

TLV225x, TLV225xA Advanced LinCMOS™ RAIL-TO-RAIL VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

- Output Swing Includes Both Supply Rails
- Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Very Low Power . . . 34 μA Per Channel Typ
- Common-Mode Input Voltage Range Includes Negative Rail
- Low Input Offset Voltage
850 μV Max at T_A = 25°C
- Wide Supply Voltage Range
2.7 V to 8 V
- Macromodel Included
- Available in Q-Temp Automotive
HighRel Automotive Applications
Configuration Control / Print Support
Qualification to Automotive Standards

description

The TLV2252 and TLV2254 are dual and quad low-voltage operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLV225x family consumes only 34 μA of supply current per channel. This micropower operation makes them good choices for battery-powered applications. This family is fully characterized at 3 V and 5 V and is optimized for low-voltage applications. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. The TLV225x has a noise level of 19 nV/√Hz at 1kHz, four times lower than competitive micropower solutions.

The TLV225x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV225xA family is available and has a maximum input offset voltage of 850 μV.

The TLV2252/4 also make great upgrades to the TLV2322/4 in standard designs. They offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442 devices. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

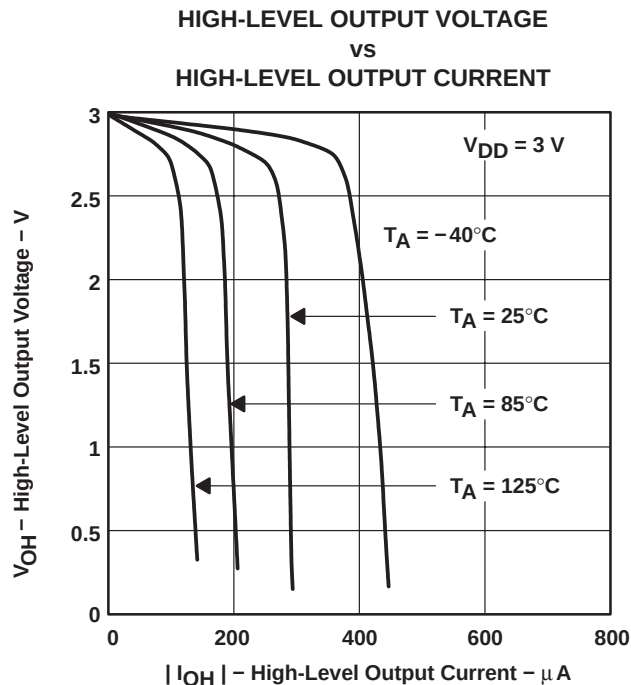


Figure 1



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Advanced LinCMOS is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997–2006, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TLV2252 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP‡ (PW)	CERAMIC FLATPACK (U)
–40°C to 125°C	850 µV 1500 µV	TLV2252AID TLV2252ID	— —	— —	TLV2252AIP TLV2252IP	TLV2252AIPWLE —	— —
–40°C to 125°C	850 µV 1500 µV	TLV2252AQD TLV2252QD	— —	— —	— —	— —	— —
–55°C to 125°C	850 µV 1500 µV	— —	TLV2252AMFK TLV2252MFK	TLV2252AMJG TLV2252MJG	— —	— —	TLV2252AMU TLV2252MU

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2252CDR).

‡ The PW package is available only left-end taped and reeled.

§ Chips are tested at 25°C.

TLV2254 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP‡ (PW)	CERAMIC FLATPACK (W)
–40°C to 125°C	850 µV 1500 µV	TLV2254AID TLV2254ID	— —	— —	TLV2254AIN TLV2254IN	TLV2254AIPWLE —	— —
–40°C to 125°C	850 µV 1500 µV	TLV2254AQD TLV2254QD	— —	— —	— —	— —	— —
–55°C to 125°C	850 µV 1500 µV	— —	TLV2254AMFK TLV2254MFK	TLV2254AMJ TLV2254MJ	— —	— —	TLV2254AMW TLV2254MW

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2254CDR).

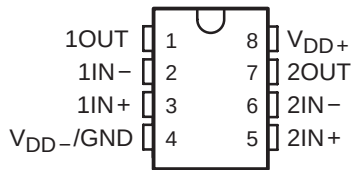
‡ The PW package is available only left-end taped and reeled.

§ Chips are tested at 25°C.

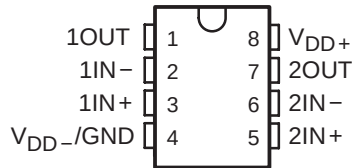
TLV225x, TLV225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

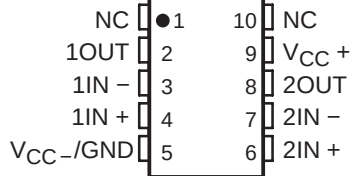
TLV2252I, TLV2252AI
TLV2252Q, TLV2252AQ
D, P, OR PW PACKAGE
(TOP VIEW)



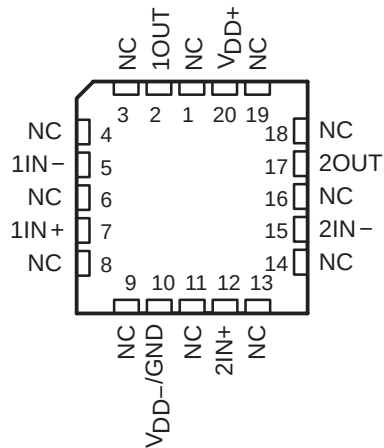
TLV2252M, TLV2252AM . . . JG PACKAGE
(TOP VIEW)



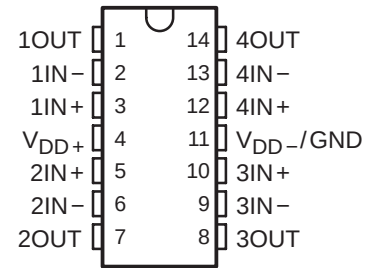
TLV2252M, TLV2252AM . . . U PACKAGE
(TOP VIEW)



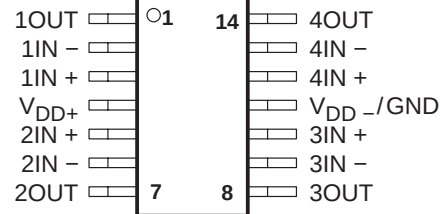
TLV2252M, TLV2252AM . . . FK PACKAGE
(TOP VIEW)



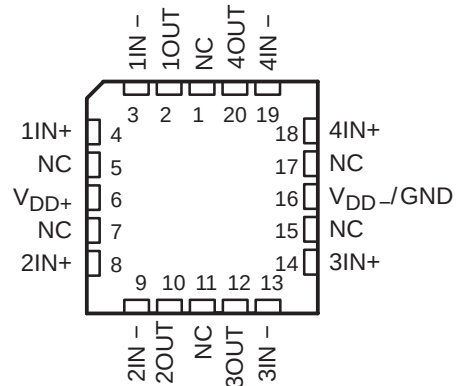
TLV2254I, TLV2254AI, TLV2254Q, TLV2254AQ . . . D OR N PACKAGE
TLV2254M, TLV2254AM . . . J OR W PACKAGE
(TOP VIEW)



TLV2254I, TLV2254AI . . . PW PACKAGE
(TOP VIEW)



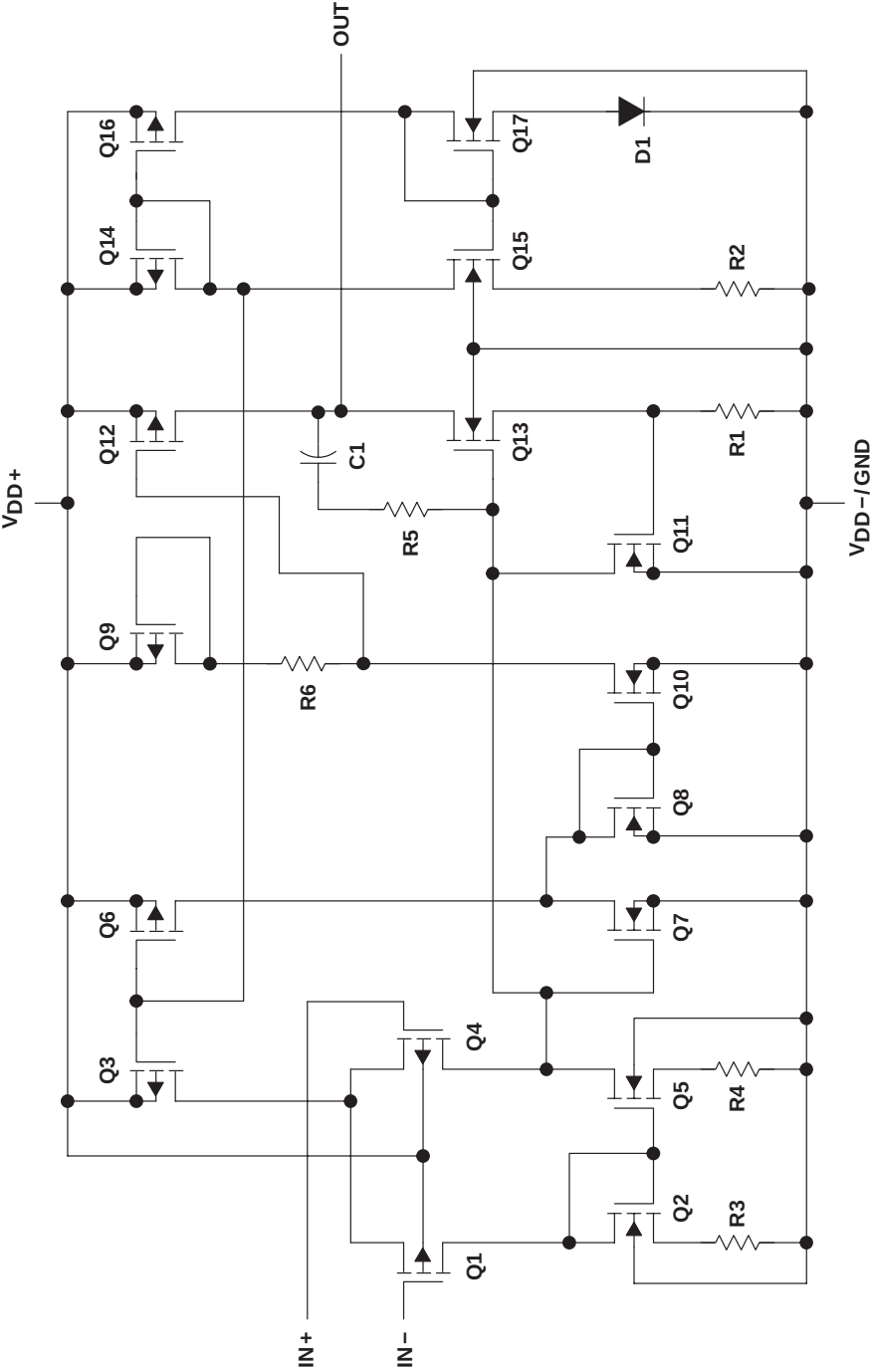
TLV2254M, TLV2254AM . . . FK PACKAGE
(TOP VIEW)



TLV225x, TLV2252xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLV2252	TLV2254
Transistors	38	76
Resistors	30	56
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	16 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1)	$V_{DD} - 0.3 \text{ V}$ to V_{DD+}
Input current, I_I (each input)	$\pm 5 \text{ mA}$
Output current, I_O	$\pm 50 \text{ mA}$
Total current into V_{DD+}	$\pm 50 \text{ mA}$
Total current out of V_{DD-}	$\pm 50 \text{ mA}$
Duration of short-circuit current (at or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : I Suffix	-40°C to 125°C
Q Suffix	-40°C to 125°C
M Suffix	-55°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P, and PW packages	260°C
J, JG, U, and W packages	300°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-} .
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below $V_{DD-} - 0.3 \text{ V}$.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D-8	725 mW	5.8 mW/°C	377 mW	145 mW
D-14	950 mW	7.6 mW/°C	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	715 mW	275 mW
J	1375 mW	11.0 mW/°C	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	546 mW	210 mW
N	1150 mW	9.2 mW/°C	598 mW	230 mW
P	1000 mW	8.0 mW/°C	520 mW	200 mW
PW-8	525 mW	4.2 mW/°C	273 mW	105 mW
PW-14	700 mW	5.6 mW/°C	364 mW	140 mW
U	700 mW	5.5 mW/°C	370 mW	150 mW
W	700 mW	5.5 mW/°C	370 mW	150 mW

recommended operating conditions

	TLV225xI		TLV225xQ		TLV225xM		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD} (see Note 1)	2.7	8	2.7	8	2.7	8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Operating free-air temperature, T_A	-40	125	-40	125	-55	125	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-} .

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TLV2252I electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2252I			TLV2252AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} = \pm 1.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		200	1500		200	850	μV
		Full range			1750			1000	
α_{VIO} Temperature coefficient of input offset voltage		25°C to 85°C		0.5			0.5		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.5	60		0.5	60	pA
		–40°C to 85°C			150			150	
		Full range			1000			1000	
I_{IB} Input bias current		25°C		1	60		1	60	pA
		–40°C to 85°C			150			150	
		Full range			1000			1000	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 2	–0.3 to 2.2		0 to 2	–0.3 to 2.2		V
		Full range	0 to 1.7			0 to 1.7			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		2.98			2.98		V
	$I_{OH} = -75\ \mu\text{A}$	25°C		2.9			2.9		
	$I_{OH} = -150\ \mu\text{A}$	Full range		2.8			2.8		
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C		10			10		mV
		Full range			80			80	
	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C		100			100		
		Full range			150			150	
	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 1\text{ mA}$	25°C		200			200		
		Full range			300			300	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 1.5\text{ V}$, $V_O = 1\text{ V to }2\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C	100	250		100	250	V/mV
			Full range	10			10		
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C		800			800	
$r_{i(d)}$ Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$, P package	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C		220			220		Ω
$CMRR$ Common-mode rejection ratio	$V_{IC} = 0\text{ to }1.7\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$	25°C		65	75		65	77	dB
		Full range		60			60		

† Full range is –40°C to 125°C.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLV2252I electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2252I			TLV2252AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to } 8\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	100		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 1.5\text{ V}$, No load	25°C		68	125		68	125	μA
		Full range			150			150	

† Full range is -40°C to 125°C .

TLV2252I operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2252I			TLV2252AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1.1\text{ V to } 1.9\text{ V}$, $R_L = 100\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C	0.07	0.1		0.07	0.1		$\text{V}/\mu\text{s}$
		Full range	0.05			0.05			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		35			35		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C		19			19		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to } 1\text{ Hz}$	25°C		0.6			0.6		μV
	$f = 0.1\text{ Hz to } 10\text{ Hz}$	25°C		1.1			1.1		
I_n Equivalent input noise current		25°C		0.6			0.6		$\text{fA}/\sqrt{\text{Hz}}$
Gain-bandwidth product	$f = 1\text{ kHz}$, $R_L = 50\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		0.187			0.187		MHz
B_{OM} Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}$, $A_V = 1$, $R_L = 50\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		60			60		kHz
ϕ_m Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		63°			63°		
Gain margin		25°C		15			15		dB

† Full range is -40°C to 125°C .

‡ Referenced to 1.5 V

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TLV2252I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2252I			TLV2252AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	200	1500		200	850		μV
		Full range		1750			1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 85°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		–40°C to 85°C		150			150		
		Full range		1000			1000		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		–40°C to 85°C		150			150		
		Full range		1000			1000		
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$	25°C	0 to 4	–0.3 to 4.2		0 to 4	–0.3 to 4.2		V
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.98			4.98			V
	$I_{OH} = -75\ \mu\text{A}$	25°C	4.9	4.94		4.9	4.94		
		Full range	4.8			4.8			
	$I_{OH} = -150\ \mu\text{A}$	25°C	4.8	4.88		4.8	4.88		
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C	0.01			0.01			V
		Full range		0.06			0.06		
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	0.09	0.15		0.09	0.15		
		Full range		0.15			0.15		
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 1\text{ mA}$	25°C	0.2	0.3		0.2	0.3		
		Full range		0.3			0.3		
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to } 4\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C	100	350	100	350		V/mV
			Full range	10		10			
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C	1700		1700			
$r_{i(d)}$ Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$, P package	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C		200			200		Ω
$CMRR$ Common-mode rejection ratio	$V_{IC} = 0\text{ to } 2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	83		70	83		dB
		Full range	70			70			

† Full range is –40°C to 125°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLV2252I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2252I			TLV2252AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C		70	125		70	125	μA
		Full range			150			150	

† Full range is -40°C to 125°C .

TLV2252I operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLV2252I			TLV2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 1.5 V to 3.5 V, R _L = 100 kΩ [‡] , C _L = 100 pF [‡]		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	36			36			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.7			0.7			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 20 kHz, R _L = 50 kΩ [‡]	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
	Gain-bandwidth product	f = 50 kHz, C _L = 100 pF [‡]	R _L = 50 kΩ [‡]	25°C	0.2			0.2			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 50 kΩ [‡]	A _V = 1, C _L = 100 pF [‡]	25°C	30			30			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ [‡] , C _L = 100 pF [‡]		25°C	63°			63°			
	Gain margin			25°C	15			15			dB

† Full range is -40°C to 125°C .

‡ Referenced to 2.5 V

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TLV2254I electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLV2254I			TLV2254AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{DD±} = ±1.5 V, V _O = 0, V _{IC} = 0, R _S = 50 Ω		25°C	200	1500		200	850	μV	
	Full range			1750			1000				
α _{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C	0.5			0.5			μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.003			0.003			μV/mo
I _{IO}	Input offset current			25°C	0.5	60	0.5		60	pA	
				–40°C to 85°C	150			150			
				Full range	1000			1000			
I _{IB}	Input bias current			25°C	1	60	1		60	pA	
				–40°C to 85°C	150			150			
				Full range	1000			1000			
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω, V _{IO} ≤5 mV	25°C	0 to 2	–0.3 to 2.2	0 to 2		–0.3 to 2.2	V		
			Full range	0 to 1.7	0 to 1.7						
V _{OH}	High-level output voltage	I _{OH} = –20 μA	25°C	2.98			2.98			V	
		I _{OH} = –75 μA	25°C	2.9			2.9				
			Full range	2.8			2.8				
		I _{OH} = –150 μA	25°C	2.8			2.8				
V _{OL}	Low-level output voltage	V _{IC} = 1.5 V, I _{OL} = 50 μA	25°C	10			10			mV	
			Full range	80			80				
		V _{IC} = 1.5 V, I _{OL} = 500 μA	25°C	100			100				
			Full range	150			150				
		V _{IC} = 1.5 V, I _{OL} = 1 mA	25°C	200			200				
			Full range	300			300				
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 1.5 V, V _O = 1 V to 2 V	R _L = 100 kΩ‡	25°C	100	225	100	225	V/mV		
				Full range	10		10				
			R _L = 1 MΩ‡	25°C	800			800			
r _{i(d)}	Differential input resistance			25°C	10 ¹²			10 ¹²			Ω
r _{i(c)}	Common-mode input resistance			25°C	10 ¹²			10 ¹²			Ω
c _{i(c)}	Common-mode input capacitance	f = 10 kHz,	N package	25°C	8			8			pF
z _o	Closed-loop output impedance	f = 25 kHz,	A _V = 10	25°C	220			220			Ω
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 1.7 V, R _S = 50 Ω	V _O = 1.5 V,	25°C	65	75	65	77	dB		
				Full range	60		60				

† Full range is –40°C to 125°C.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLV2254I electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2254I			TLV2254AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	100		dB
		Full range	80			80			
I_{DD} Supply current (four amplifiers)	$V_O = 1.5\text{ V}$, No load	25°C		135	250		135	250	μA
		Full range			300			300	

† Full range is -40°C to 125°C .

TLV2254I operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2254I			TLV2254AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 0.7\text{ V to }1.7\text{ V}$, $R_L = 100\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C	0.07	0.1		0.07	0.1		$\text{V}/\mu\text{s}$
		Full range	0.05			0.05			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		35			35		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C		19			19		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		0.6			0.6		μV
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.1			1.1		
I_n Equivalent input noise current		25°C		0.6			0.6		$\text{fA}/\sqrt{\text{Hz}}$
Gain-bandwidth product	$f = 1\text{ kHz}$, $R_L = 50\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		0.187			0.187		MHz
B_{OM} Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}$, $A_V = 1$, $R_L = 50\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		60			60		kHz
ϕ_m Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		63°			63°		
Gain margin		25°C		15			15		dB

† Full range is -40°C to 85°C .

‡ Referenced to 1.5 V

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TLV2254I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A †	TLV2254I			TLV2254AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{DD±} = ±2.5 V, V _O = 0, V _{IC} = 0, R _S = 50 Ω	25°C	200		1500	200		850	μV
			Full range			1750			1000	
α _{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C	0.5			0.5			μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			μV/mo
I _{IO}	Input offset current		25°C	0.5		60	0.5		60	pA
			–40°C to 85°C			150			150	
			Full range			1000			1000	
I _{IB}	Input bias current		25°C	1		60	1		60	pA
			–40°C to 85°C			150			150	
			Full range			1000			1000	
V _{ICR}	Common-mode input voltage range	V _{IO} ≤5 mV, R _S = 50 Ω	25°C	0 to 4	–0.3 to 4.2	0 to 4		–0.3 to 4.2	V	
			Full range	0 to 3.5		0 to 3.5				
V _{OH}	High-level output voltage	I _{OH} = –20 μA	25°C	4.98		4.98			V	
		I _{OH} = –75 μA	25°C	4.9	4.94	4.9	4.94			
			Full range	4.8		4.8				
		I _{OH} = –150 μA	25°C	4.8	4.88	4.8	4.88			
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 50 μA	25°C	0.01		0.01			V	
			Full range	0.06		0.06				
		V _{IC} = 2.5 V, I _{OL} = 500 μA	25°C	0.09	0.15	0.09	0.15			
			Full range	0.15		0.15				
		V _{IC} = 2.5 V, I _{OL} = 1 mA	25°C	0.2	0.3	0.2	0.3			
			Full range	0.3		0.3				
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V	R _L = 100 kΩ‡	25°C	100	350	100	350	V/mV	
				Full range	10		10			
			R _L = 1 MΩ‡	25°C	1700		1700			
r _{i(d)}	Differential input resistance		25°C	10 ¹²		10 ¹²		Ω		
r _{i(c)}	Common-mode input resistance		25°C	10 ¹²		10 ¹²		Ω		
c _{i(c)}	Common-mode input capacitance	f = 10 kHz, N package	25°C	8		8		pF		
z _o	Closed-loop output impedance	f = 25 kHz, A _V = 10	25°C	200		200		Ω		
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 2.7 V, V _O = 2.5 V, R _S = 50 Ω	25°C	70	83	70	83	dB		
			Full range	70		70				

† Full range is –40°C to 125°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLV2254I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2254I			TLV2254AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load	25°C		140	250		140	250	μA
		Full range			300			300	

† Full range is – 40°C to 125°C.

TLV2254I operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLV2254I			TLV2254AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 1.4 V to 2.6 V, R _L = 100 kΩ [‡] , C _L = 100 pF [‡]		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	36			36			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.7			0.7			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 20 kHz, R _L = 50 kΩ [‡]	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
	Gain-bandwidth product	f = 50 kHz, C _L = 100 pF [‡]	R _L = 50 kΩ [‡] ,	25°C	0.2			0.2			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 50 kΩ [‡] ,	A _V = 1, C _L = 100 pF [‡]	25°C	30			30			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ [‡] , C _L = 100 pF [‡]		25°C	63°			63°			
	Gain margin			25°C	15			15			dB

† Full range is – 40°C to 125°C.

‡ Referenced to 2.5 V

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TLV2252Q, and TLV2252M electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2252Q, TLV2252M			TLV2252AQ, TLV2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} \pm \pm 1.5\text{ V}, V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C		200	1500		200	850	μV
		Full range			1750			1000	
α_{VIO} Temperature coefficient of input offset voltage		25°C to 85°C		0.5			0.5		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.5	60		0.5	60	pA
		125°C			1000			1000	
I_{IB} Input bias current		25°C		1	60		1	60	pA
		125°C			1000			1000	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	0 to 2	-0.3 to 2.2		0 to 2	-0.3 to 2.2		V
		Full range	0 to 1.7			0 to 1.7			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		2.98			2.98		V
	$I_{OH} = -75\ \mu\text{A}$	25°C		2.9			2.9		
		Full range		2.8			2.8		
	$I_{OH} = -150\ \mu\text{A}$	25°C		2.8			2.8		
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V}, I_{OL} = 50\ \mu\text{A}$	25°C		10			10		mV
	$V_{IC} = 1.5\text{ V}, I_{OL} = 500\ \mu\text{A}$	25°C		100	150		100	150	
		Full range			165			165	
	$V_{IC} = 1.5\text{ V}, I_{OL} = 1\text{ mA}$	25°C		200	300		200	300	
		Full range			300			300	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 1.5\text{ V}, V_O = 1\text{ V to }2\text{ V}$	25°C	100	250		100	250		V/mV
		Full range		10			10		
		25°C		800			800		
$r_{i(d)}$ Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}, \text{ P package}$	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}, A_V = 10$	25°C		220			220		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }1.7\text{ V}, V_O = 1.5\text{ V}, R_S = 50\ \Omega$	25°C	65	75		65	77		dB
		Full range		60			60		
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }8\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95		80	100		dB
		Full range		80			80		
I_{DD} Supply current	$V_O = 1.5\text{ V}, \text{ No load}$	25°C		68	125		68	125	μA
		Full range			150			150	

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLV2252Q, and TLV2252M operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2252Q, TLV2252M			TLV2252AQ, TLV2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 0.8\text{ V to }1.4\text{ V}, \quad R_L = 100\text{ k}\Omega^\ddagger, \quad C_L = 100\text{ pF}^\ddagger$	25°C	0.07	0.1		0.07	0.1		V/ μs
		Full range	0.05			0.05			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		35			35		nV/ $\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C		19			19		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		0.6			0.6		μV
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.1			1.1		
I_n Equivalent input noise current		25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
	Gain-bandwidth product $f = 1\text{ kHz}, \quad R_L = 50\text{ k}\Omega^\ddagger, \quad C_L = 100\text{ pF}^\ddagger$	25°C		0.187			0.187		MHz
B_{OM} Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}, \quad A_V = 1, \quad R_L = 50\text{ k}\Omega^\ddagger, \quad C_L = 100\text{ pF}^\ddagger$	25°C		60			60		kHz
ϕ_m Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger, \quad C_L = 100\text{ pF}^\ddagger$	25°C		63°			63°		
	Gain margin	25°C		15			15		dB

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 1.5 V

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TLV2252Q, and TLV2252M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2252Q, TLV2252M			TLV2252AQ, TLV2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} \pm \pm 2.5\text{ V}, V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C	200	1500		200	850		μV
		Full range		1750		1000			
α_{VIO} Temperature coefficient of input offset voltage		25°C to 85°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		125°C		1000		1000			
I_{IB} Input bias current		25°C	1	60		1	60		pA
		125°C		1000		1000			
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}, R_S = 50\ \Omega$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		V
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.98			4.98			V
	$I_{OH} = -75\ \mu\text{A}$	25°C	4.9	4.94		4.9	4.94		
	Full range		4.8			4.8			
	$I_{OH} = -150\ \mu\text{A}$	25°C	4.8	4.88		4.8	4.88		
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}, I_{OL} = 50\ \mu\text{A}$	25°C	0.01			0.01			V
	$V_{IC} = 2.5\text{ V}, I_{OL} = 500\ \mu\text{A}$	25°C	0.09	0.15		0.09	0.15		
	Full range			0.15			0.15		
	$V_{IC} = 2.5\text{ V}, I_{OL} = 1\text{ mA}$	25°C	0.2	0.3		0.2	0.3		
	Full range			0.3			0.3		
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}, V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C	100	350	100	350		V/mV
		Full range	10			10			
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C	1700		1700			
$r_{i(d)}$ Differential input resistance		25°C	10^{12}			10^{12}			Ω
$r_{i(c)}$ Common-mode input resistance		25°C	10^{12}			10^{12}			Ω
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}, \text{ P package}$	25°C	8			8			pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}, A_V = 10$	25°C	200			200			Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}, V_O = 2.5\text{ V}, R_S = 50\ \Omega$	25°C	70	83		70	83		dB
		Full range	70			70			
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95		80	95		dB
		Full range	80			80			

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLV2252Q, and TLV2252M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2252Q, TLV2252M			TLV2252AQ, TLV2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C		70	125		70	125	μA
		Full range			150			150	

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

TLV2252Q, and TLV2252M operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2252Q, TLV2252M			TLV2252AQ, TLV2252AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1.25\text{ V}$ to 2.75 V , $R_L = 100\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C	0.07	0.12		0.07	0.12		$\text{V}/\mu\text{s}$
		Full range	0.05			0.05			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		36			36		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C		19			19		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz}$ to 1 Hz	25°C		0.7			0.7		μV
	$f = 0.1\text{ Hz}$ to 10 Hz	25°C		1.1			1.1		
I_n Equivalent input noise current		25°C		0.6			0.6		$\text{fA}/\sqrt{\text{Hz}}$
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{ V}$ to 2.5 V , $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$		0.2%			0.2%		
		$A_V = 10$		1%			1%		
Gain-bandwidth product	$f = 50\text{ kHz}$, $C_L = 100\text{ pF}^\ddagger$	$R_L = 50\text{ k}\Omega^\ddagger$, 25°C		0.2			0.2		MHz
B_{OM} Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$, $C_L = 100\text{ pF}^\ddagger$, 25°C		30			30		kHz
ϕ_m Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		63°			63°		
Gain margin		25°C		15			15		dB

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TLV2254Q, and TLV2254M electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 1.5\text{ V}, V_{IC} = 0, R_S = 50\ \Omega$	25°C	200	1500		200	850		μV
		Full range		1750			1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		125°C		1000			1000		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		125°C		1000			1000		
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	0 to 2	-0.3 to 2.2		0 to 2	-0.3 to 2.2		V
		Full range	0 to 1.7			0 to 1.7			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		2.98			2.98		V
	$I_{OH} = -75\ \mu\text{A}$	25°C		2.9			2.9		
		Full range		2.8			2.8		
	$I_{OH} = -150\ \mu\text{A}$	25°C		2.8			2.8		
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V}, I_{OL} = 50\ \mu\text{A}$	25°C		10			10		mV
	$V_{IC} = 1.5\text{ V}, I_{OL} = 500\ \mu\text{A}$	25°C		100	150		100	150	
		Full range			165			165	
	$V_{IC} = 1.5\text{ V}, I_{OL} = 1\text{ mA}$	25°C		200	300		200	300	
		Full range			300			300	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 1.5\text{ V}, V_O = 1\text{ V to }2\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C	100	225		100	225	V/mV
			Full range	10			10		
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C		800			800	
$r_{i(d)}$ Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}, \text{ N package}$	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}, A_V = 10$	25°C		220			220		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }1.7\text{ V}, V_O = 1.5\text{ V}, R_S = 50\ \Omega$	25°C	65	75		65	77		dB
		Full range	60			60			
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }8\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95		80	100		dB
		Full range	80			80			

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2254Q, and TLV2254M electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD} Supply current (four amplifiers)	$V_O = 1.5\text{ V}$, No load	25°C		135	250		135	250	μA
		Full range			300			300	

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

TLV2254Q, and TLV2254M operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 0.5\text{ V}$ to 1.7 V , $R_L = 100\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C	0.07	0.1		0.07	0.1		$\text{V}/\mu\text{s}$
		Full range	0.05			0.05			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		35			35		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C		19			19		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz}$ to 1 Hz	25°C		0.6			0.6		μV
	$f = 0.1\text{ Hz}$ to 10 Hz	25°C		1.1			1.1		
I_n Equivalent input noise current		25°C		0.6			0.6		$\text{fA}/\sqrt{\text{Hz}}$
Gain-bandwidth product	$f = 1\text{ kHz}$, $R_L = 50\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		0.187			0.187		MHz
B_{OM} Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}$, $A_V = 1$, $R_L = 50\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		60			60		kHz
ϕ_m Phase margin at unity gain Gain margin	$R_L = 50\text{ k}\Omega^\ddagger$	25°C		63°			63°		dB
	$C_L = 100\text{ pF}^\ddagger$	25°C		15			15		

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 1.5 V

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TLV2254Q, and TLV2254M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} \pm \pm 2.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	200	1500		200	850		μV
		Full range		1750			1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		125°C		1000			1000		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		125°C		1000			1000		
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		V
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.98			4.98		V
	$I_{OH} = -75\ \mu\text{A}$	25°C	4.9	4.94		4.9	4.94		
		Full range	4.8			4.8			
	$I_{OH} = -150\ \mu\text{A}$	25°C	4.8	4.88		4.8	4.88		
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C		0.01			0.01		V
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C		0.09 0.15			0.09 0.15		
		Full range		0.15			0.15		
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 1\text{ mA}$	25°C		0.2 0.3			0.2 0.3		
		Full range		0.3			0.3		
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	25°C	100	350		100	350		V/mV
		Full range	10			10			
		25°C		1700			1700		
$r_{i(d)}$ Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$, N package	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C		200			200		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	83		70	83		dB
		Full range	70			70			
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
		Full range	80			80			

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLV2254Q, and TLV2254M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load	25°C		140	250		140	250	μA
		Full range			300			300	

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

TLV2254Q, and TLV2254M operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 0.5 V to 3.5 V, R _L = 100 kΩ [‡] , C _L = 100 pF [‡]		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	36			36			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.7			0.7			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 20 kHz, R _L = 50 kΩ [‡]	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
	Gain-bandwidth product	f = 50 kHz, C _L = 100 pF [‡]	R _L = 50 kΩ [‡] ,	25°C	0.2			0.2			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 50 kΩ [‡] ,	A _V = 1, C _L = 100 pF [‡]	25°C	30			30			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ [‡] , C _L = 100 pF [‡]		25°C	63°			63°			
	Gain margin			25°C	15			15			dB

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

TLV225x, TLV225xA
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution vs Common-mode voltage	2 – 5 6, 7
α_{VIO}	Input offset voltage temperature coefficient	Distribution	8 – 11
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	12
V_I	Input voltage	vs Supply voltage vs Free-air temperature	13 14
V_{OH}	High-level output voltage	vs High-level output current	15, 18
V_{OL}	Low-level output voltage	vs Low-level output current	16, 17, 19
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	20
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	21 22
V_{ID}	Differential input voltage	vs Output voltage	23, 24
A_{VD}	Differential voltage amplification	vs Load resistance	25
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	26, 27 28, 29
z_o	Output impedance	vs Frequency	30, 31
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	32 33
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	34, 35 36
I_{DD}	Supply current	vs Supply voltage	37, 38
SR	Slew rate	vs Load capacitance vs Free-air temperature	39 40
V_O	Inverting large-signal pulse response		41, 42
V_O	Voltage-follower large-signal pulse response		43, 44
V_O	Inverting small-signal pulse response		45, 46
V_O	Voltage-follower small-signal pulse response		47, 48
V_n	Equivalent input noise voltage	vs Frequency	49, 50
	Input noise voltage	Over a 10-second period	51
	Integrated noise voltage	vs Frequency	52
THD + N	Total harmonic distortion plus noise	vs Frequency	53
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	54 55
ϕ_m	Phase margin	vs Frequency vs Load capacitance	26, 27 56
	Gain margin	vs Load capacitance	57
B_1	Unity-gain bandwidth	vs Load capacitance	58
	Overestimation of phase margin	vs Load capacitance	59

TYPICAL CHARACTERISTICS

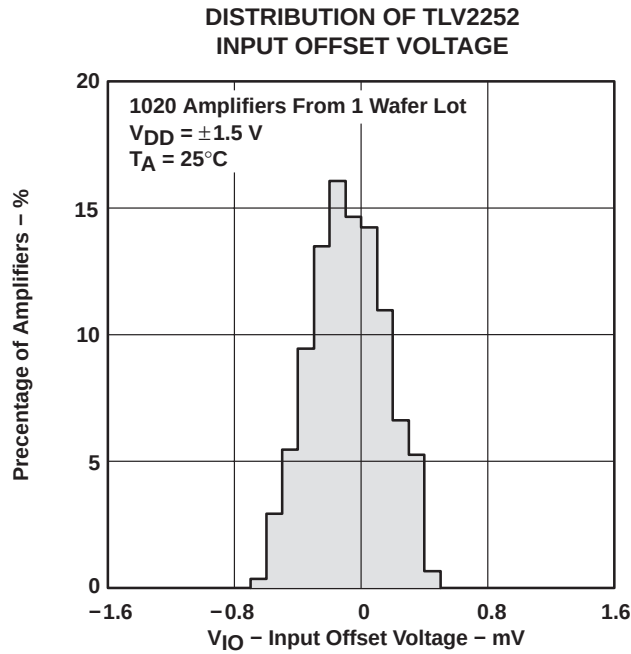


Figure 2

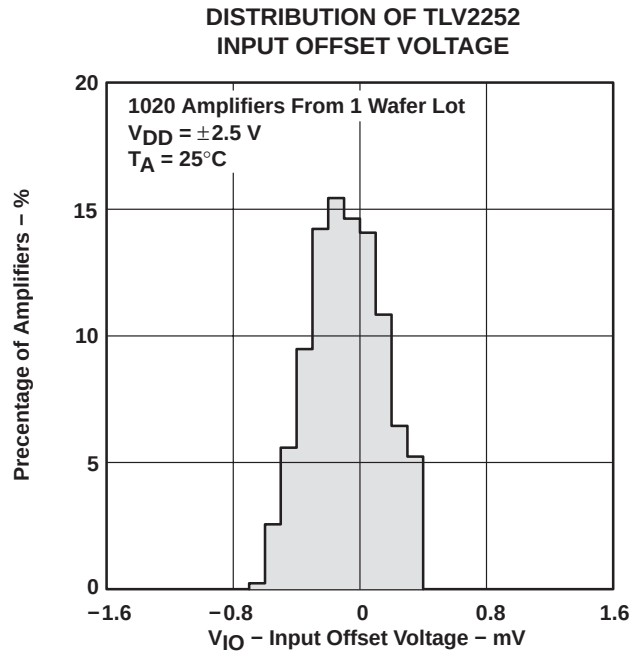


Figure 3

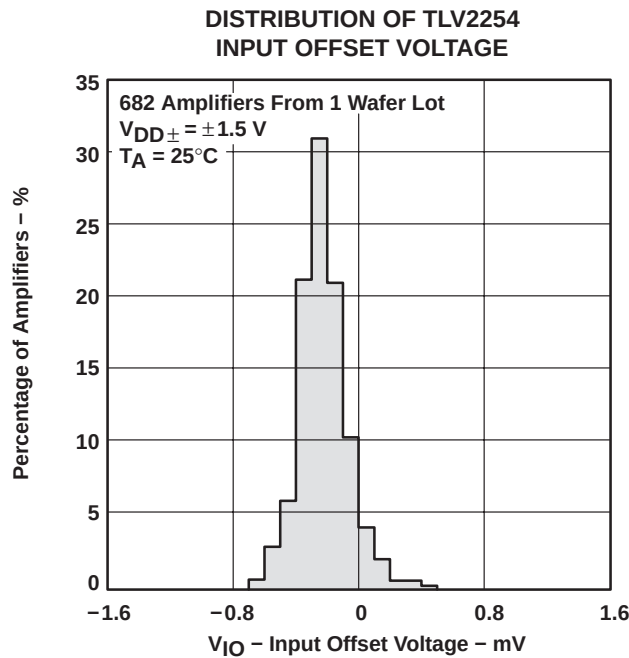


Figure 4

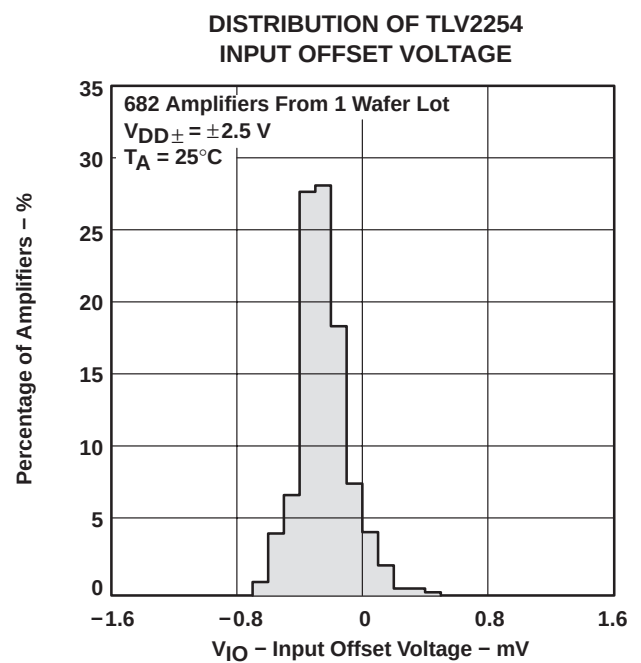


Figure 5

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TYPICAL CHARACTERISTICS

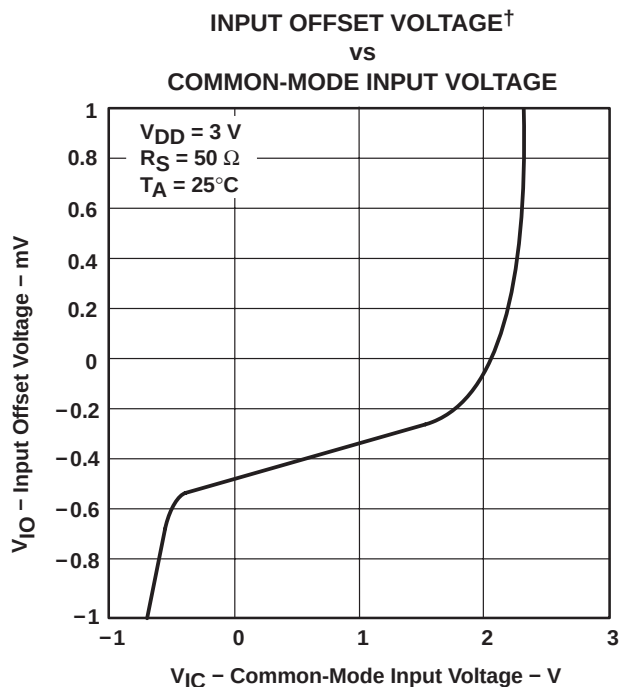


Figure 6

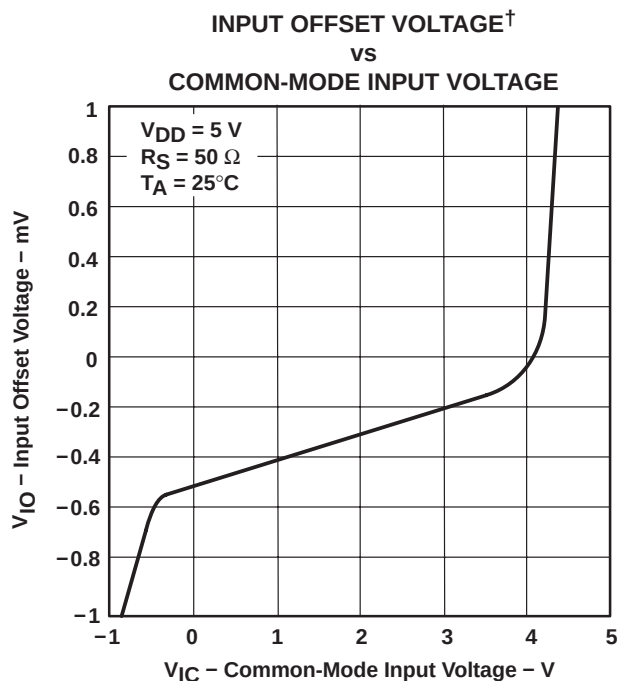


Figure 7

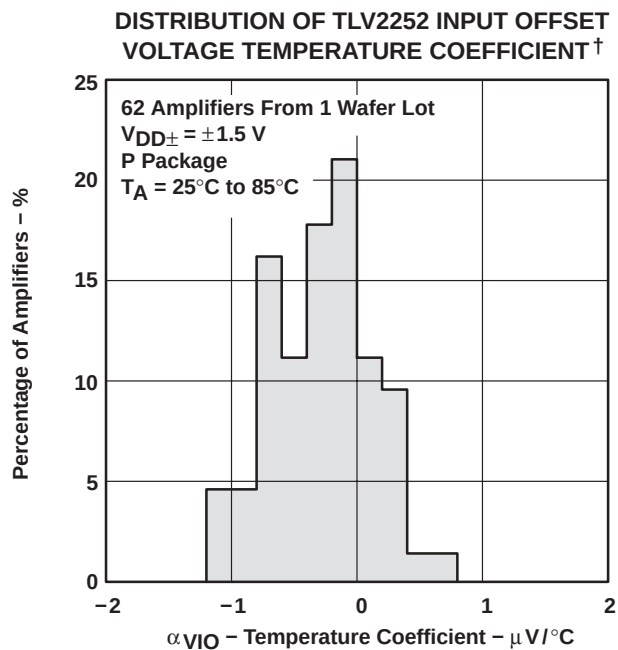


Figure 8

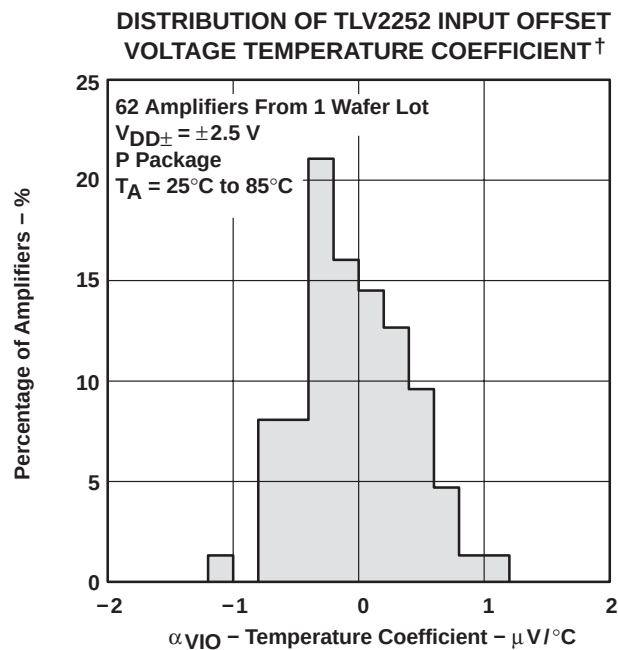


Figure 9

[†] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V . For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V .

TYPICAL CHARACTERISTICS

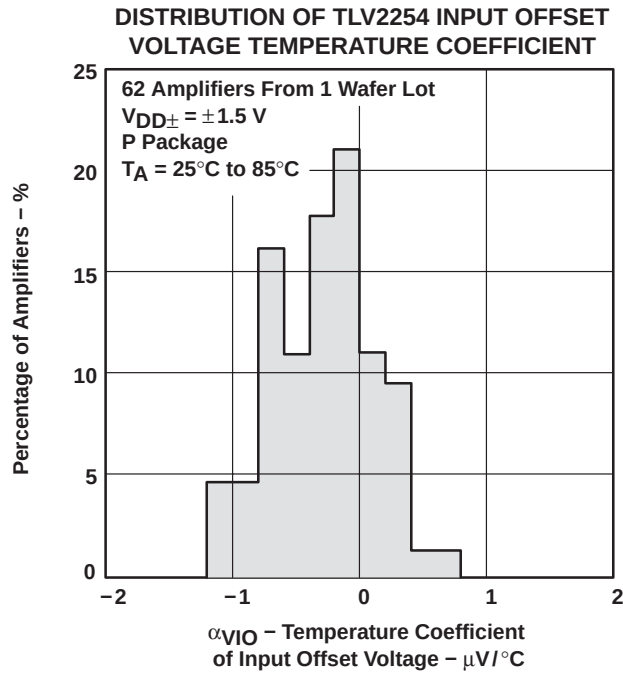


Figure 10

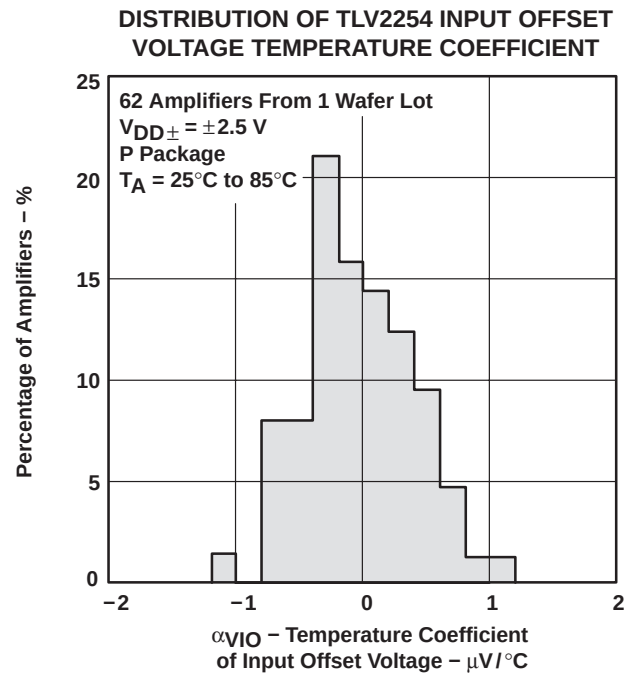


Figure 11

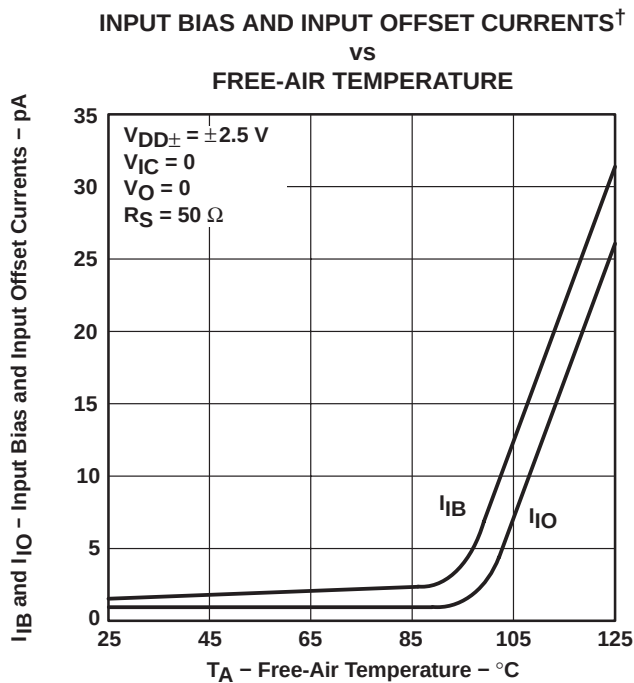


Figure 12

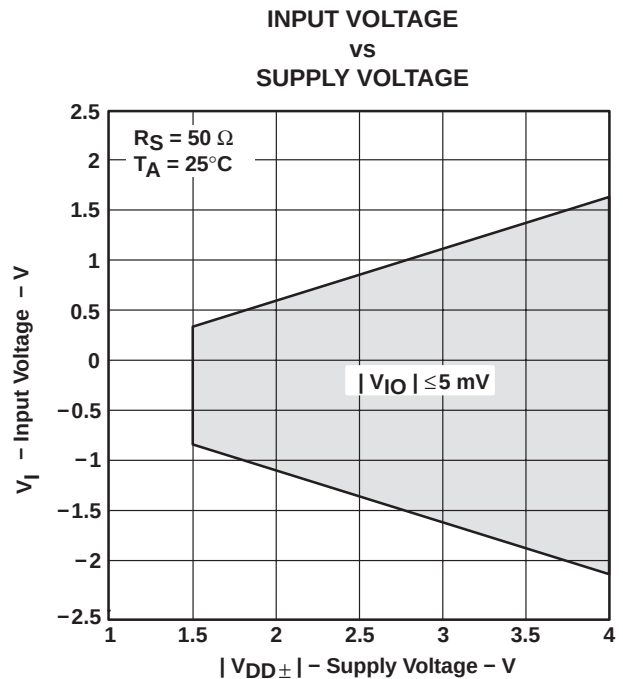


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TYPICAL CHARACTERISTICS

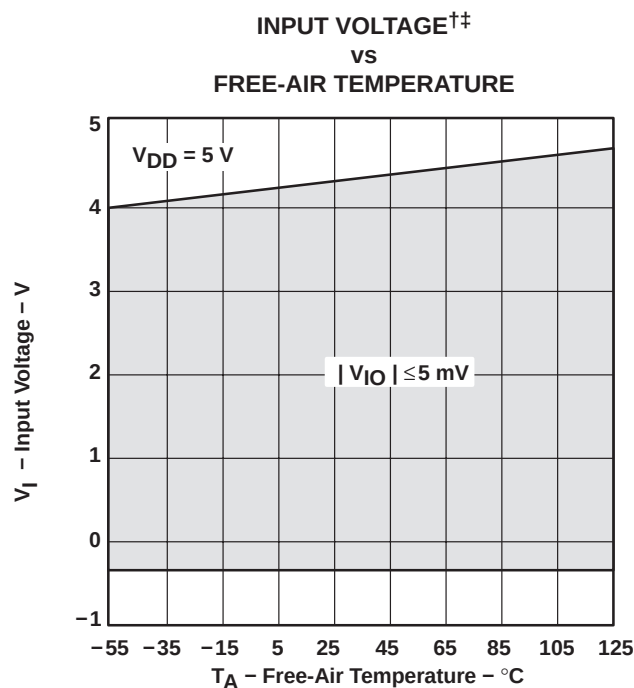


Figure 14

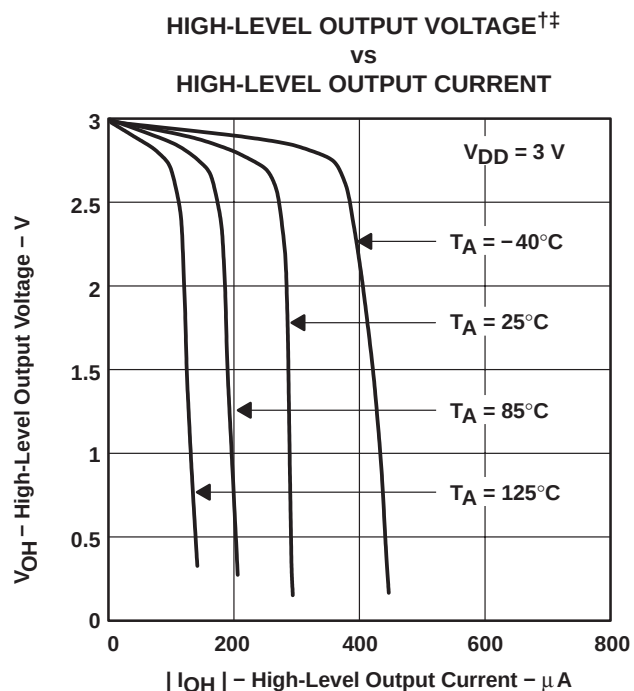


Figure 15

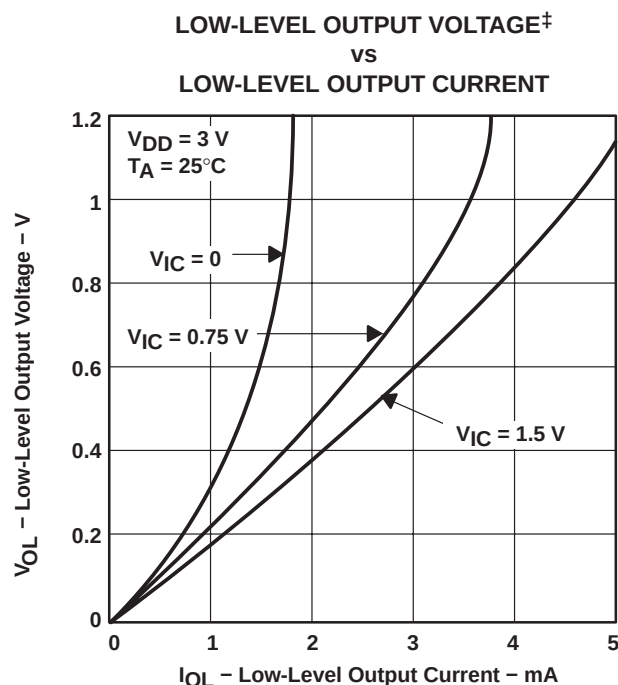


Figure 16

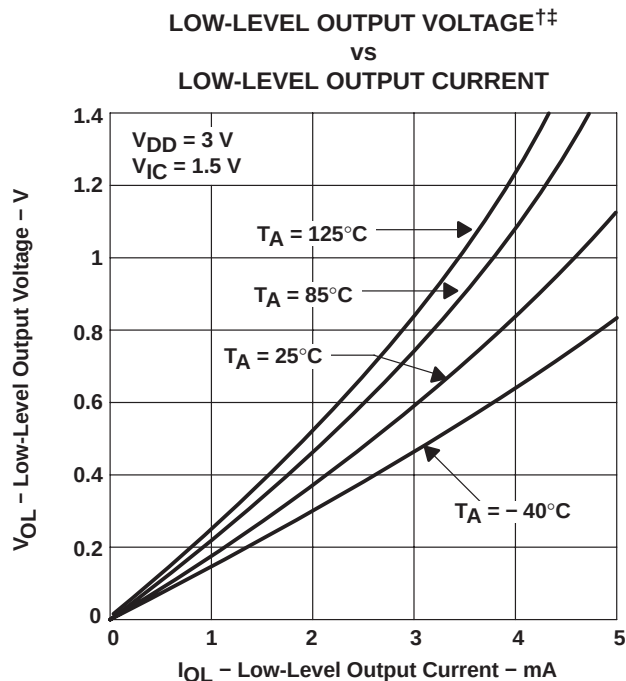
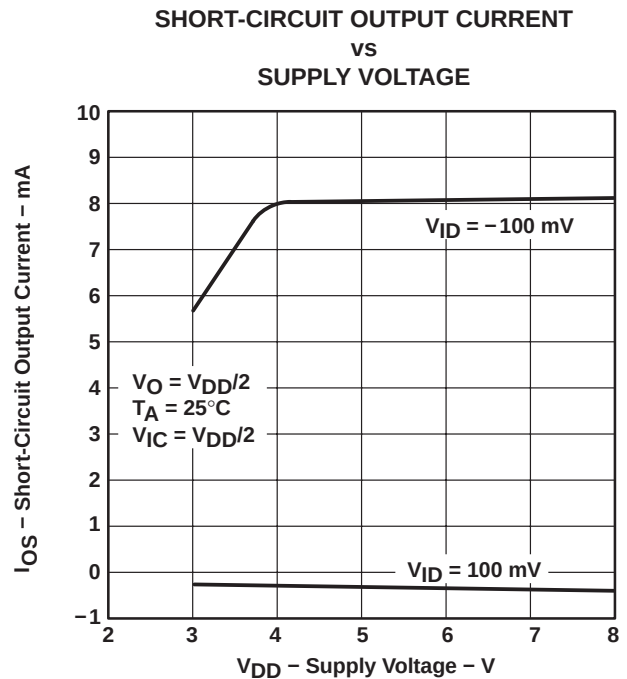
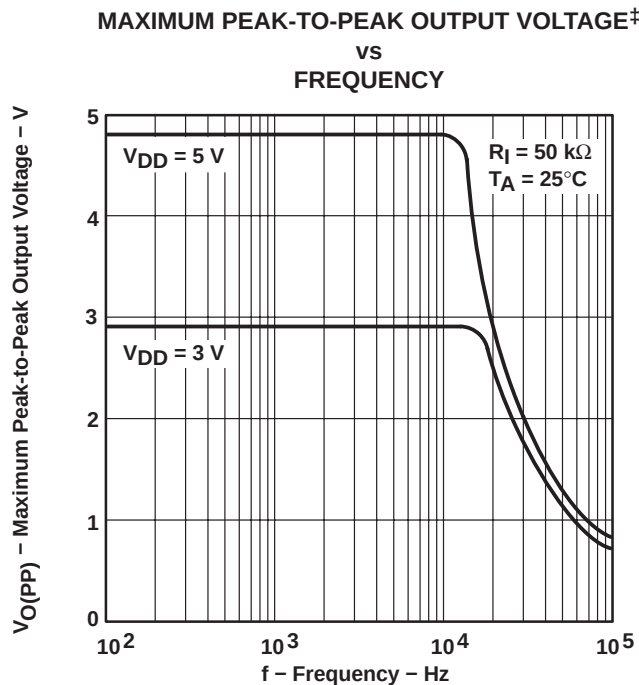
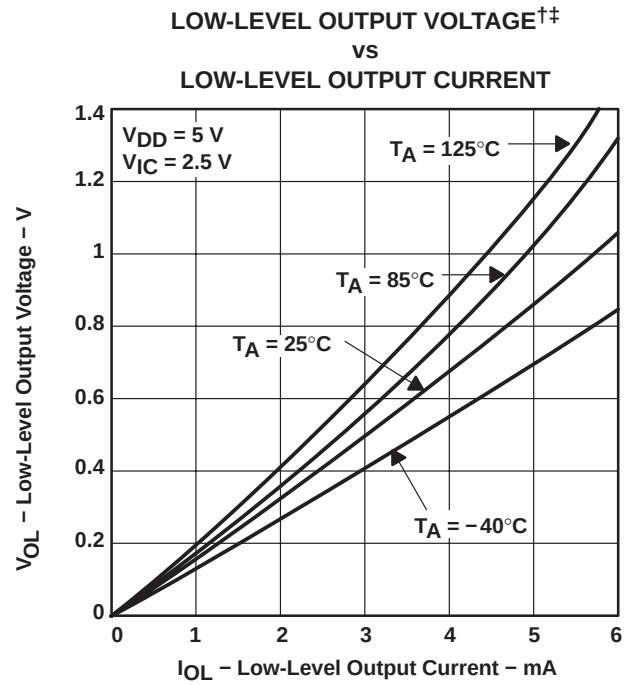
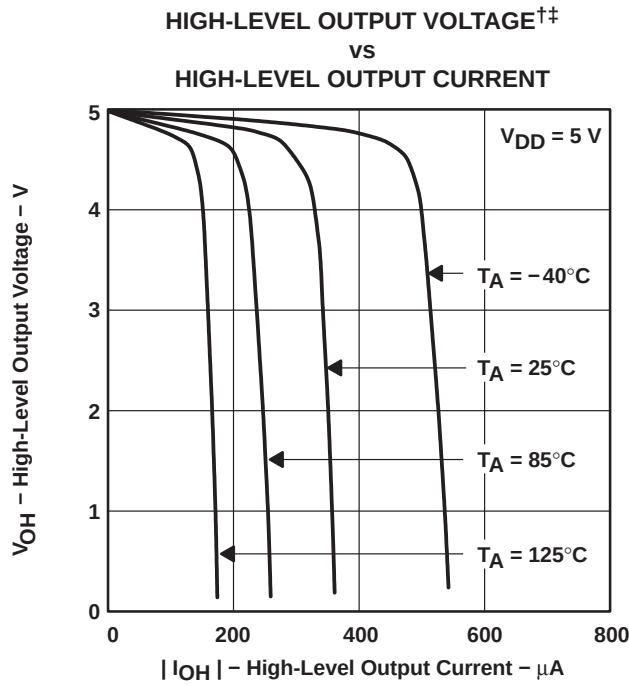


Figure 17

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

^{††} For all curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 \text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TYPICAL CHARACTERISTICS

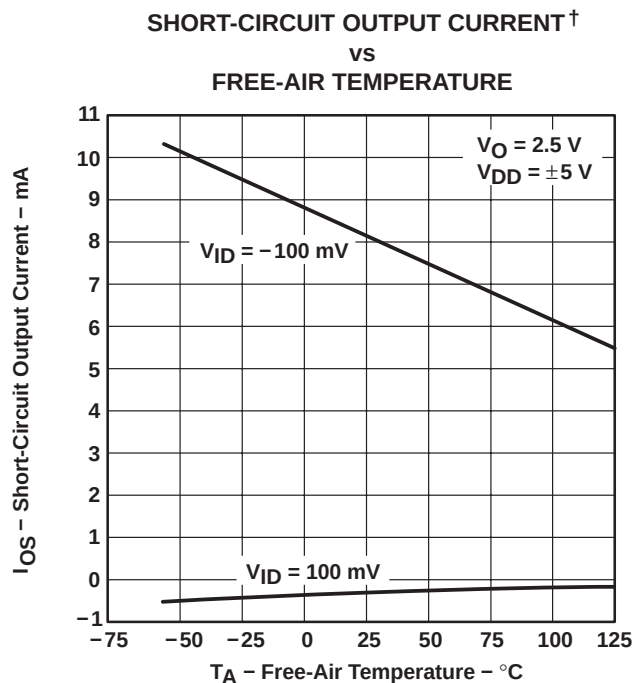


Figure 22

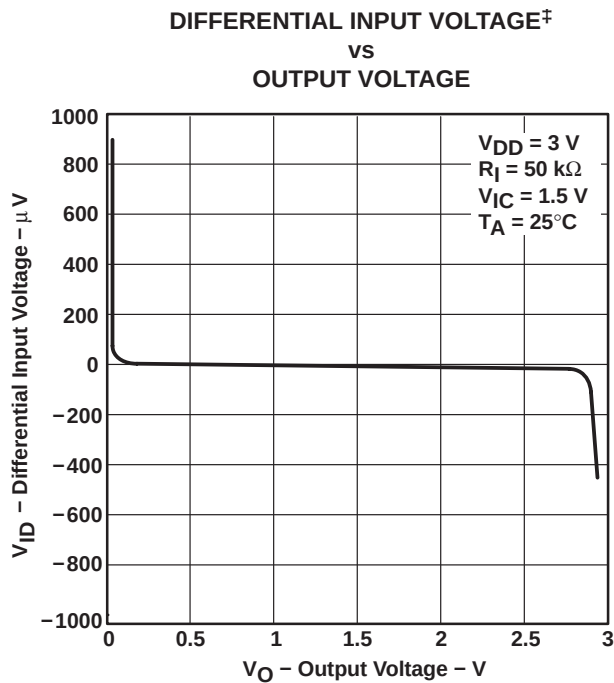


Figure 23

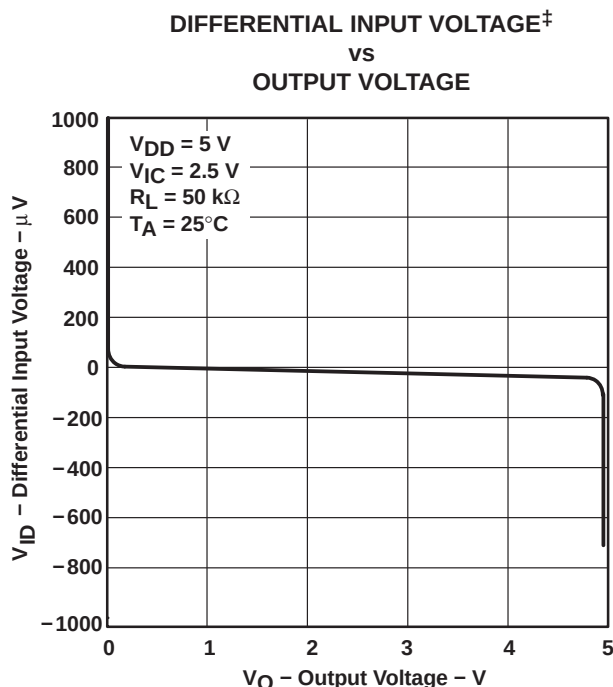


Figure 24

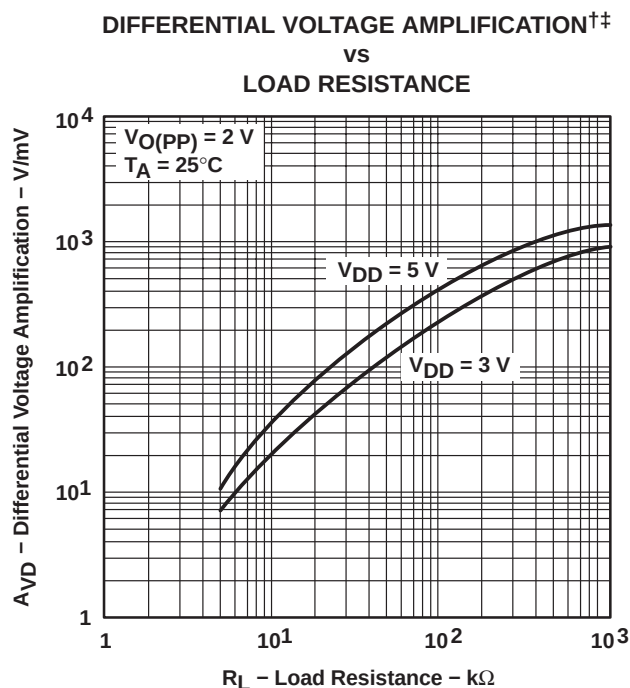


Figure 25

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE† AMPLIFICATION AND PHASE MARGIN VS FREQUENCY

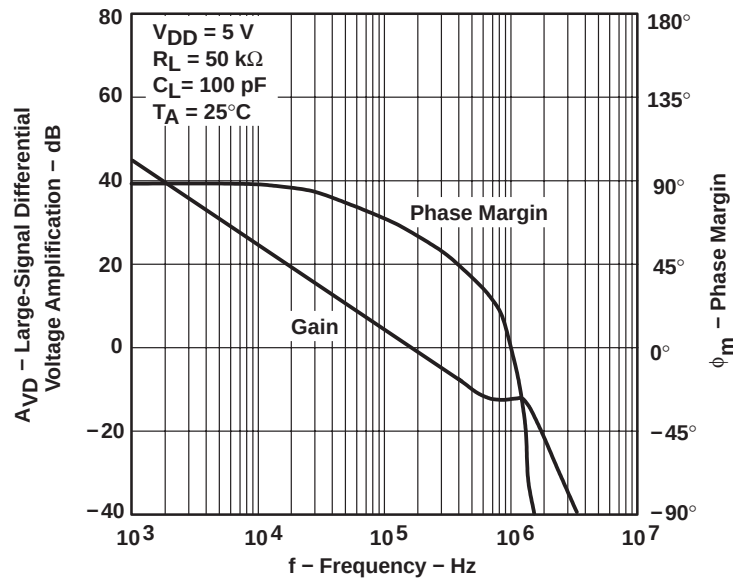


Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE† AMPLIFICATION AND PHASE MARGIN VS FREQUENCY

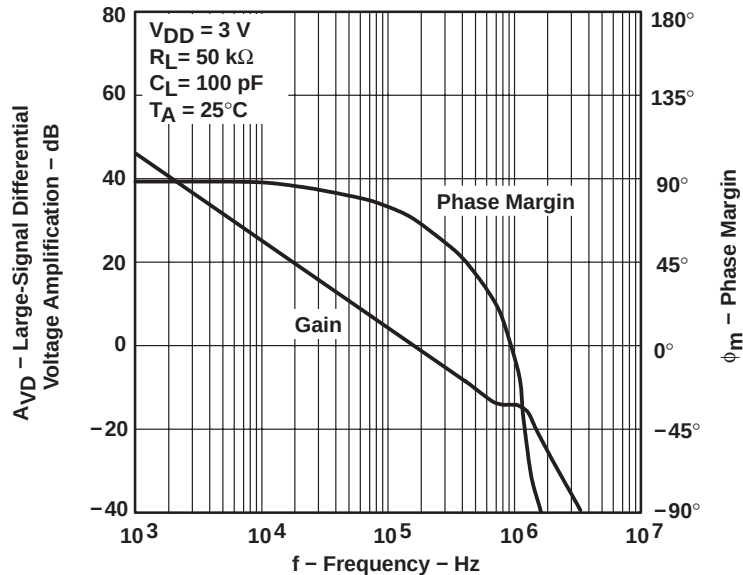


Figure 27

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL^{†‡}
VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

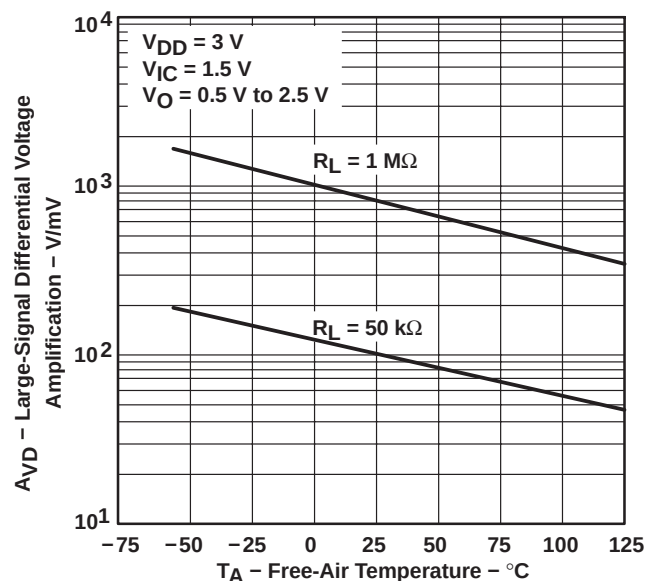


Figure 28

LARGE-SIGNAL DIFFERENTIAL^{†‡}
VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

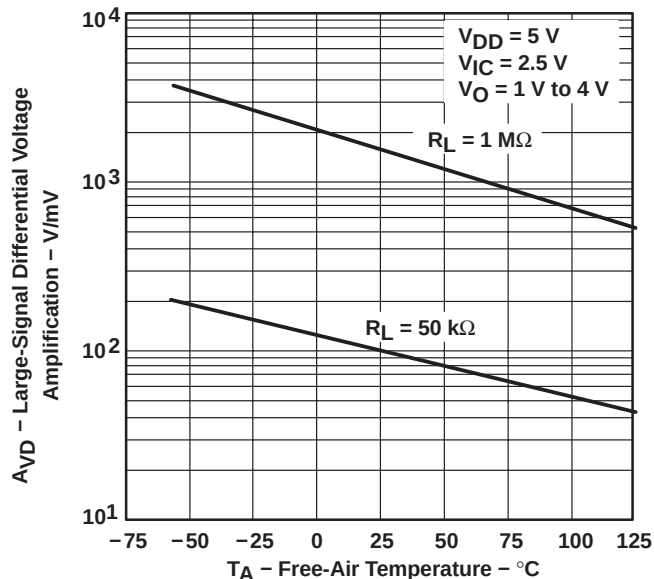


Figure 29

OUTPUT IMPEDANCE[‡]
vs
FREQUENCY

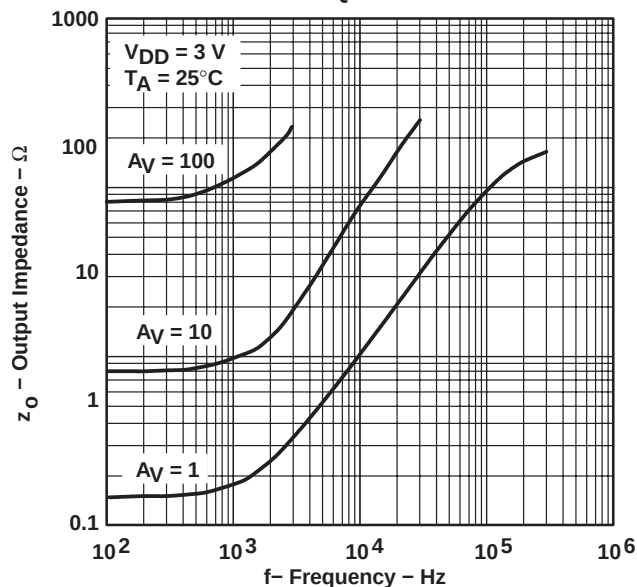


Figure 30

OUTPUT IMPEDANCE[‡]
vs
FREQUENCY

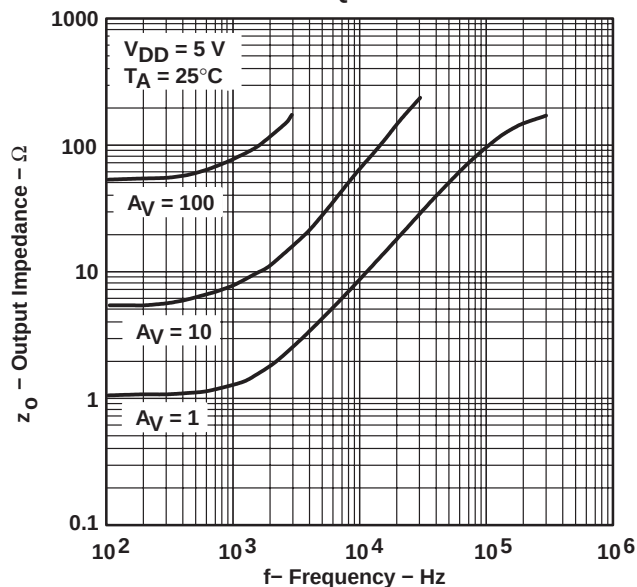


Figure 31

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

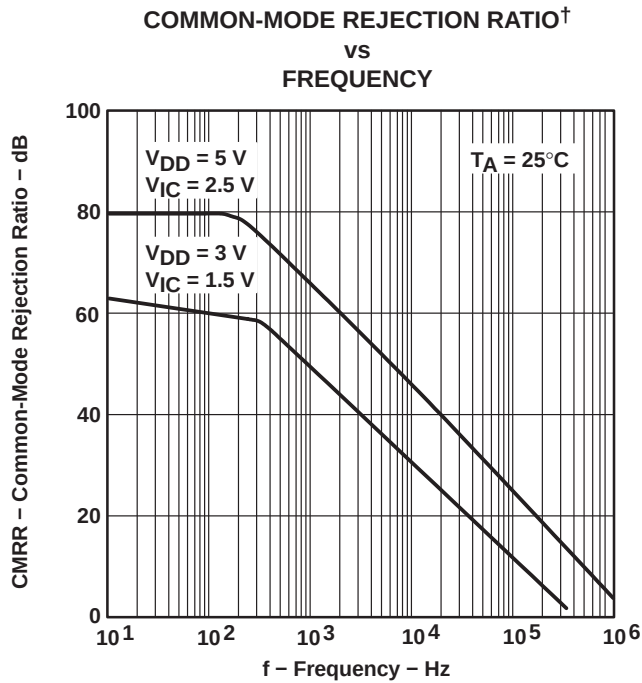


Figure 32

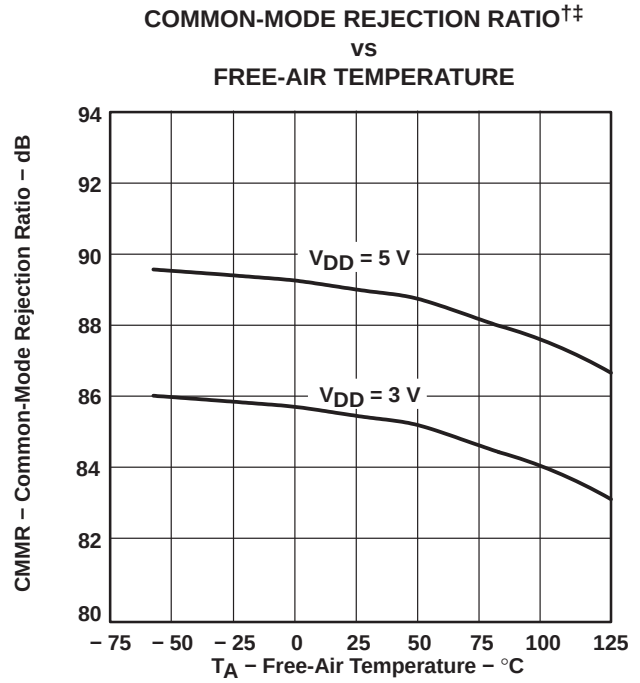


Figure 33

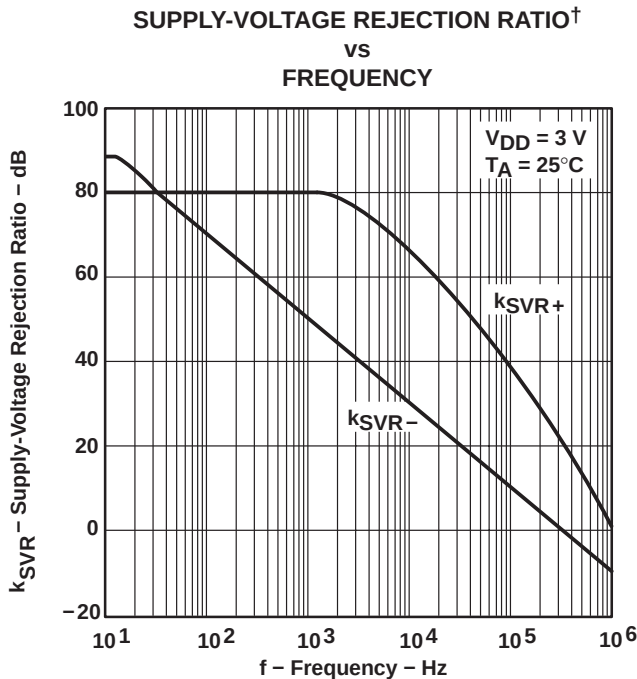


Figure 34

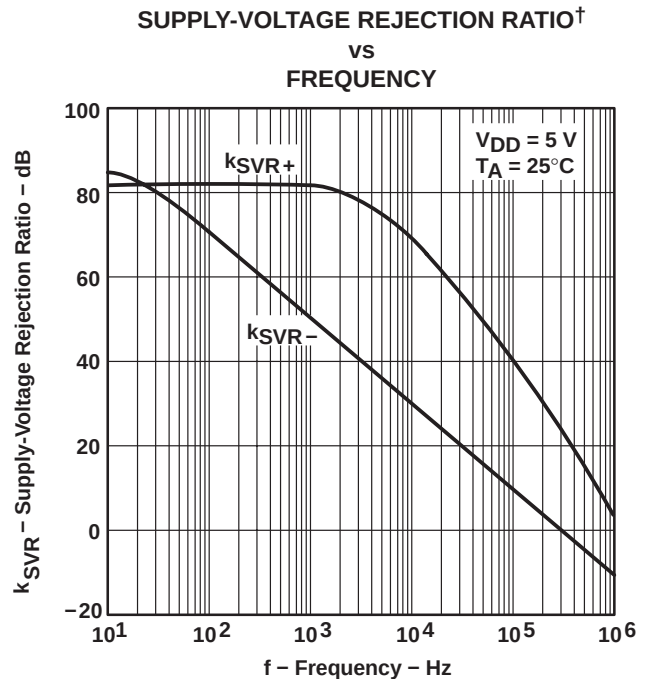


Figure 35

[†] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

^{††} Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TYPICAL CHARACTERISTICS

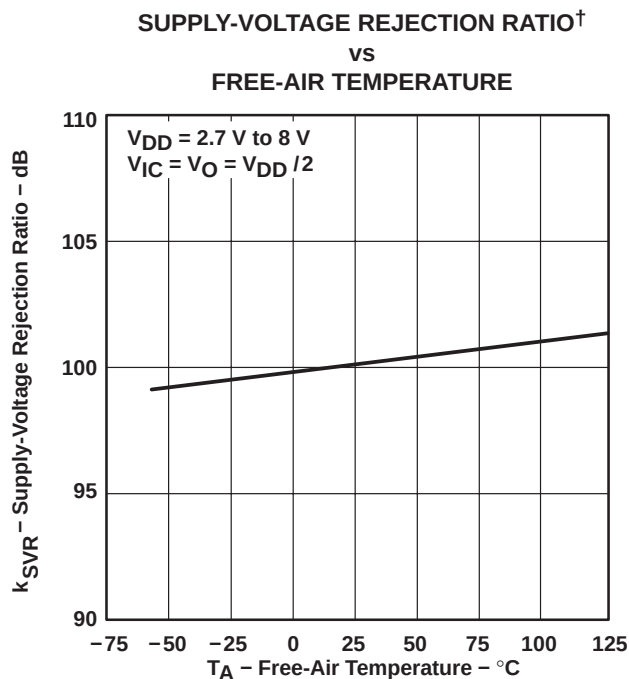


Figure 36

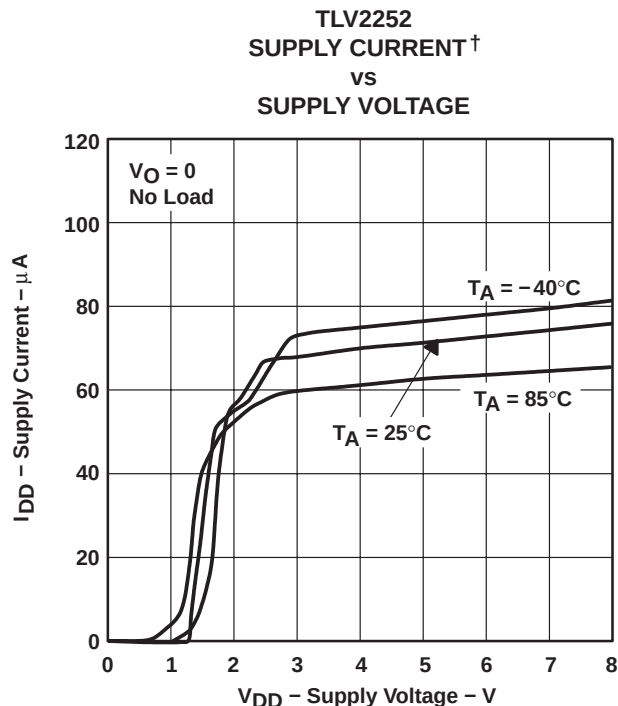


Figure 37

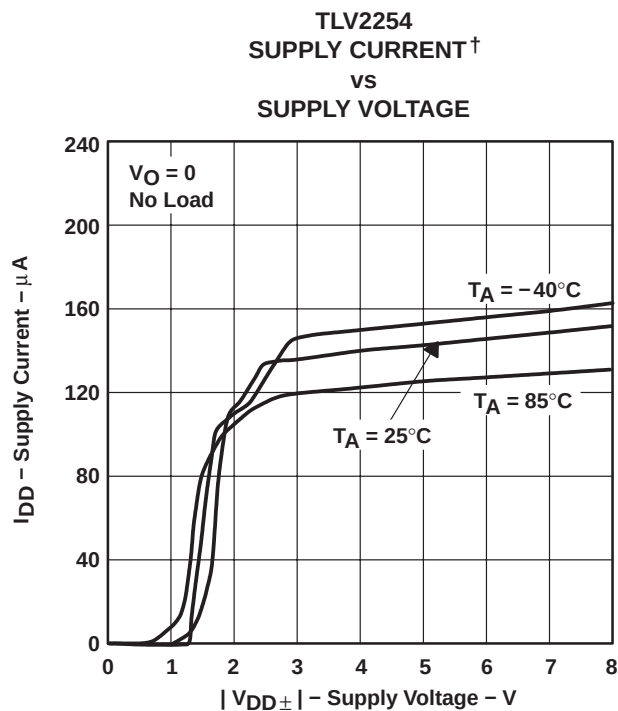


Figure 38

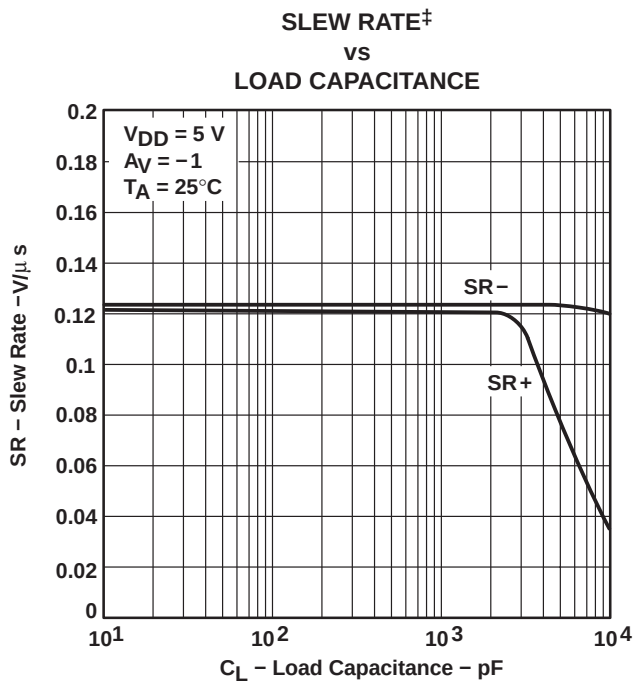
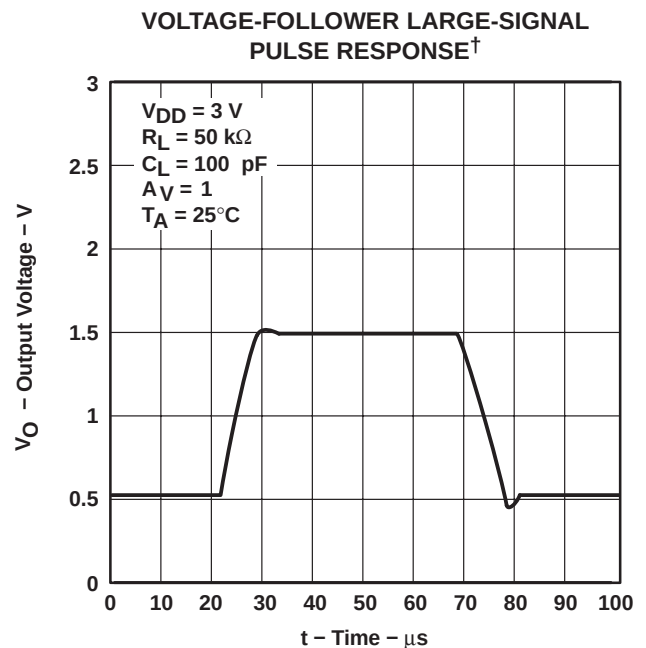
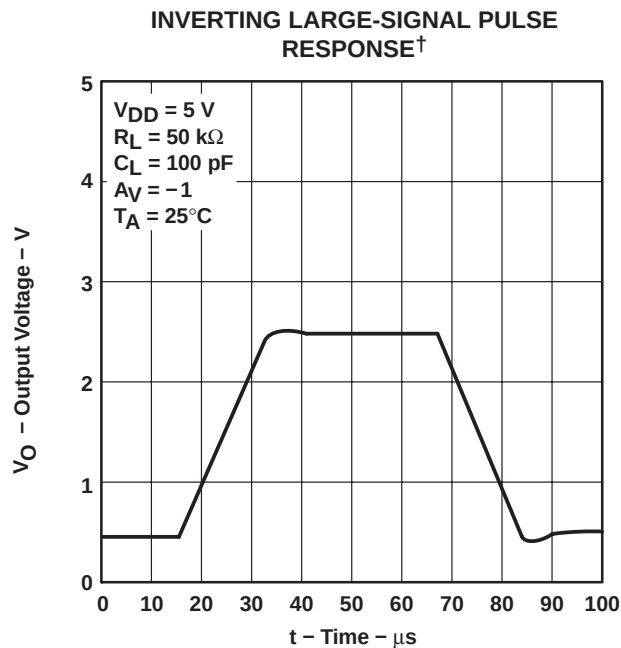
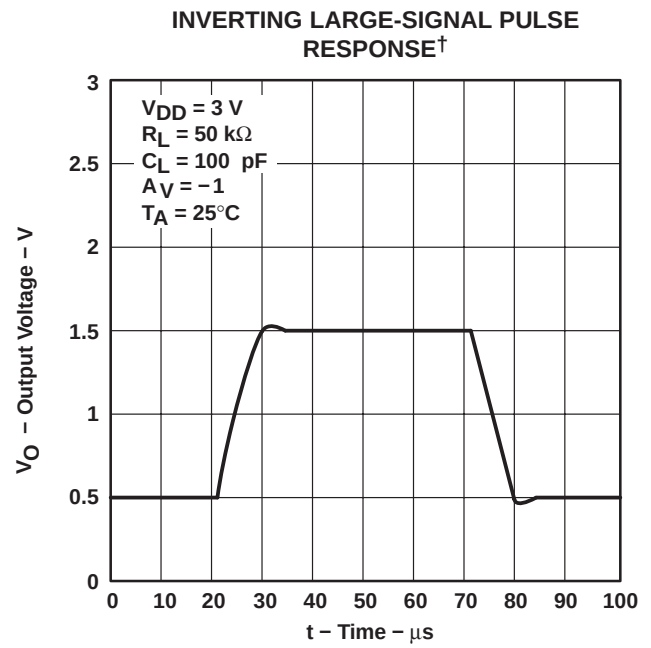
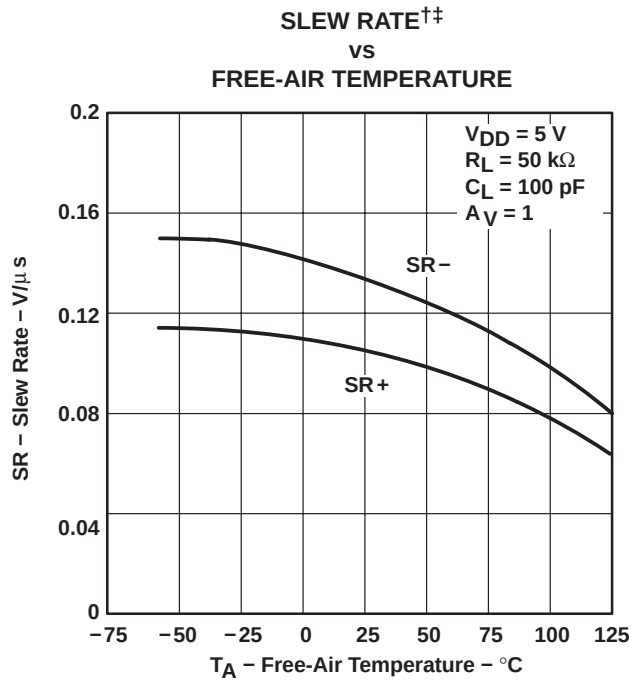


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 \text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL
PULSE RESPONSE†

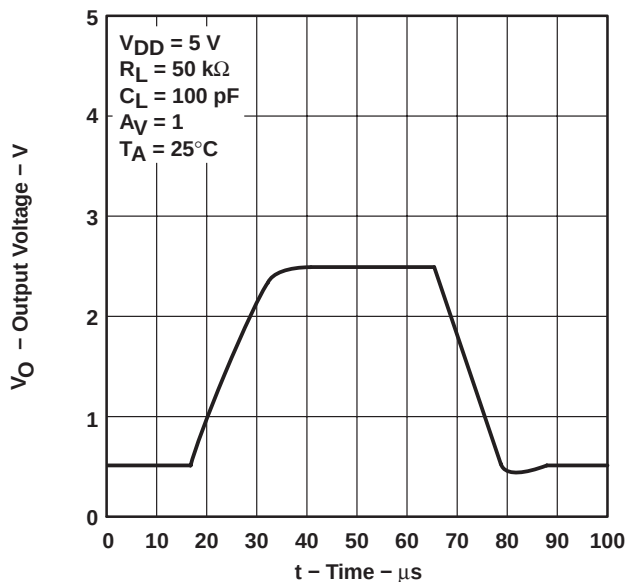


Figure 44

INVERTING SMALL-SIGNAL
PULSE RESPONSE†

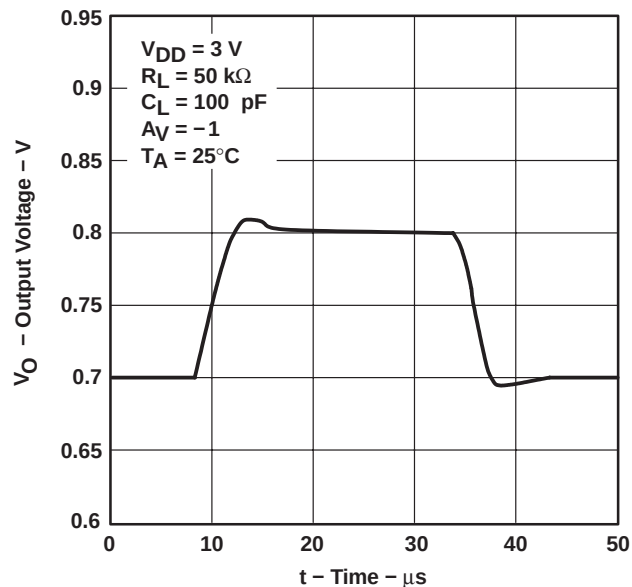


Figure 45

INVERTING SMALL-SIGNAL
PULSE RESPONSE†

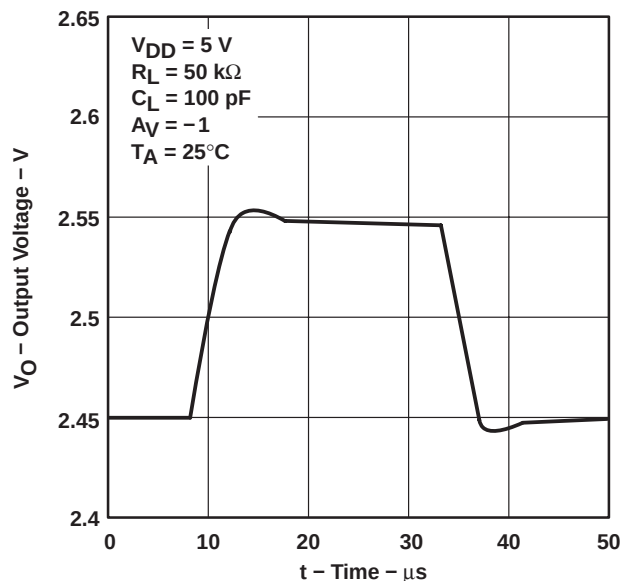


Figure 46

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE†

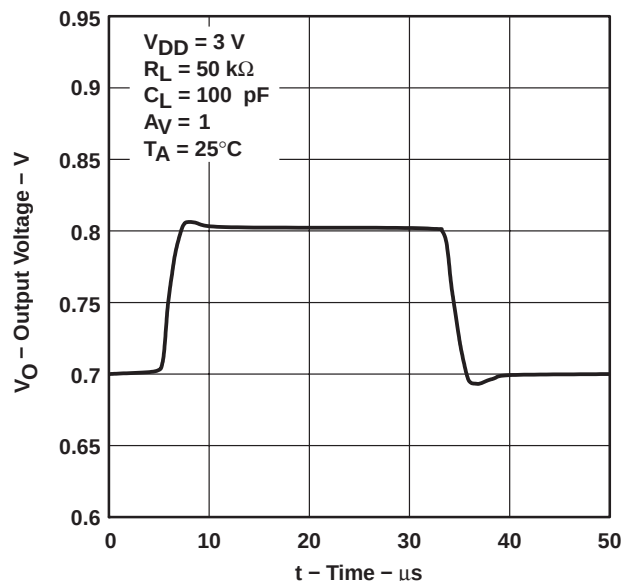
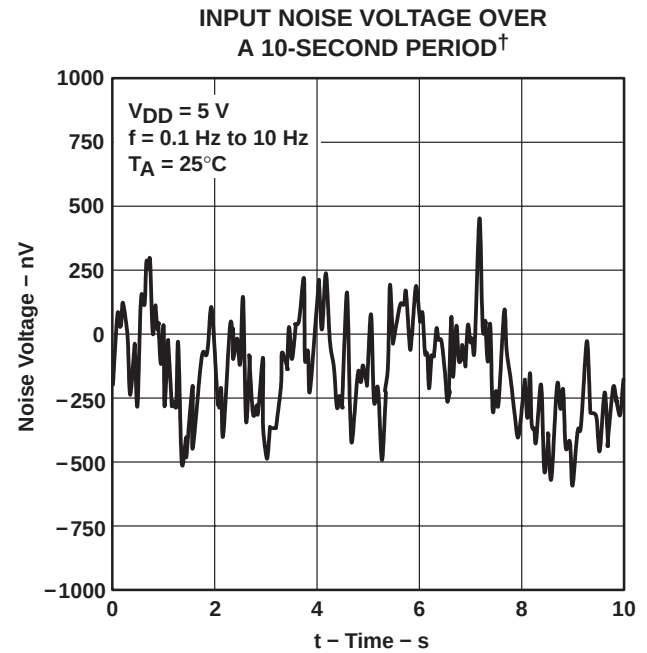
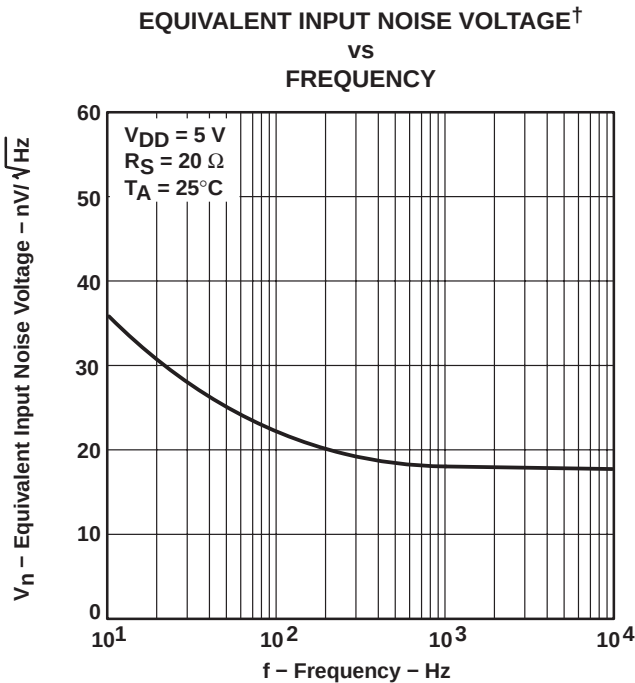
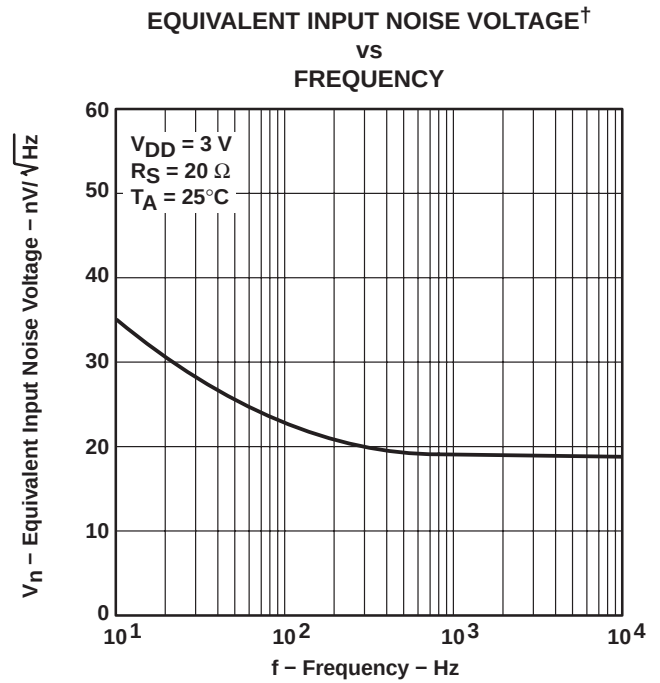
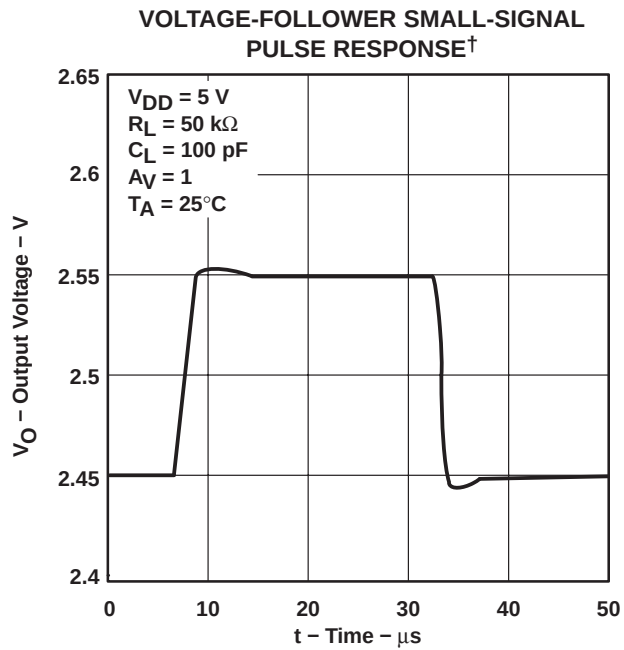


Figure 47

† For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

TYPICAL CHARACTERISTICS

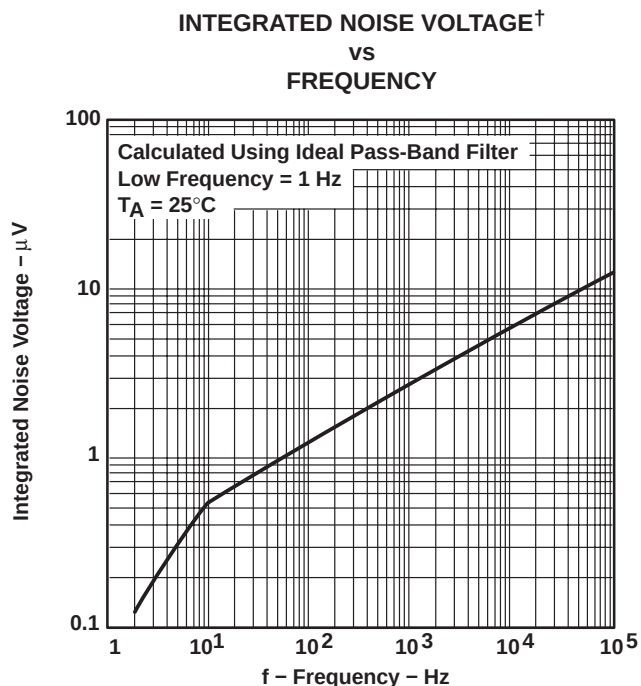


Figure 52

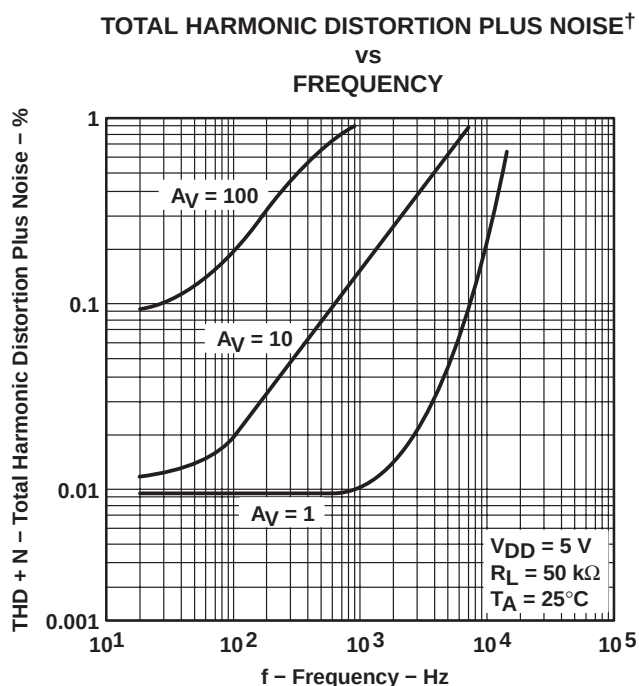


Figure 53

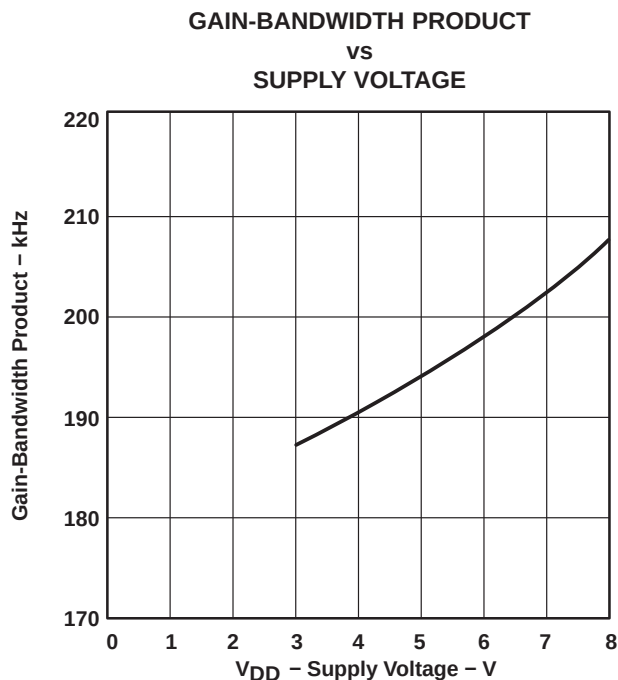


Figure 54

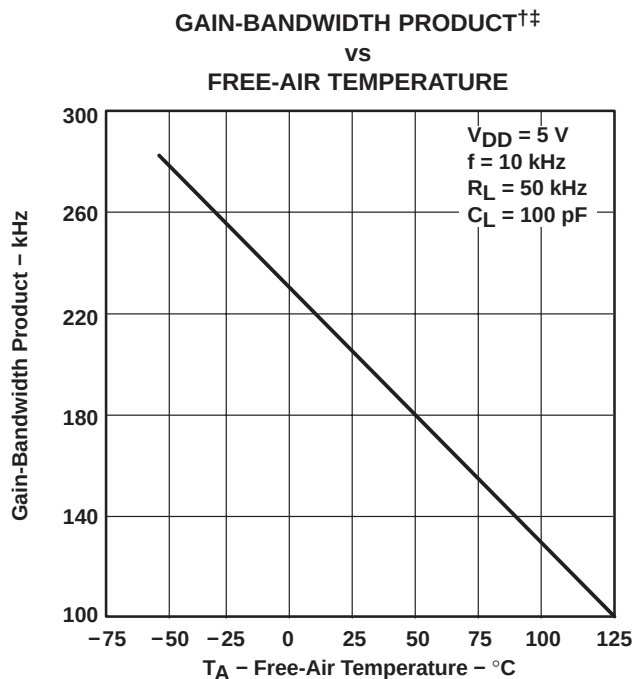
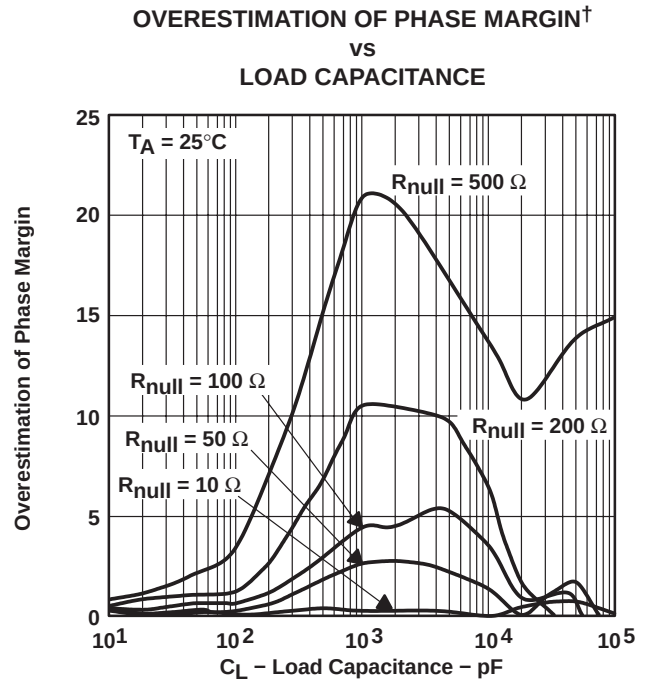
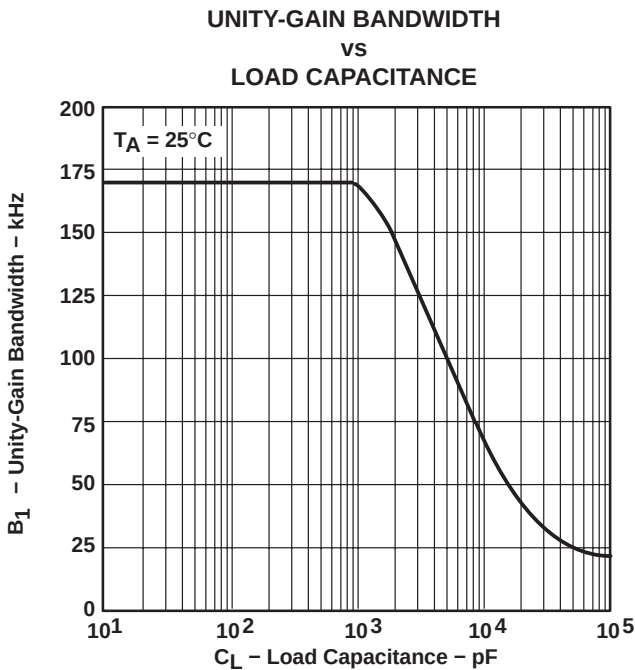
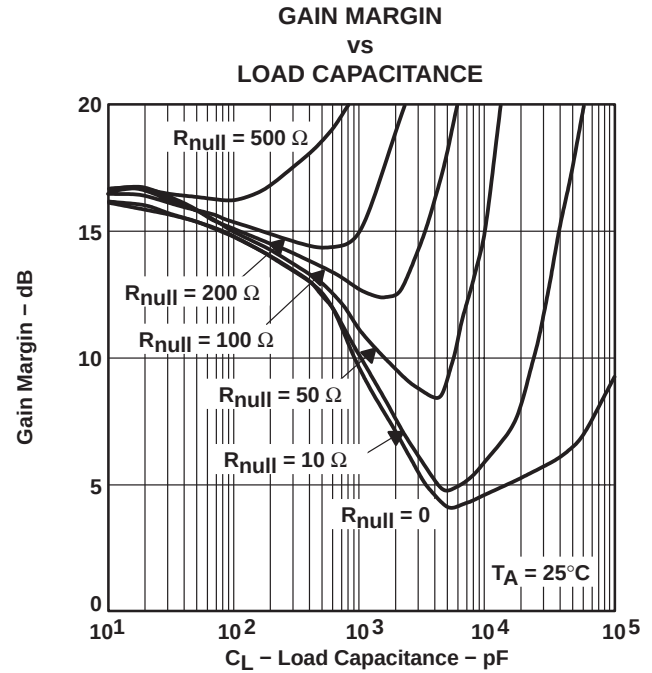
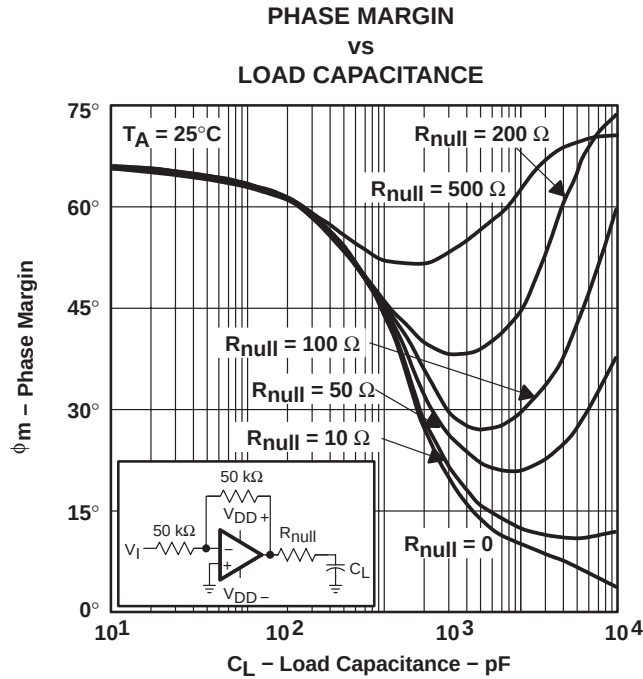


Figure 55

[†] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



† See application information

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V . For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V .
 ‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLV225x, TLV225xA

Advanced LinCMOS™ RAIL-TO-RAIL

VERY LOW-POWER OPERATIONAL AMPLIFIERS

SLOS185D – FEBRUARY 1997 – REVISED AUGUST 2006

APPLICATION INFORMATION

driving large capacitive loads

The TLV2252 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 56 and Figure 57 illustrate its ability to drive loads up to 1000 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 60) improves the gain and phase margins when driving large capacitive loads. Figure 55 and Figure 56 show the effects of adding series resistances of 10 Ω , 50 Ω , 100 Ω , 200 Ω , and 500 Ω . The addition of this series resistor has two effects: the first adds a zero to the transfer function and the second reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1} \left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L \right) \quad (1)$$

Where :

$\Delta\phi_{m1}$ = improvement in phase margin

UGBW = unity-gain bandwidth frequency

R_{null} = output series resistance

C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 58). To use equation 1, UGBW must be approximated from Figure 58.

Using equation 1 alone overestimates the improvement in phase margin as illustrated in Figure 59. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin.

Using Figure 60, with equation 1 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

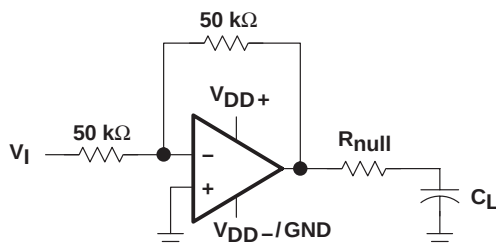


Figure 60. Series-Resistance Circuit

39

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9550401QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9550401QPA TLV2262M	Samples
5962-9550403QHA	ACTIVE	CFP	U	10	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9550403QHA TLV2262AM	Samples
5962-9550403QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9550403QPA TLV2262AM	Samples
5962-9566601QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9566601QPA TLV2252M	Samples
5962-9566603QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9566603QPA TLV2252AM	Samples
TLV2252AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2252A	Samples
TLV2252AIDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2252A	Samples
TLV2252AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2252A	Samples
TLV2252AIDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2252A	Samples
TLV2252AIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2252AI	Samples
TLV2252AIPW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY252A	Samples
TLV2252AIPWG4	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY252A	Samples
TLV2252AIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY252A	Samples
TLV2252AMJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9566603QPA TLV2252AM	Samples
TLV2252AQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		V2252A	Samples
TLV2252ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2252I	Samples
TLV2252IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2252I	Samples
TLV2252IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2252I	Samples
TLV2252IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2252IP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2252MJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9566601QPA TLV2252M	Samples
TLV2254AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2254AI	Samples
TLV2254AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2254AI	Samples
TLV2254AIN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2254AIN	Samples
TLV2254AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2254A	Samples
TLV2254AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2254A	Samples
TLV2254AIPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2254A	Samples
TLV2254AQD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2254A	Samples
TLV2254ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2254I	Samples
TLV2254IDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2254I	Samples
TLV2254IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2254I	Samples
TLV2254IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2254IN	Samples
TLV2262AMJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9550403QPA TLV2262AM	Samples
TLV2262AMUB	ACTIVE	CFP	U	10	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9550403QHA TLV2262AM	Samples
TLV2262MJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9550401QPA TLV2262M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV2252, TLV2252A, TLV2252AM, TLV2252M, TLV2254A, TLV2262AM, TLV2262M :

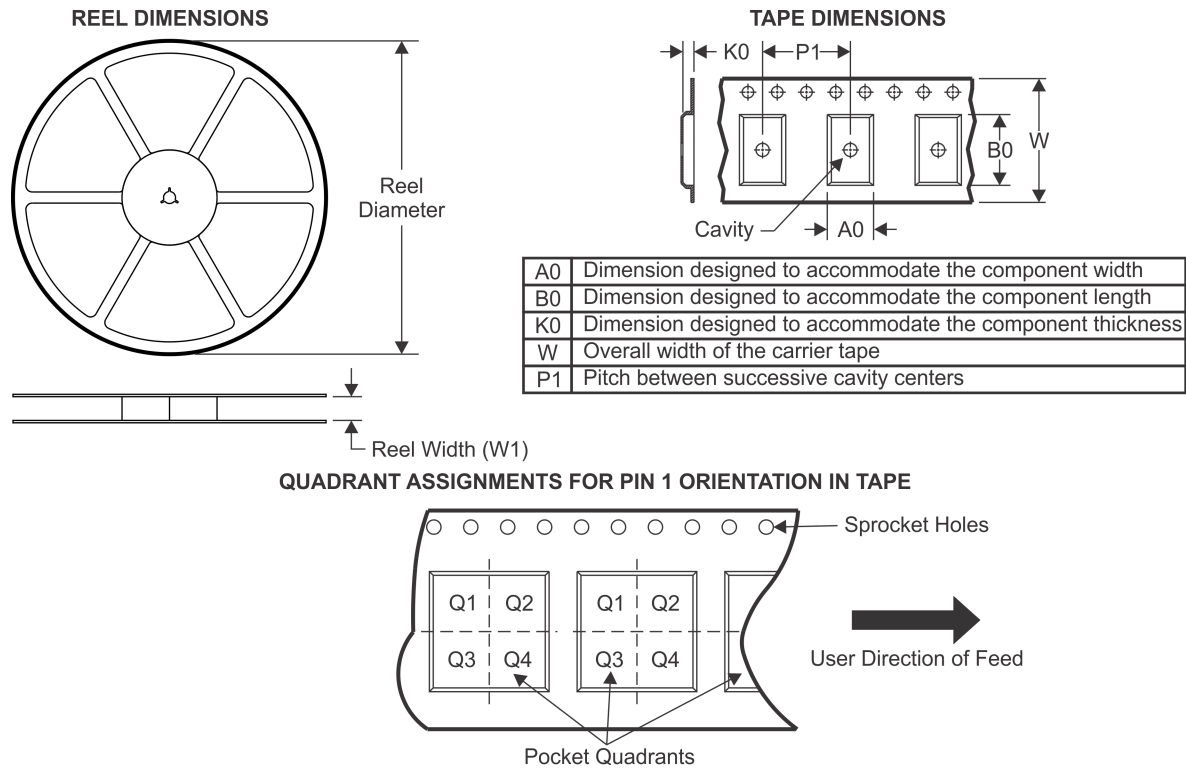
- Catalog : [TLV2252A](#), [TLV2252](#), [TLV2262A](#), [TLV2262](#)
- Automotive : [TLV2252-Q1](#), [TLV2252A-Q1](#), [TLV2252A-Q1](#), [TLV2252-Q1](#), [TLV2262A-Q1](#)
- Enhanced Product : [TLV2252A-EP](#), [TLV2252A-EP](#), [TLV2254A-EP](#)
- Military : [TLV2252M](#), [TLV2252AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

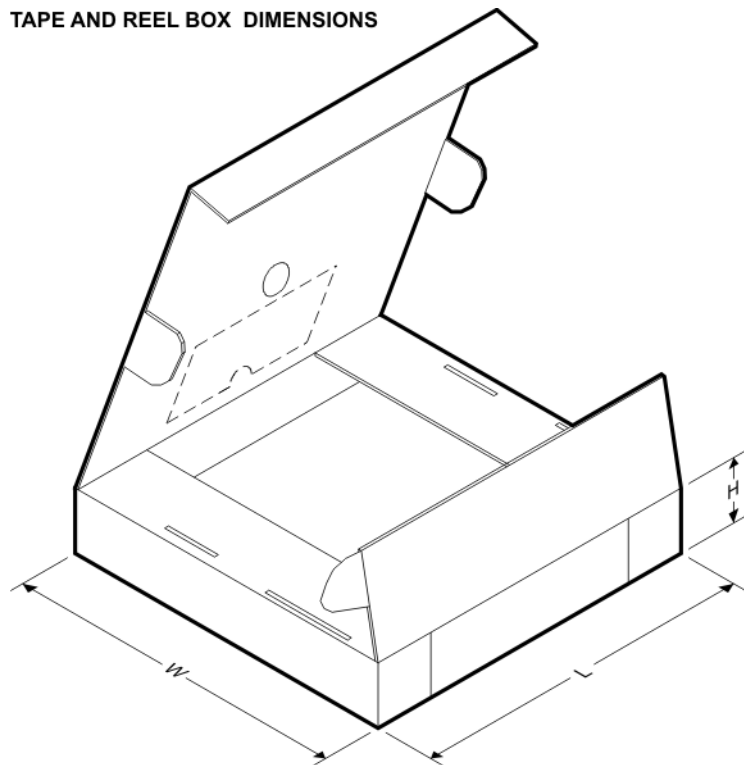
TAPE AND REEL INFORMATION



*All dimensions are nominal

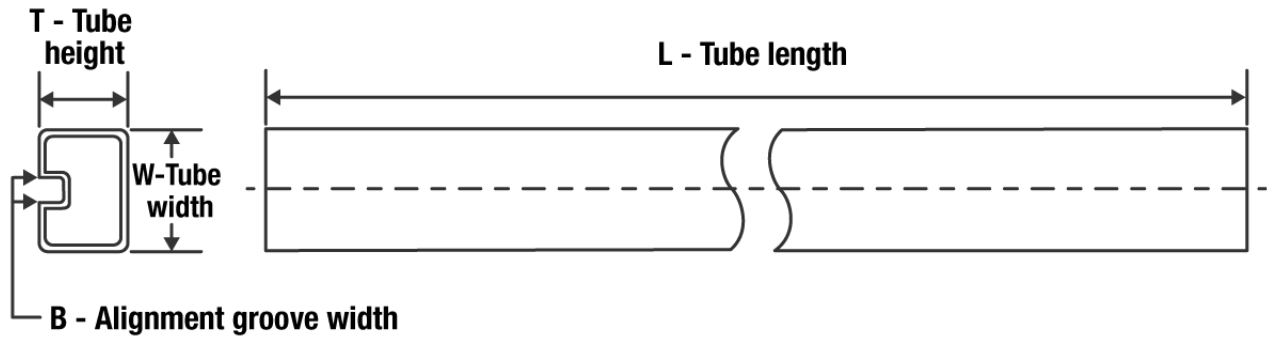
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2252AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2252AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2252IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2254AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2254AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2254IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



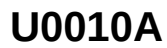
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2252AIDR	SOIC	D	8	2500	340.5	336.1	25.0
TLV2252AIPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
TLV2252IDR	SOIC	D	8	2500	340.5	336.1	25.0
TLV2254AIDR	SOIC	D	14	2500	350.0	350.0	43.0
TLV2254AIPWR	TSSOP	PW	14	2000	853.0	449.0	35.0
TLV2254IDR	SOIC	D	14	2500	350.0	350.0	43.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLV2252AID	D	SOIC	8	75	507	8	3940	4.32
TLV2252AID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2252AIDG4	D	SOIC	8	75	507	8	3940	4.32
TLV2252AIDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLV2252AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2252AIPW	PW	TSSOP	8	150	530	10.2	3600	3.5
TLV2252AIPWG4	PW	TSSOP	8	150	530	10.2	3600	3.5
TLV2252ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2252ID	D	SOIC	8	75	507	8	3940	4.32
TLV2252IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2254AID	D	SOIC	14	50	505.46	6.76	3810	4
TLV2254AIN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2254AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLV2254AQD	D	SOIC	14	50	505.46	6.76	3810	4
TLV2254ID	D	SOIC	14	50	505.46	6.76	3810	4
TLV2254IDG4	D	SOIC	14	50	505.46	6.76	3810	4
TLV2254IN	N	PDIP	14	25	506	13.97	11230	4.32



CFP - 2.03 mm max height

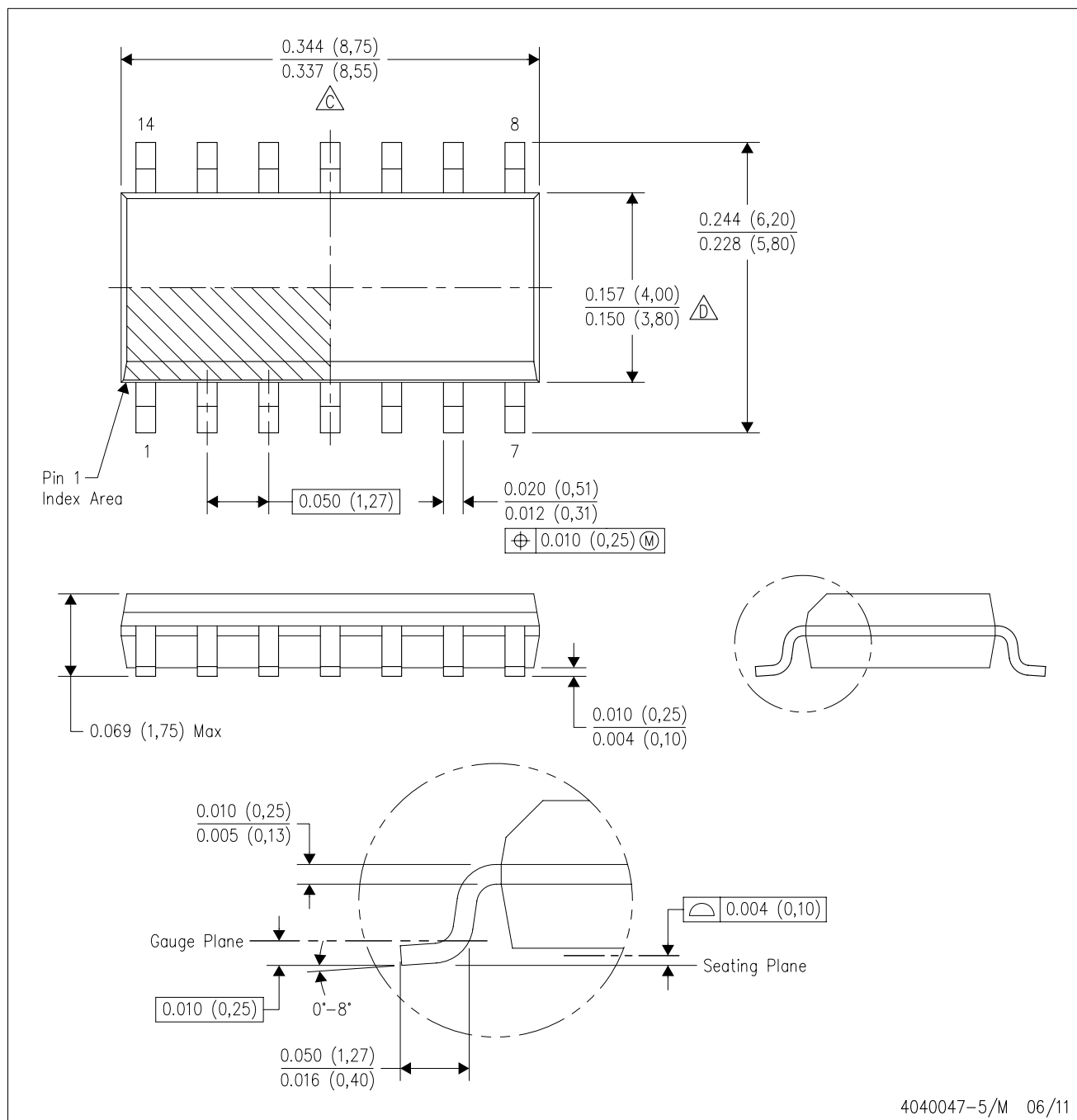
.045 MAX TYP
 .010 ± .002
 PIN 1 ID
 .27 MAX GLASS
 .005 MIN TYP
 1
 10
 .27 MAX GLASS
 5
 6
 8X .050 ± .005
 10X .017 ± .002
 5X .32 ± .01
 .241^{+.019}_{-.003}
 5X .32 ± .01
 .005 ± .001
 .067^{+.013}_{-.012}
 .045
 .026



**TEXAS
INSTRUMENTS**
www.ti.com

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



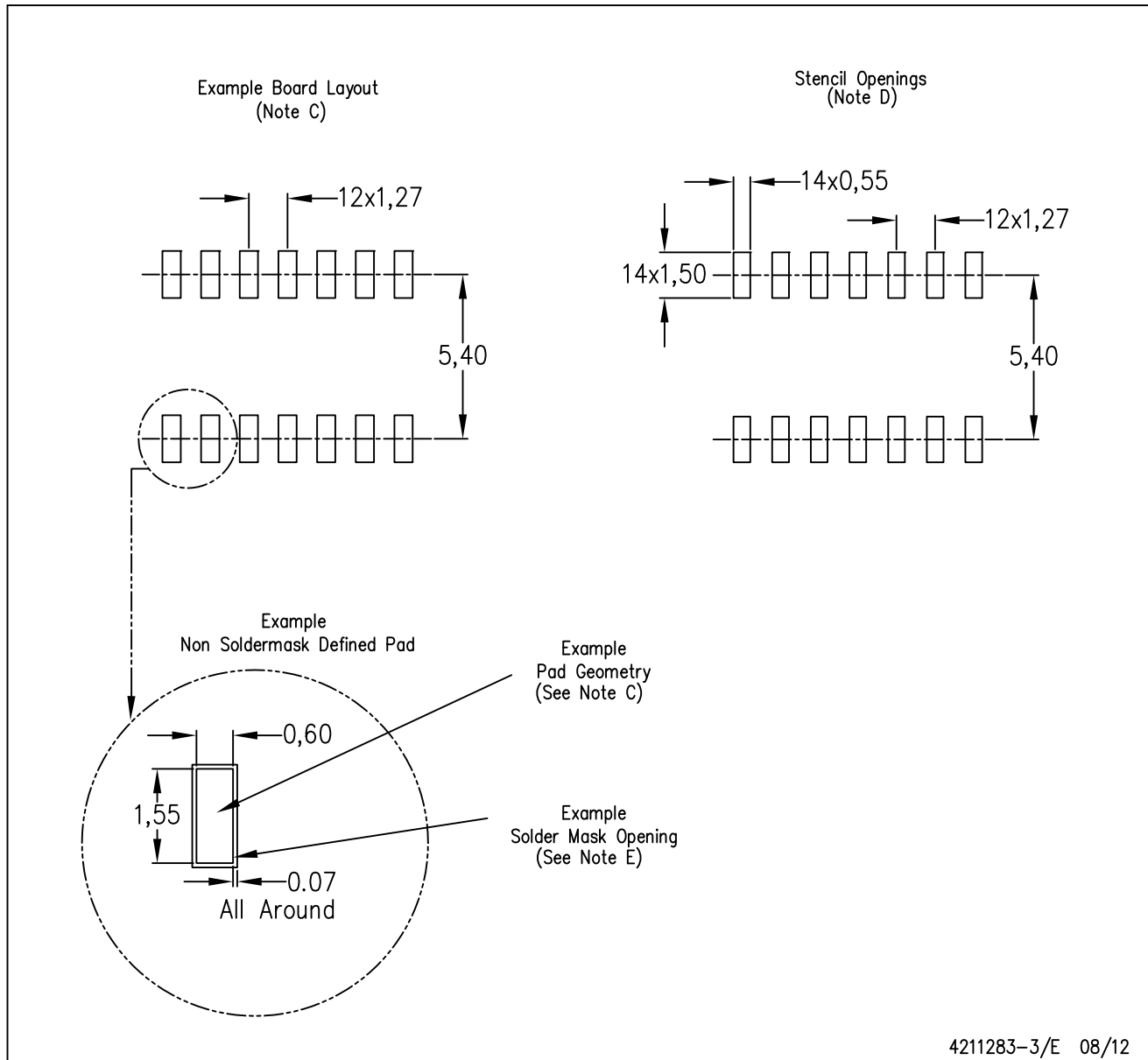
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

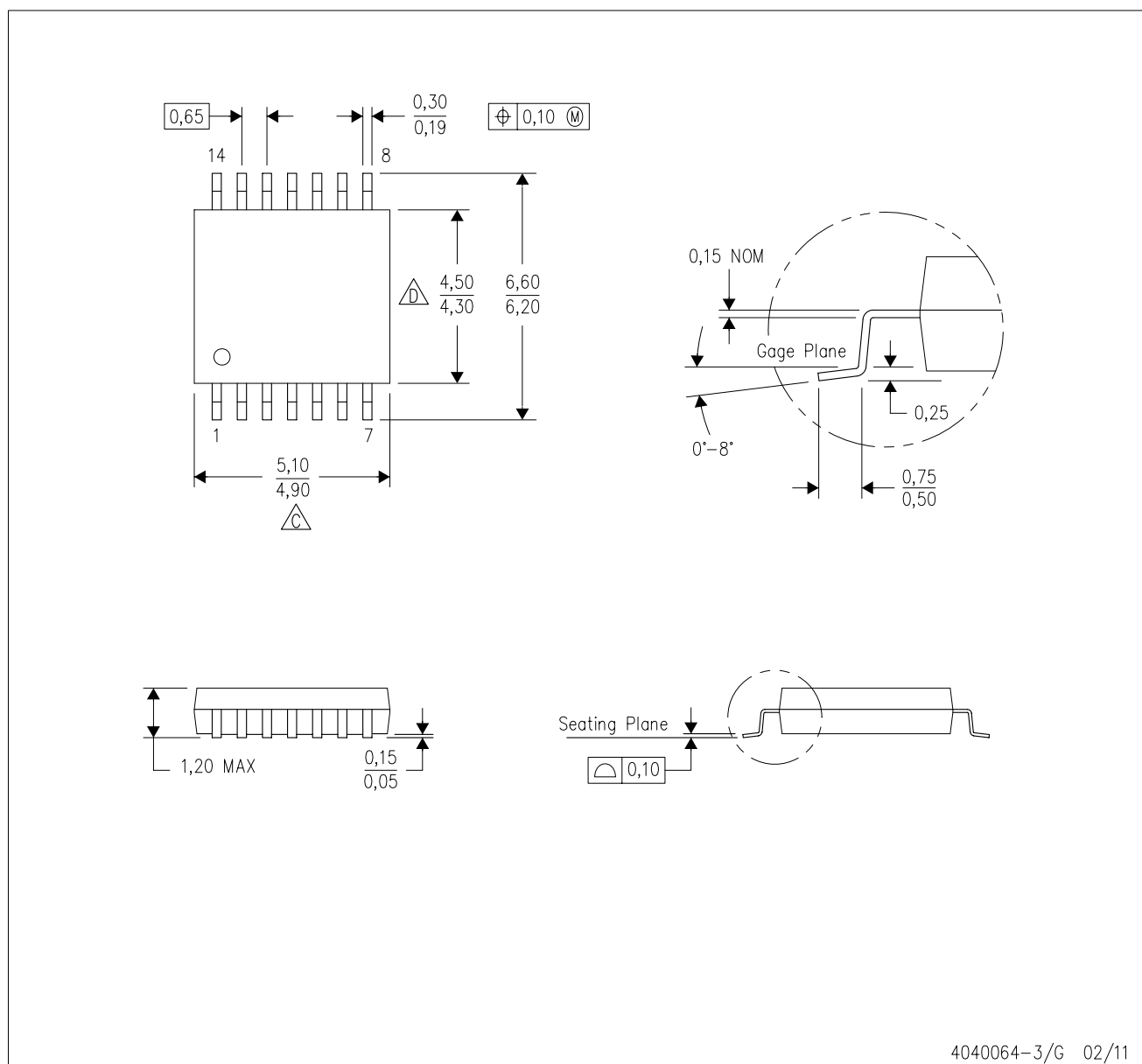
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



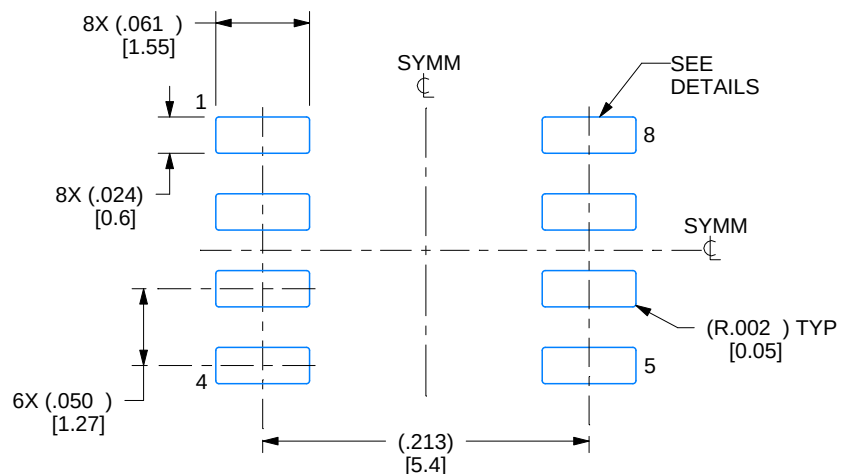
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

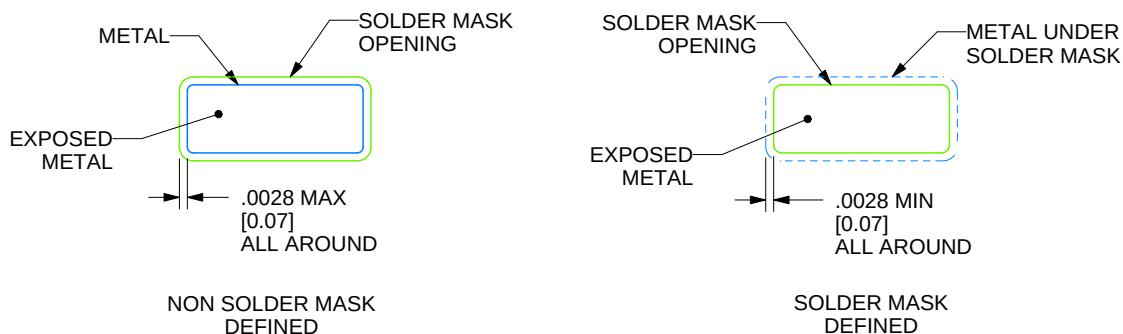
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

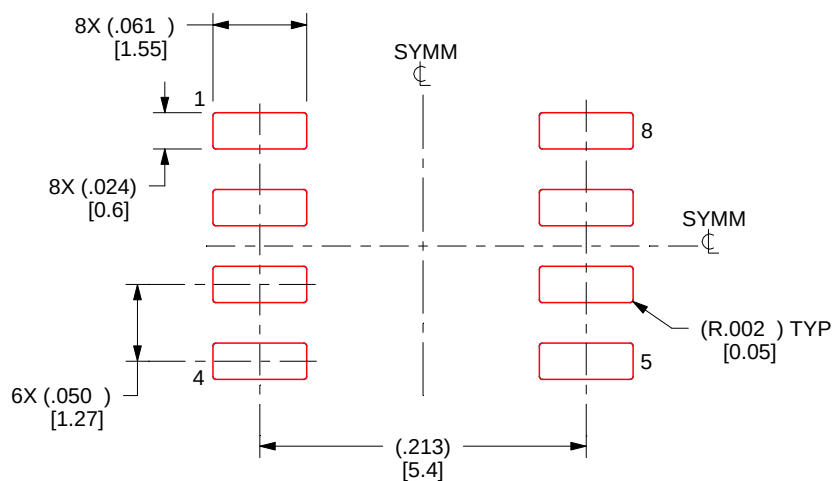
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

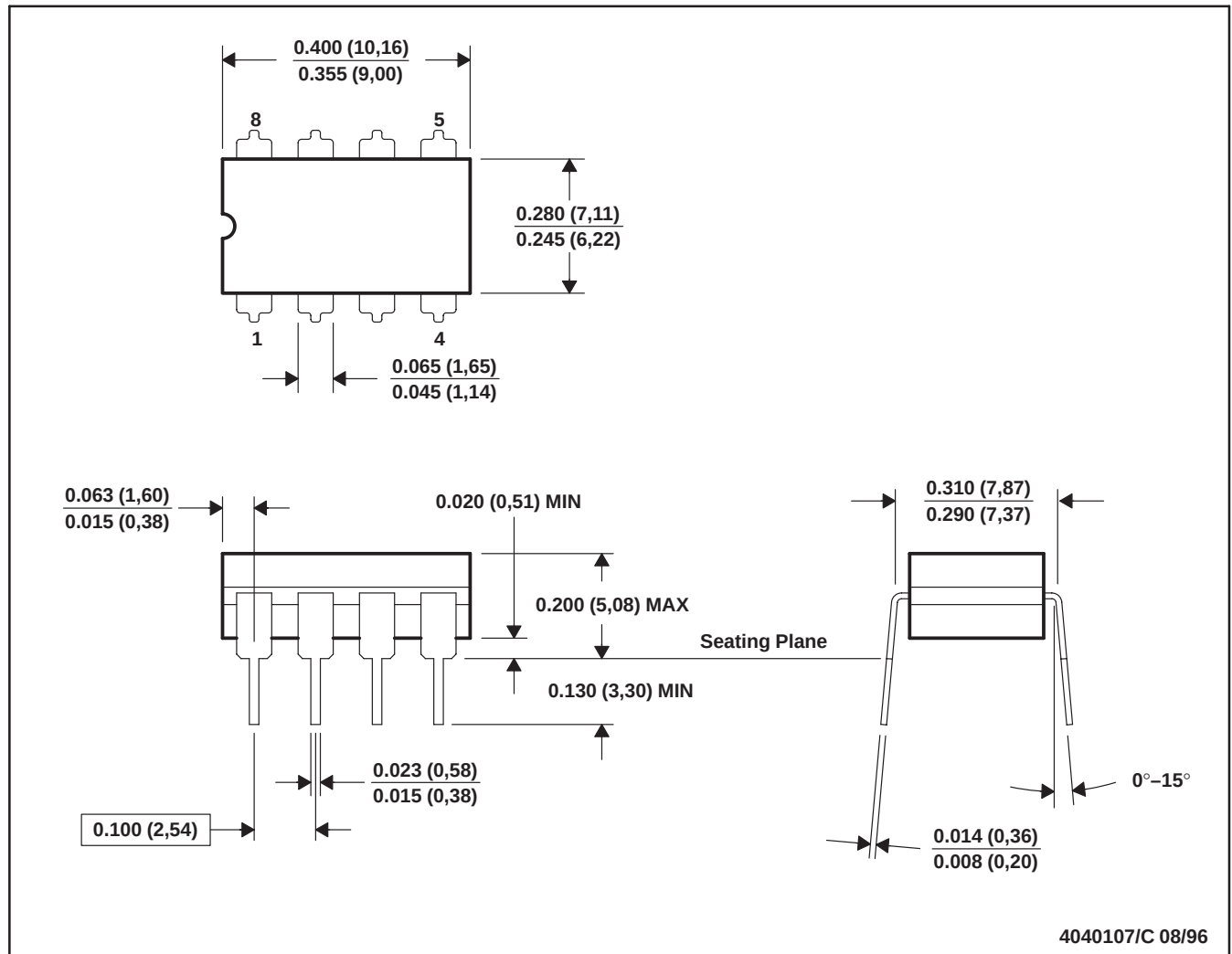
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

JG (R-GDIP-T8)

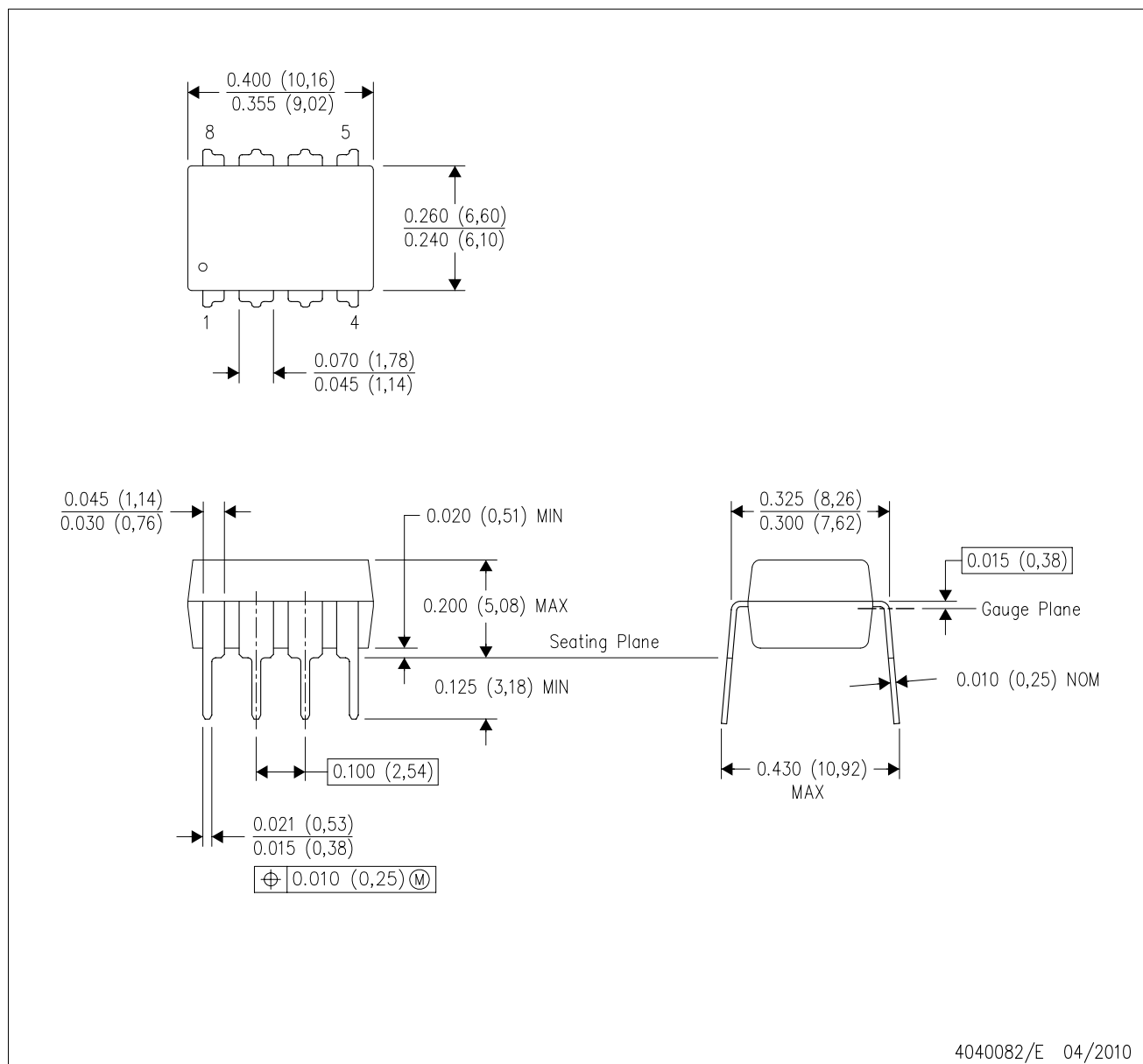
CERAMIC DUAL-IN-LINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification.
 - E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

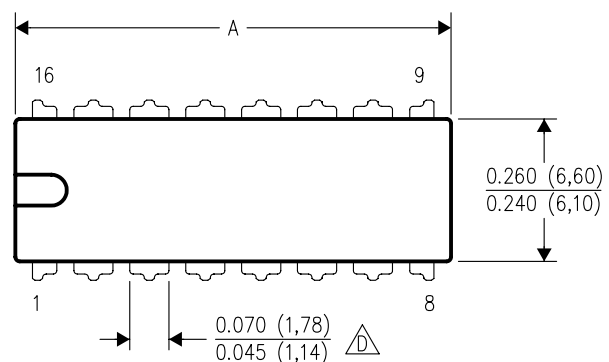


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

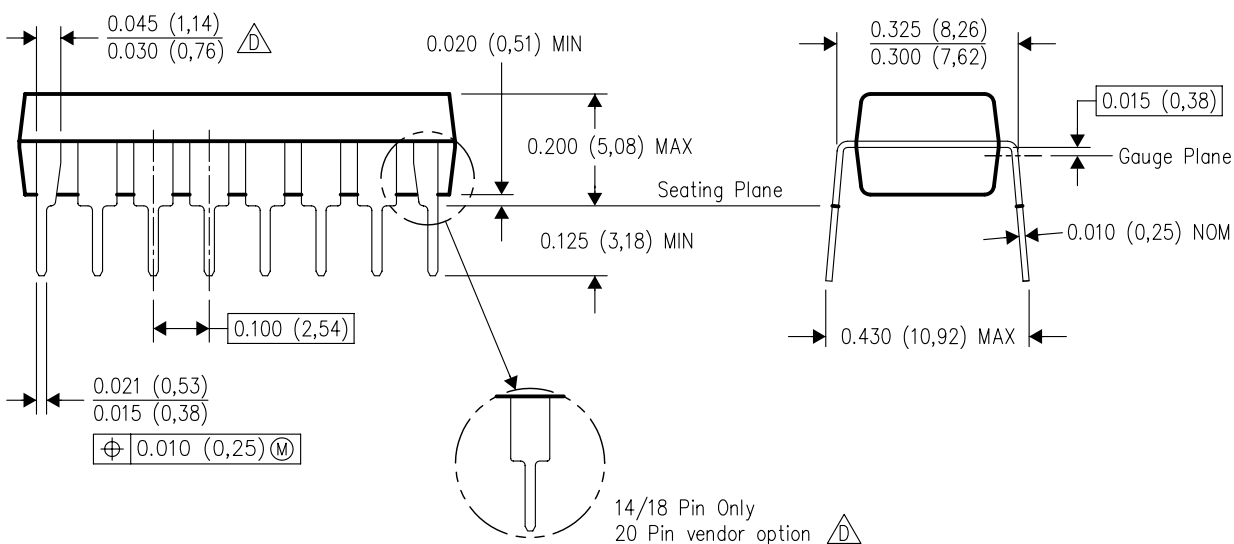
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

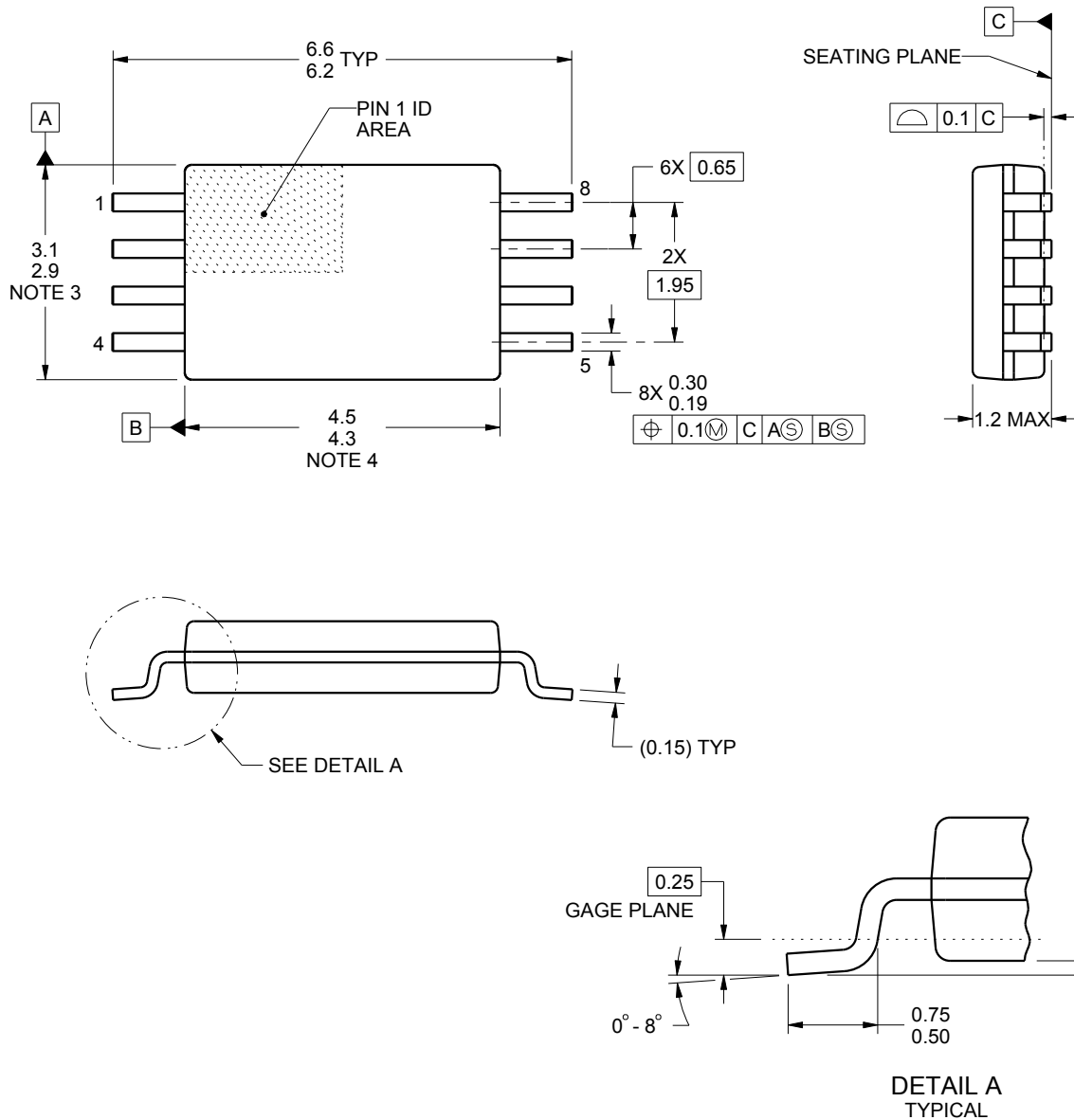
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

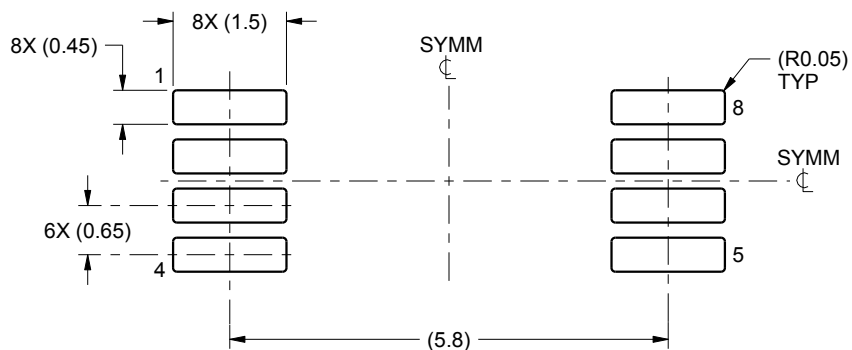
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

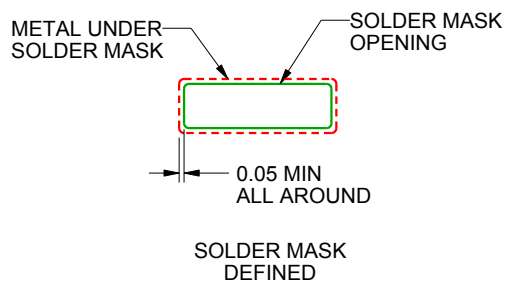
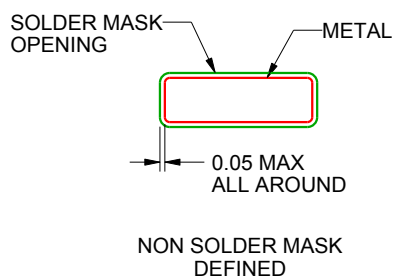
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

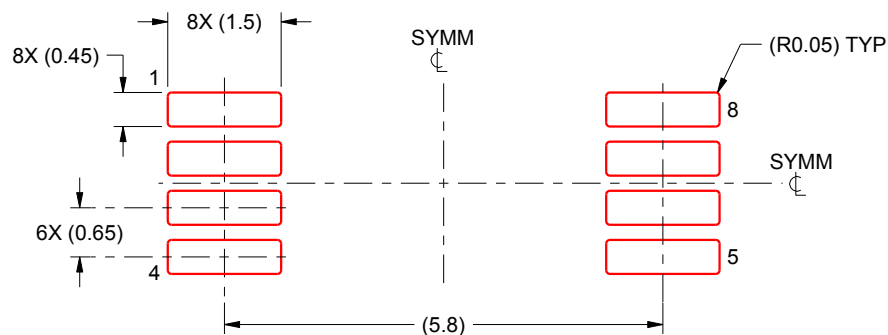
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated