

# 省电型流控螺线管驱动器

查询样品: [DRV120](#)

## 特性

- 用于控制螺线管电流的带有脉宽调制 (**PWM**) 的集成金属氧化物半导体场效应晶体管 (**MOSFET**)
  - 用于调节螺线管电流的外部感测电阻器
- 螺线管电流的快速斜升以保证激活
- 在保持模式中, 为了实现低功耗和热耗散, 螺线管电流被减少
- 可外部设定峰值电流、峰值电流的保持时间、保持电流和 **PWM** 时钟频率。它们还可以在无需外部组件的情况下在标称值上运行。
- 内部电源电压调节
  - 高达 **28V** 的外部电源电压

- 保护
  - 热关断
  - 欠压闭锁 (**UVLO**)
  - 最大斜升时间
  - 可选状态 (**STATUS**) 输出
- 运行温度范围: **-40°C 至 105°C**
- **8 引脚和 14 引脚 薄型小外形尺寸 (TSSOP) 封装选项**

## 应用范围

- 电动机械驱动器: 螺线管、阀门、继电器
- 大型家用电器、太阳能、运输

## 说明

DRV120 是一款针对螺线管的 **PWM** 电流驱动器。它被设计成使用控制良好的电流来调节电流以确保激活并同时减少功率耗散。螺线管电流快速斜升以确保阀门或者继电器的打开。在最初的斜升后, 螺线管电流被保持在峰值以确保正确运行, 这之后, 为了避免过热问题并减少功率耗散, 这个电流被减少至较低的保持水平。

使用一个外部电容器对峰值电流的持续时间进行设定。电流斜波峰值和保持电平、以及 **PWM** 频率可由外部电阻器独立设定。如果针对相应参数的默认值适用于应用的话, 外部设置电阻器也可被省略。

DRV120 可由 6V 至 28V 的外部电源供电运行。

## ORDERING INFORMATION<sup>(1)</sup>

PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
(TSSOP-8) - PW	Reel of 2000	DRV120PWR	120
(TSSOP-14) - PW	Reel of 2000	DRV120APWR	120A

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## TYPICAL APPLICATION

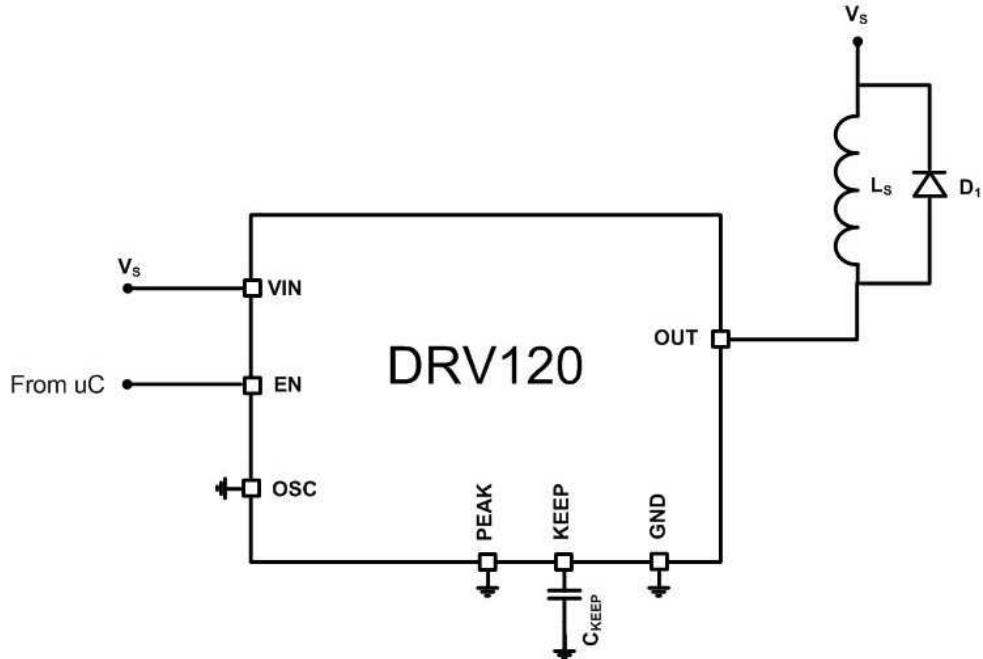


Figure 1. Default Configuration With 8-Pin TSSOP Option

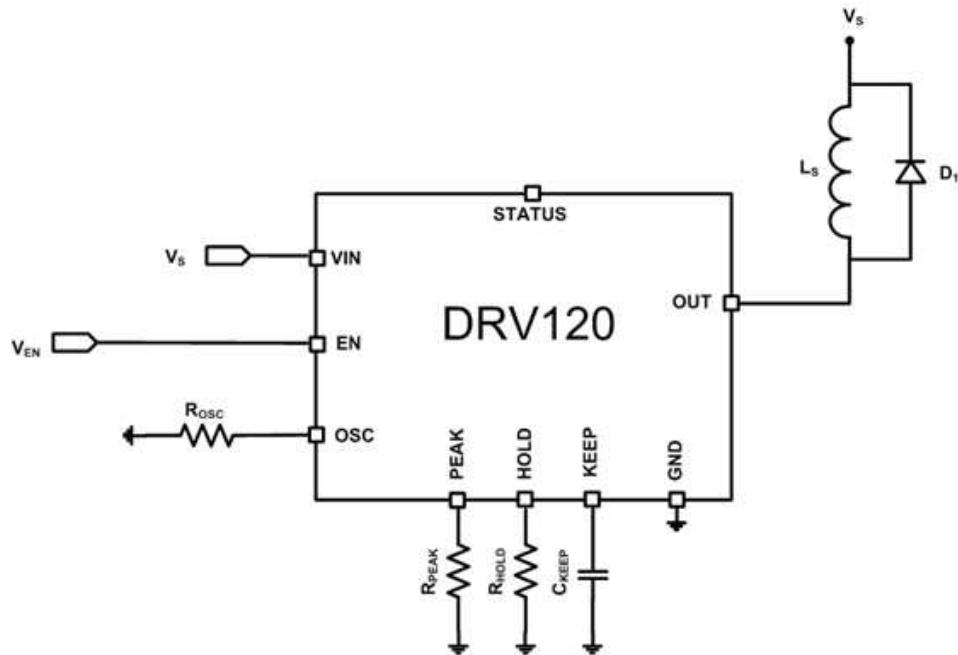


Figure 2. External Parameter Setting for 14-Pin TSSOP Option

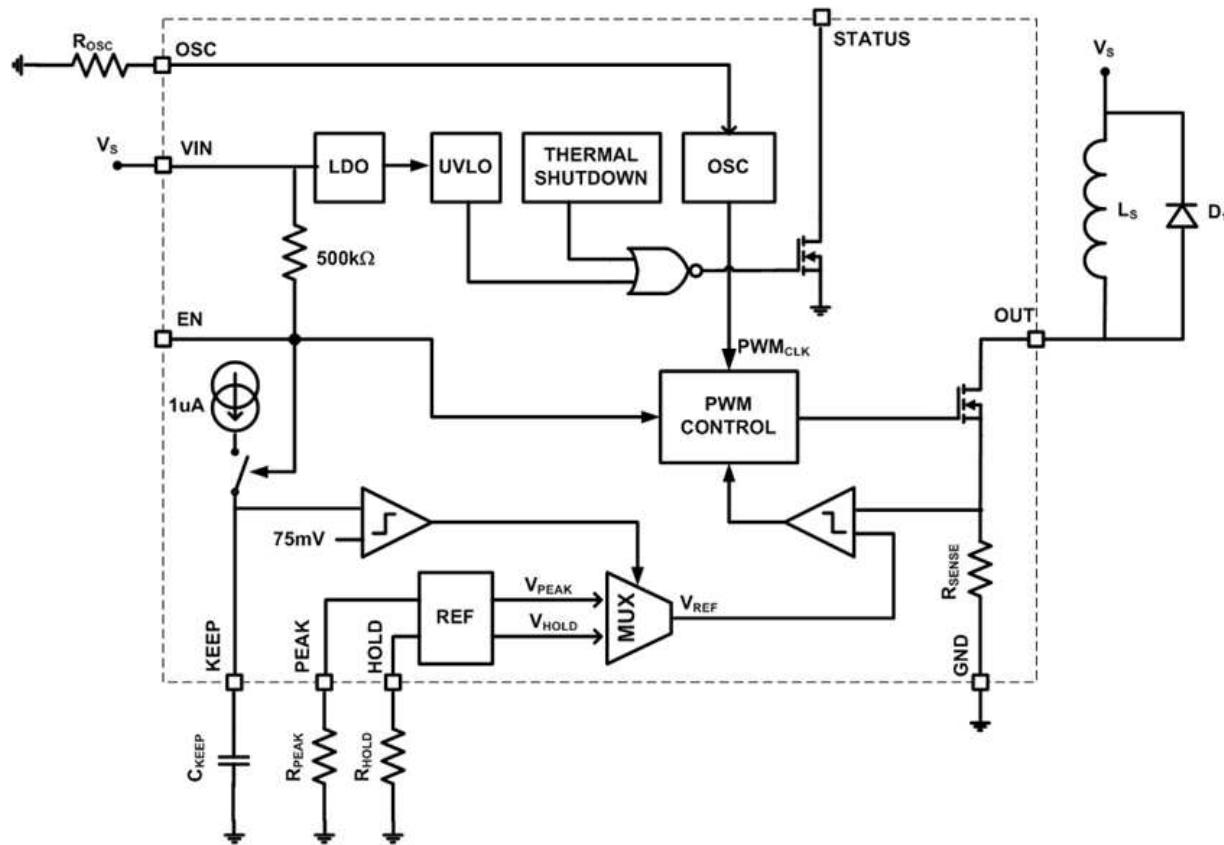
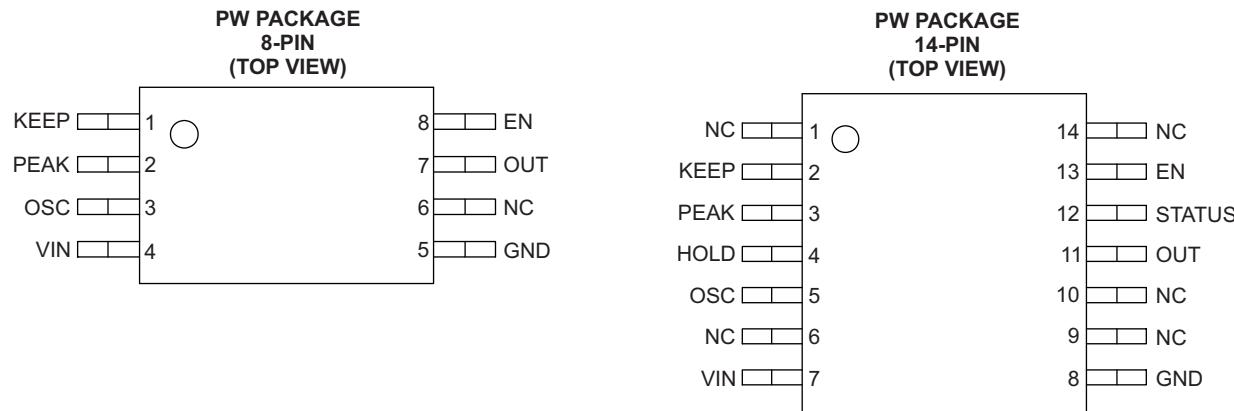
**DEVICE INFORMATION**
**Functional Block Diagram**


Table 1. TERMINAL FUNCTIONS

NAME	PIN (8-PIN PW) <sup>(1)</sup>	PIN (14-PIN PW)	DESCRIPTION
NC	6	1, 6, 9, 10, 14	No connect
KEEP	1	2	Keep time set
PEAK	2	3	Peak current set
HOLD	-	4	Hold current set
OSC	3	5	PWM frequency set
VIN	4	7	6-V to 28-V supply
GND	5	8	Ground
OUT	7	11	Controlled current sink
STATUS	-	12	Open drain fault indicator
EN	8	13	Enable

(1) In the 8-pin package, the HOLD pin is not bonded out. For this package, the HOLD mode is configured to default (internal) settings.



**ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>**

		VALUE	UNIT
VIN	Input voltage range	–0.3 to 28	V
	Voltage range on EN, STATUS, PEAK, HOLD, OSC, SENSE, RAMP	–0.3 to 7	V
	Voltage range on OUT	–0.3 to 28	V
ESD rating	HBM (human body model)	2000	V
	CDM (charged device model)	500	
T <sub>J</sub>	Operating virtual junction temperature range	–40 to 125	°C
T <sub>stg</sub>	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

**RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I <sub>OUT</sub>	Average solenoid DC current			125	mA
V <sub>IN</sub>	Supply voltage	6	12	26	V
C <sub>IN</sub>	Input capacitor	1	4.7		μF
L	Solenoid inductance			1	H
T <sub>A</sub>	Operating ambient temperature	–40		105	°C

**THERMAL INFORMATION**

THERMAL METRIC	DRV120	DRV120	UNITS
	PW	PW	
	8 PINS	14 PINS	
θ <sub>JA</sub>	183.8	122.6	°C/W
θ <sub>JCTop</sub>	69.2	51.2	
θ <sub>JB</sub>	112.6	64.3	
Ψ <sub>JT</sub>	10.4	6.5	
Ψ <sub>JB</sub>	110.9	63.7	
θ <sub>JCbot</sub>	N/A	N/A	

- (1) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然对流条件下的结至环境热阻。
- (2) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
- (3) 按照 JESD51-8 中的说明，通过在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
- (4) 结至顶部特征参数，Ψ<sub>JT</sub>，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ<sub>JA</sub>。
- (5) 结至电路板特征参数，Ψ<sub>JB</sub>，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ<sub>JA</sub>。
- (6) 通过在外露（电源）焊盘上进行冷板测试仿真来获得结至芯片外壳（底部）热阻。不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 14$  V,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$ , over operating free-air temperature range (unless otherwise noted)

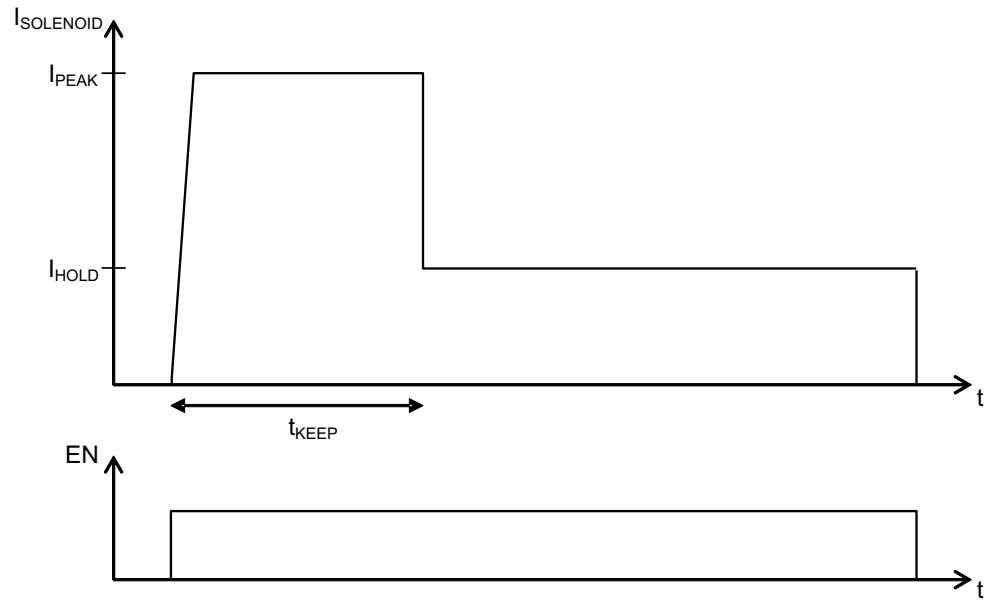
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
$I_Q$	Standby current	$EN = 0, V_{IN} = 14$ V		100	150	$\mu\text{A}$
	Quiescent current	$EN = 1, V_{IN} = 14$ V		300	400	
<b>CURRENT DRIVER</b>						
$R_{OUT}$	OUT to GND resistance	$I_{OUT} = 200$ mA		1.7	2.5	$\Omega$
$f_{PWM}$	PWM frequency	OSC = GND	15	20	25	kHz
$D_{MAX}$	Maximum PWM duty cycle			100		%
$D_{MIN}$	Minimum PWM duty cycle			9		%
$t_D$	Start-up delay	Delay between EN going high until driver enabled <sup>(1)</sup> , $f_{PWM} = 20$ kHz		25	50	$\mu\text{s}$
<b>CURRENT CONTROLLER, INTERNAL SETTINGS</b>						
$I_{PEAK}$	Peak current	PEAK = GND	160	200	240	mA
$I_{HOLD}$	Hold current	HOLD = GND	40	50	60	mA
<b>CURRENT CONTROLLER, EXTERNAL SETTINGS</b>						
$t_{KEEP}^{(2)}$	Externally set keep time at peak current	$C_{KEEP} = 1 \mu\text{F}$		75		ms
$I_{PEAK}$	Externally set peak current	$R_{PEAK} = 50 \text{ k}\Omega$		250		mA
		$R_{PEAK} = 200 \text{ k}\Omega$		83		
$I_{HOLD}$	Externally set hold current	$R_{HOLD} = 50 \text{ k}\Omega$		100		mA
		$R_{HOLD} = 200 \text{ k}\Omega$		33		
$f_{PWM}$	Externally set PWM frequency	$R_{OSC} = 50 \text{ k}\Omega$		60		kHz
		$R_{OSC} = 200 \text{ k}\Omega$		20		
<b>LOGIC INPUT LEVELS (EN)</b>						
$V_{IL}$	Input low level			1.3		V
$V_{IH}$	Input high level		1.65			V
$R_{EN}$	Input pull-up resistance		350	500		$\text{k}\Omega$
<b>LOGIC OUTPUT LEVELS (STATUS)</b>						
$V_{OL}$	Output low level	Pull-down activated, $I_{STATUS} = 2$ mA		0.3		V
$I_{IL}$	Output leakage current	Pull-down deactivated, $V(\text{STATUS}) = 5$ V		1		$\mu\text{A}$
<b>UNDERVOLTAGE LOCKOUT</b>						
$V_{UVLO}$	Undervoltage lockout threshold			4.6		V
<b>THERMAL SHUTDOWN</b>						
$T_{TSD}$	Junction temperature shutdown threshold			160		$^\circ\text{C}$
$T_{TSU}$	Junction temperature startup threshold			140		$^\circ\text{C}$

(1) Logic HIGH between 4 V and 7 V. Note: absolute max voltage rating is 7 V.

(2) Either internal or external  $t_{KEEP}$  time setting is selected to be activated during manufacturing of production version of DRV120.

## FUNCTIONAL DESCRIPTION

DRV120 controls the current through the solenoid as shown in [Figure 3](#). Activation starts when EN pin voltage is pulled high either by an external driver or internal pull-up. In the beginning of activation, DRV120 allows the load current to ramp up to the peak value  $I_{PEAK}$  and it regulates it at the peak value for the time,  $t_{KEEP}$ , before reducing it to  $I_{HOLD}$ . The load current is regulated at the hold value as long as the EN pin is kept high. The initial current ramp-up time depends on the inductance and resistance of the solenoid. Once EN pin is driven to GND, DRV120 allows the solenoid current to decay to zero.



**Figure 3. Typical Current Waveform Through the Solenoid**

$t_{KEEP}$  is set externally by connecting a capacitor to the KEEP pin. A constant current is sourced from the KEEP pin that is driven into an external capacitor resulting in a linear voltage ramp. When the KEEP pin voltage reaches 75 mV, the current regulation reference voltage,  $V_{REF}$ , is switched from  $V_{PEAK}$  to  $V_{HOLD}$ . Dependency of  $t_{KEEP}$  from the external capacitor size can be calculated by:

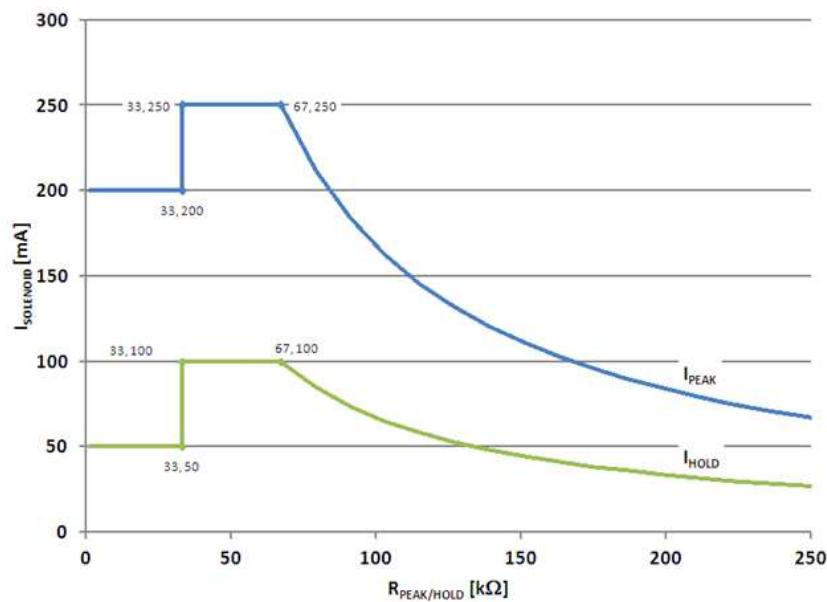
$$t_{KEEP} [s] = C_{KEEP} [F] \cdot 75 \cdot 10^3 \left[ \frac{s}{F} \right] \quad (1)$$

The current control loop regulates, cycle-by-cycle, the solenoid current by using an internal current sensing resistor and MOSFET switch. During the ON-cycle, current flows from OUT pin to GND pin through the internal switch as long as voltage over current sensing resistor is less than  $V_{REF}$ . As soon as the current sensing voltage is above  $V_{REF}$ , the internal switch is immediately turned off until the next ON-cycle is triggered by the internal PWM clock signal. In the beginning of each ON-cycle, the internal switch is turned on and stays on for at least the time determined by the minimum PWM signal duty cycle,  $D_{MIN}$ .

$I_{PEAK}$  and  $I_{HOLD}$  depend on fixed resistance values  $R_{PEAK}$  and  $R_{HOLD}$  as shown in [Figure 4](#). If the PEAK pin is connected to ground or if  $R_{PEAK}$  is below 33.33 k $\Omega$  (typ value), then  $I_{PEAK}$  is at its default value (internal setting). The  $I_{PEAK}$  value can alternatively be set by connecting an external resistor to ground from the PEAK pin. For example, if a 50-k $\Omega$  ( $= R_{PEAK}$ ) resistor is connected between PEAK and GND, then the externally set  $I_{PEAK}$  level will be 250 mA. If  $R_{PEAK} = 200$  k $\Omega$  is, then the externally set  $I_{PEAK}$  level will be 83 mA. HOLD current external setting,  $I_{HOLD}$ , works in the same way, but current levels are 40% of the  $I_{PEAK}$ . External settings for  $I_{PEAK}$  and  $I_{HOLD}$  are independent of each other.  $I_{PEAK}$  and  $I_{HOLD}$  values can be calculated by using the formula below.

$$I_{PEAK} = \frac{250mA}{R_{PEAK}} \cdot 66.67k\Omega; 66.67k\Omega < R_{PEAK} < 550k\Omega \quad (2)$$

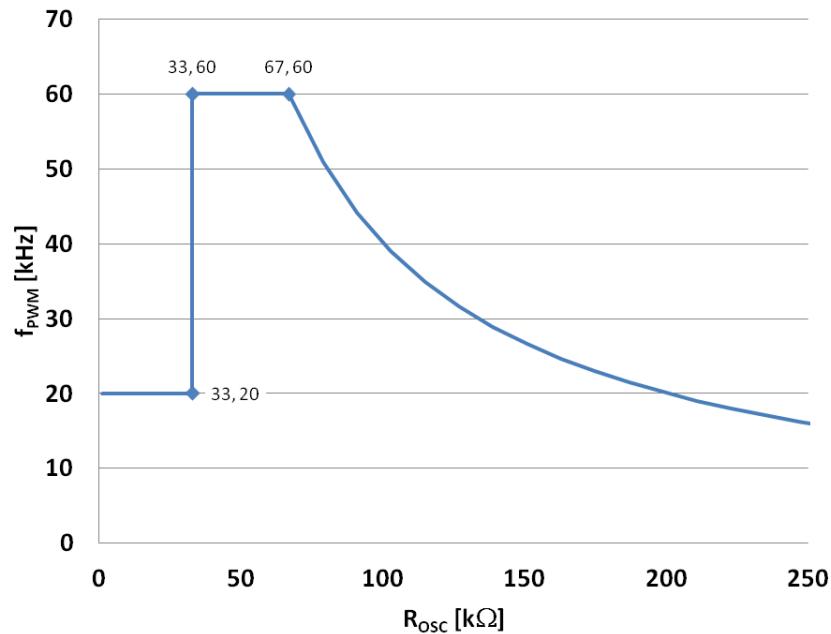
$$I_{HOLD} = \frac{100mA}{R_{HOLD}} \cdot 66.67k\Omega; 66.67k\Omega < R_{HOLD} < 250k\Omega \quad (3)$$



**Figure 4. PEAK and HOLD Mode Current Settings**

Frequency of the internal PWM clock signal,  $\text{PWM}_{\text{CLK}}$ , that triggers each ON-cycle can be adjusted by external resistor,  $R_{\text{OSC}}$ , connected between OSC and GND. Frequency as a function of resistor value is shown in [Figure 5](#). Default frequency is used when OSC is connected to GND directly. PWM frequency as a function of external fixed adjustment resistor value (greater than 66.67 k $\Omega$ ) is given below.

$$f_{\text{PWM}} = \frac{60\text{kHz}}{R_{\text{OSC}}} \cdot 66.67\text{k}\Omega; 66.67\text{k}\Omega < R_{\text{OSC}} < 2\text{M}\Omega \quad (4)$$



**Figure 5. PWM Clock Frequency Setting**

Open-drain STATUS output is deactivated if either under voltage lockout or thermal shutdown blocks have triggered.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV120APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	120A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
DRV120PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	120	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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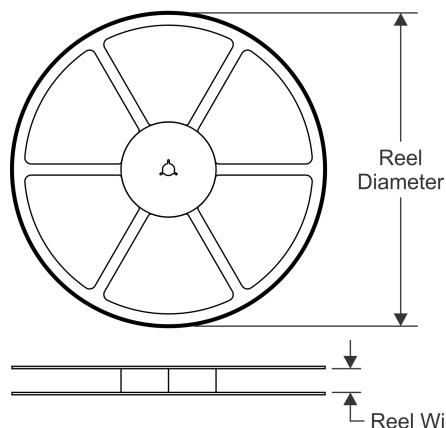
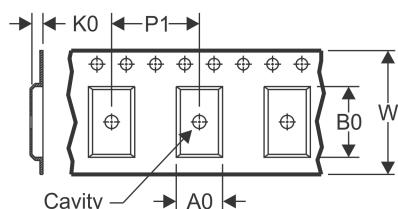
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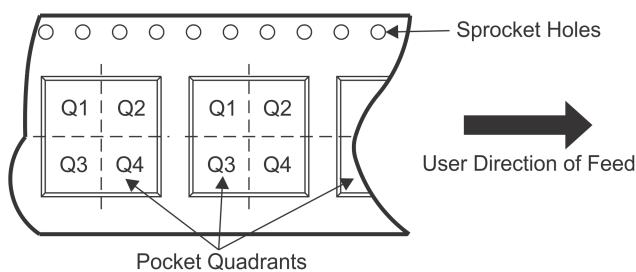
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## PACKAGE OPTION ADDENDUM

10-Dec-2020

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV120APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV120PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

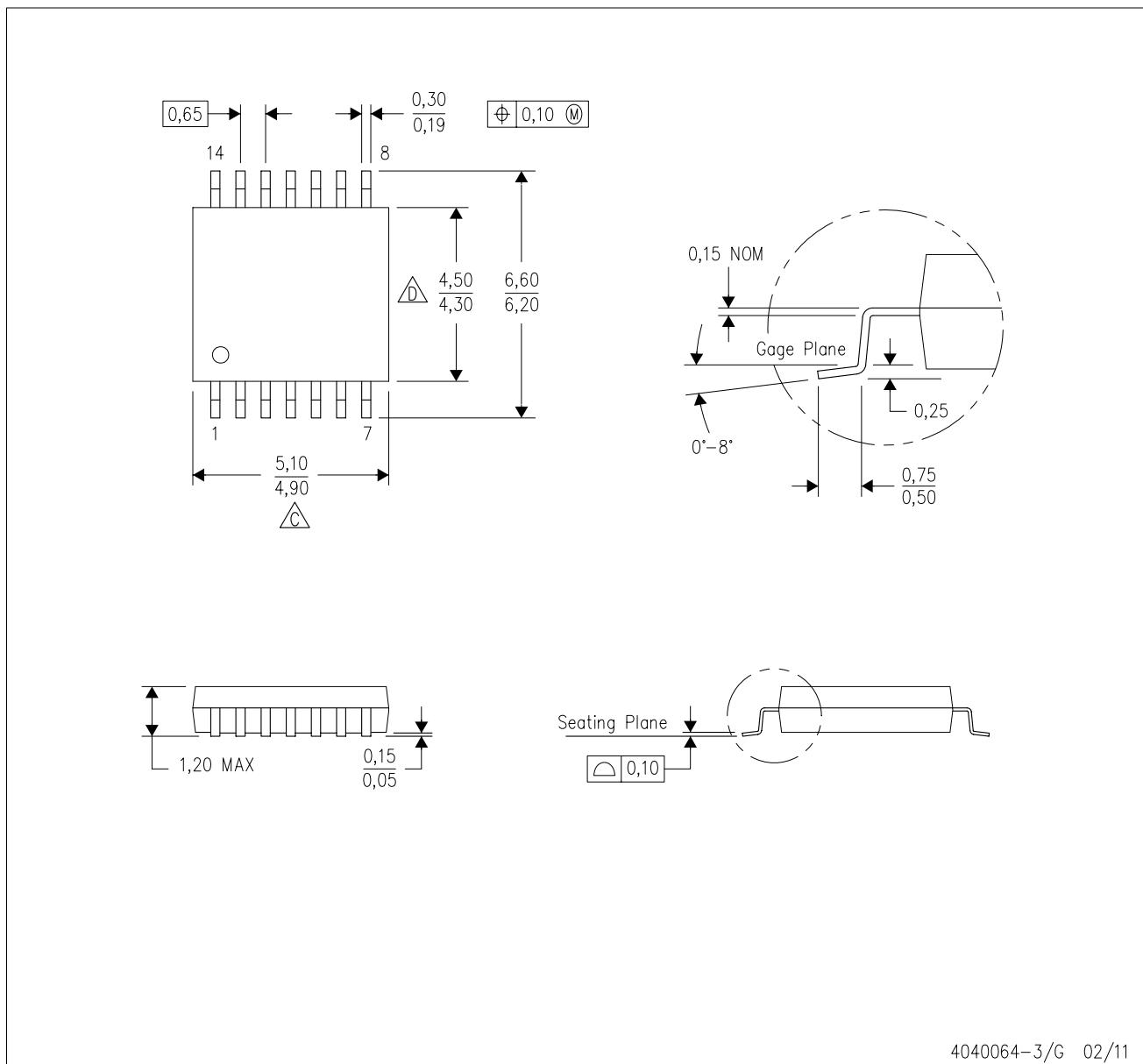
**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV120APWR	TSSOP	PW	14	2000	853.0	449.0	35.0
DRV120PWR	TSSOP	PW	8	2000	853.0	449.0	35.0

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

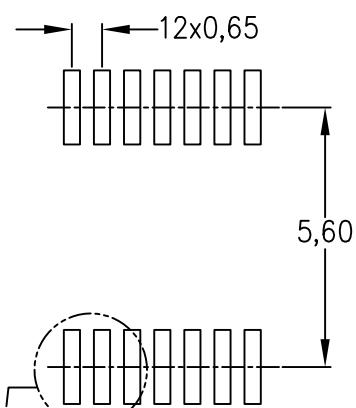
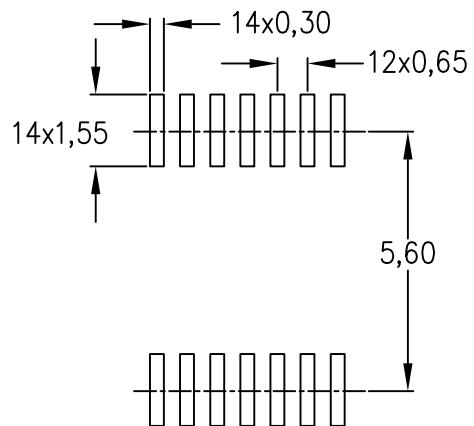
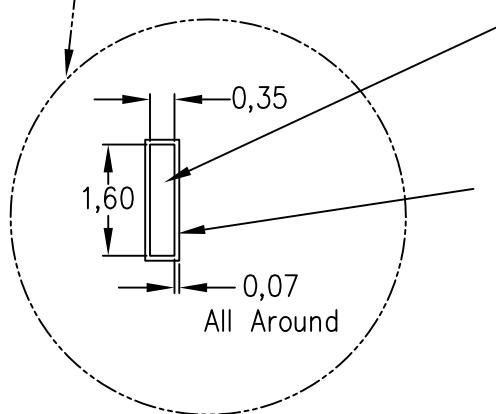
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

4211284-2/G 08/15

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

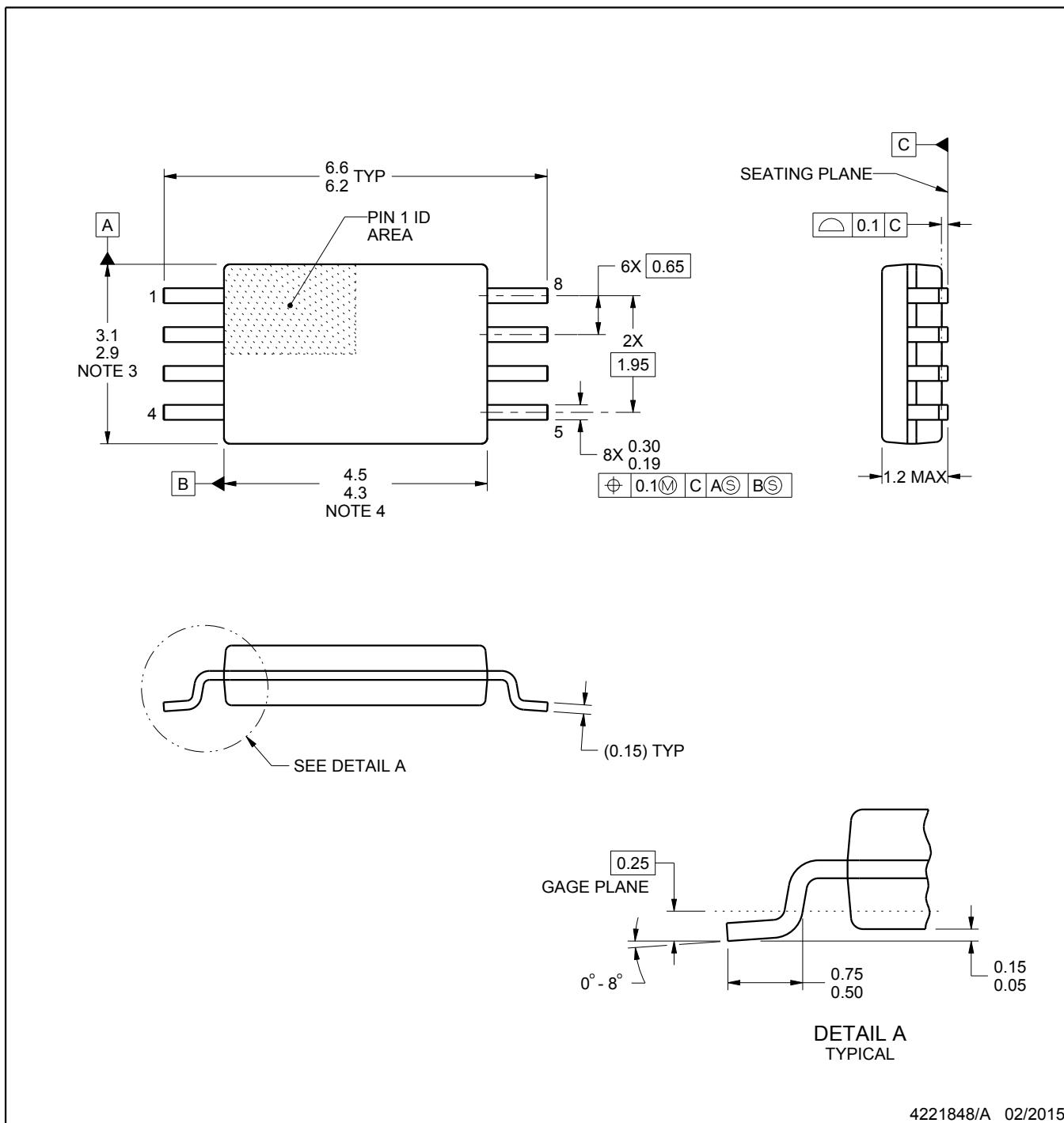
# PACKAGE OUTLINE

PW0008A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

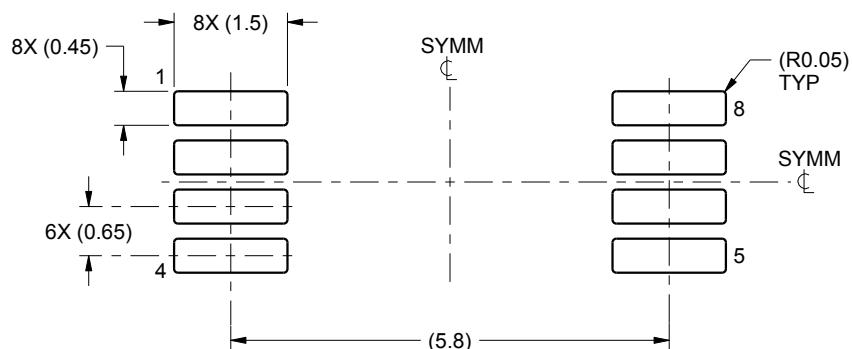
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

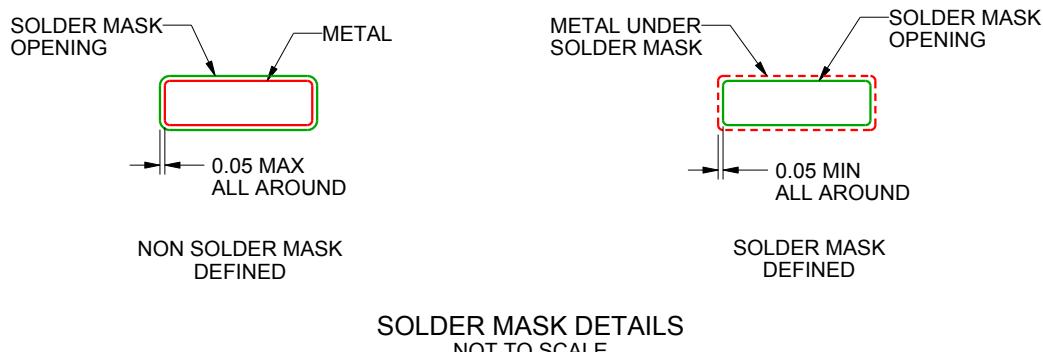
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



4221848/A 02/2015

NOTES: (continued)

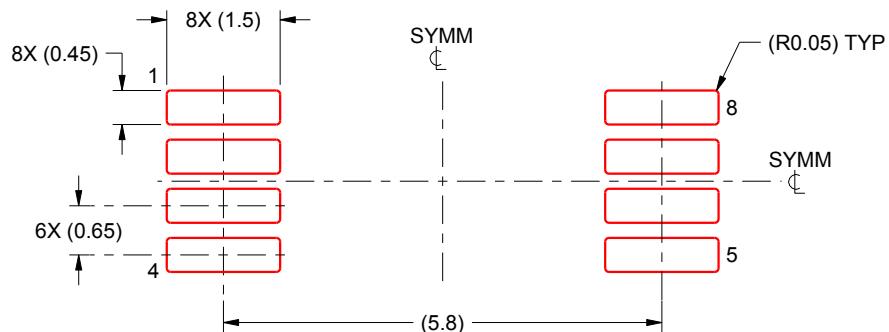
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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