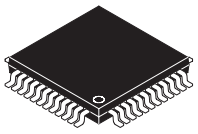
TEXAS INSTRUMENTS



SLAS352C − DECEMBER 2001 − REVISED AUGUST 2004

# 14-BIT, 400-MSPS DIGITAL-TO-ANALOG CONVERTER

## FEATURES

- **400-MSPS Update Rate**
- **LVDS-Compatible Input Interface**
- **Spurious Free Dynamic Range (SFDR) to Nyquist**
  - **69 dBc at 70-MHz IF, 400 MSPS**
- **W-CDMA Adjacent Channel Power Ratio ACPR**
  - **73 dBc at 30.72-MHz IF, 122.88 MSPS**
  - **71 dBc at 61.44-MHz IF, 245.76 MSPS**
- **Differential Scalable Current Outputs: 2 mA to 20 mA**
- **On-Chip 1.2-V Reference**
- **Single 3.3-V Supply Operation**
- **Power Dissipation: 820 at $f_{clk}$ = 400 MSPS, $f_{out}$ = 70 MHz**
- **Package: 48-Pin HTQFP PowerPad™, $T_{JA}$ = 28.8°C/W**

## APPLICATIONS

- **Cellular Base Transceiver Station Transmit Channel**
  - **CDMA: WCDMA, CDMA2000, IS−95**
  - **TDMA: GSM, IS−136, EDGE/GPRS**
  - **Supports Single-Carrier and Multicarrier Applications**
- **Test and Measurement: Arbitrary Waveform Generation**
- **Direct Digital Synthesis (DDS)**
- **Cable Modem Headend**

## DESCRIPTION

The DAC5675 is a 14-bit resolution high-speed digital-to-analog converter. The DAC5675 is designed for high-speed digital data transmission in wired and wireless communication systems, high-frequency direct-digital synthesis (DDS), and waveform reconstruction in test and measurement applications. The DAC5675 has excellent spurious free dynamic range (SFDR) at high intermediate frequencies, which makes the DAC5675 well suited for multicarrier transmission in TDMA and CDMA based cellular base transceiver stations BTS.

The DAC5675 operates from a single-supply voltage of 3.3 V. Power dissipation is 820 mW at $f_{clk}$ = 400 MSPS, $f_{out}$ = 70 MHz. The DAC5675 provides a nominal full-scale differential current output of 20 mA, supporting both single-ended and differential applications. The output current can be directly fed to the load with no additional external output buffer required. The output is referred to the analog supply voltage AVDD.

The DAC5675 is manufactured on Texas Instruments advanced high-speed mixed-signal BiCMOS process.

The DAC5675 comprises a LVDS (low-voltage differential signaling) interface. LVDS features a low differential voltage swing with a low constant power consumption across frequency, allowing for high speed data transmission with low noise levels, i.e., low electromagnetic interference (EMI). LVDS is typically implemented in low-voltage digital CMOS processes, making it the ideal technology for high-speed interfacing between the DAC5675 and high-speed low-voltage CMOS ASICs or FPGAs. The DAC5675 current-source-array architecture supports update rates of up to 400 MSPS. On-chip edge-triggered input latches provide for minimum setup and hold times thereby relaxing interface timing.



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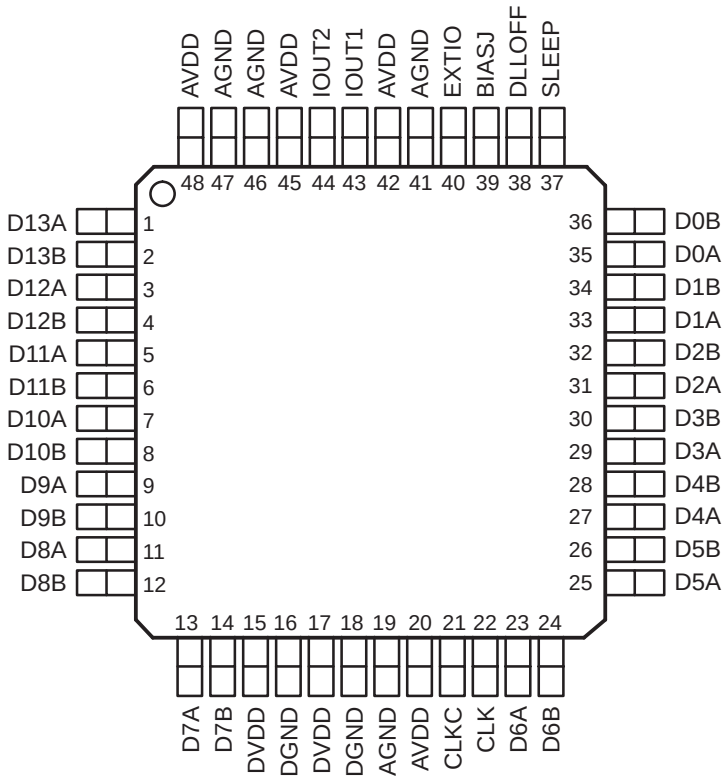
## DESCRIPTION (continued)

The DAC5675 has been specifically designed for a differential transformer coupled output with a 50-Ω doubly terminated load. With the 20-mA full-scale output current, both a 4:1 impedance ratio (resulting in an output power of 4 dBm) and 1:1 impedance ratio transformer (-2 dBm) is supported. The last configuration is preferred for optimum performance at high output frequencies and update rates. The output voltage compliance ranges from 2.15 V to AVDD + 0.03 V.

An accurate on-chip 1.2-V temperature compensated bandgap reference and control amplifier allows the user to adjust this output current from 20 mA down to 2 mA. This provides 20-dB gain range control capabilities. Alternatively, an external reference voltage may be applied. The DAC5675 features a SLEEP mode, which reduces the standby power to approximately 150 mW.

The DAC5675 is available in a 48-pin HTQFP thermally enhanced PowerPad package. This package increases thermal efficiency in a standard size IC package. The device is characterized for operation over the industrial temperature range of −40°C to 85°C.

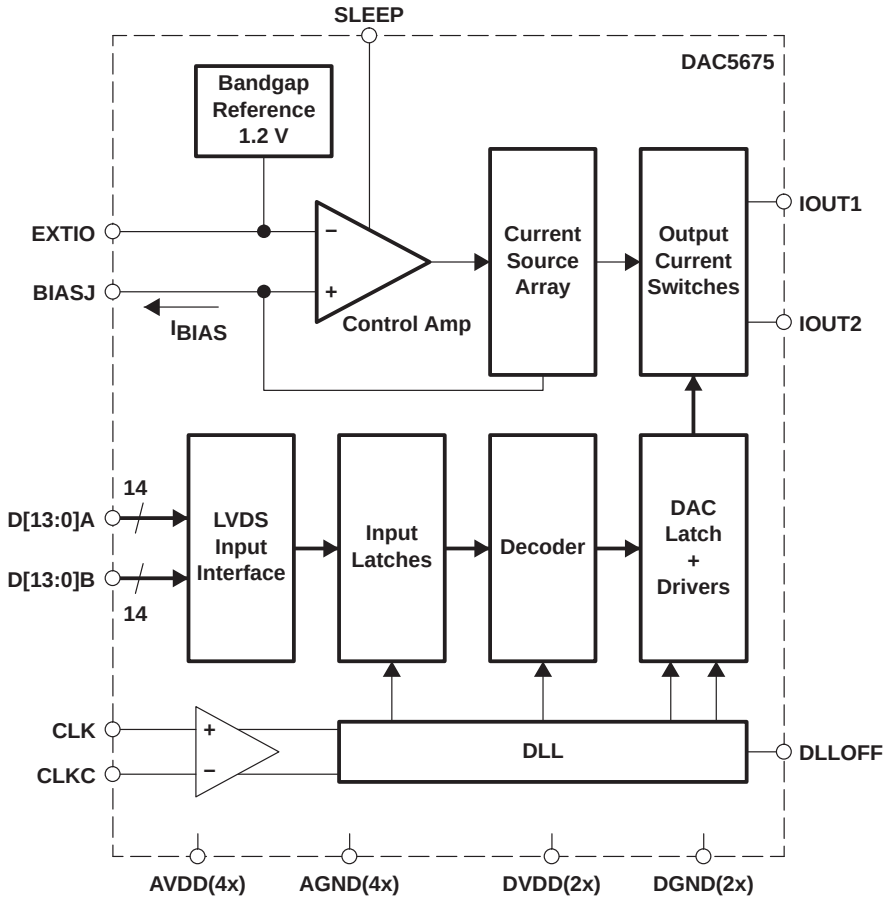
**PHP PACKAGE**
**(TOP VIEW)**




**AVAILABLE OPTIONS**

| $T_A$ | PACKAGED DEVICE |
|---|---|
| | 48-HTQFP PowerPAD PLASTIC QUAD FLATPACK |
| −40°C to 85°C | DAC5675IPHP |
| | DAC5675IPHPR |

## functional block diagram



## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AGND | 19, 41, 46, 47 | I | Analog negative supply voltage (ground) |
| AVDD | 20, 42, 45, 48 | I | Analog positive supply voltage |
| BIASJ | 39 | O | Full-scale output current bias |
| CLK | 22 | I | External clock input |
| CLKC | 21 | I | Complementary external clock input |
| D[13..0]A | 1, 3, 5, 7, 9, 11, 13, 23, 25, 27, 29, 31, 33, 35 | I | LVDS positive input, data bits 0 through 13<br>D13A is most significant data bit (MSB)<br>D0A is least significant data bit (MSB) |
| D[13..0]B | 2, 4, 6, 8, 10, 12, 14, 24, 26, 28, 30, 32, 34, 36 | I | LVDS negative input, data bits 0 through 13<br>D13B is most significant data bit (MSB)<br>D0B is least significant data bit (MSB) |
| DGND | 16, 18 | I | Digital negative supply voltage (ground) |
| DLLOFF | 38 | I | High DLL off / Low = DLL on |
| DVDD | 15, 17 | I | Digital positive supply voltage |
| EXTIO | 40 | I/O | Internal reference output or external reference input. Requires a 0.1-μF decoupling capacitor to AGND when used as reference output. |
| IOUT1 | 43 | O | DAC current output. Full scale when all input bits are set 1. Connect reference side of DAC load resistors to AVDD |
| IOUT2 | 44 | O | DAC complementary current output. Full scale when all input bits are 0. Connect reference side of DAC load resistors to AVDD |
| SLEEP | 37 | I | Asynchronous hardware power down input. Active high. No pull down or pull up.<br>Must be asserted high or low. |

## detailed description

Figure 1 shows a simplified block diagram of the current steering DAC5675. The DAC5675 consists of a segmented array of non-transistor current sources, capable of delivering a full-scale output current up to 20 mA. Differential current switches direct the current of each current source to either one of the complementary output nodes IOUT1 or IOUT2. The complementary current output thus enables differential operation, canceling out common mode noise sources (digital feed-through, on-chip and PCB noise), dc offsets, even order distortion components, thereby doubling signal output power.

The full-scale output current is set using an external resistor ($R_{BIAS}$) in combination with an on-chip bandgap voltage reference source (1.2 V) and control amplifier. The current ($I_{BIAS}$) through resistor $R_{BIAS}$ is mirrored internally to provide a full-scale output current equal to 16 times $I_{BIAS}$. The full-scale current is adjustable from 20 mA down to 2 mA by using the appropriate bias resistor value.

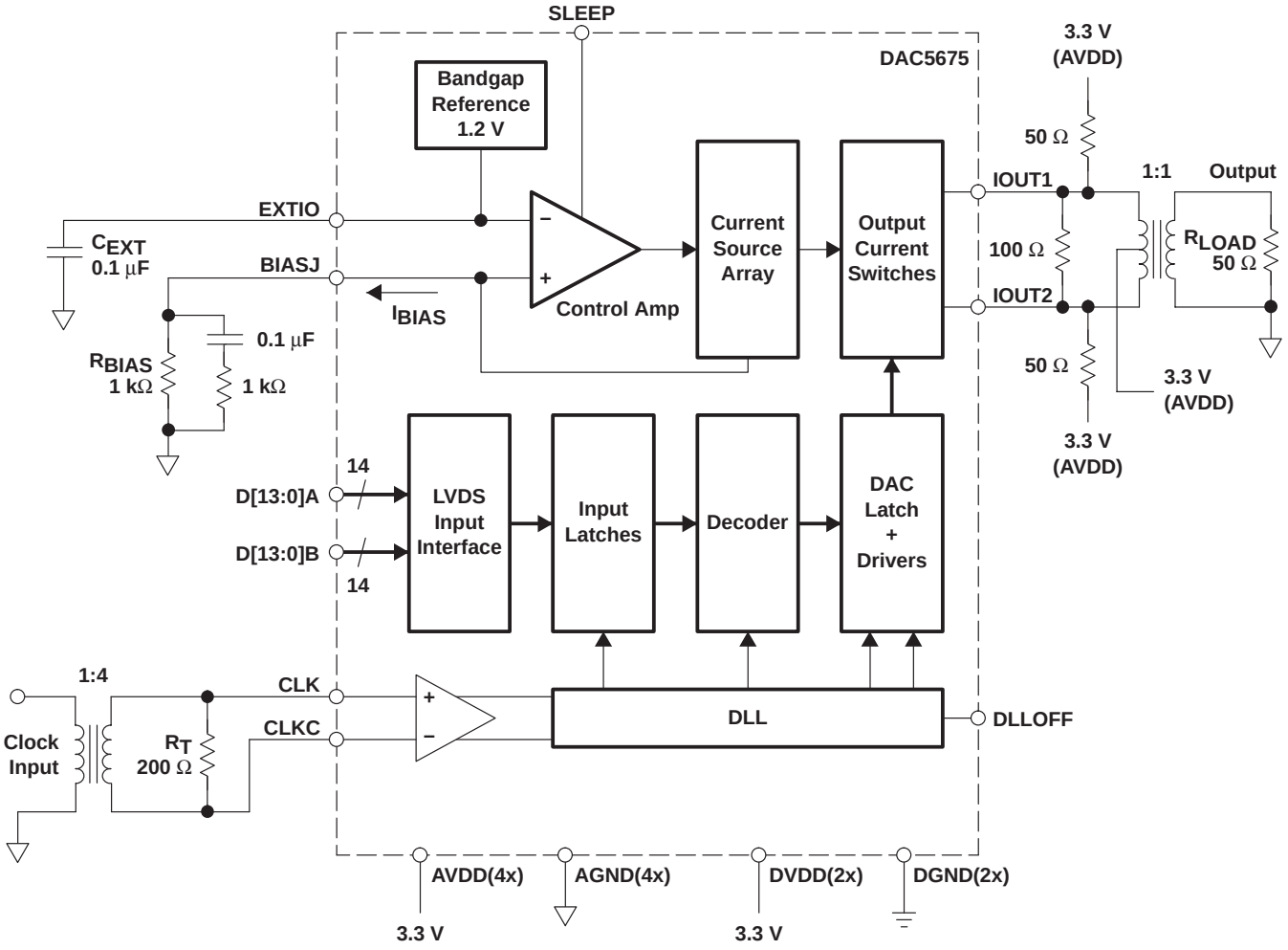



**Figure 1. Application Schematic**

## detailed description (continued)

### digital inputs

The DAC5675 comprises a low voltage differential signaling (LVDS) bus input interface. The LVDS features a low differential voltage swing with low constant power consumption (~4 mA per complementary data input) across frequency. The differential characteristic of LVDS allows for high-speed data transmission with low electromagnetic interference (EMI) levels. The LVDS input minimum and maximum input threshold table lists the LVDS input levels. Figure 2 shows the equivalent complementary digital input interface for the DAC5675, valid for pins D[13..0]A and D[13..0]B. Note that the LVDS interface features internal 110-Ω resistors for proper termination. Figure 3 shows the LVDS input timing measurement circuit and waveforms. A common mode level of 1.2 V and a differential input swing of 0.8 V is applied to the inputs.

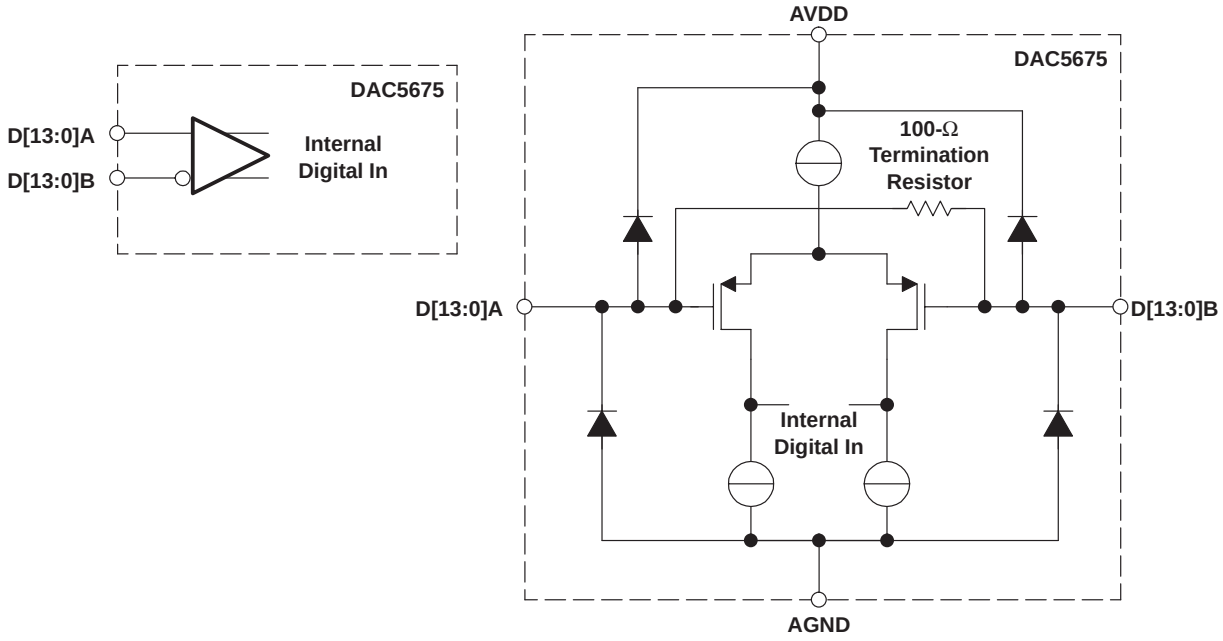



**Figure 2. LVDS Digital Equivalent Input**

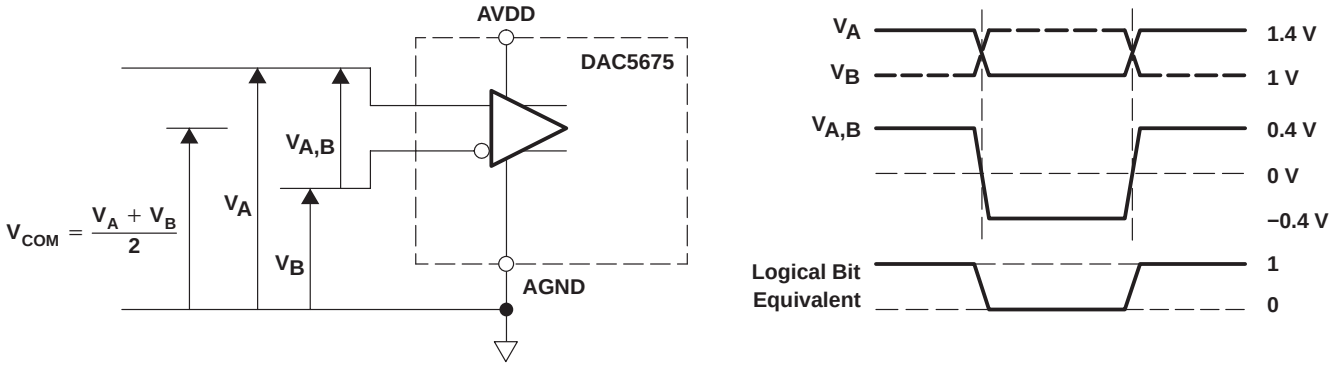



**Figure 3. LVDS Timing Test Circuit and Input Test Levels**

**digital inputs (continued)**

Figure 4 shows a schematic of the equivalent CMOS/TTL-compatible digital inputs of the DAC5675, valid for pins SLEEP and DLLOFF.

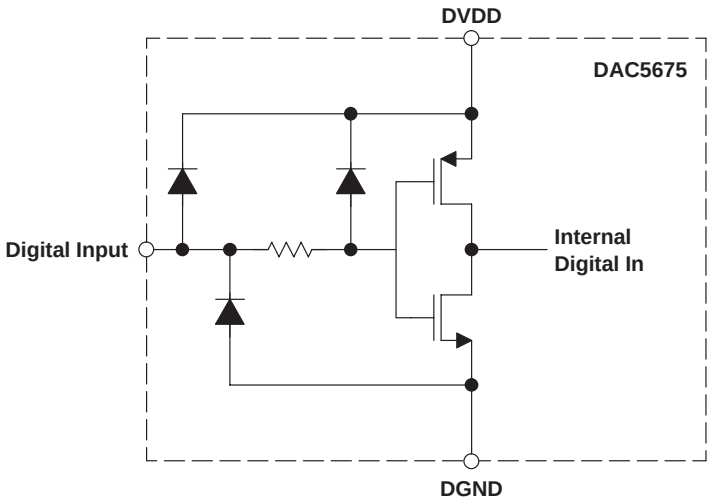



**Figure 4. CMOS/TTL Digital Equivalent Input**

**clock input and timing**

The DAC5675 comprises a delay locked loop DLL for internal clock alignment. Enabling the DLL is controlled by pin DLLOFF. The DLL should be enabled for update rates in excess of 100 MSPS. The DLL works only to maximize setup and hold times of the digital input and does not affect the analog output of the DAC. Figure 5 shows the clock and data input timing diagram. The DAC5675 features a differential clock input. Internal edge-triggered flip-flops latch the input word on the rising edge of the positive clock input CLK (falling edge of the negative/complementary clock input CLKC). The DAC core is updated with the data word on the following rising edge of the positive clock input CLK (falling edge of CLKC). This results in a conversion latency of one clock cycle. The DAC5675 provides for minimum setup and hold times (>0.25 ns), allowing for noncritical external interface timing. The clock duty cycle can be chosen arbitrarily under the timing constraints listed in the *electrical characteristics* section. However, a 50% duty cycle gives the optimum dynamic performance.

The DAC5675 clock input can be driven by a differential sine wave. The ac coupling, in combination with internal biasing ensures that the sine wave input is centered at the optimum common-mode voltage that is required for the internal clock buffer. The DAC5675 clock input can also be driven single-ended, this is shown in Figure 6. The best SFDR performance is typically achieved by driving the inputs differentially.

**clock input and timing (continued)**

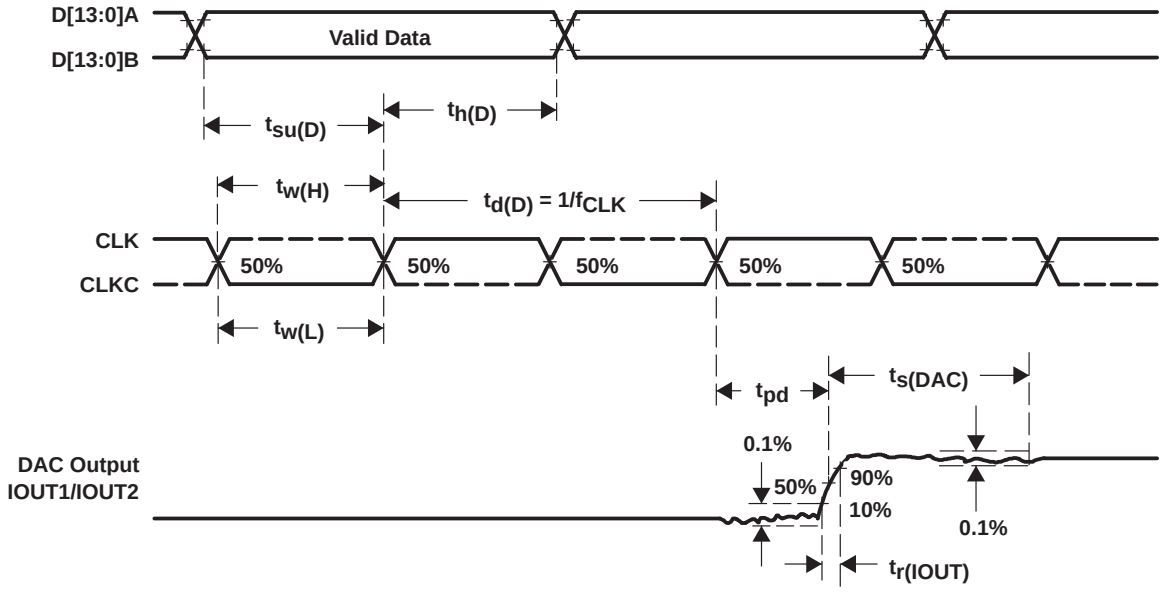



**Figure 5. Timing Diagram**

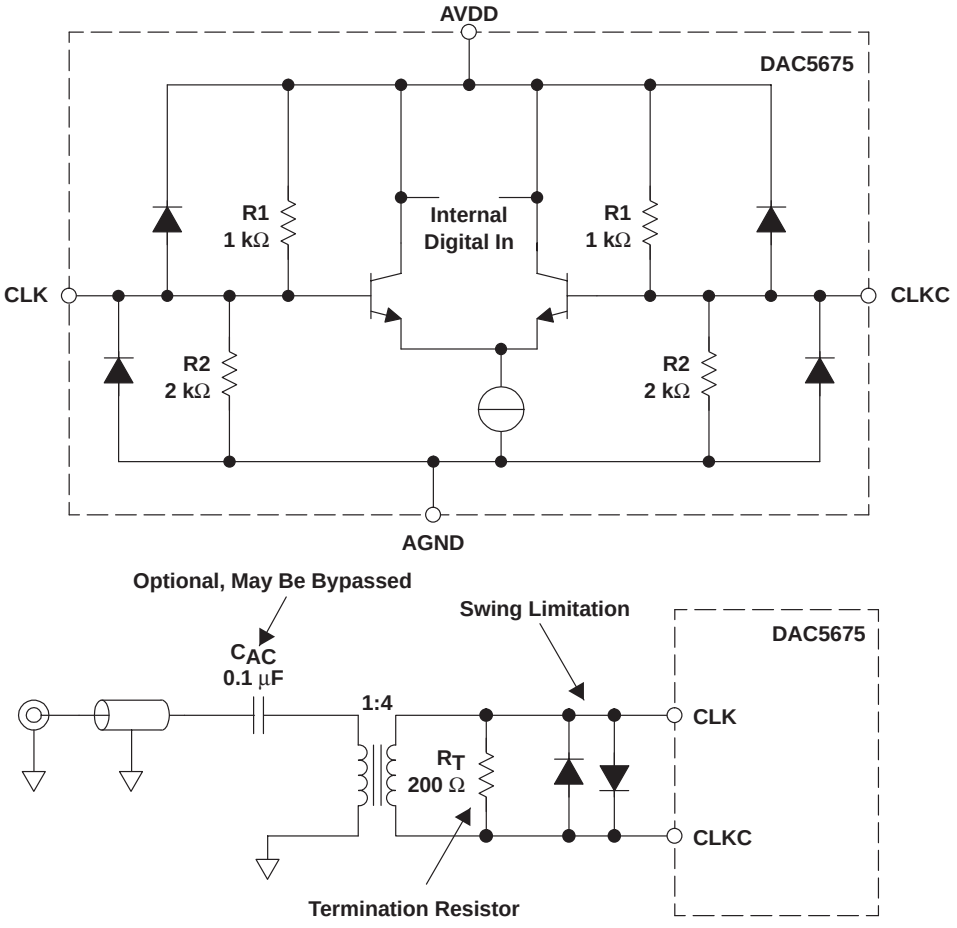



**Figure 6. Clock Equivalent Input**

**clock input and timing (continued)**

Figure 7 shows the equivalent schematic of the differential clock input buffer. The input nodes are internally self-biased enabling ac coupling of the clock inputs. Figure 8 shows the preferred configuration for driving the DAC5675.

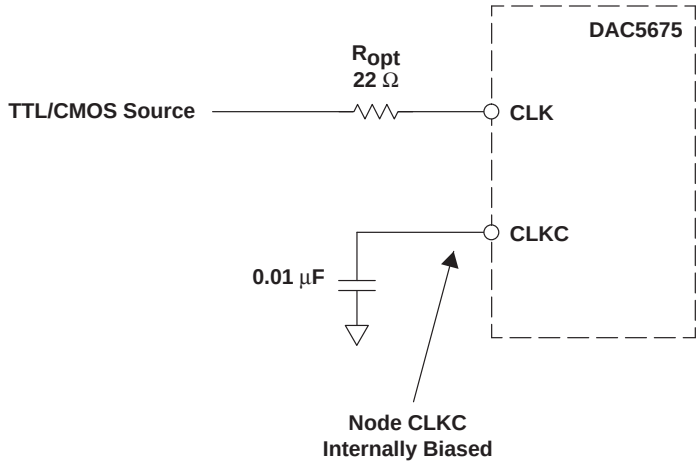



**Figure 7. Driving the DAC5675 With a Single-Ended TTL/CMOS Clock Source**

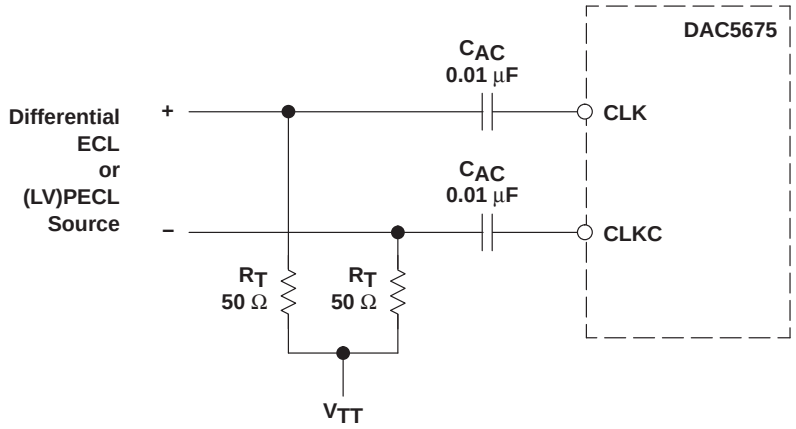



**Figure 8. Driving the DAC5675 With a Differential ECL/PECL Clock Source**

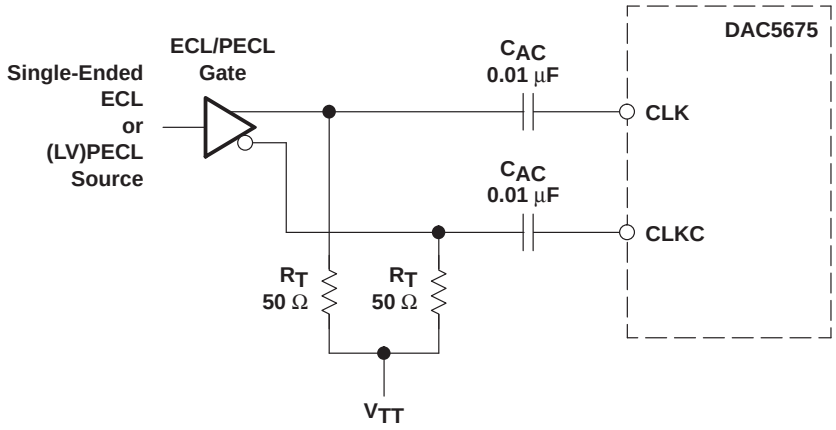



**Figure 9. Driving the DAC5675 With a Single-Ended ECL/PECL Clock Source**

## detailed description (continued)

### supply inputs

The DAC5675 comprises separate analog and digital supplies, i.e., $AV_{DD}$ and $DV_{DD}$ respectively. These supply inputs can be set independently from 3.6 V down to 3.15 V.

### DAC transfer function

The DAC5675 delivers complementary output currents IOUT1 and IOUT2. The DAC supports straight binary coding, with D13 being the MSB and D0 the LSB (For ease of notation we denote D13..D10 as the logical bit equivalent of the complementary LVDS inputs D[13..0]A and D[13..0]B). Output current IOUT1 equals the approximate full-scale output current when all input bits are set high, i.e., the binary input word has the decimal representation 16383. Full-scale output current flows through terminal IOUT2 when all input bits are set low (mode 0, straight binary input). The relation between IOUT1 and IOUT2 can thus be expressed as:

$$IOUT1 = IO_{(FS)} - IOUT2$$

where $IO_{(FS)}$ is the full-scale output current. The output currents can be expressed as:

$$IOUT1 = \frac{I_{O(FS)} \times CODE}{16384}$$

$$IOUT2 = \frac{I_{O(FS)} \times (16383 - CODE)}{16384}$$

where CODE is the decimal representation of the DAC data input word. Output currents IOUT1 and IOUT2 drive a load $R_L$. $R_L$ is the combined impedance for the termination resistance and/or transformer load resistance, $R_{LOAD}$ (see Figures 11 and 12). This would translate into single-ended voltages VOUT1 and VOUT2 at terminal IOUT1 and IOUT2, respectively, of:

$$VOUT1 = IOUT1 \times R_L = \frac{CODE \times I_{O(FS)} \times R_L}{16384}$$

$$VOUT2 = IOUT2 \times R_L = \frac{(16383 - CODE) \times I_{O(FS)} \times R_L}{16384}$$

The differential output voltage $VOUT_{(DIFF)}$ can thus be expressed as:

$$VOUT_{(DIFF)} = VOUT1 - VOUT2 = \frac{(2CODE - 16383) \times I_{O(FS)} \times R_L}{16384}$$

The latter equation shows that applying the differential output results in doubling of the signal power delivered to the load. Since the output currents IOUT1 and IOUT2 are complementary, they become additive when processed differentially. Note that care should be taken not to exceed the compliance voltages at node IOUT1 and IOUT2, which leads to increased signal distortion.

## detailed description (continued)

### reference operation

The DAC5675 comprises a bandgap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor $R_{BIAS}$. The bias current $I_{BIAS}$ through resistor $R_{BIAS}$ is defined by the on-chip bandgap reference voltage and control amplifier. The full-scale output current equals 16 times this bias current. The full-scale output current $IO_{(FS)}$ is thus expressed as:

$$I_{O(FS)} = 16 \times I_{BIAS} = \frac{16 \times V_{EXTIO}}{R_{BIAS}}$$

where $V_{EXTIO}$ is the voltage at terminal EXTIO. The bandgap reference voltage delivers an accurate voltage of 1.2 V. This reference can be override by applying a external voltage to terminal EXTIO. The bandgap reference can additionally be used for external reference operation. In that case, an external buffer with high impedance input should be applied in order to limit the bandgap load current to a maximum of 100 nA. The capacitor $C_{EXT}$ may be omitted. Terminal EXTIO serves as either a input or output node. The full-scale output current is adjustable from 20 mA down to 2 mA by varying resistor $R_{BIAS}$.

### analog current outputs

Figure 10 shows a simplified schematic of the current source array output with corresponding switches. Differential non switches direct the current of each individual PMOS current source to either the positive output node IOUT1 or its complementary negative output node IOUT2. The output impedance is determined by the stack of the current sources and differential switches, and is >300 kΩ in parallel with an output capacitance of 5 pF.

The external output resistors are referred to the positive supply AVDD.

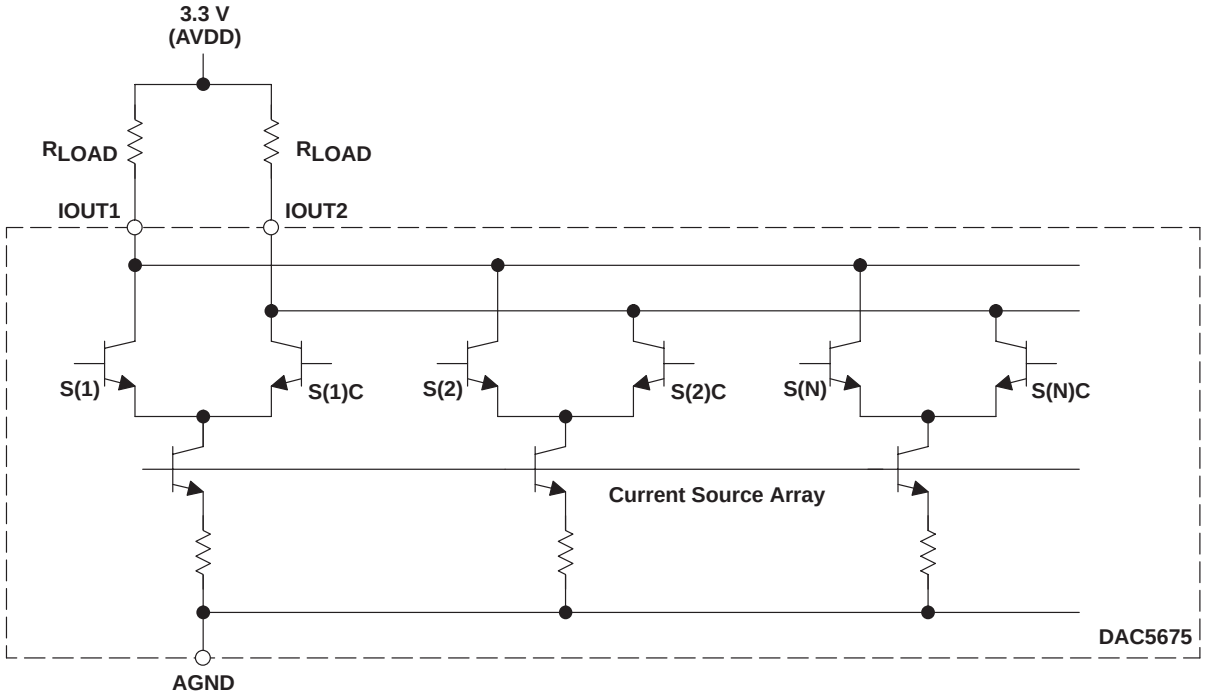



**Figure 10. Equivalent Analog Current Output**

**analog current outputs (continued)**

The DAC5675 can easily be configured to drive a doubly terminated 50-Ω cable using a properly selected transformer. Figure 11 and Figure 12 show the 1:1 and 4:1 impedance ratio configuration. These configurations provide maximum rejection of common-mode noise sources and even order distortion components, thereby doubling the DAC's power to the output. The center tap on the primary side of the transformer is terminated to AVDD, enabling a dc current flow for both IOUT1 and IOUT2. Note that the ac performance of the DAC5675 is optimum and specified using a 1:1 differential transformer coupled output.

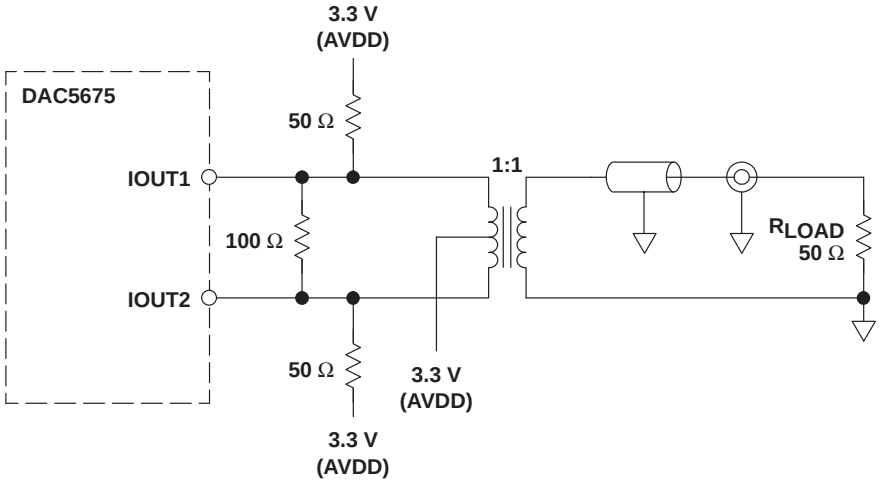



**Figure 11. Driving a Doubly Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer**

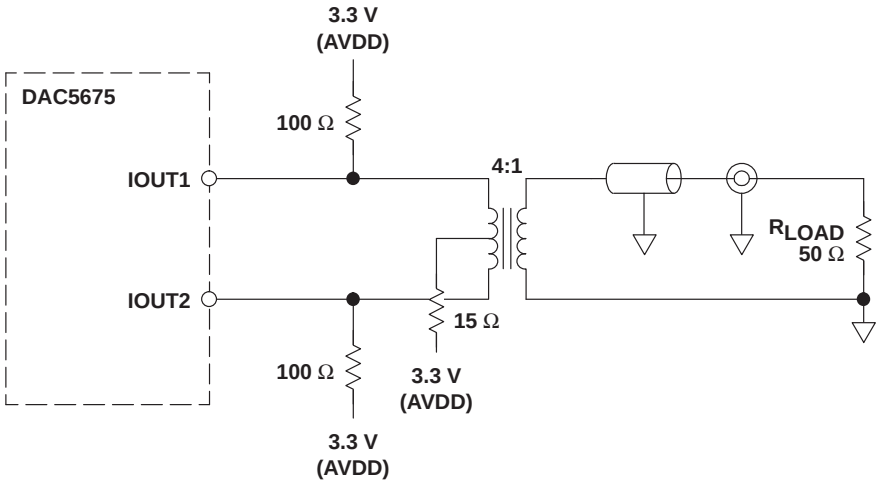
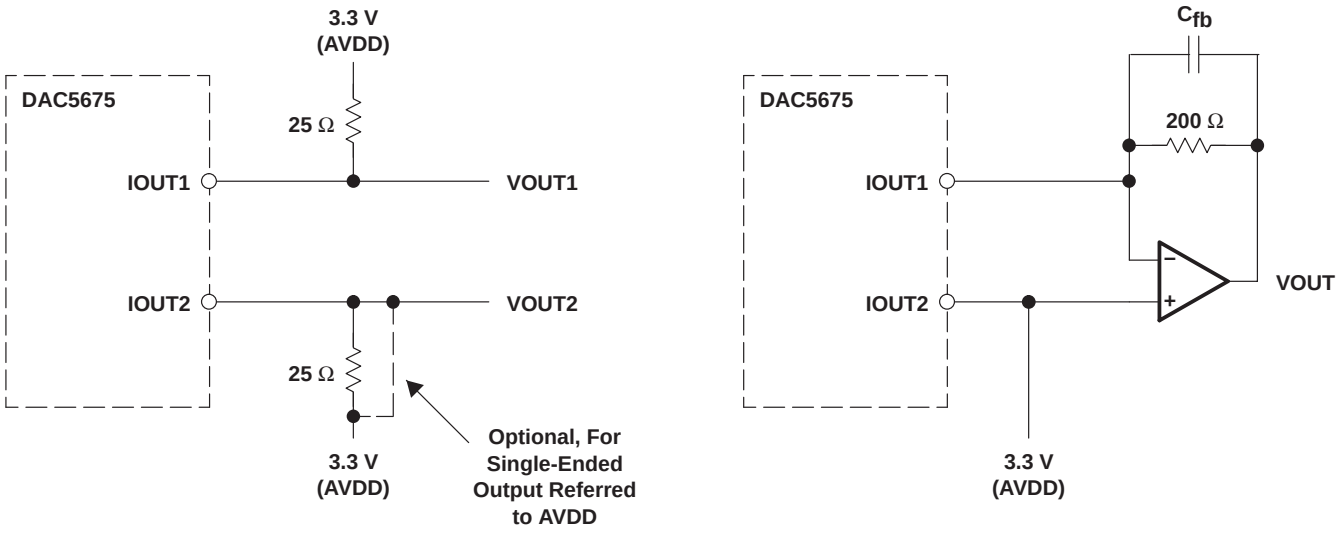



**Figure 12. Driving a Doubly Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer**

### analog current outputs (continued)

Figure 13(a) shows the typical differential output configuration with two external matched resistor loads. The nominal resistor load of 25 Ω gives a differential output swing of 1 $V_{PP}$ (0.5-$V_{PP}$ single-ended) when applying a 20-mA full-scale output current. The output impedance of the DAC5675 slightly depends on the output voltage at nodes IOUT1 and IOUT2. Consequently, for optimum dc-integral nonlinearity, the configuration of Figure 13(b) should be chosen. In this current/voltage (I-V) configuration, terminal IOUT1 is kept at AVDD by the inverting operational amplifier. The complementary output should be connected to AVDD to provide a dc-current path for the current sources switched to IOUT1. The amplifier's maximum output swing and the DACs full-scale output current determine the value of the feedback resistor ($R_{FB}$). The capacitor ($C_{FB}$) filters the steep edges of the DAC5675 current output, thereby reducing the operational amplifier's slew-rate requirements. In this configuration, the op amp should operate at a supply voltage higher than the resistors output reference voltage AVDD due to its positive and negative output swing around AVDD. Node IOUT1 should be selected if a single-ended unipolar output is desired.




**(a) Unbuffered Differential and Single-Ended Resistor and Buffered**

**(b) Buffered Single-Ended Output Configuration**

**Figure 13. Output Configurations**

### sleep mode

The DAC5675 features a power-down mode that turns off the output current and reduces the supply current to approximately 45 mA. The power-down mode is activated by applying a logic level 1 to the SLEEP pin (e.g., by connecting the SLEEP pin to the AVDD pin). The SLEEP pin must be connected. Power-up and power-down activation times depend on the value of the external capacitor at node SLEEP. For a nominal capacitor value of 0.1-μF, powerdown takes less than 5 μs and approximately 3 ms to power back up.

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range: $AV_{DD}$‡ . . . . . −0.3 V to 3.6 V
$DV_{DD}$§ . . . . . −0.3 V to 3.6 V
$AV_{DD}$ to $DV_{DD}$ . . . . . −3.6 V to 3.6 V
Voltage between AGND and DGND . . . . . −0.3 V to 0.5 V
CLK, CLKC, SLEEP§ . . . . . −0.3 V to DVDD + 0.3 V
Digital input D[13..0]A, D[13..0]B§ . . . . . −0.3 V to DVDD + 0.3 V
IOUT1, IOUT2‡ . . . . . −1.0 V to AVDD + 0.3 V
EXTIO, BIASJ‡ . . . . . −0.3 V to AVDD + 0.3 V
Peak input current (any input) . . . . . 20 mA
Peak total input current (all inputs) . . . . . −30 mA
Operating free-air temperature range, $T_A$ (DAC5675I) . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Measured with respect to AGND
§ Measured with respect to DGND

## recommended operating conditions

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Output update rate | DLL disabled, DLLOFF = 1 | | | 100 | MSPS |
| | DLL enabled, DLLOFF = 0(1) | 100 | | 400 | |
| Analog supply voltage, $AV_{DD}$ | | 3.15 | 3.3 | 3.6 | V |
| Digital supply voltage, $DV_{DD}$ | | 3.15 | 3.3 | 3.6 | V |
| Input reference voltage, $V_{(EXTIO)}$ | | 0.6 | 1.2 | 1.25 | V |
| Full-scale output current, $I_{O(FS)}$ | | 2 | | 20 | mA |
| Output compliance range | AVDD = 3.15 to 3.45 V, $I_{O(FS)}$ = 20 mA | $AV_{DD}$−1 | | $AV_{DD}$+0.3 | V |
| Clock differential Input voltage, \|CLK−CLKC\| | | 0.4 | | 0.8 | V |
| Clock pulse width high, $t_{w(H)}$ | | | 1.25 | | ns |
| Clock pulse width low, $t_{w(L)}$ | | | 1.25 | | ns |
| Clock duty cycle | | 40% | | 60% | |
| Operating free-air temperature, $T_A$ | | −40 | | 85 | °C |

NOTE: 1. If changes to the main clock frequency or phase are initiated during operation, the DLL circuitry on the DAC5675 has a tendency to lose lock on the clock signal. When this situation occurs, the output data from the DAC5675 may be corrupted.

## electrical characteristics over recommended operating free-air temperature range, $AV_{DD}$ = 3.3 V, $DV_{DD}$ = 3.3 V, $I_{O(FS)}$ = 20 mA (unless otherwise noted)

### dc specifications

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Resolution** | | | 14 | | | Bit |
| **DC Accuracy (see Note 1)** | | | | | | |
| INL | Integral nonlinearity | $T_{MIN}$ to $T_{MAX}$ | −4 | ±2 | 4 | LSB |
| DNL | Differential nonlinearity | | −2 | ±1.5 | 2 | |
| **Monotonicity** | | | Monotonic 12-b level | | | |
| **Analog Output** | | | | | | |
| | Offset error | | | 0.02 | | %FSR |
| | Gain error | Without internal reference | −10 | | 10 | %FSR |
| | | With internal reference | −10 | | 10 | |
| | Output resistance | | | 300 | | kΩ |
| | Output capacitance | | | 5 | | pF |
| **Reference Output** | | | | | | |
| $V_{(EXTIO)}$ | Reference voltage | | 1.17 | 1.23 | 1.29 | V |
| | Reference output current (see Note 2) | | | 100 | | nA |
| **Reference Input** | | | | | | |
| | Input resistance | | | 1 | | MΩ |
| | Small signal bandwidth | | | 1.4 | | MHz |
| | Input capacitance | | | 100 | | pF |
| **Temperature Coefficients** | | | | | | |
| | Offset drift | | | 0 | | ppm of FSR/°C |
| | Gain drift | Without internal reference | | ±50 | | ppm of FSR/°C |
| | | With internal reference | | ±100 | | |
| $\Delta V_{(EXTIO)}$ | Reference voltage drift | | | ±50 | | ppm/°C |
| **Power Supply** | | | | | | |
| $I_{(AVDD)}$ | Analog supply current (see Note 3) | | | 175 | | mA |
| $I_{(DVDD)}$ | Digital supply current (see Note 3) | | | 100 | | mA |
| $I_{(AVDD)}$ | Sleep mode supply current | Sleep mode | | 45 | | mA |
| $P_D$ | Power dissipation (see Note 4) | $AV_{DD}$ = 3.3 V, $DV_{DD}$ = 3.3 V | | 820 | 900 | mW |
| APSRR | Analog and digital power supply rejection ratio | $AV_{DD}$ = 3.15 V to 3.45 V | −0.5 | | 0.5 | %FSR/V |
| DPSSR | | | −0.5 | | 0.5 | |

NOTES: 1. Measured differential at IOUT1 and IOUT2. 2.5 Ω to AVDD
2. Use an external buffer amplifier with high impedance input to drive any external load.
3. Measured at $f_{CLK}$ = 400 MSPS and $f_{OUT}$ = 70 MHz
4. Measured for 50-Ω $R_L$ at IOUT1 and IOUT2, $f_{CLK}$ = 400 MSPS and $f_{OUT}$ = 70 MHz.

## electrical characteristics over recommended operating free-air temperature range, $AV_{DD}$ = 3.3 V, $DV_{DD}$ = 3.3 V, $I_{O(FS)}$ = 20 mA, differential transformer coupled output, 50-Ω doubly terminated load (unless otherwise noted)

### ac specifications

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Analog Output** | | | | | | |
| $t_{s(DAC)}$ | Output settling time to 0.1% | Transition: code x2000 to x23FF | | 12 | | ns |
| $t_{pd}$ | Output propagation delay | | | 1 | | ns |
| $t_{r(IOUT)}$ | Output rise time 10% to 90% | | | 2 | | ns |
| $t_{f(IOUT)}$ | Output fall time 90% to 10% | | | 2 | | ns |
| | Output noise | $IOUT_{FS}$ = 20 mA | | 55 | | pA/√Hz |
| | | $IOUT_{FS}$ = 2 mA | | 30 | | pA/√Hz |
| **AC Linearity** | | | | | | |
| THD | Total harmonic distortion | $f_{CLK}$ = 100 MSPS, $f_{OUT}$ = 20 MHz, $T_A$ = 25°C | | 72 | | dBc |
| | | $f_{CLK}$ = 160 MSPS, $f_{OUT}$ = 41 MHz, $T_A$ = 25°C | | 67 | | |
| | | $f_{CLK}$ = 200 MSPS, $f_{OUT}$ = 70 MHz, $T_A$ = 25°C | | 63 | | |
| | | $f_{CLK}$ = 400 MSPS, $f_{OUT}$ = 20 MHz, $T_{MIN}$ to $T_{MAX}$ | | 72 | | |
| | | $f_{CLK}$ = 400 MSPS, $f_{OUT}$ = 70 MHz, $T_A$ = 25°C | | 64 | | |
| | | $f_{CLK}$ = 400 MSPS, $f_{OUT}$ = 140 MHz, $T_A$ = 25°C | | 58 | | |
| SFDR | Spurious free dynamic range to Nyquist | $f_{CLK}$ = 100 MSPS, $f_{OUT}$ = 20 MHz, $T_A$ = 25°C | | 77 | | dBc |
| | | $f_{CLK}$ = 160 MSPS, $f_{OUT}$ = 41 MHz, $T_A$ = 25°C | | 70 | | |
| | | $f_{CLK}$ = 200 MSPS, $f_{OUT}$ = 70 MHz, $T_A$ = 25°C | | 70 | | |
| | | $f_{CLK}$ = 400 MSPS, $f_{OUT}$ = 20 MHz, $T_{MIN}$ to $T_{MAX}$ | | 73 | | |
| | | $f_{CLK}$ = 400 MSPS, $f_{OUT}$ = 70 MHz, $T_A$ = 25°C | | 69 | | |
| | | $f_{CLK}$ = 400 MSPS, $f_{OUT}$ = 140 MHz, $T_A$ = 25°C | | 58 | | |
| SFDR | Spurious free dynamic range within a window, 5-MHz span | $f_{CLK}$ = 100 MSPS, $f_{OUT}$ = 20 MHz, $T_A$ = 25°C | | 88 | | dBc |
| | | $f_{CLK}$ = 160 MSPS, $f_{OUT}$ = 41 MHz, $T_A$ = 25°C | | 83 | | |
| | | $f_{CLK}$ = 200 MSPS, $f_{OUT}$ = 70 MHz, $T_A$ = 25°C | | 80 | | |
| | | $f_{CLK}$ = 400 MSPS, $f_{OUT}$ = 20 MHz, $T_{MIN}$ to $T_{MAX}$ | | 88 | | |
| | | $f_{CLK}$ = 400 MSPS, $f_{OUT}$ = 70 MHz, $T_A$ = 25°C | | 80 | | |
| | | $f_{CLK}$ = 400 MSPS, $f_{OUT}$ = 140 MHz, $T_A$ = 25°C | | 73 | | |
| ACPR | Adjacent channel power ratio WCDMA with 3.84 MHz BW, 5-MHz channel spacing† | $f_{CLK}$ = 122.88 MSPS, IF = 30.72 MHz, $T_A$ = 25°C (See Figure 14) | | 73 | | dB |
| | | $f_{CLK}$ = 245.76 MSPS, IF = 61.44 MHz, $T_A$ = 25°C (See Figure 15) | | 71 | | |
| | | $f_{CLK}$ = 399.32 MSPS, IF = 153.36 MHz, $T_A$ = 25°C (See Figure 17) | | 68 | | dB |
| IMD | Two-tone intermodulation to Nyquist (each tone at −6 dBFS) | $f_{CLK}$ = 400 MSPS, $f_{OUT1}$ = 70 MHz, $f_{OUT2}$ = 71 MHz, $T_A$ = 25°C | | 67 | | dBc |
| | | $f_{CLK}$ = 400 MSPS, $f_{OUT1}$ = 140 MHz, $f_{OUT2}$ = 141 MHz, $T_A$ = 25°C | | 63 | | |
| | Four-tone intermodulation, 15-MHz span, missing center tone (each tone at –16 dBFS) | $f_{CLK}$ = 156 MSPS, $f_{OUT}$ = 15.6, 15.8, 16.2, 16.4 MHz | | 72 | | dBc |
| | | $f_{CLK}$ = 400 MSPS, $f_{OUT}$ = 68.1, 69.3, 71.2, 72 MHz | | 74 | | |

† Spectrum analyzer (ACPR) performance taken into account for the calculation of the DAC5675 ACPR performance.

## electrical characteristics over recommended operating free-air temperature range, $AV_{DD}$ = 3.3 V, $DV_{DD}$ = 3.3 V (unless otherwise noted)

### digital specifications

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LVDS Interface: nodes D[13..0]A, D[13..0]B** | | | | | | |
| $V_{ITH+}$ | Positive-going differential input voltage threshold | See LVDS min/max threshold voltages table | | 100 | | mV |
| $V_{ITH-}$ | Negative-going differential input voltage threshold | | | −100 | | |
| $Z_T$ | Internal termination impedance | | 90 | | 132 | Ω |
| $C_I$ | Input capacitance | | | 2 | | pF |
| **CMOS interface: node SLEEP** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 2 | 3.3 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0 | 0.8 | V |
| $I_{IH}$ | High-level input current | | −10 | | 10 | µA |
| $I_{IL}$ | Low-level input current | | −10 | | 10 | µA |
| | Input capacitance | | | 2 | | pF |
| **Clock interface: node CLK, CLKC** | | | | | | |
| | Input resistance | Node CLK, CLKC | | 670 | | Ω |
| | Input capacitance | Node CLK, CLKC | | 2 | | pF |
| | Input resistance | Differential | | 1.3 | | kΩ |
| | Input capacitance | Differential | | 1 | | pF |
| **Timing** | | | | | | |
| $t_{su}$ | Input setup time | | | 1.5 | | ns |
| $t_h$ | Input hold time | | | 0.25 | | ns |
| $t_{LPH}$ | Input latch pulse high time | | | 2 | | ns |
| $t_{DD}$ | Digital delay time | | | 1 | | clk |

## electrical characteristics over recommended operating free-air temperature range, $AV_{DD}$ = 3.3 V, $DV_{DD}$ = 3.3 V, $I_{O(FS)}$ = 20 mA (unless otherwise noted)

### LVDS input minimum and maximum input threshold and logical bit equivalent

| APPLIED VOLTAGES | | RESULTING DIFFERENTIAL INPUT VOLTAGE | RESULTING COMMON-MODE INPUT VOLTAGE | LOGICAL BIT BINARY EQUIVALENT | COMMENT |
|---|---|---|---|---|---|
| $V_A$ [V] | $V_B$ [V] | $V_{A,B}$ [mV] | $V_{COM}$ [V] | | |
| 1.25 | 1.15 | 200 | 1.2 | 1 | Operation with minimum differential voltage (±200 mV) applied to the complementary inputs versus common mode range |
| 1.15 | 1.25 | −200 | 1.2 | 0 | |
| 2.4 | 2.3 | 200 | 2.35 | 1 | |
| 2.3 | 2.4 | −200 | 2.35 | 0 | |
| 0.1 | 0 | 200 | 0.05 | 1 | |
| 0 | 0.1 | −200 | 0.05 | 0 | |
| 1.5 | 0.9 | 600 | 1.2 | 1 | Operation with maximum differential voltage (±600 mV) applied to the complementary inputs versus common mode range |
| 0.9 | 1.5 | −600 | 1.2 | 0 | |
| 2.4 | 1.8 | 600 | 2.1 | 1 | |
| 1.8 | 2.4 | −600 | 2.1 | 0 | |
| 0.6 | 0 | 600 | 0.3 | 1 | |
| 0 | 0.6 | −600 | 0.3 | 0 | |

Specifications subject to change

## TYPICAL CHARACTERISTICS

**POWER vs FREQUENCY**

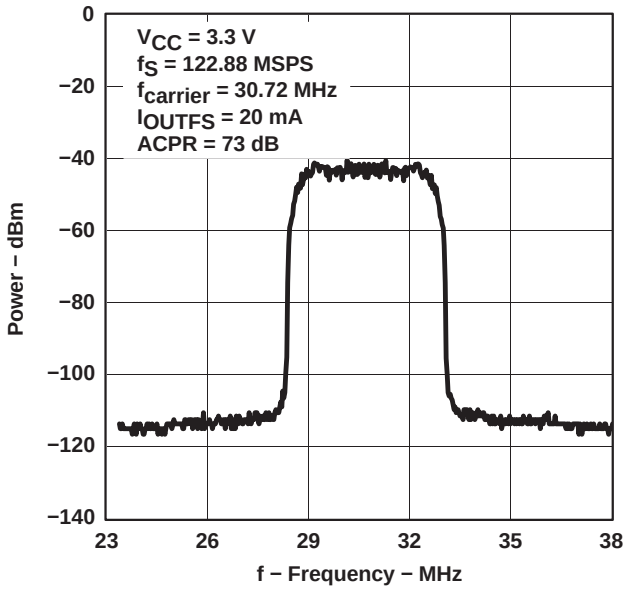



**Figure 14**

**POWER vs FREQUENCY**

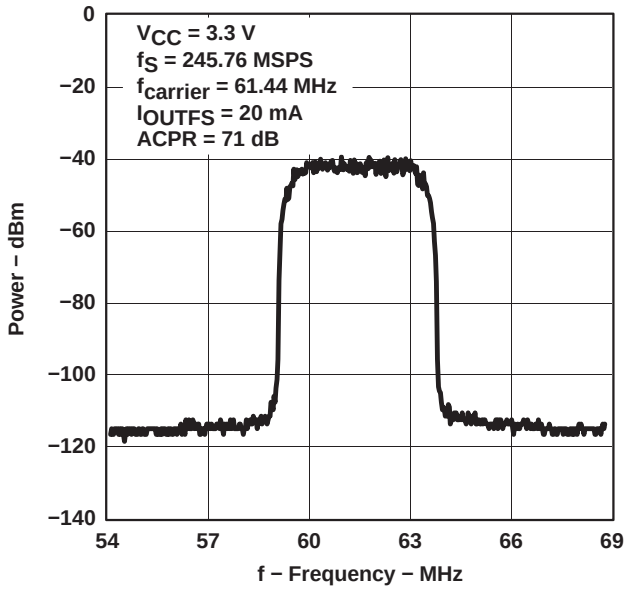



**Figure 15**

**ACPR vs FREQUENCY**

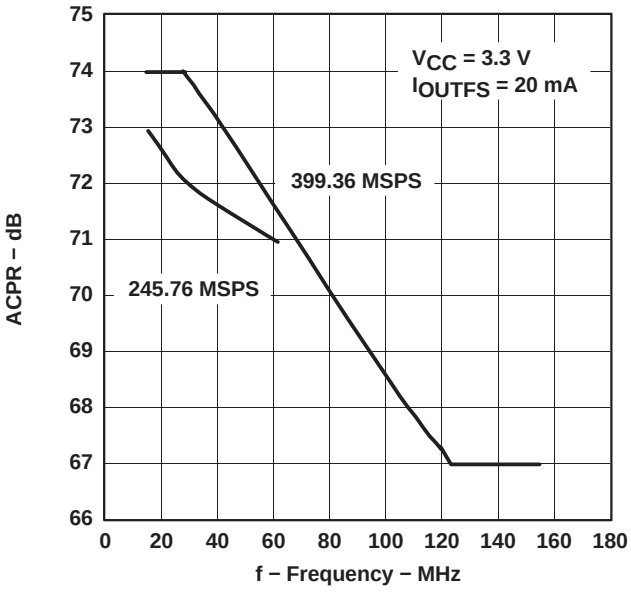



**Figure 16**

**POWER vs FREQUENCY**

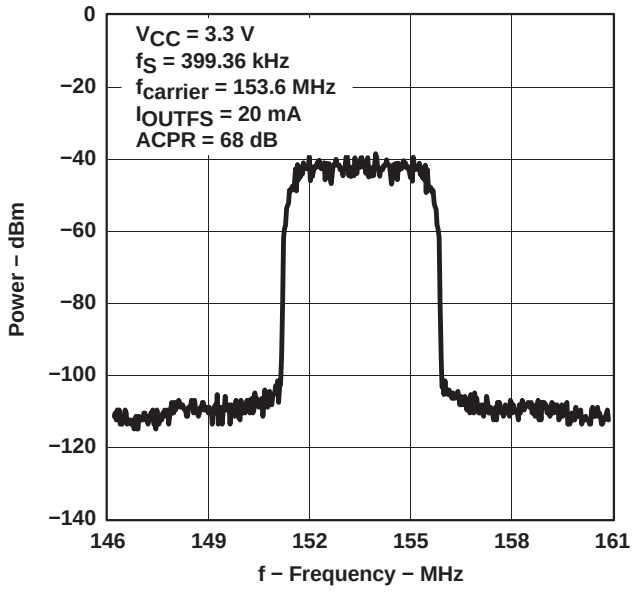



**Figure 17**

## TYPICAL CHARACTERISTICS

POWER
vs
FREQUENCY

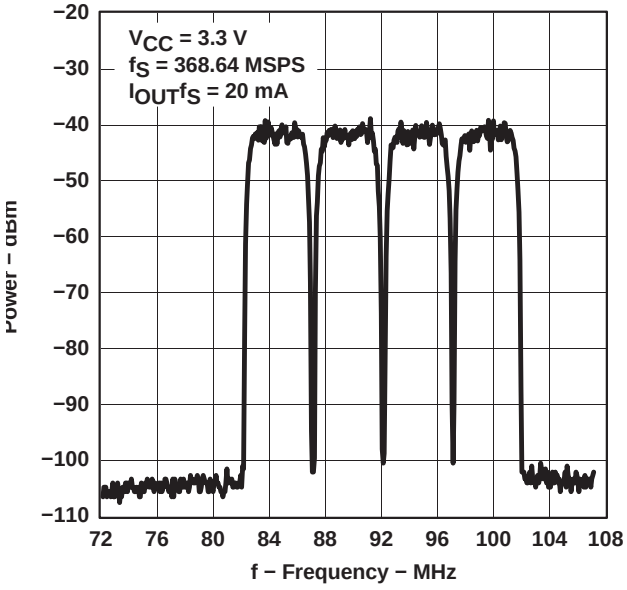



Figure 18

POWER
vs
FREQUENCY

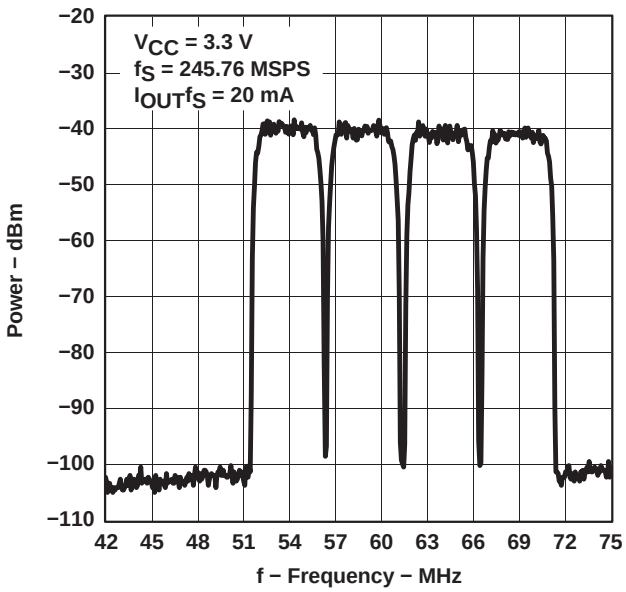



Figure 19

ADJACENT CHANNEL POWER RATIO
vs
DUTY CYCLE

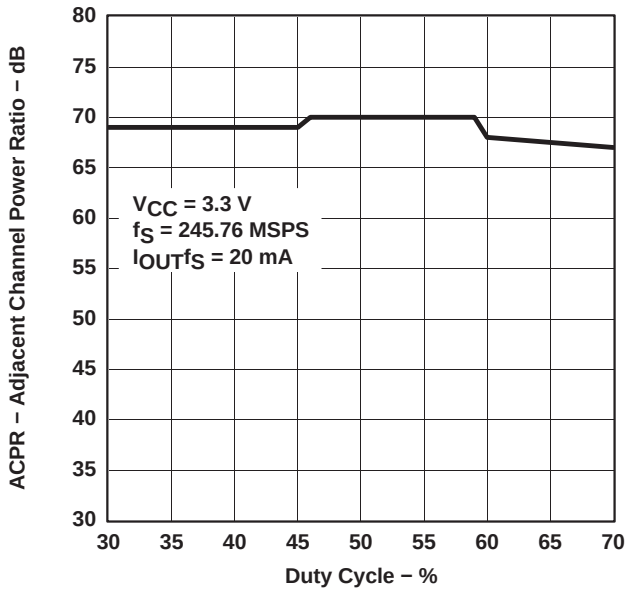



Figure 20

POWER
vs
FREQUENCY

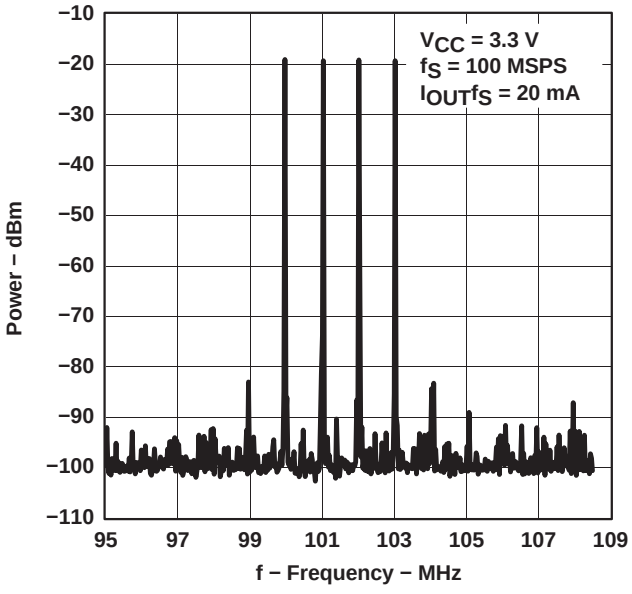



Figure 21

## TYPICAL CHARACTERISTICS

**INTEGRAL NONLINEARITY**
**vs**
**INPUT CODE**

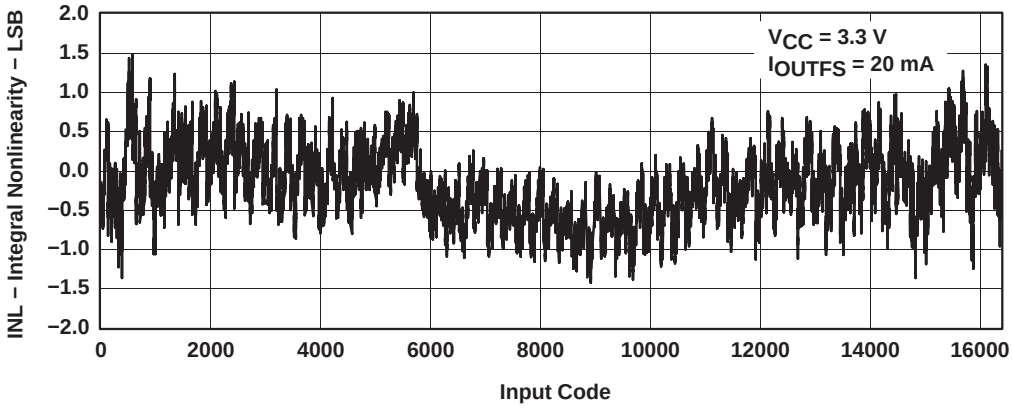



**Figure 22**

**DIFFERENTIAL NONLINEARITY**
**vs**
**INPUT CODE**

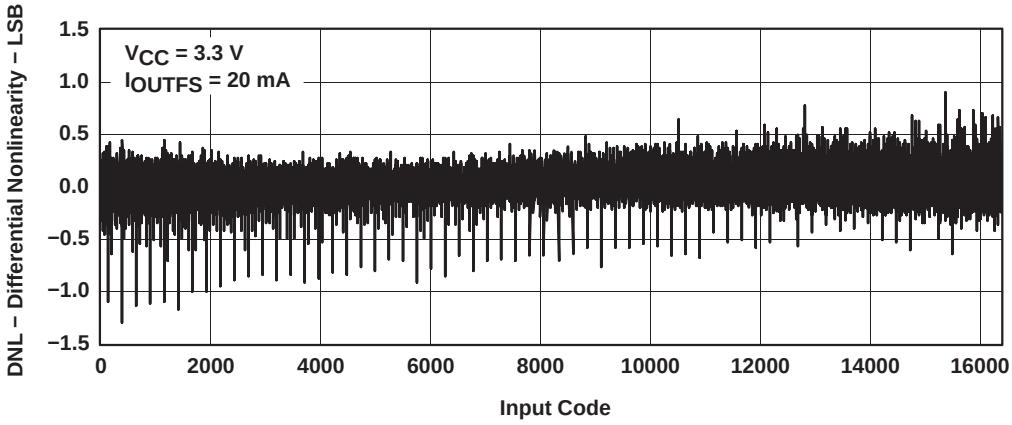



**Figure 23**

## TYPICAL CHARACTERISTICS

**SPURIOUS-FREE DYNAMIC RANGE vs OUTPUT FREQUENCY**

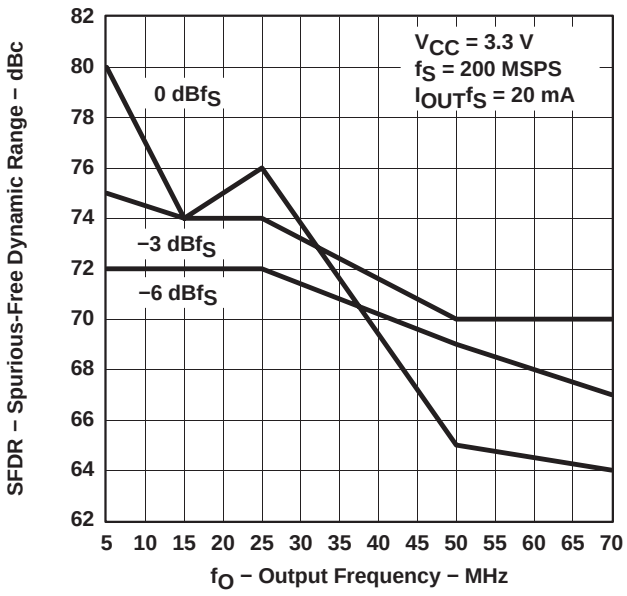



Figure 24

**SPURIOUS-FREE DYNAMIC RANGE vs OUTPUT FREQUENCY**

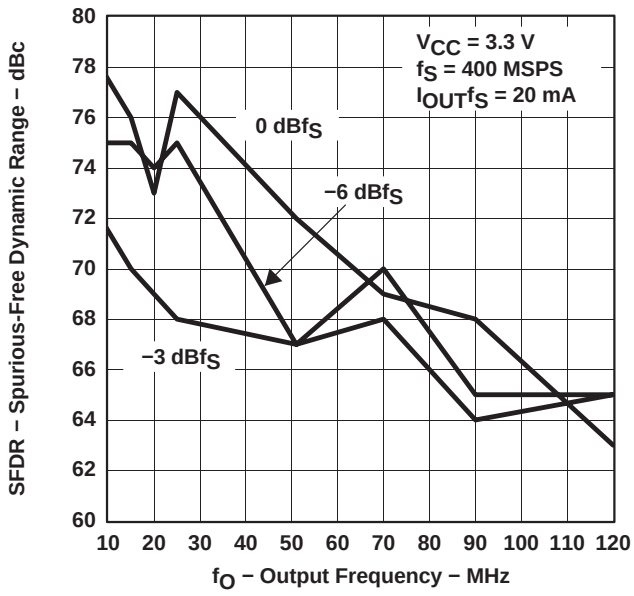



Figure 25

**POWER DISSIPATION vs SAMPLING FREQUENCY**

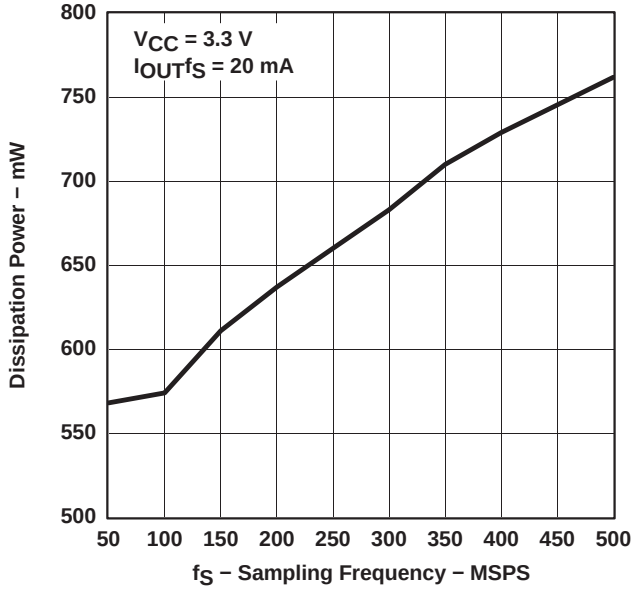



Figure 26

**INTERMODULATION vs INPUT FREQUENCY**

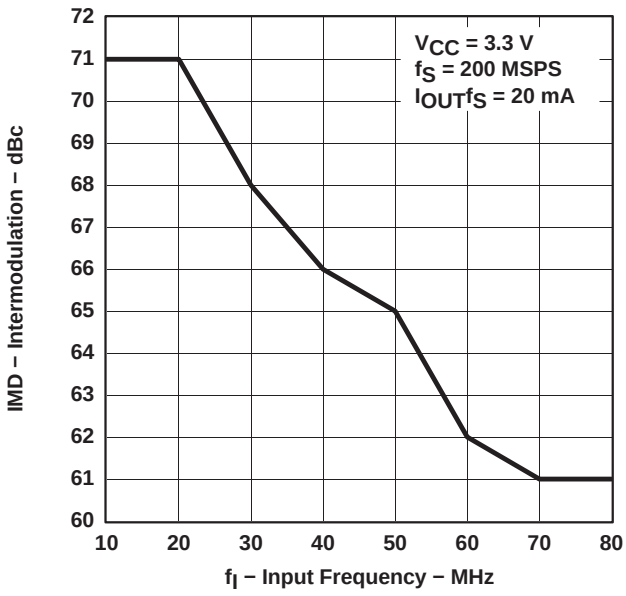



Figure 27

## TYPICAL CHARACTERISTICS

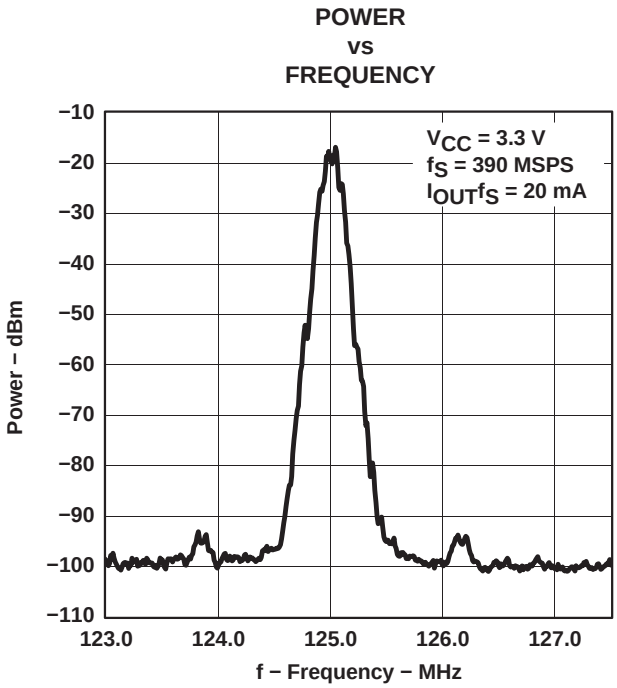



**Figure 28**

## DEFINITIONS

### definitions of specifications and terminology

Gain error is defined as the percentage error in the ratio between the measured full-scale output current and the value of 16 x $V_{(EXTIO)}/R_{BIAS}$. A $V_{(EXTIO)}$ of 1.25 V is used to measure the gain error with external reference voltage applied. With internal reference, this error includes the deviation of $V_{(EXTIO)}$ (internal bandgap reference voltage) from the typical value of 1.25 V.

Offset error is defined as the percentage error in the ratio of the differential output current (IOUT1−IOUT2) and the half of the full-scale output current for input code 8192.

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental output signal.

SNR is the ratio of the rms value of the fundamental output signal to the rms sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and dc.

SINAD is the ratio of the rms value of the fundamental output signal to the rms sum of all other spectral components below the Nyquist frequency, including noise and harmonics, but excluding dc.

ACPR or adjacent channel power ratio is defined for a 3.84 Mcps 3GPP W−CDMA input signal measured in a 3.9-MHz bandwidth at a 5-MHz offset from the carrier with a 12-dB peak-to-average ratio.

APSSR or analog power supply ratio is the percentage variation of full-scale output current versus a 5% variation of the analog power supply AVDD from the nominal. This is a dc measurement.

DPSSR or digital power supply ratio is the percentage variation of full-scale output current versus a 5% variation of the digital power supply DVDD from the nominal. This is a dc measurement.

## DAC5675 evaluation board

An EVM (evaluation module) board for the DAC5675 digital-to-analog converter is available for evaluation. This board allows the user the flexibility to operate the DAC5675 in various configurations. The digital inputs are designed to be driven either directly from various pattern generators and or from LVDS bus drivers.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DAC5675IPHP | ACTIVE | HTQFP | PHP | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | DAC5675I | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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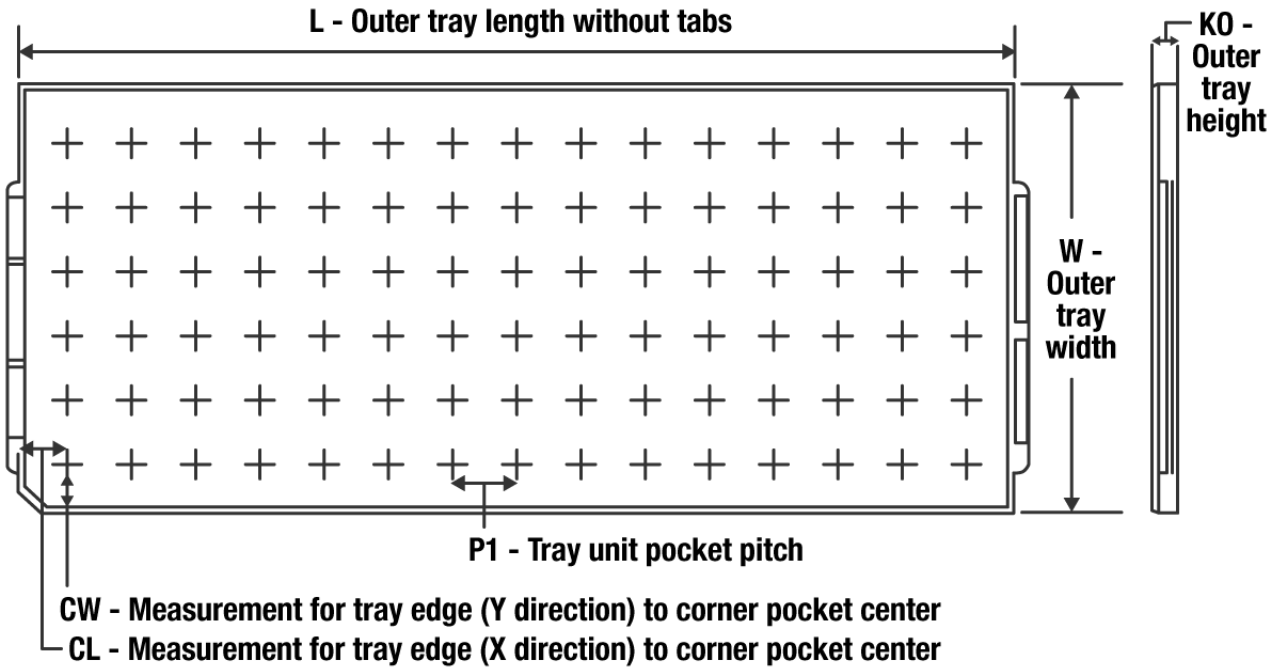
**OTHER QUALIFIED VERSIONS OF DAC5675 :**

- Enhanced Product: DAC5675-EP

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DAC5675IPHP | PHP | HTQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |

# GENERIC PACKAGE VIEW

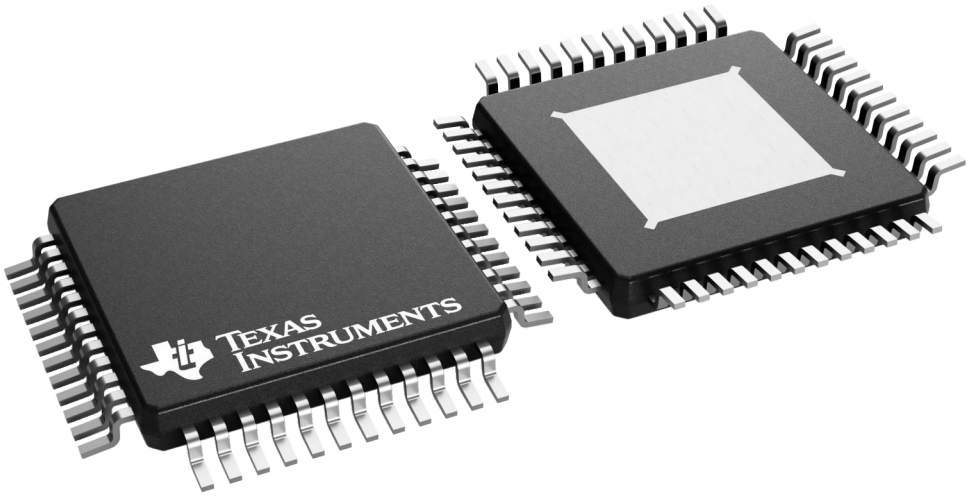
## PHP 48

## TQFP - 1.2 mm max height

**7 x 7, 0.5 mm pitch**

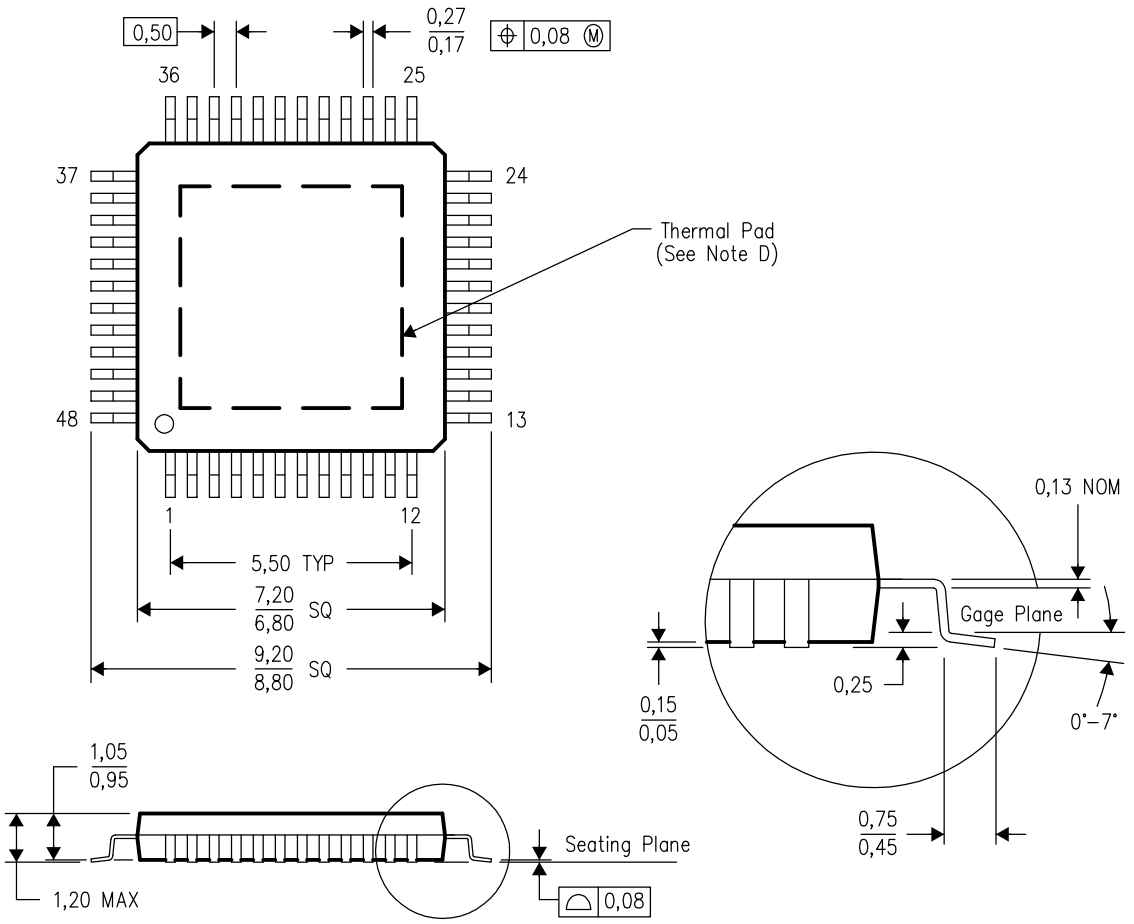
QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4226443/A

## PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

**PowerPAD is a trademark of Texas Instruments.**

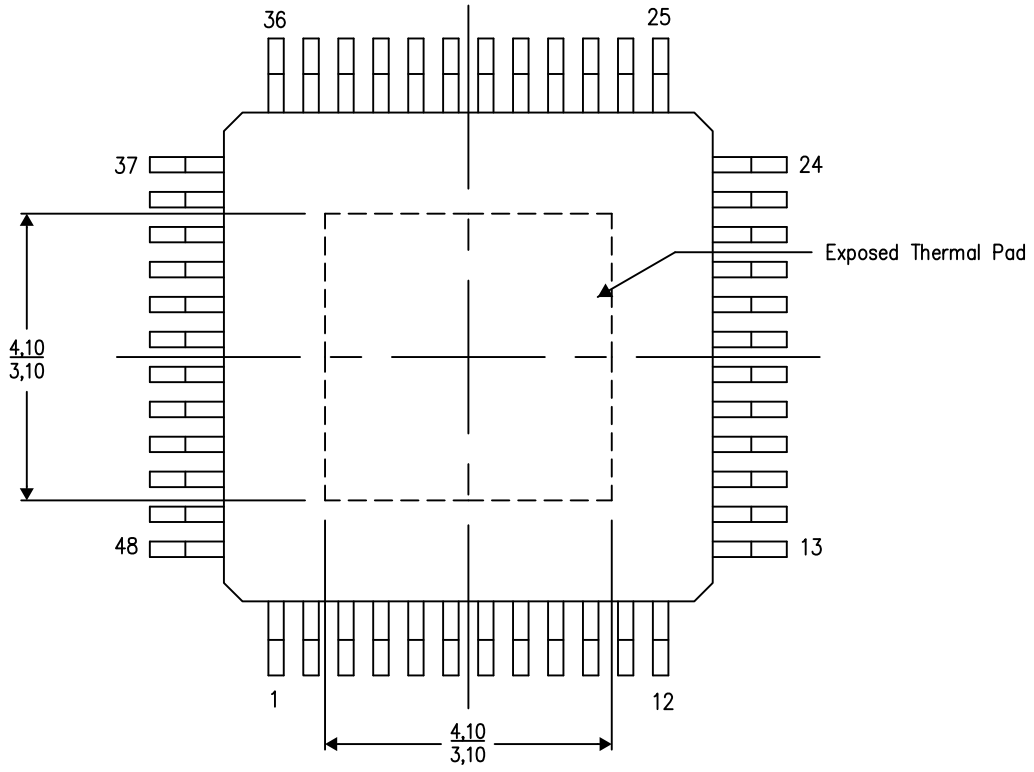
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

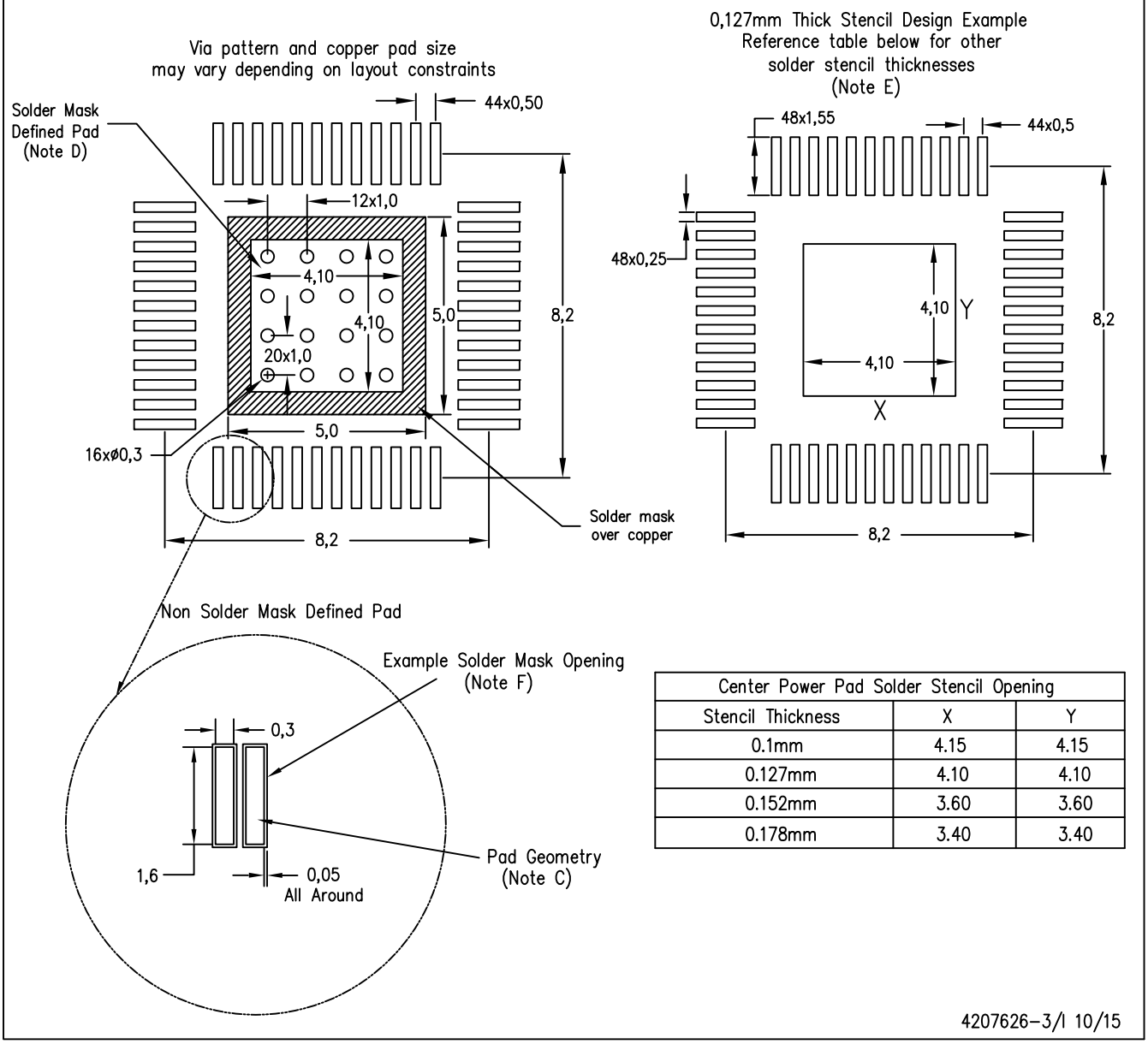
Exposed Thermal Pad Dimensions

4206329–3/P 03/15

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

# PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 4.15 | 4.15 |
| 0.127mm | 4.10 | 4.10 |
| 0.152mm | 3.60 | 3.60 |
| 0.178mm | 3.40 | 3.40 |

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting options for vias placed in the thermal pad.

**PowerPAD is a trademark of Texas Instruments**

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