SLLS165G − JANUARY 1994 − REVISED MARCH 2006

- **Integrated Asynchronous Communications Element**
- **Consists of Four Improved TL16C550 ACEs Plus Steering Logic**
- **In FIFO Mode, Each ACE Transmitter and Receiver Is Buffered With 16-Byte FIFO to Reduce the Number of Interrupts to CPU**
- **In TL16C450 Mode, Hold and Shift Registers Eliminate Need for Precise Synchronization Between the CPU and Serial Data**
- **Up to 16-MHz Clock Rate for up to 1-Mbaud Operation**
- **Programmable Baud Rate Generators Which Allow Division of Any Input Reference Clock by 1 to ($2^{16}-1$) and Generate an Internal 16 × Clock**
- **Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or From the Serial Data Stream**
- **Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
  - **Baud Generation (DC to 1-Mbit Per Second)**
- **False Start Bit Detection**
- **Complete Status Reporting Capabilities**
- **Line Break Generation and Detection**
- **Internal Diagnostic Capabilities:**
  - **Loopback Controls for Communications Link Fault Isolation**
  - **Break, Parity, Overrun, Framing Error Simulation**
- **Fully Prioritized Interrupt System Controls**
- **Modem Control Functions ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$, and $\overline{\text{DCD}}$)**
- **3-State Outputs Provide TTL Drive Capabilities for Bidirectional Data Bus and Control Bus**

description

The TL16C554 and the TL16C554I are enhanced quadruple versions of the TL16C550B asynchronous communications element (ACE). Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the quadruple ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the operation performed and any error conditions encountered.

The TL16C554 and the TL16C554I quadruple ACE can be placed in an alternate FIFO mode, which activates the internal FIFOs to allow 16 bytes (plus three bits of error data per byte in the receiver FIFO) to be stored in both receive and transmit modes. To minimize system overhead and maximize system efficiency, all logic is on the chip. Two terminal functions allow signaling of direct memory access (DMA) transfers. Each ACE includes a programmable baud rate generator that can divide the timing reference clock input by a divisor between 1 and ($2^{16}-1$).

The TL16C554 and the TL16C554I are available in a 68-pin plastic-leaded chip-carrier (PLCC) FN package and in an 80-pin (TQFP) PN package.

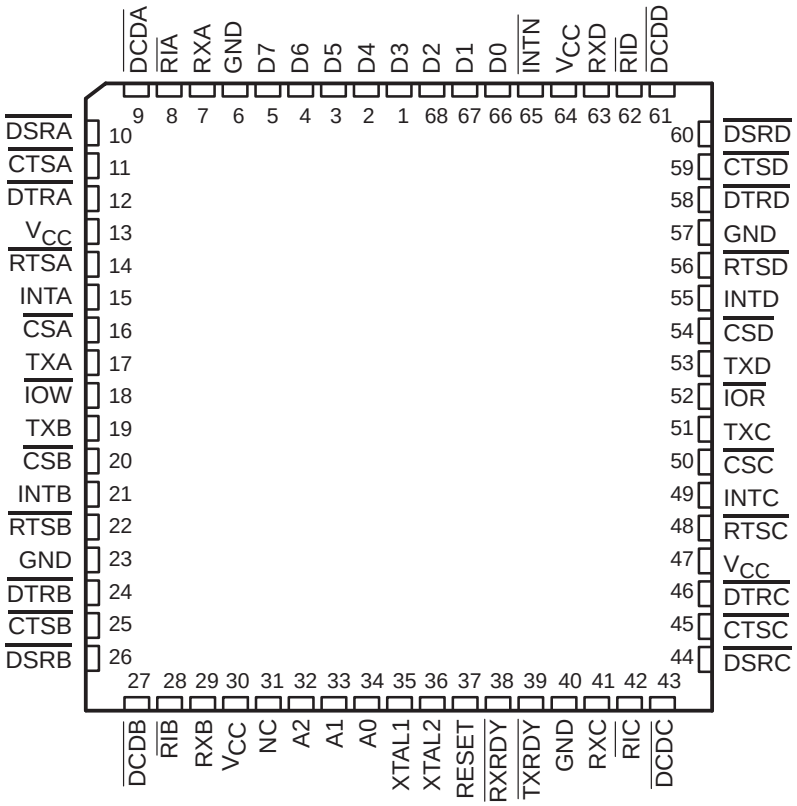


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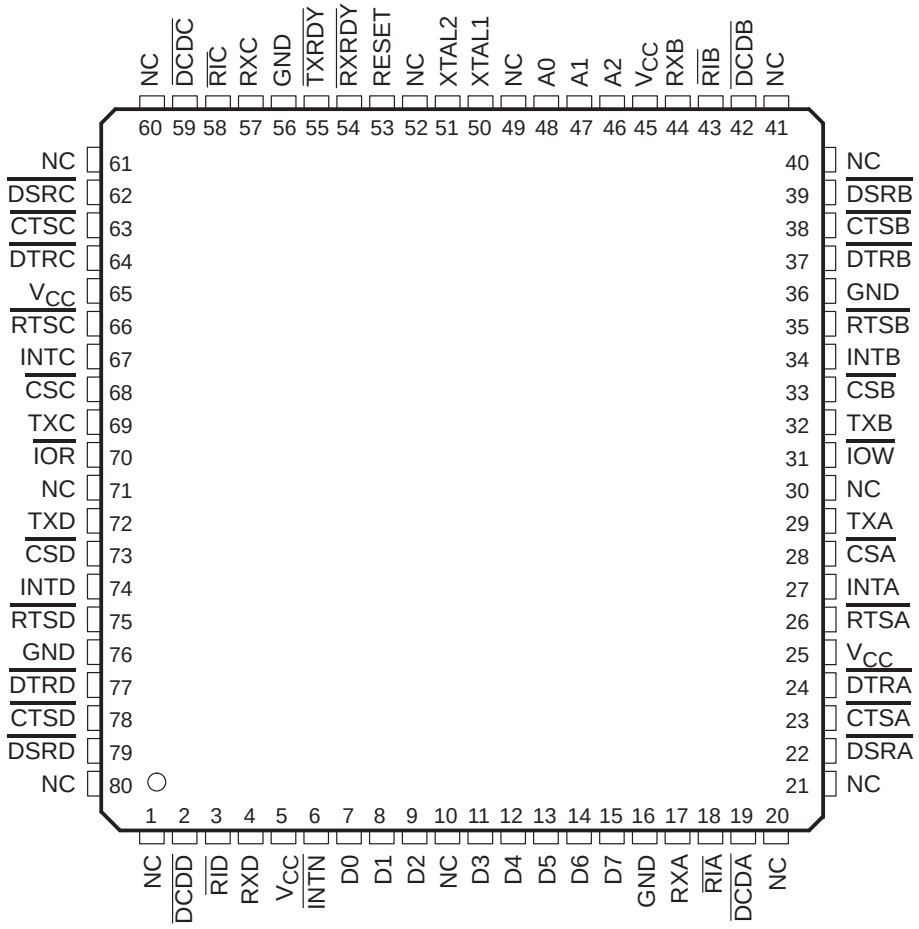
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FN PACKAGE
(TOP VIEW)



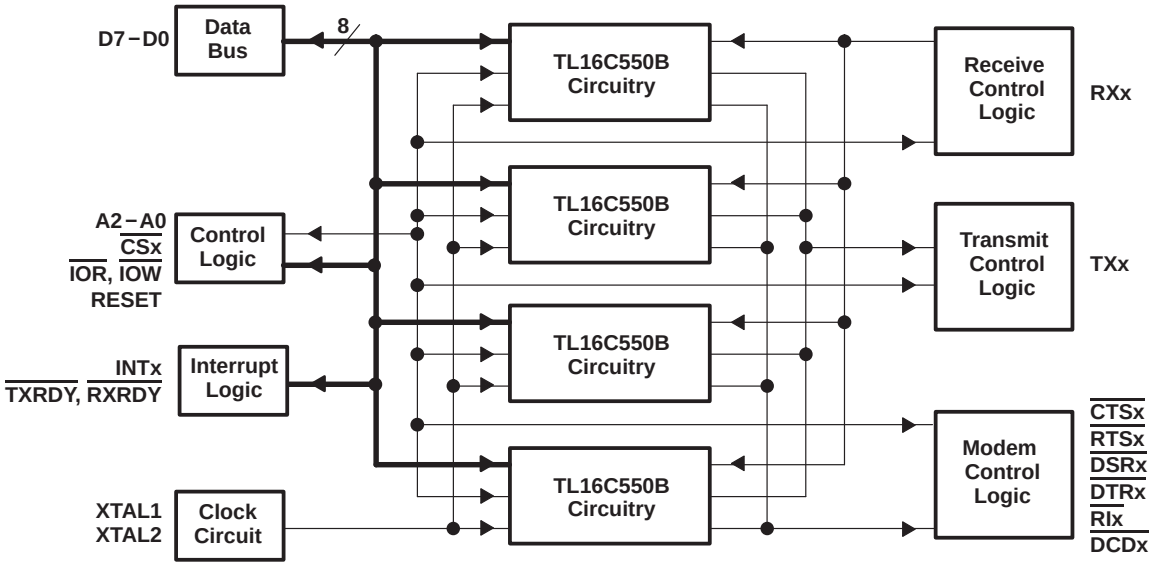
NC − No internal connection

PN PACKAGE
(TOP VIEW)



NC − No internal connection

functional block diagram†



† For TL16C550 circuitry, refer to the TL16C550B data sheet.

Terminal Functions

TERMINAL NAME	FN NO.	PN NO.	I/O	DESCRIPTION
A0 A1 A2	34 33 32	48 47 46	I	Register select terminals. A0, A1, and A2 are three inputs used during read and write operations to select the ACE register to read or write.
$\overline{CSA}$, $\overline{CSB}$, CSC, CSD	16, 20, 50, 54	28, 33, 68, 73	I	Chip select. Each chip select ($\overline{CSx}$) enables read and write operations to its respective channel.
$\overline{CTSA}$, $\overline{CTSB}$, CTSC, CTSD	11, 25, 45, 59	23, 38, 63, 78	I	Clear to send. $\overline{CTSx}$ is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register. $\overline{CTS}$ has no affect on the transmit or receive operation.
D7−D0	66−68 1−5	15−11, 9−7	I/O	Data bus. Eight data lines with 3-state outputs provide a bidirectional path for data, control, and status information between the TL16C554 and the CPU. D0 is the least significant bit (LSB).
$\overline{DCDA}$, $\overline{DCDB}$, DCDC, DCDD	9, 27, 43, 61	19,42, 59, 2	I	Data carrier detect. A low on $\overline{DCDx}$ indicates the carrier has been detected by the modem. The condition of this signal is checked by reading bit 7 of the modem status register.
$\overline{DSRA}$, $\overline{DSRB}$, DSRC, DSRD	10, 26, 44, 60	22, 39, 62, 79	I	Data set ready. $\overline{DSRx}$ is a modem status signal. Its condition can be checked by reading bit 5 (DSR) of the modem status register. $\overline{DSR}$ has no affect on the transmit or receive operation.
$\overline{DTRA}$, $\overline{DTRB}$, DTRC, DTRD	12, 24, 46, 58	24, 37, 64, 77	O	Data terminal ready. $\overline{DTRx}$ is an output that indicates to a modem or data set that the ACE is ready to establish communications. It is placed in the active state by setting the DTR bit of the modem control register. $\overline{DTRx}$ is placed in the inactive state (high) either as a result of the master reset during loop mode operation or clearing bit 0 ($\overline{DTR}$) of the modem control register.
GND	6, 23, 40, 57	16, 36, 56, 76		Signal and power ground
$\overline{INTN}$	65	6	I	Interrupt normal. $\overline{INTN}$ operates in conjunction with bit 3 of the modem status register and affects operation of the interrupts (INTA, INTB, INTC, and INTD) for the four universal asynchronous receiver/transceivers (UARTs) per the following table.

$\overline{INTN}$	OPERATION OF INTERRUPTS
Brought low or allowed to float	Interrupts are enabled according to the state of OUT2 (MCR bit 3). When the MCR bit 3 is cleared, the 3-state interrupt output of that UART is in the high-impedance state. When the MCR bit 3 is set, the interrupt output of the UART is enabled.
Brought high	Interrupts are always enabled, overriding the OUT2 enables.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL FN NO.	TERMINAL PN NO.	I/O	DESCRIPTION
INTA, INTB, INTC, INTD	15, 21, 49, 55	27, 34, 67, 74	O	External interrupt output. The INTx outputs go high (when enabled by the interrupt register) and inform the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, receiver data available or timeout (FIFO mode only), transmitter holding register empty, and an enabled modem status interrupt. The interrupt is disabled when it is serviced or as the result of a master reset.
$\overline{\text{IOR}}$	52	70	I	Read strobe. A low level on $\overline{\text{IOR}}$ transfers the contents of the TL16C554 data bus to the external CPU bus.
$\overline{\text{IOW}}$	18	31	I	Write strobe. $\overline{\text{IOW}}$ allows the CPU to write into the selected address by the address register.
RESET	37	53	I	Master reset. When active, RESET clears most ACE registers and sets the state of various signals. The transmitter output and the receiver input is disabled during reset time.
$\overline{\text{RIA}}$, $\overline{\text{RIB}}$, $\overline{\text{RIC}}$, $\overline{\text{RID}}$	8, 28, 42, 62	18, 43, 58, 3	I	Ring detect indicator. A low on $\overline{\text{RIx}}$ indicates the modem has received a ring signal from the telephone line. The condition of this signal can be checked by reading bit 6 of the modem status register.
$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$, $\overline{\text{RTSC}}$, $\overline{\text{RTSD}}$	14, 22, 48, 56	26, 35, 66, 75	O	Request to send. When active, $\overline{\text{RTSx}}$ informs the modem or data set that the ACE is ready to receive data. Writing a 1 in the modem control register sets this bit to a low state. After reset, this terminal is set high. These terminals have no affect on the transmit or receive operation.
RXA, RXB RXC, RXD	7, 29, 41, 63	17, 44, 57, 4	I	Serial input. RXx is a serial data input from a connected communications device. During loopback mode, the RXx input is disabled from external connection and connected to the TXx output internally.
$\overline{\text{RXRDY}}$	38	54	O	Receive ready. $\overline{\text{RXRDY}}$ goes low when the receive FIFO is full. It can be used as a single transfer or multitransfer.
TXA, TXB TXC, TXD	17, 19, 51, 53	29, 32, 69, 72	O	Transmit outputs. TXx is a composite serial data output that is connected to a communications device. TXA, TXB, TXC, and TXD are set to the marking (high) state as a result of reset.
$\overline{\text{TXRDY}}$	39	55	O	Transmit ready. $\overline{\text{TXRDY}}$ goes low when the transmit FIFO is full. It can be used as a single transfer or multitransfer function.
VCC	13, 30, 47, 64	5, 25, 45, 65		Power supply
XTAL1	35	50	I	Crystal input 1 or external clock input. A crystal can be connected to XTAL1 and XTAL2 to utilize the internal oscillator circuit. An external clock can be connected to drive the internal clock circuits.
XTAL2	36	51	O	Crystal output 2 or buffered clock output (see XTAL1).

absolute maximum ratings over free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range at any input, V_I . . . . . −0.5 V to 7 V
Output voltage range, V_O . . . . . −0.5 V to V_{CC} + 3 V
Continuous total power dissipation at (or below) 70°C . . . . . 500 mW
Operating free-air temperature range, T_A: TL16C554 . . . . . −0°C to 70°C
TL16C554I . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage levels are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Clock high-level input voltage at XTAL1, $V_{IH(CLK)}$		2		V_{CC}	V
Clock low-level input voltage at XTAL1, $V_{IL(CLK)}$		−0.5		0.8	V
High-level input voltage, V_{IH}		2		V_{CC}	V
Low-level input voltage, V_{IL}		−0.5		0.8	V
Clock frequency, f_{clock}				16	MHz
Operating free-air temperature, T_A	TL16C554	0		70	°C
	TL16C554I	−40		85	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}‡	High-level output voltage	I_{OH} = −1 mA	2.4			V
V_{OL}‡	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{Ikg}	Input leakage current	V_{CC} = 5.25 V, GND = 0, V_I = 0 to 5.25 V, All other terminals floating			±10	µA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V, GND = 0, V_O = 0 to 5.25 V, Chip selected in write mode or chip deselected			±20	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, RX, $\overline{DSR}$, $\overline{DCD}$, CTS, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kilobits per second			50	mA
$C_{i(XTAL1)}$	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, All other terminals grounded, f = 1 MHz, T_A = 25°C		15	20	pF
$C_{o(XTAL2)}$	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters apply for all outputs except XTAL2.

clock timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 1)

		MIN	MAX	UNIT
t_{w1}	Pulse duration, clock high (external clock)	31		ns
t_{w2}	Pulse duration, clock low (external clock)	31		ns
t_{w3}	Pulse duration, RESET	1000		ns

read cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 4)

		MIN	MAX	UNIT
t_{w4}	Pulse duration, $\overline{IOR}$ low	75		ns
t_{su1}	Setup time, $\overline{CSx}$ valid before $\overline{IOR}$ low (see Note 2)	10		ns
t_{su2}	Setup time, A2−A0 valid before $\overline{IOR}$ low (see Note 2)	15		ns
t_{h1}	Hold time, A2−A0 valid after $\overline{IOR}$ high (see Note 2)	0		ns
t_{h2}	Hold time, $\overline{CSx}$ valid after $\overline{IOR}$ high (see Note 2)	0		ns
t_{d1}	Delay time, $t_{su2} + t_{w4} + t_{d2}$ (see Note 3)	140		ns
t_{d2}	Delay time, $\overline{IOR}$ high to $\overline{IOR}$ or $\overline{IOW}$ low	50		ns

NOTES: 2. The internal address strobe is always active.
3. In the FIFO mode, t_{d1} = 425 ns (min) between reads of the receiver FIFO and the status registers (interrupt identification register and line status register).

write cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 5)

		MIN	MAX	UNIT
t_{w5}	Pulse duration, $\overline{IOW}\downarrow$	50		ns
t_{su3}	Setup time, $\overline{CSx}$ valid before $\overline{IOW}\downarrow$ (see Note 2)	10		ns
t_{su4}	Setup time, A2−A0 valid before $\overline{IOW}\downarrow$ (see Note 2)	15		ns
t_{su5}	Setup time, D7−D0 valid before $\overline{IOW}\uparrow$	10		ns
t_{h3}	Hold time, A2−A0 valid after $\overline{IOW}\uparrow$ (see Note 2)	5		ns
t_{h4}	Hold time, $\overline{CSx}$ valid after $\overline{IOW}\uparrow$ (see Note 2)	5		ns
t_{h5}	Hold time, D7−D0 valid after $\overline{IOW}\uparrow$	25		ns
t_{d3}	Delay time, $t_{su4} + t_{w5} + t_{d4}$	120		ns
t_{d4}	Delay time, $\overline{IOW}\uparrow$ to $\overline{IOW}$ or $\overline{IOR}\downarrow$	55		ns

NOTE 2: The internal address strobe is always active.

read cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Note 4 and Figure 4)

PARAMETER		MIN	MAX	UNIT
t_{en}	Enable time, $\overline{IOR}\downarrow$ to D7−D0 valid		30	ns
t_{dis}	Disable time, $\overline{IOR}\uparrow$ to D7−D0 released	0	20	ns

NOTE 4: V_{OL} and V_{OH} (and the external loading) determine the charge and discharge time.

transmitter switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 6, 7, and 8)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d5}	Delay time, INTx↓ to TXx↓ at start		8	24	RCLK cycles
t_{d6}	Delay time, TXx↓ at start to INTx↑	See Note 5	8	8	RCLK cycles
t_{d7}	Delay time, $\overline{IOW}$ high or low (WR THR) to INTx↑	See Note 5	16	32	RCLK cycles
t_{d8}	Delay time, TXx↓ at start to $\overline{TXRDY}$↓	C_L = 100 pF		8	RCLK cycles
t_{pd1}	Propagation delay time, $\overline{IOW}$ (WR THR)↓ to INTx↓	C_L = 100 pF		35	ns
t_{pd2}	Propagation delay time, $\overline{IOR}$ (RD IIR)↑ to INTx↓	C_L = 100 pF		30	ns
t_{pd3}	Propagation delay time, $\overline{IOW}$ (WR THR)↑ to $\overline{TXRDY}$↑	C_L = 100 pF		50	ns

NOTE 5: If the transmitter interrupt delay is active, this delay is lengthened by one character time minus the last stop bit time.

receiver switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 9 through 13)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d9}	Delay time, stop bit to INTx↑ or stop bit to $\overline{RXRDY}$↓ or read RBR to set interrupt	See Note 6		1	RCLK cycle
t_{pd4}	Propagation delay time, Read RBR/LSR to INTx↓/LSR interrupt↓	C_L = 100 pF, See Note 7		40	ns
t_{pd5}	Propagation delay time, $\overline{IOR}$ RCLK↓ to $\overline{RXRDY}$↑	See Note 7		30	ns

NOTES: 6. The receiver data available indicator, the overrun error indicator, the trigger level interrupts, and the active $\overline{RXRDY}$ indicator are delayed three RCLK (internal receiver timing clock) cycles in the FIFO mode (FCR0 = 1). After the first byte has been received, status indicators (PE, FE, BI) are delayed three RCLK cycles. These indicators are updated immediately for any further bytes received after $\overline{IOR}$ goes active for a read from the RBR register. There are eight RCLK cycle delays for trigger change level interrupts.

7. RCLK is an internal signal derived from divisor latch LSB (DLL) and divisor latch MSB (DLM) divisor latches.

modem control switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Figure 14)

PARAMETER		MIN	MAX	UNIT
t_{pd6}	Propagation delay time, $\overline{IOW}$ (WR MCR)↑ to $\overline{RTSx}$, $\overline{DTRx}$↑		50	ns
t_{pd7}	Propagation delay time, modem input $\overline{CTSx}$, $\overline{DSRx}$, and $\overline{DCDx}$ ↓↑ to INTx↑		30	ns
t_{pd8}	Propagation delay time, $\overline{IOR}$ (RD MSR)↑ to interrupt↓		35	ns
t_{pd9}	Propagation delay time, $\overline{RIx}$↑ to $\overline{INTx}$↑		30	ns

PARAMETER MEASUREMENT INFORMATION

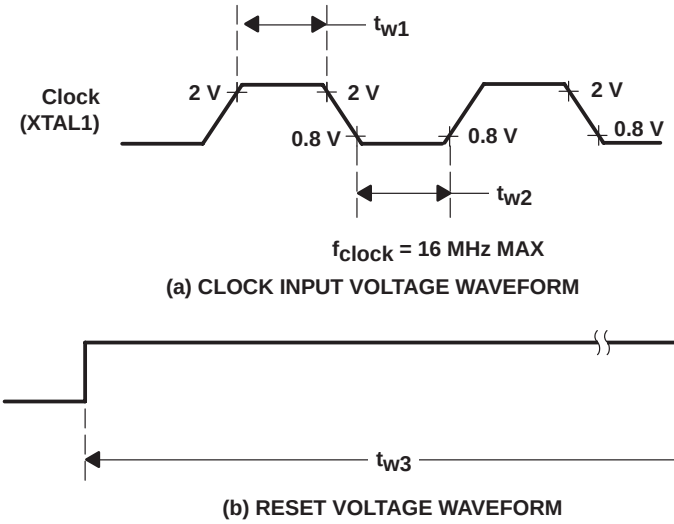
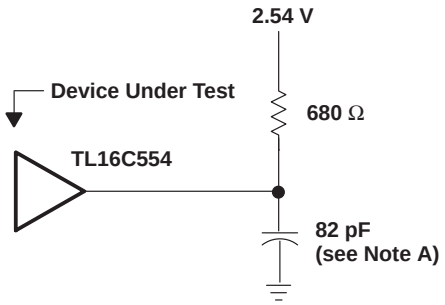


Figure 1. Clock Input and RESET Voltage Waveforms



NOTE A: This includes scope and jig capacitance.

Figure 2. Output Load Circuit

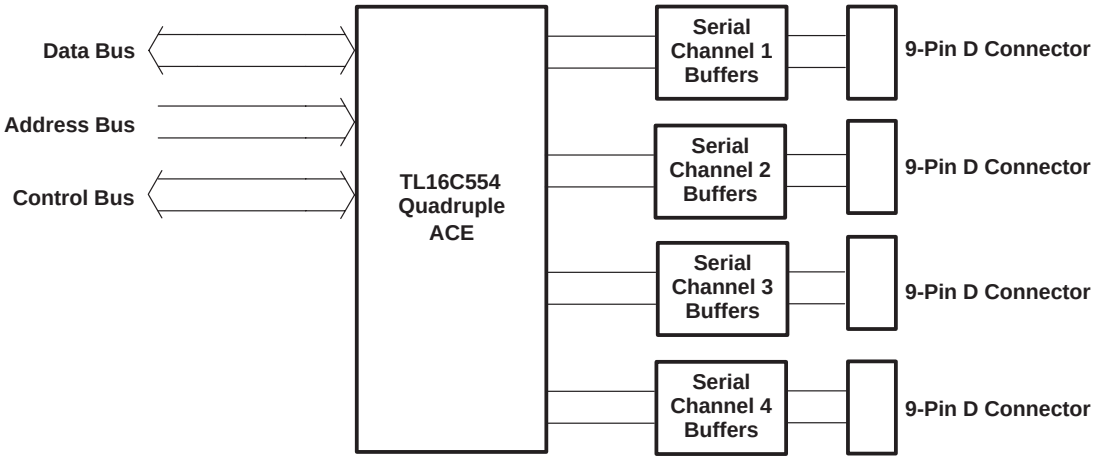


Figure 3. Basic Test Configuration

PARAMETER MEASUREMENT INFORMATION

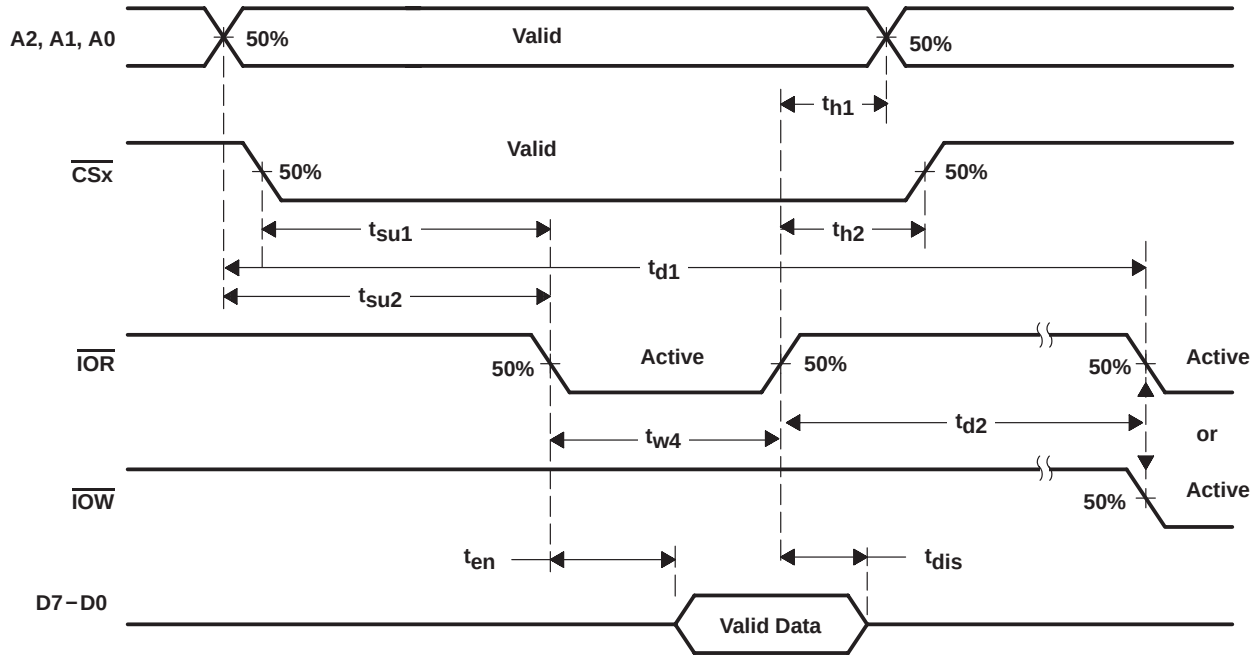


Figure 4. Read Cycle Timing Waveforms

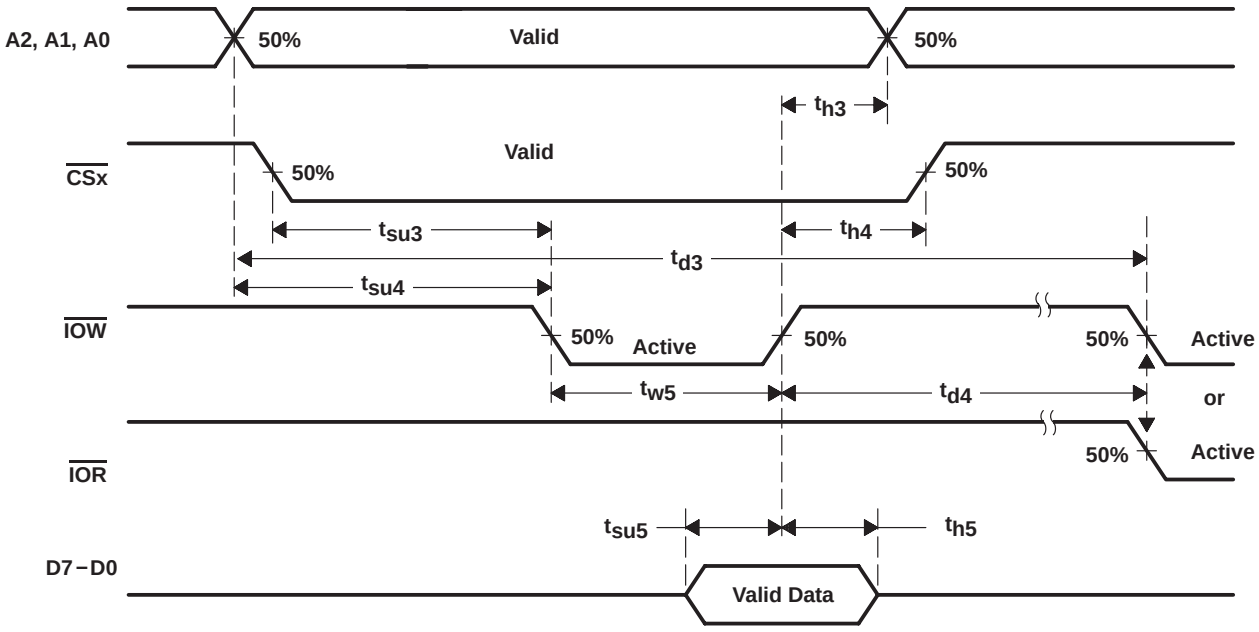


Figure 5. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

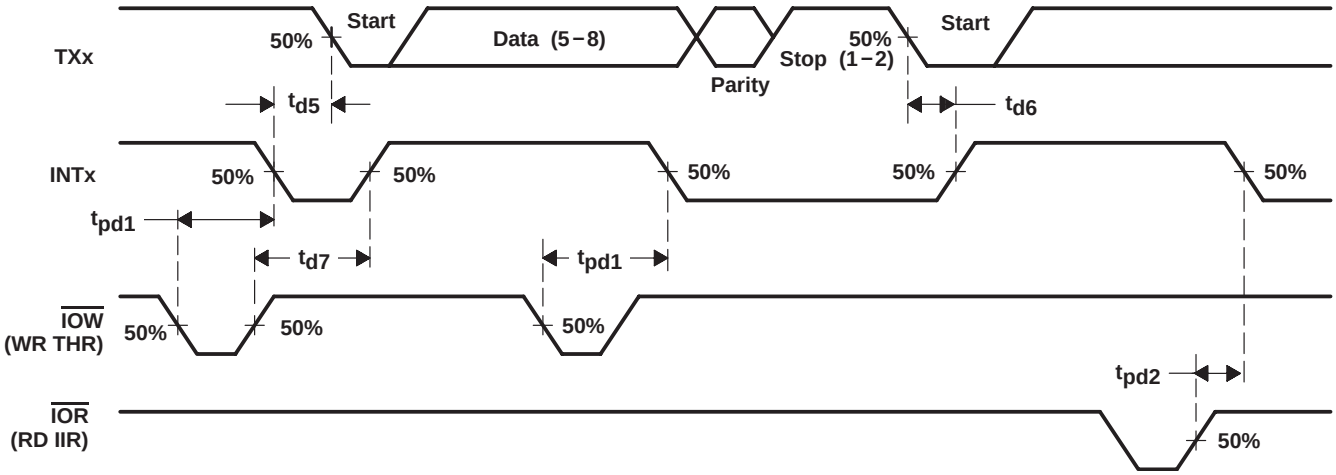


Figure 6. Transmitter Timing Waveforms

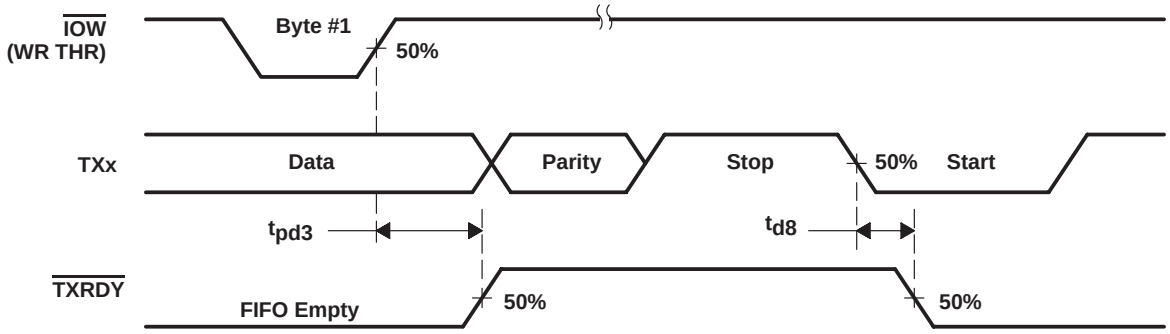


Figure 7. Transmitter Ready Mode 0 Timing Waveforms

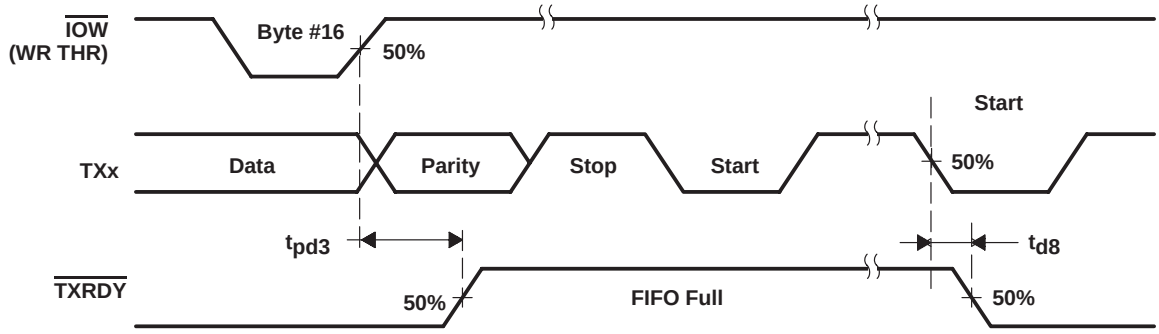


Figure 8. Transmitter Ready Mode 1 Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

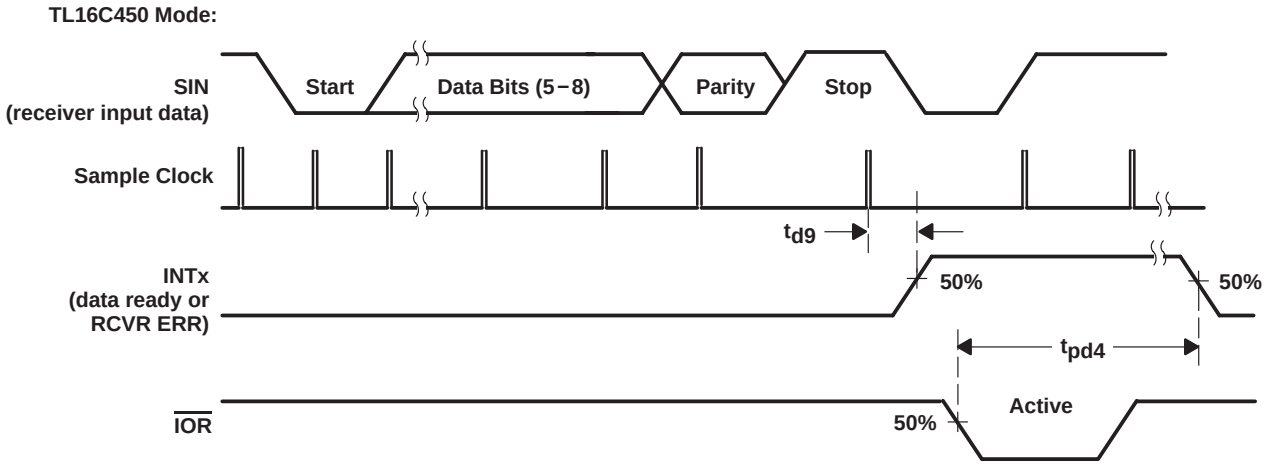


Figure 9. Receiver Timing Waveforms

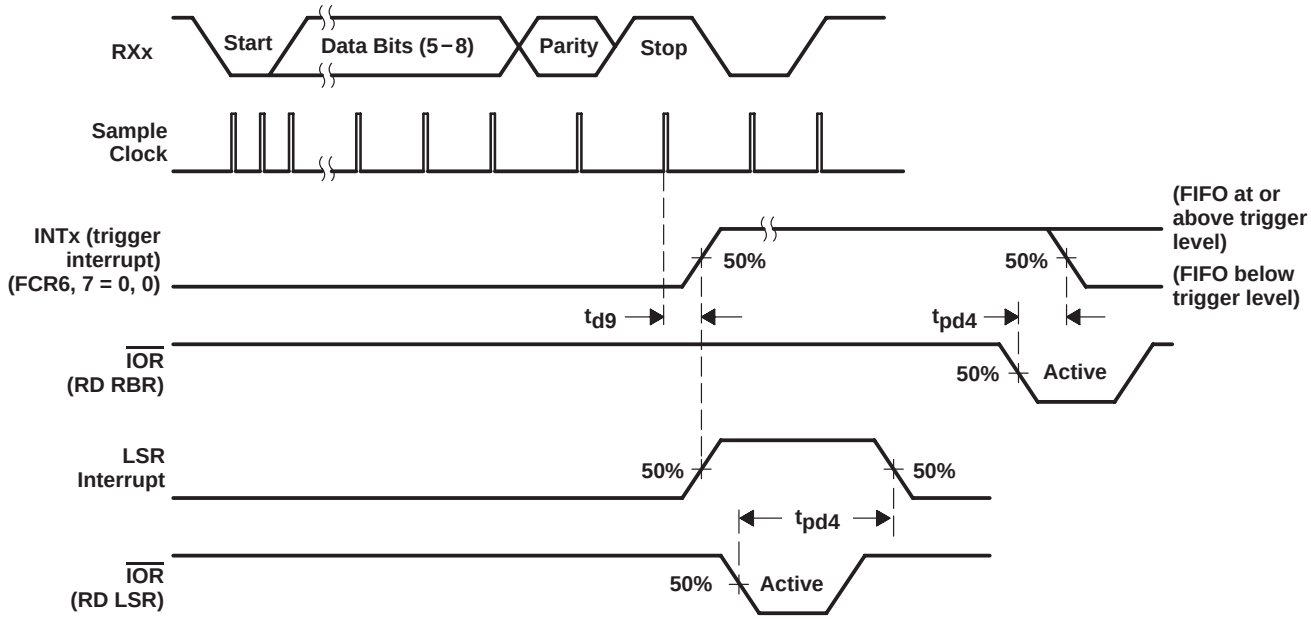
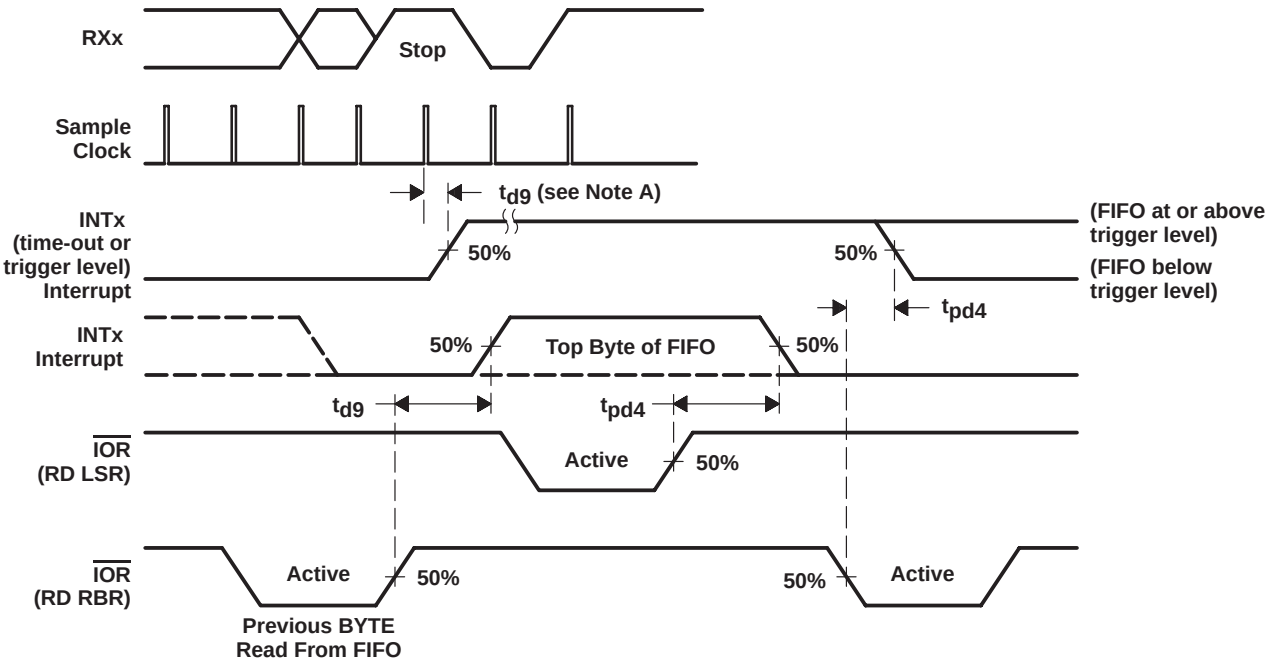


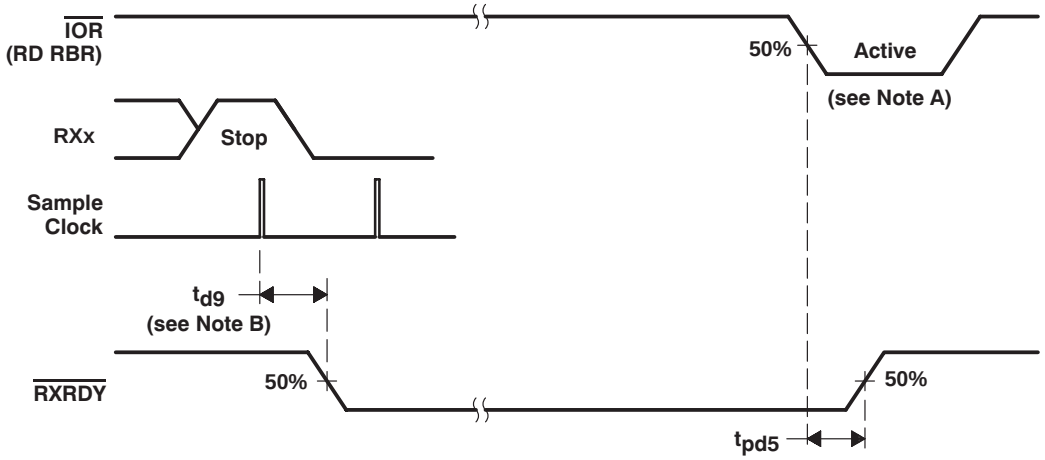
Figure 10. Receiver FIFO First Byte (Sets RDR) Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: This is the reading of the last byte in the FIFO.

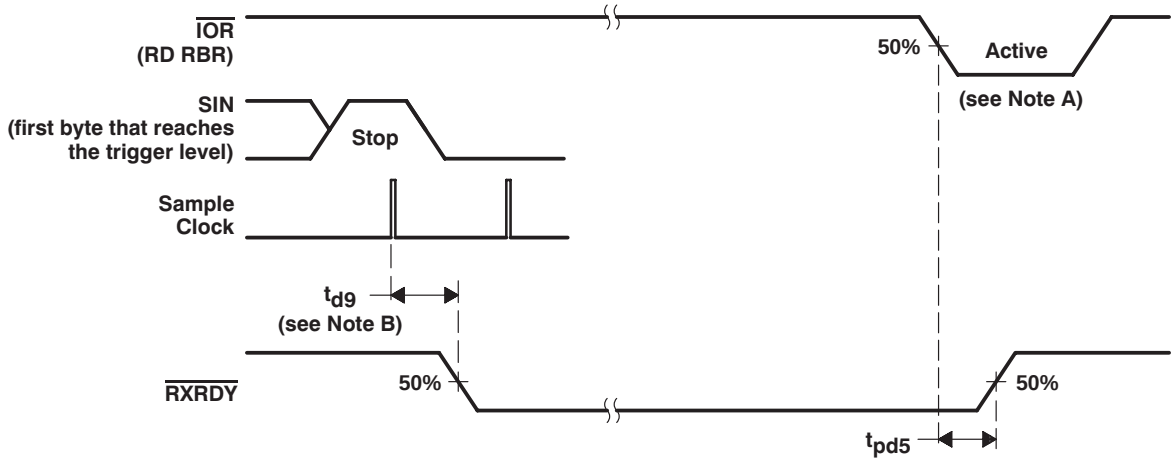
Figure 11. Receiver FIFO After First Byte (After RDR Set) Waveforms



NOTES: A. This is the reading of the last byte in the FIFO.
B. If FCR0 = 1, then t_{d9} = 3 RCLK cycles. For a time-out interrupt, t_{d9} = 8 RCLK cycles.

Figure 12. Receiver Ready Mode 0 Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This is the reading of the last byte in the FIFO.
B. If FCR0 = 1, t_{d9} = 3 RCLK cycles. For a trigger change level interrupt, t_{d9} = 8 RCLK.

Figure 13. Receiver Ready Mode 1 Timing Waveforms

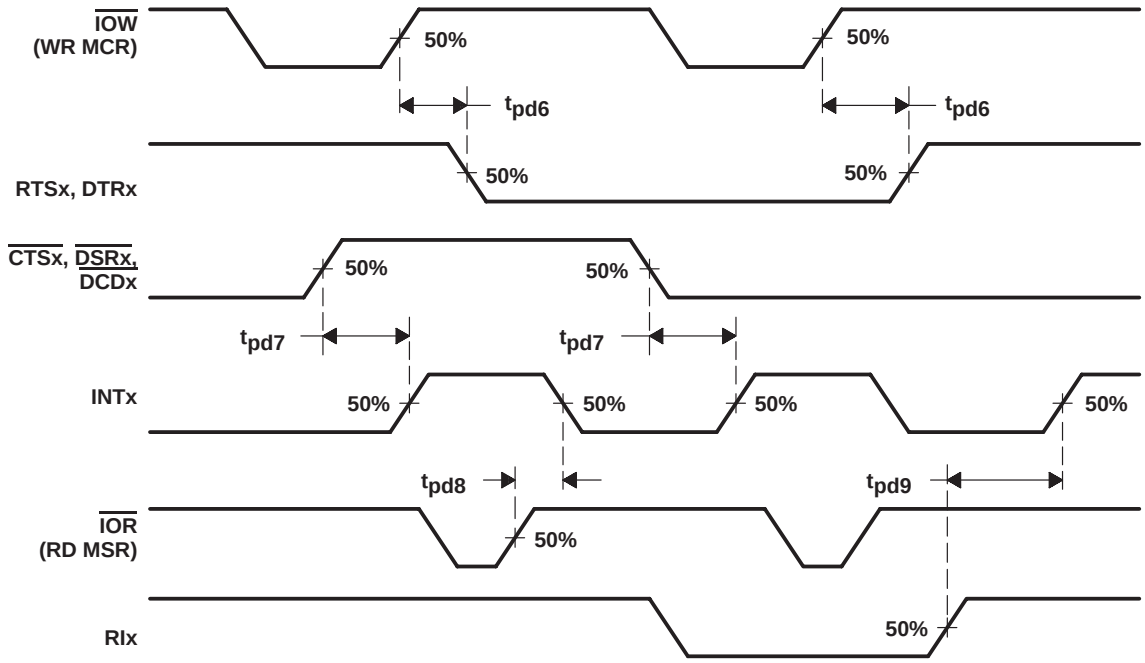


Figure 14. Modem Control Timing Waveforms

PRINCIPLES OF OPERATION

Three types of information are stored in the internal registers used in the ACE: control, status, and data. Mnemonic abbreviations for the registers are shown in Table 1. Table 2 defines the address location of each register and whether it is read only, write only, or read writable.

Table 1. Internal Register Mnemonic Abbreviations

CONTROL	MNEMONIC	STATUS	MNEMONIC	DATA	MNEMONIC
Line control register	LCR	Line status register	LSR	Receiver buffer register	RBR
FIFO control register	FCR	Modem status register	MSR	Transmitter holding register	THR
Modem control register	MCR				
Divisor latch LSB	DLL				
Divisor latch MSB	DLM				
Interrupt enable register	IER				

Table 2. Register Selection†

DLAB‡	A2§	A1§	A0§	READ MODE	WRITE MODE
0	0	0	0	Receiver buffer register	Transmitter holding register
0	0	0	1		Interrupt enable register
X	0	1	0	Interrupt identification register	FIFO control register
X	0	1	1		Line control register
X	1	0	0		Modem control register
X	1	0	1	Line status register	
X	1	1	0	Modem status register	
X	1	1	1	Scratchpad register	Scratchpad register
1	0	0	0		LSB divisor latch
1	0	0	1		MSB divisor latch

X = irrelevant, 0 = low level, 1 = high level
† The serial channel is accessed when either $\overline{CSA}$ or $\overline{CSD}$ is low.
‡ DLAB is the divisor latch access bit and bit 7 in the LCR.
§ A2−A0 are device terminals.

Individual bits within the registers with the bit number in parenthesis are referred to by the register mnemonic. For example, LCR7 refers to line control register bit 7. The transmitter buffer register and receiver buffer register are data registers that hold from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The ACE data registers are double buffered (TL16450 mode) or FIFO buffered (FIFO mode) so that read and write operations can be performed when the ACE is performing the parallel-to-serial or serial-to-parallel conversion.

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 1. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

ADDRESS	REGISTER MNEMONIC	REGISTER ADDRESS							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	RBR (read only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
0	THR (write only)	Data BIt 7	Data BIt 6	Data BIt 5	Data BIt 4	Data BIt 3	Data BIt 2	Data BIt 1	Data BIt 0
0†	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1†	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1	IER	0	0	0	0	(EDSSI) Enable modem status interrupt	(ERLSI) Enable receiver line status interrupt	(ETBEI) Enable transmitter holding register empty interrupt	(ERBI) Enable received data available interrupt
2	FCR (write only)	Receiver Trigger (MSB)	Receiver Trigger (LSB)	Reserved	Reserved	DMA mode select	Transmit FIFO reset	Receiver FIFO reset	FIFO Enable
2	IIR (read only)	FIFOs Enabled‡	FIFOs Enabled‡	0	0	Interrupt ID Bit (3)‡	Interrupt ID Bit (2)	Interrupt ID Bit (1)	0 If interrupt pending
3	LCR	(DLAB) Divisor latch access bit	Set break	Stick parity	(EPS) Even parity select	(PEN) Parity enable	(STB) Number of stop bits	(WLSB1) Word length select bit 1	(WLSB0) Word length select bit 0
4	MCR	0	0	0	Loop	OUT2 Enable external interrupt (INT)	Reserved	(RTS) Request to send	(DTR) Data terminal ready
5	LSR	Error in receiver FIFO‡	(TEMT) Transmitter registers empty	(THRE) Transmitter holding register empty	(BI) Break interrupt	(FE) Framing error	(PE) Parity error	(OE) Overrun error	(DR) Data ready
6	MSR	(DCD) Data carrier detect	(RI) Ring indicator	(DSR) Data set ready	(CTS) Clear to send	(ΔDCD) Delta data carrier detect	(TERI) Trailing edge ring indicator	(ΔDSR) Delta data set ready	(ΔCTS) Delta clear to send
7	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

† DLAB = 1
‡ These bits are always 0 when FIFOs are disabled.

PRINCIPLES OF OPERATION

FIFO control register (FCR)

The FCR is a write-only register at the same location as the IIR. It enables the FIFOs, sets the trigger level of the receiver FIFO, and selects the type of DMA signalling.

- Bit 0: FCR0 enables the transmit and receiver FIFOs. All bytes in both FIFOs can be cleared by clearing FCR0. Data is cleared automatically from the FIFOs when changing from the FIFO mode to the TL16C450 mode (see FCR bit 0) and vice versa. Programming of other FCR bits is enabled by setting FCR0.
- Bit 1: When set, FCR1 clears all bytes in the receiver FIFO and resets its counter. This does not clear the shift register.
- Bit 2: When set, FCR2 clears all bytes in the transmit FIFO and resets the counter. This does not clear the shift register.
- Bit 3: When set, FCR3 changes $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ from mode 0 to mode 1 if FCR0 is set.
- Bits 4 and 5: FCR4 and FCR5 are reserved for future use.
- Bits 6 and 7: FCR6 and FCR7 set the trigger level for the receiver FIFO interrupt (see Table 4).

Table 4. Receiver FIFO Trigger Level

BIT		RECEIVER FIFO TRIGGER LEVEL (BYTES)
7	6	
0	0	01
0	1	04
1	0	08
1	1	14

FIFO interrupt mode operation

The following receiver status occurs when the receiver FIFO and receiver interrupts are enabled.

1. LSR0 is set when a character is transferred from the shift register to the receiver FIFO. When the FIFO is empty, it is reset.
2. IIR = 06 receiver line status interrupt has higher priority than the receive data available interrupt IIR = 04.
3. Receive data available interrupt is issued to the CPU when the programmed trigger level is reached by the FIFO. As soon as the FIFO drops below its programmed trigger level, it is cleared.
4. IIR = 04 (receive data available indicator) also occurs when the FIFO reaches its trigger level. It is cleared when the FIFO drops below the programmed trigger level.

The following receiver FIFO character time-out status occurs when receiver FIFO and receiver interrupts are enabled.

PRINCIPLES OF OPERATION

FIFO interrupt mode operation (continued)

1. When the following conditions exist, a FIFO character time-out interrupt occurs:
   a. Minimum of one character in FIFO
   b. Last received serial character is longer than four continuous previous character times ago. (If two stop bits are programmed, the second one is included in the time delay.)
   c. The last CPU of the FIFO read is more than four continuous character times earlier. At 300 baud and 12-bit characters, the FIFO time-out interrupt causes a latency of 160 ms maximum from received character to interrupt issued.
2. By using the XTAL1 input for a clock signal, the character times can be calculated. The delay is proportional to the baud rate.
3. The time-out timer is reset after the CPU reads the receiver FIFO or after a new character is received. This occurs when there has been no time-out interrupt.
4. A time-out interrupt is cleared and the timer is reset when the CPU reads a character from the receiver FIFO.

Transmit interrupts occurs as follows when the transmitter and transmit FIFO interrupts are enabled (FCR0 =1, IER1 = 1).

1. When the transmitter FIFO is empty, the transmitter holding register interrupt (IIR = 02) occurs. The interrupt is cleared when the transmitter holding register is written to or the IIR is read. One to sixteen characters can be written to the transmit FIFO when servicing this interrupt.
2. The transmitter FIFO empty indicators are delayed one character time minus the last stop bit time whenever the following occurs:

   THRE = 1, and there has not been a minimum of two bytes at the same time in transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 is immediate, however, assuming it is enabled.

Receiver FIFO trigger level and character time-out interrupts have the same priority as the receive data available interrupt. The transmitter holding register empty interrupt has the same priority as the transmitter FIFO empty interrupt.

FIFO polled mode operation

Clearing IER0, IER1, IER2, IER3, or all to zero with FCR0 = 1 puts the ACE into the FIFO polled mode. receiver and transmitter are controlled separately. Either or both can be in the polled mode.

In the FIFO polled mode, there is no time-out condition indicated or trigger level reached. However, the Receiver and transmit FIFOs still have the capability of holding characters. The LSR must be read to determine the ACE status.

interrupt enable register (IER)

The IER independently enables the four serial channel interrupt sources that activate the interrupt (INTA, B, C, D) output. All interrupts are disabled by clearing IER0 − IER3 of the IER. Interrupts are enabled by setting the appropriate bits of the IER. Disabling the interrupt system inhibits the IIR and the active (high) interrupt output. All other system functions operate in their normal manner, including the setting of the LSR and MSR. The contents of the IER are shown in Table 3 and described in the following bulleted list:

PRINCIPLES OF OPERATION

interrupt enable register (IER) (continued)

- Bit 0: When IER0 is set, IER0 enables the received data available interrupt and the timeout interrupts in the FIFO mode.
- Bit 1: When IER1 is set, the transmitter holding register empty interrupt is enabled.
- Bit 2: When IER2 is set, the receiver line status interrupt is enabled.
- Bit 3: When IER3 is set, the modem status interrupt is enabled.
- Bits 4 − 7: IER4 − IER7. These four bits of the IER are cleared.

interrupt identification register (IIR)

In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

- Priority 1 − Receiver line status (highest priority)
- Priority 2 − Receiver data ready or receiver character timeout
- Priority 3 − Transmitter holding register empty
- Priority 4 − Modem status (lowest priority)

Information indicating that a prioritized interrupt is pending and the type of interrupt that is stored in the IIR. The IIR indicates the highest priority interrupt pending. The contents of the IIR are indicated in Table 5.

Table 5. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER				INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	—	None	None	—
0	1	1	0	First	Receiver line status	OE, PE, FE, or BI	LSR read
0	1	0	0	Second	Received data available	Receiver data available or trigger level reached	RBR read until FIFO drops below the trigger level
1	1	0	0	Second	Character time-out indicator	No characters have been removed from or input to the receiver FIFO during the last four character times, and there is at least one character in it during this time.	RBR read
0	0	1	0	Third	THRE	THRE	IIR read if THRE is the interrupt source or THR write
0	0	0	0	Fourth	Modem status	$\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{RI}}$, or $\overline{\text{DCD}}$	

PRINCIPLES OF OPERATION

interrupt identification register (IIR) (continued)

- Bit 0: IIR0 indicates whether an interrupt is pending. When IIR0 is cleared, an interrupt is pending.
- Bits 1 and 2: IIR1 and IIR2 identify the highest priority interrupt pending as indicated in Table 5.
- Bit 3: IIR3 is always cleared when in the TL16C450 mode. This bit is set along with bit 2 when in the FIFO mode and a trigger change level interrupt is pending.
- Bits 4 and 5: IIR4 and IIR5 are always cleared.
- Bits 6 and 7: IIR6 and IIR7 are set when FCR0 = 1.

line control register (LCR)

The format of the data character is controlled by the LCR. The LCR may be read. Its contents are described in the following bulleted list and shown in Figure 15.

- Bits 0 and 1: LCR0 and LCR1 are word length select bits. These bits program the number of bits in each serial character and are shown in Figure 15.
- Bit 2: LCR2 is the stop bit select bit. This bit specifies the number of stop bits in each transmitted character. The receiver always checks for one stop bit.
- Bit 3: LCR3 is the parity enable bit. When LCR3 is set, a parity bit between the last data word bit and stop bit is generated and checked.
- Bit 4: LCR4 is the even parity select bit. When this bit is set and parity is enabled (LCR3 is set), even parity is selected. When this bit is cleared and parity is enabled, odd parity is selected.
- Bit 5: LCR5 is the stick parity bit. When parity is enabled (LCR3 is set) and this bit is set, the transmission and reception of a parity bit is placed in the opposite state from the value of LCR4. This forces parity to a known state and allows the receiver to check the parity bit in a known state.
- Bit 6: LCR6 is a break control bit. When this bit is set, the serial outputs TXx are forced to the spacing state (low). The break control bit acts only on the serial output and does not affect the transmitter logic. If the following sequence is used, no invalid characters are transmitted because of the break.

  Step 1. Load a zero byte in response to the transmitter holding register empty (THRE) status indicator.

  Step 2. Set the break in response to the next THRE status indicator.

  Step 3. Wait for the transmitter to be idle when transmitter empty status signal is set (TEMT = 1); then clear the break when the normal transmission has to be restored.
- Bit 7: LCR7 is the divisor latch access bit (DLAB) bit. This bit must be set to access the divisor latches DLL and DLM of the baud rate generator during a read or write operation. LCR7 must be cleared to access the receiver buffer register, the transmitter holding register, or the interrupt enable register.

PRINCIPLES OF OPERATION

line control register (LCR) (continued)

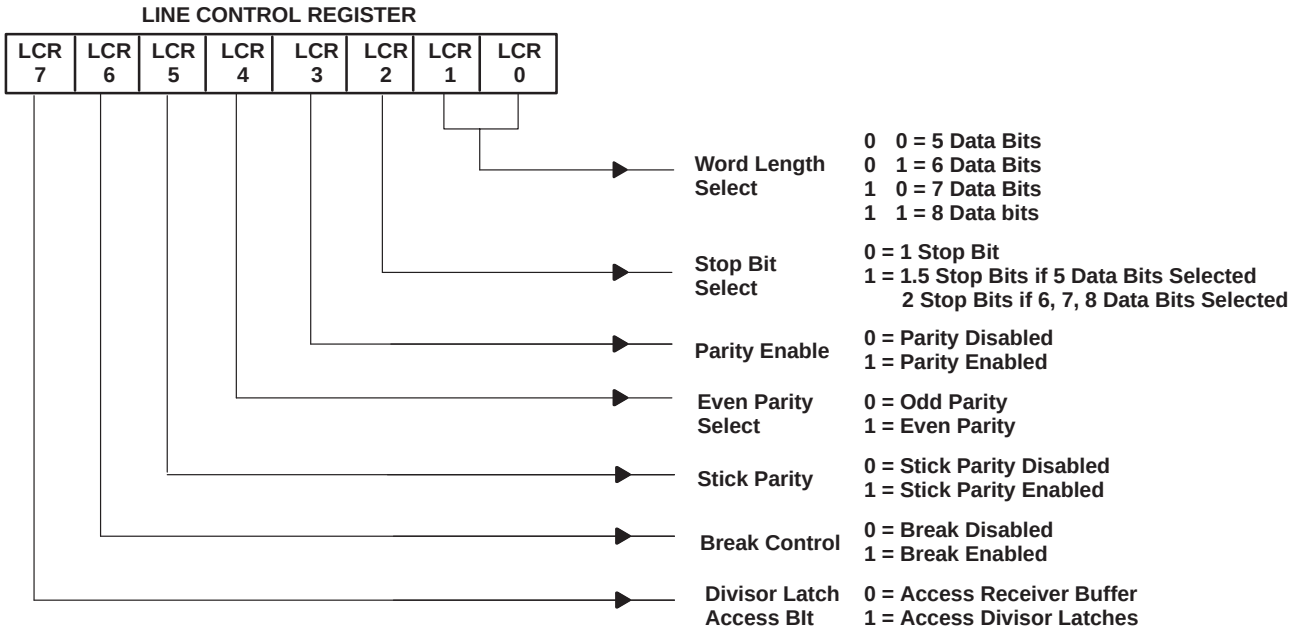


Figure 15. Line Control Register Contents

line status register (LSR)

The LSR is a single register that provides status indicators. The LSR shown in Table 6 is described in the following bulleted list:

- Bit 0: LSR0 is the data ready (DR) bit. Data ready is set when an incoming character is received and transferred into the receiver buffer register or the FIFO. LSR0 is cleared by a CPU read of the data in the receiver buffer register or the FIFO.
- Bit 1: LSR1 is the overrun error (OE) bit. An overrun error indicates that data in the receiver buffer register is not read by the CPU before the next character is transferred into the receiver buffer register overwriting the previous character. The OE indicator is cleared whenever the CPU reads the contents of the LSR. An overrun error occurs in the FIFO mode after the FIFO is full and the next character is completely received. The overrun error is detected by the CPU on the first LSR read after it happens. The character in the shift register is not transferred to the FIFO, but it is overwritten.
- Bit 2: LSR2 is the parity error (PE) bit. A parity error indicates that the received data character does not have the correct parity as selected by LCR3 and LCR4. The PE bit is set upon detection of a parity error and is cleared when the CPU reads the contents of the LSR. In the FIFO mode, the parity error is associated with a particular character in the FIFO. LSR2 reflects the error when the character is at the top of the FIFO.
- Bit 3: LSR3 is the framing error (FE) bit. A framing error indicates that the received character does not have a valid stop bit. LSR3 is set when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is cleared when the CPU reads the contents of the LSR. In the FIFO mode, the framing error is associated with a particular character in the FIFO. LSR3 reflects the error when the character is at the top of the FIFO.

PRINCIPLES OF OPERATION

line status register (LSR) (continued)

- Bit 4: LSR4 is the break interrupt (BI) bit. Break interrupt is set when the received data input is held in the spacing (low) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is cleared when the CPU reads the contents of the LSR. In the FIFO mode, this is associated with a particular character in the FIFO. LSR2 reflects the BI when the break character is at the top of the FIFO. The error is detected by the CPU when its associated character is at the top of the FIFO during the first LSR read. Only one zero character is loaded into the FIFO when BI occurs.

LSR1 − LSR4 are the error conditions that produce a receiver line status interrupt (priority 1 interrupt in the interrupt identification register) when any of the conditions are detected. This interrupt is enabled by setting IER2 in the interrupt enable register.

- Bit 5: LSR5 is the transmitter holding register empty (THRE) bit. THRE indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set when a character is transferred from the transmitter holding register (THR) into the transmitter shift register (TSR). LSR5 is cleared by the loading of the THR by the CPU. LSR5 is not cleared by a CPU read of the LSR. In the FIFO mode, when the transmit FIFO is empty, this bit is set. It is cleared when one byte is written to the transmit FIFO. When the THRE interrupt is enabled by IER1, THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.
- Bit 6: LSR6 is the transmitter register empty (TEMT) bit. TEMT is set when the THR and the TSR are both empty. LSR6 is cleared when a character is loaded into THR and remains low until the character is transferred out of TXx. TEMT is not cleared by a CPU read of the LSR. In the FIFO mode, when both the transmitter FIFO and shift register are empty, this bit is set.
- Bit 7: LSR7 is the receiver FIFO error bit. The LSR7 bit is cleared in the TL16C450 mode (see FCR bit 0). In the FIFO mode, it is set when at least one of the following data errors is in the FIFO: parity error, framing error, or break interrupt indicator. It is cleared when the CPU reads the LSR if there are no subsequent errors in the FIFO.

NOTE

The LSR may be written. However, this function is intended only for factory test. It should be considered as read only by applications software.

Table 6. Line Status Register BIts

LSR BITS	1	0
LSR0 data ready (DR)	Ready	Not ready
LSR1 overrun error (OE)	Error	No error
LSR2 parity error (PE)	Error	No error
LSR3 framing error (FE)	Error	No error
LSR4 break interrupt (BI)	Break	No break
LSR5 transmitter holding register empty (THRE)	Empty	Not empty
LSR6 transmitter register empty (TEMT)	Empty	Not empty
LSR7 receiver FIFO error	Error in FIFO	No error in FIFO

PRINCIPLES OF OPERATION

modem control register (MCR)

The MCR controls the interface with the modem or data set as described in Figure 16. MCR can be written and read. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their control bits in this register. A high input asserts a low signal (active) at the output terminals. MCR bits 0, 1, 2, 3, and 4 are shown as follows:

- Bit 0: When MCR0 is set, the $\overline{DTR}$ output is forced low. When MCR0 is cleared, the $\overline{DTR}$ output is forced high. The $\overline{DTR}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.
- Bit1: When MCR1 is set, the $\overline{RTS}$ output is forced low. When MCR1 is cleared, the $\overline{RTS}$ output is forced high. The $\overline{RTS}$ output of the serial channel may be input into an inverting line driver to obtain the proper polarity input at the modem or data set.
- Bit 2: MCR2 has no affect on operation.
- Bit 3: When MCR3 is set, the external serial channel interrupt is enabled.
- Bit 4: MCR4 provides a local loopback feature for diagnostic testing of the channel. When MCR4 is set, serial output TXx is set to the marking (high) state and SIN is disconnected. The output of the TSR is looped back into the RSR input. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected. The modem control outputs ($\overline{DTR}$ and $\overline{RTS}$) are internally connected to the four modem control inputs. The modem control output terminals are forced to their inactive (high) state on the TL16C554. In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Interrupt control is fully operational; however, interrupts are generated by controlling the lower four MCR bits internally. Interrupts are not generated by activity on the external terminals represented by those four bits.
- Bit 5 − Bit 7: MCR5, MCR6, and MCR7 are permanently cleared.

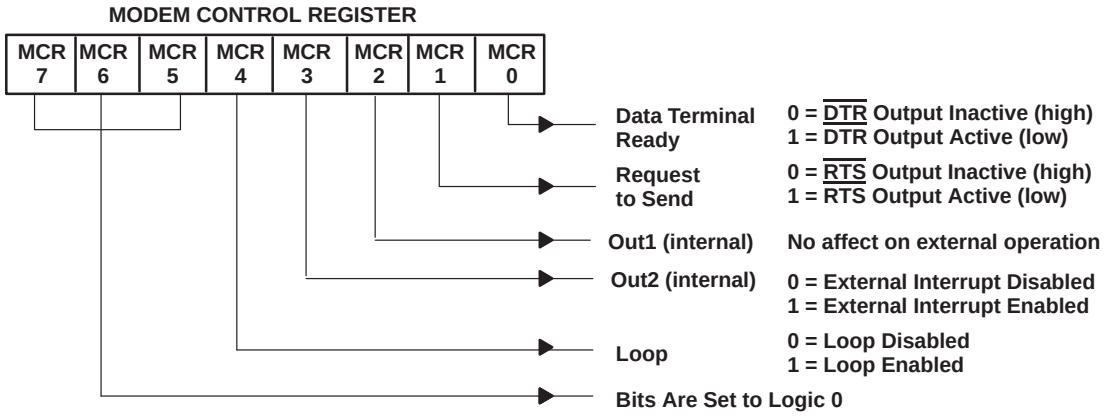


Figure 16. Modem Control Register Contents

PRINCIPLES OF OPERATION

modem status register (MSR)

The MSR provides the CPU with status of the modem input lines for the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the ACE. It also reads the current status of four bits of the MSR that indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set when a control input from the modem changes states and are cleared when the CPU reads the MSR.

The modem input lines are $\overline{\text{CTS}}$, DSR, and $\overline{\text{DCD}}$. MSR4 − MSR7 are status indicators of these lines. A status bit = 1 indicates the input is low. When the status bit is cleared, the input is high. When the modem status interrupt in the IER is enabled (IIR3 is set), an interrupt is generated whenever MSR0 − MSR3 is set. The MSR is a priority 4 interrupt. The contents of the MSR are described in Table 7.

- Bit 0: MSR0 is the delta clear-to-send (ΔCTS) bit. DCTS indicates that the $\overline{\text{CTS}}$ input to the serial channel has changed state since it was last read by the CPU.
- Bit 1: MSR1 is the delta data set ready (ΔDSR) bit. ΔDSR indicates that the $\overline{\text{DSR}}$ input to the serial channel has changed states since the last time it was read by the CPU.
- Bit 2: MSR2 is the trailing edge of ring indicator (TERI) bit. TERI indicates that the $\overline{\text{RIx}}$ input to the serial channel has changed states from low to high since the last time it was read by the CPU. High-to-low transitions on RI do not activate TERI.
- Bit 3: MSR3 is the delta data carrier detect (ΔDCD) bit. ΔDCD indicates that the $\overline{\text{DCD}}$ input to the serial channel has changed states since the last time it was read by the CPU.
- Bit 4: MSR4 is the clear-to-send (CTS) bit. CTS is the complement of the $\overline{\text{CTS}}$ input from the modem indicating to the serial channel that the modem is ready to receive data from SOUT. When the serial channel is in the loop mode (MCR4 = 1), MSR4 reflects the value of RTS in the MCR.
- Bit 5: MSR5 is the data set ready DSR bit. DSR is the complement of the $\overline{\text{DSR}}$ input from the modem to the serial channel that indicates that the modem is ready to provide received data from the serial channel receiver circuitry. When the channel is in the loop mode (MCR4 is set), MSR5 reflects the value of DTR in the MCR.
- Bit 6: MSR6 is the ring indicator (RI) bit. RI is the complement of the $\overline{\text{RIx}}$ inputs. When the channel is in the loop mode (MCR4 is set), MSR6 reflects the value of $\overline{\text{OUT1}}$ in the MCR.
- Bit 7: MSR7 is the data carrier detect (DCD) bit. Data carrier detect indicates the status of the data carrier detect ($\overline{\text{DCD}}$) input. When the channel is in the loop mode (MCR4 is set), MSR7 reflects the value of OUT2 in the MCR.

Reading the MSR clears the delta modem status indicators but has no affect on the other status bits. For LSR and MSR, the setting of status bits is inhibited during status register read operations. If a status condition is generated during a read $\overline{\text{IOR}}$ operation, the status bit is not set until the trailing edge of the read. When a status bit is set during a read operation and the same status condition occurs, that status bit is cleared at the trailing edge of the read instead of being set again. In the loopback mode when modem status interrupts are enabled, $\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{RI}}$, and $\overline{\text{DCD}}$ inputs are ignored; however, a modem status interrupt can still be generated by writing to MCR3−MCR0. Applications software should not write to the MSR.

PRINCIPLES OF OPERATION

modem status register (MSR) (continued)

Table 7. Modem Status Register BIts

MSR BIT	MNEMONIC	DESCRIPTION
MSR0	ΔCTS	Delta clear to send
MSR1	ΔDSR	Delta data set ready
MSR2	TERI	Trailing edge of ring indicator
MSR3	ΔDCD	Delta data carrier detect
MSR4	CTS	Clear to send
MSR5	DSR	Data set ready
MSR6	RI	Ring indicator
MSR7	DCD	Data carrier detect

programming

The serial channel of the ACE is programmed by the control registers LCR, IER, DLL, DLM, MCR, and FCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control registers can be written in any order, the IER should be written last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the ACE serial channel is not transmitting or receiving data.

programmable baud rate generator

The ACE serial channel contains a programmable baud rate generator (BRG) that divides the clock (dc to 8 MHz) by any divisor from 1 to ($2^{16}-1$). Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These divisor latch registers must be loaded during initialization. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 3.072 MHz, and 8 MHz. With these frequencies, standard bit rates from 50 kbps to 512 kbps are available. Tables 8, 9, 10, and 11 illustrate the divisors needed to obtain standard rates using these three frequencies. The output frequency of the baud rate generator is 16× the data rate [divisor # = clock + (baud rate × 16)] referred to in this document as RCLK.

PRINCIPLES OF OPERATION

programmable baud rate generator (continued)

Table 8. Baud Rates Using an 1.8432-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.690
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.860

Table 9. Baud Rates Using an 3.072-MHz Crystal

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	0.312
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.230
9600	20	—
19200	10	—
38400	5	—

PRINCIPLES OF OPERATION

programmable baud rate generator (continued)

Table 10. Baud Rates Using an 8-MHz Clock

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	10000	—
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	333	0.010
300	1667	0.020
600	883	0.040
1200	417	0.080
1800	277	0.080
2000	250	—
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.400

PRINCIPLES OF OPERATION

programmable baud rate generator (continued)

Table 11. Baud Rates Using an 16-MHz Clock

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	20000	0
75	13334	0.00
110	9090	0.01
134.5	7434	0.01
150	6666	0.01
300	3334	−0.02
600	1666	0.04
1200	834	−0.08
1800	554	0.28
2000	500	0.00
2400	416	0.16
3600	278	−0.08
4800	208	0.16
7200	138	0.64
9600	104	0.16
19200	52	0.16
38400	26	0.16
56000	18	−0.79
128000	8	−2.34
256000	4	−2.34
512000	2	−2.34
1000000	1	0.00

receiver

Serial asynchronous data is input into the RXx terminal. The ACE continually searches for a high-to-low transition from the idle state. When the transition is detected, a counter is reset and counts the 16× clock to 7 1/2, which is the center of the start bit. The start bit is valid when the RXx is still low. Verifying the start bits prevents the receiver from assembling a false data character due to a low going noise spike on the RXx input.

The LCR determines the number of data bits in a character (LCR0, LCR1). When parity is enabled, LCR3 and the polarity of parity LCR4 are needed. Status for the receiver is provided in the LSR. When a full character is received including parity and stop bits, the data received indicator in LSR0 is set. The CPU reads the RBR, which clears LSR0. If the character is not read prior to a new character transfer from the RSR to the RBR, the overrun error status indicator is set in LSR1. If there is a parity error, the parity error is set in LSR2. If a stop bit is not detected, a framing error indicator is set in LSR3.

In the FIFO mode operation, the data character and the associated error bits are stored in the receiver FIFO. If the data into RXx is a symmetrical square wave, the center of the data cells occurs within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16× clock cycle prior to being detected.

PRINCIPLES OF OPERATION

reset

After power up, the ACE RESET input should be held high for one microsecond to reset the ACE circuits to an idle mode until initialization. A high on RESET causes the following:

1. It initializes the transmitter and receiver internal clock counters.
2. It clears the LSR, except for transmitter register empty (TEMT) and transmit holding register empty (THRE), which are set. The MCR is also cleared. All of the discrete lines, memory elements, and miscellaneous logic associated with these register bits are also cleared or turned off. The LCR, divisor latches, RBR, and transmitter buffer register are not affected.

$\overline{\text{RXRDY}}$ operation

In mode 0, $\overline{\text{RXRDY}}$ is asserted (low) when the receive FIFO is not empty; it is released (high) when the FIFO is empty. In this way, the receiver FIFO is read when $\overline{\text{RXRDY}}$ is asserted (low).

In mode 1, $\overline{\text{RXRDY}}$ is asserted (low) when the receive FIFO has filled to the trigger level or a character time-out has occurred (four character times with no transmission of characters); it is released (high) when the FIFO is empty. In this mode, multiple received characters are read by the DMA device, reducing the number of times it is interrupted.

$\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ outputs from each of the four internal ACEs of the TL16C554 are ANDed together internally. This combined signal is brought out externally to $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$.

Following the removal of the reset condition (RESET low), the ACE remains in the idle mode until programmed. A hardware reset of the ACE sets the THRE and TEMT status bits in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE. A summary of the effect of a reset on the ACE is given in Table 12.

Table 12. RESET Affects on Registers and Signals

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt enable register	Reset	All bits cleared (0−3 forced and 4−7 permanent)
Interrupt identification register	Reset	Bit 0 is set, bits 1, 2, 3, 6, and 7 are cleared, Bits 4−5 are permanently cleared
Line control register	Reset	All bits cleared
Modem control register	Reset	All bits cleared (5−7 permanent)
FIFO control register	Reset	All bits cleared
Line status register	Reset	All bits cleared, except bits 5 and 6 are set
Modem status register	Reset	Bits 0−3 cleared, bits 4−7 input signals
TXx	Reset	High
Interrupt (RCVR ERRS)	Read LSR/Reset	Low
Interrupt (receiver data ready)	Read RBR/Reset	Low
Interrupt (THRE)	Read IIR/Write THR/Reset	Low
Interrupt (modem status changes)	Read MSR/Reset	Low
$\overline{\text{RTS}}$	Reset	High
$\overline{\text{DTR}}$	Reset	High

PRINCIPLES OF OPERATION

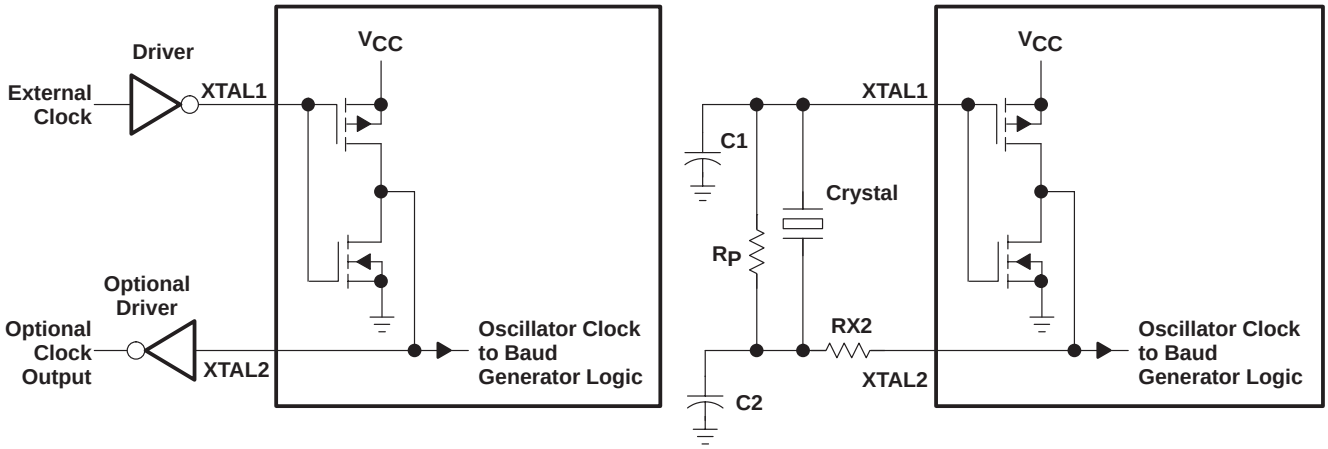
scratchpad register

The scratch register is an 8-bit read/write register that has no affect on either channel in the ACE. It is intended to be used by the programmer to hold data temporarily.

$\overline{\text{TXRDY}}$ operation

In mode 0, $\overline{\text{TXRDY}}$ is asserted (low) when the transmit FIFO is empty; it is released (high) when the FIFO contains at least one byte. In this way, the FIFO is written with 16 bytes when $\overline{\text{TXRDY}}$ is asserted (low).

In mode 1, $\overline{\text{TXRDY}}$ is asserted (low) when the transmit FIFO is not full; in this mode, the transmit FIFO is written with another byte when $\overline{\text{TXRDY}}$ is asserted (low).



TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	R_P	RX2	C1	C2
3.1 MHz	1 MΩ	1.5 kΩ	10−30 pF	40−60 pF
1.8 MHz	1 MΩ	1.5 kΩ	10−30 pF	40−60 pF

Figure 17. Typical Clock Circuits

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL16C554FN	ACTIVE	PLCC	FN	68	18	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TL16C554FN	Samples
TL16C554FNR	ACTIVE	PLCC	FN	68	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TL16C554FN	Samples
TL16C554IFN	ACTIVE	PLCC	FN	68	18	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TL16C554IFN	Samples
TL16C554IFNR	ACTIVE	PLCC	FN	68	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TL16C554IFN	Samples
TL16C554IPN	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TL16C554IPN	Samples
TL16C554PN	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TL16C554PN	Samples
TL16C554PNR	ACTIVE	LQFP	PN	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TL16C554PN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

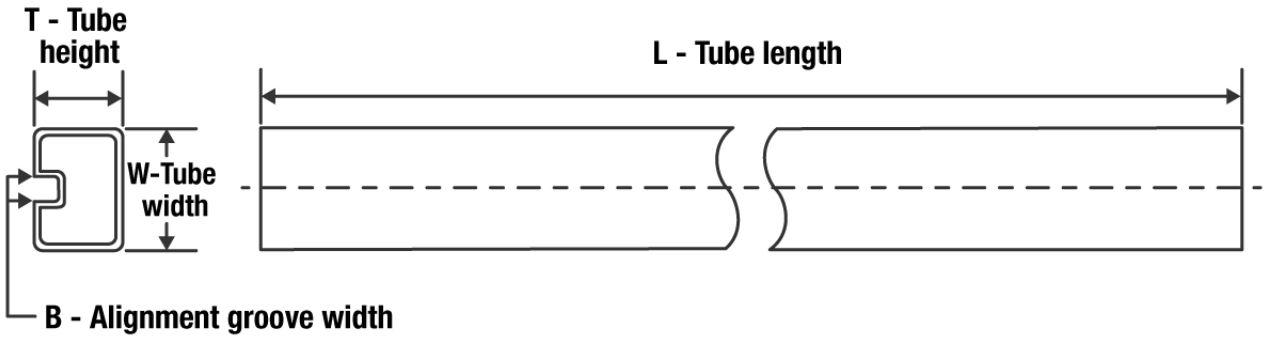
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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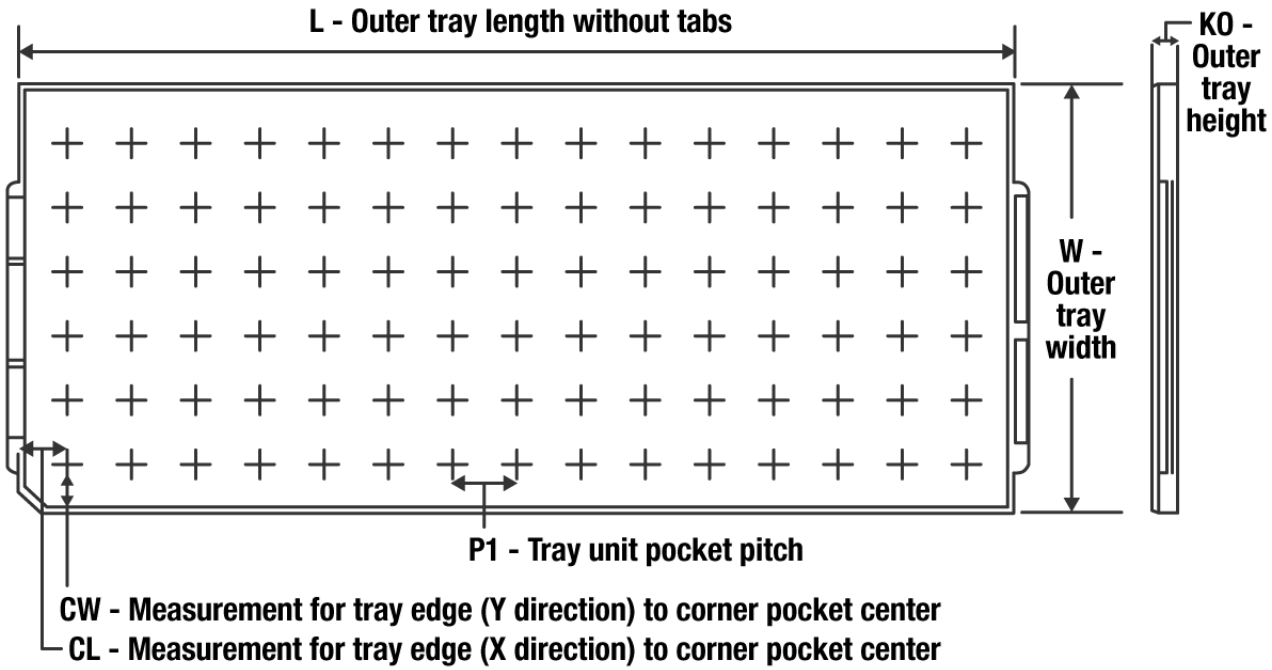
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL16C554FN	FN	PLCC	68	18	506.98	25.91	5330	5.33
TL16C554IFN	FN	PLCC	68	18	506.98	25.91	5330	5.33

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TL16C554IPN	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95
TL16C554PN	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95

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