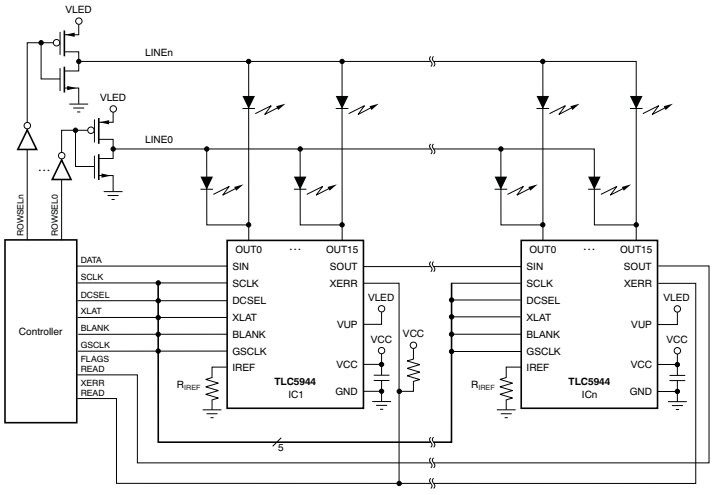
16-Channel, 12-Bit PWM LED Driver with 6-Bit Dot Correction and Pre-Charge FET

FEATURES

- 16 Channels, Constant Current Sink Output
- 60-mA Capability (Constant Current Sink)
- 12-Bit (4096 Steps) Grayscale Control with PWM
- 6-Bit (64 Steps) Dot Correction with Sink Current
- Internal Pre-Charge FET to Prevent LED Ghosting Phenomenon on Multiplexed LED Systems
- LED Power-Supply Voltage up to 15 V
- V_{CC} = 3.0 V to 5.5 V
- Constant Current Accuracy:
  - Channel-to-Channel = ±1%
  - Device-to-Device = ±3%
- CMOS Logic Level I/O
- 30-MHz Data Transfer Rate
- 33-MHz Grayscale Control Clock
- Continuous Base LED Open Detection (LOD):
  - Detect LED opening and LED short to GND during display with auto output off function
- Thermal Shutdown (TSD):
  - Automatic shutdown at over-temperature conditions
  - Restart under normal temperature
- Pre-Thermal Warning (PTW):
  - High temperature operation alert
- Readable Error Information:
  - LED Open Detection (LOD)
  - Thermal Error Flag (TEF)
  - Pre-Thermal Warning (PTW)
- Noise Reduction:
  - 4-channel grouped delay to prevent inrush current
- Operating Temperature: –40°C to +85°C

APPLICATIONS

- Monochrome, Multicolor, Full-Color LED Displays Using Multiplexing System
- LED Signboards Using Multiplexing System



Typical Application Circuit (Multiple Daisy-Chained TLC5944s)

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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DESCRIPTION

The TLC5944 is a 16-channel, constant current sink driver. Each channel is individually adjustable with 4096 pulse-width modulated (PWM) steps and 64 constant sink current (dot correction) steps. The dot correction (DC) adjusts for brightness variations between LEDs. Both grayscale (GS) control and DC are accessible via a common serial interface port. The maximum current value of all 16 channels can be set by a single external resistor.

The TLC5944 has an internal pre-charge FET to prevent the ghost-lighting phenomenon that occurs on multiplexed LED systems. The TLC5944 has three error detection circuits for LED open detection (LOD), a thermal error flag (TEF), and a pre-thermal warning (PTW). The LOD detects a broken or disconnected LED, and a shorted LED to GND during the display period. The TEF indicates a too-high temperature condition; when the TEF is set, all output drivers are turned off by the thermal shutdown (TSD) protection. Additionally, when the TEF is cleared, all output drivers are restarted. The PTW indicates that the IC is operating in a high temperature condition. The output drivers remain on when PTW is set.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLC5944	HTSSOP-28 PowerPAD™	TLC5944PWPR	Tape and Reel, 2000
		TLC5944PWP	Tube, 50
TLC5944	5 mm × 5 mm QFN-32	TLC5944RHBR	Tape and Reel, 3000
		TLC5944RHBT	Tape and Reel, 250

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			TLC5944	UNIT
V_{CC}	Supply voltage, V_{CC}		–0.3 to +6.0	V
V_{UP}	Pre-charge voltage		–0.3 to +16	V
I_{OUT}	Output current (dc)	XERR	6	mA
		OUT0 to OUT15	70	mA
V_{IN}	Input voltage range: SIN, SCLK, XLAT, BLANK, GSCLK, DCSEL, IREF		–0.3 to V_{CC} + 0.3	V
V_{OUT}	Output voltage range	SOUT, XERR	–0.3 to V_{CC} + 0.3	V
		OUT0 to OUT15	–0.3 to V_{UP} + 0.3	V
$T_{J(max)}$	Operating junction temperature		+150	°C
T_{STG}	Storage temperature range		–55 to +150	°C
	ESD rating	Human body model (HBM)	2	kV
		Charged device model (CDM)	500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) All voltage values are with respect to network ground terminal.

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RECOMMENDED OPERATING CONDITIONS

At T_A= –40°C to +85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5944			UNIT
			MIN	NOM	MAX	
DC Characteristics: V_{CC} = 3 V to 5.5 V						
V_{CC}	Supply voltage		3.0		5.5	V
V_{UP}	Pre-charge voltage		3.0		15	V
V_O	Voltage applied to output	OUT0 to OUT15			V_{UP}	V
V_{IH}	High-level input voltage		0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.3 × V_{CC}	V
I_{OH}	High-level output current	SOUT			–1	mA
I_{OL}	Low-level output current	SOUT			1	mA
		XERR			5	mA
I_{OLC}	Constant output sink current	OUT0 to OUT15			60	mA
T_A	Operating free-air temperature		–40		+85	°C
T_J	Operating junction temperature		–40		+125	°C
AC Characteristics: V_{CC} = 3 V to 5.5 V						
$f_{CLK\ (sclk)}$	Data shift clock frequency	SCLK			30	MHz
$f_{CLK\ (gsclk)}$	Grayscale control clock frequency	GSCLK			33	MHz
T_{WH0}/T_{WL0}	Pulse duration	SCLK, GSCLK	10			ns
T_{WH1}		XLAT, BLANK	15			ns
T_{SU0}	Setup time	SIN–SCLK↑	5			ns
T_{SU1}		BLANK↓–GSCLK↑	15			ns
T_{SU2}		XLAT↑–SCLK↑	100			ns
T_{SU3}		XLAT↓–SCLK↑ (for SID reading only)	20			ns
T_{SU4}		DCSEL–SCLK↑	10			ns
T_{SU5}		DCSEL–XLAT↑	10			ns
T_{H0}	Hold time	SIN–SCLK↑	3			ns
T_{H1}		XLAT↑–SCLK↑	10			ns
T_{H2}		DCSEL–SCLK↓	10			ns
T_{H3}		DCSEL–XLAT↑	100			ns

DISSIPATION RATINGS

PACKAGE	OPERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
HTSSOP-28 with PowerPAD soldered (1)	31.67 mW/°C	3958 mW	2533 mW	2058 mW
HTSSOP-28 with PowerPAD not soldered (2)	16.21 mW/°C	2026 mW	1296 mW	1053 mW
QFN-32 (3)	27.86 mW/°C	3482 mW	2228 mW	1811 mW

(1) With PowerPAD soldered onto copper area on printed circuit board (PCB); 2-oz. copper. For more information, see SLMA002 (available for download at www.ti.com).
(2) With PowerPAD not soldered onto copper area on PCB.
(3) The package thermal impedance is calculated in accordance with JESD51-5.

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ELECTRICAL CHARACTERISTICS

At V_{CC} = 3.0 V to 5.5 V and T_A = –40°C to +85°C. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5944			UNIT
			MIN	TYP	MAX	
V_{OH}	High-level output voltage	I_{OH} = –1 mA at SOUT	V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA at SOUT	0		0.4	V
		I_{OL} = 5 mA at XERR	0		0.4	V
I_{IN}	Input current	V_{IN} = V_{CC} or GND at SIN, SCLK, XLAT, GSCLK, BLANK, DCSEL	–1		1	µA
I_{CC1}	Supply current (V_{CC})	SIN/SCLK/GSCLK/XLAT/DCSEL = low, BLANK = high, DCn = 3Fh, V_{OUTn} = 1 V, R_{IREF} = 24 kΩ		1	2	mA
I_{CC2}		SIN/SCLK/GSCLK/XLAT/DCSEL = low, BLANK = high, DCn = 3Fh, V_{OUTn} = 1 V, R_{IREF} = 1.6 kΩ		5	10	mA
I_{CC3}		SCLK = 30 MHz, GSCLK = 33 MHz, SIN = 15 MHz, XLAT/DCSEL = low, BLANK = low during 4095 GSCLK period and high during 1 GSCLK period, GSn = FFFh, DCn = 3Fh, V_{OUTn} = 1 V, R_{IREF} = 1.6 kΩ		17	35	mA
I_{CC4}		SCLK = 30 MHz, GSCLK = 33 MHz, SIN = 15 MHz, XLAT/DCSEL = low, BLANK = low during 4095 GSCLK period and high during 1 GSCLK period, GSn = FFFh, DCn = 3Fh, V_{OUTn} = 1 V, R_{IREF} = 820 Ω		30	60	mA
$I_{O(LC)}$	Constant output current	All OUTn = ON, DCn = 3Fh, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1 kΩ (see Figure 9), at OUT0 to OUT15	54	60	66	mA
$I_{O(LKG)}$	Leakage output current	All OUTn for constant current driver, all output off, BLANK = high, V_{OUTn} = V_{OUTfix} = 15 V, V_{UP} = 15 V, R_{IREF} = 820 Ω (see Figure 10), at OUT0 to OUT15			0.1	µA
$I_{O(LKG1)}$		All OUTn for pre-charge FET, all output off, BLANK = low, V_{OUTn} = V_{OUTfix} = 0 V, V_{UP} = 15 V, R_{IREF} = 820 Ω (see Figure 10), at OUT0 to OUT15			–10	µA
$I_{O(LKG2)}$		XERR, no error status, V_{OUTn} = 5.5 V			1	µA
$\Delta I_{O(LC)}$	Constant current error (channel-to-channel)(1)	All OUTn = ON, DCn = 3Fh, V_{OUTn} = 1 V, R_{IREF} = 820 Ω, at OUT0 to OUT15		±1	±3	%
$\Delta I_{O(LC1)}$	Constant current error (device-to-device)(2)	All OUTn = ON, DCn = 3Fh, V_{OUTn} = 1 V, R_{IREF} = 820 Ω, at OUT0 to OUT15		±3	±6	%
$\Delta I_{O(LC2)}$	Line regulation(3)	All OUTn = ON, DCn = 3Fh, V_{OUTn} = 1 V, R_{IREF} = 820 Ω, at OUT0 to OUT15		±0.5	±1	%/V

(1) The deviation of each output from the average of OUT0–OUT15 constant current. Deviation is calculated by the formula:

$$\Delta\ (\%) = \left(\frac{I_{OUTn}}{\frac{(I_{OUT0} + I_{OUT1} + \ldots + I_{OUT14} + I_{OUT15})}{16}} - 1 \right) \times 100$$

(2) The deviation of the OUT0–OUT15 constant current average from the ideal constant current value. Deviation is calculated by the following formula:

$$\Delta\ (\%) = \left(\frac{\frac{(I_{OUT0} + I_{OUT1} + \ldots I_{OUT14} + I_{OUT15})}{16} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is calculated by the formula:

$$I_{OUT(IDEAL)} = 40.5 \times \left(\frac{1.20}{R_{IREF}} \right)$$

(3) Line regulation is calculated by this equation:

$$\Delta\ (\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{CC} = 5.5\ V) - (I_{OUTn} \text{ at } V_{CC} = 3.0\ V)}{(I_{OUTn} \text{ at } V_{CC} = 3.0\ V)} \right) \times \frac{100}{5.5\ V - 3\ V}$$

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ELECTRICAL CHARACTERISTICS (continued)

At V_{CC} = 3.0 V to 5.5 V and T_A = –40°C to +85°C. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5944			UNIT
			MIN	TYP	MAX	
$\Delta I_{O(LC3)}$	Load regulation(4)	All OUTn = ON, DCn = 3Fh, V_{OUTn} = 1 V to 3 V, R_{IREF} = 820 Ω, at OUT0 to OUT15		±1	±3	%/V
R_{PCHG}	Pre-charge FET on-resistance	V_{UP} = 3 V, V_{OUTn} = 1 V, BLANK = high, OUT0 to OUT15		1	3	kΩ
$T_{(TEF)}$	Thermal error flag threshold	Junction temperature(5)	+150	+162	+175	°C
$T_{(HYST)}$	Thermal error flag hysteresis	Junction temperature(5)	+5	+10	+20	°C
$T_{(PTW)}$	Pre-thermal warning threshold	Junction temperature(5)	+105	+120	+135	°C
$T_{(HYSP)}$	Pre-thermal warning hysteresis	Junction temperature(5)	+5	+10	+20	°C
V_{LOD}	LED open detection threshold	All OUTn = ON	0.2	0.3	0.4	V
V_{IREF}	Reference voltage output	R_{IREF} = 820 Ω	1.16	1.20	1.24	V

(4) Load regulation is calculated by the equation:

$$\Delta\ (\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3\ V) - (I_{OUTn} \text{ at } V_{OUTn} = 1\ V)}{(I_{OUTn} \text{ at } V_{OUTn} = 1\ V)} \right) \times \frac{100}{3\ V - 1\ V}$$

(5) Not tested. Specified by design.

SWITCHING CHARACTERISTICS

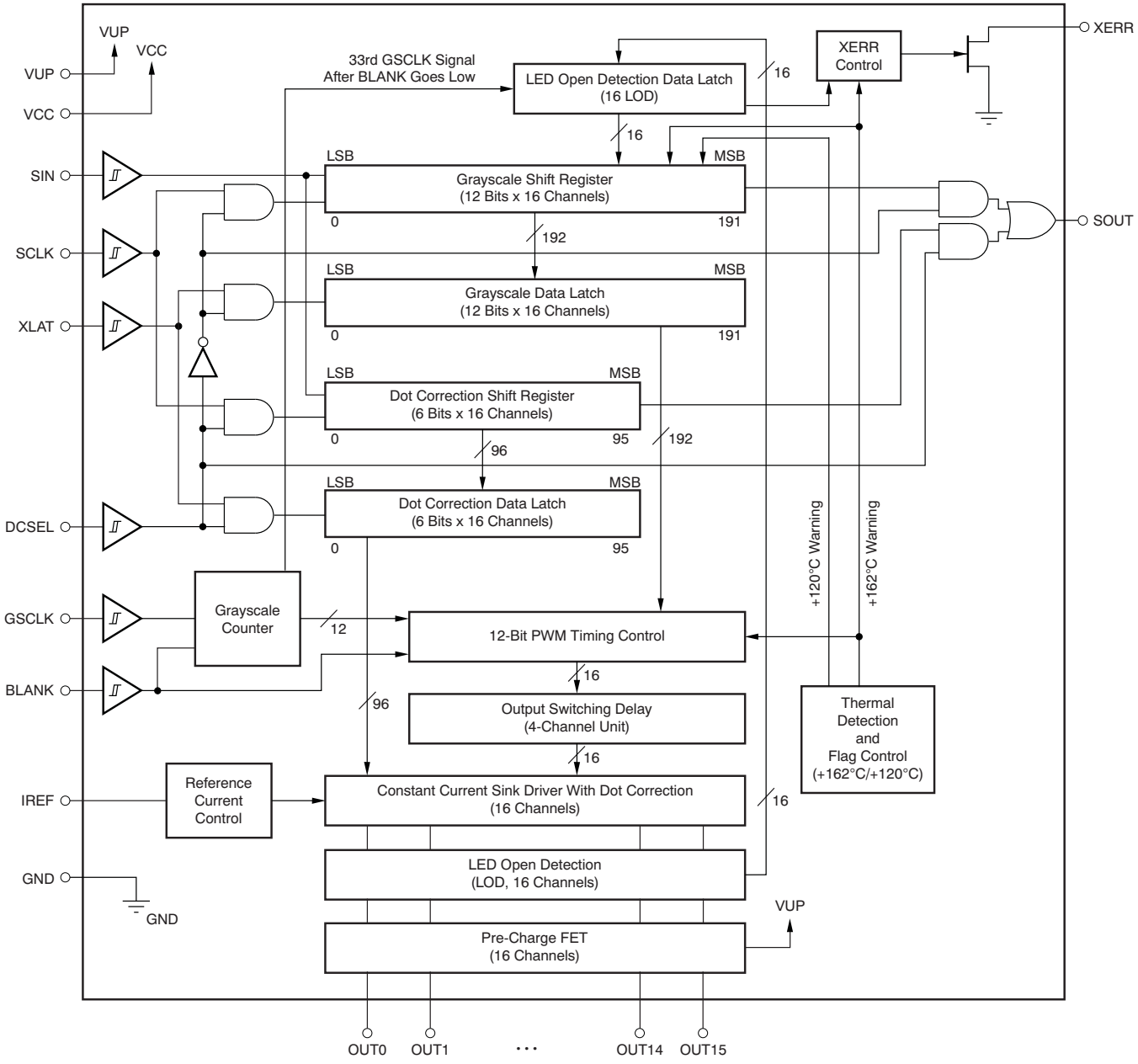
At V_{CC} = 3.0 V to 5.5 V, T_A = –40°C to +85°C, C_L = 15 pF, R_L = 68 Ω, R_{IREF} = 820 Ω, V_{LED} = 5.0 V, and V_{UP} = 5.0 V. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5944			UNIT
			MIN	TYP	MAX	
t_{R0}	Rise time	SOUT (see Figure 6)			16	ns
t_{R1}		OUTn, DCn = 3Fh (see Figure 5)		10	30	
t_{F0}	Fall time	SOUT (see Figure 6)			16	ns
t_{F1}		OUTn, DCn = 3Fh (see Figure 5)		10	30	
t_{F2}		XERR, $C_{L\ XERR}$ = 100 pF, $R_{L\ XERR}$ = 1 kΩ, V_{XERR} = 5 V (see Figure 7)			50	ns
t_{D0}	Propagation delay time	SCLK↑ to SOUT			25	ns
t_{D1}		DCSEL to SOUT			25	ns
t_{D2}		BLANK↑ to OUT0 sink current off		20	40	ns
t_{D3}		GSCLK↑ to OUT0/4/8/12	5	18	40	ns
t_{D4}		GSCLK↑ to OUT1/5/9/13	20	42	73	ns
t_{D5}		GSCLK↑ to OUT2/6/10/14	35	66	106	ns
t_{D6}		GSCLK↑ to OUT3/7/11/15	50	90	140	ns
t_{D7}		XLAT↑ to IOUT (dot correction)			50	ns
t_{D8}		BLANK↑ to pre-charge FET on, $R_{L\ PRE}$ = 10 kΩ, constant current driver off (see Figure 8)	10	35	130	ns
t_{ON_ERR}	Output on-time error(1)	GSn = 001h, GSCLK = 33 MHz	–20		10	ns

(1) Output on-time error is calculated by the following formula: T_{ON_ERR} (ns) = t_{OUTON} – T_{GSCLK}. t_{OUTON} is the actual on-time of the constant current driver. T_{GSCLK} is the period of GSCLK.

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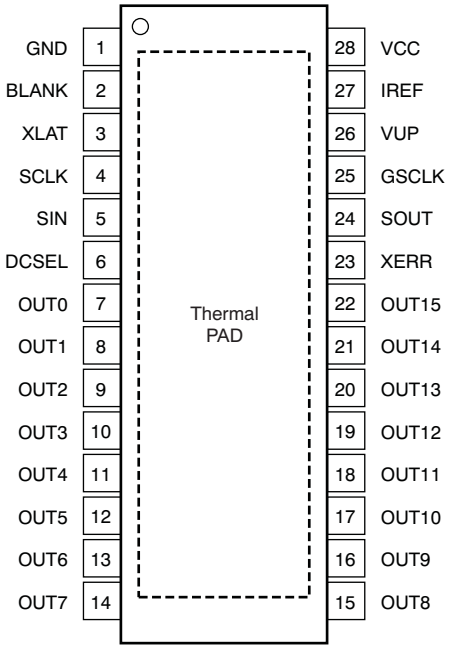
FUNCTIONAL BLOCK DIAGRAM



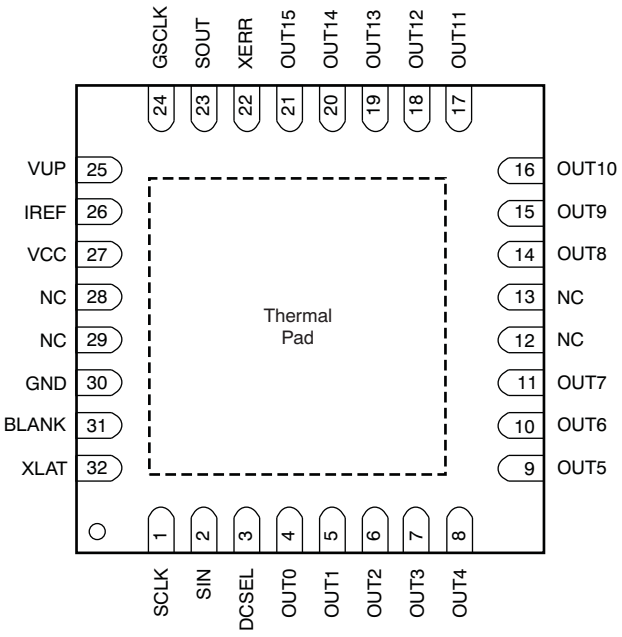
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DEVICE INFORMATION

PWP PACKAGE
HTSSOP-28 PowerPAD
(TOP VIEW)



RHB PACKAGE
5mm × 5mm QFN-32
(TOP VIEW)



NC = No internal connection.

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	PWP	RHB		
SIN	5	2	I	Serial data input for grayscale and dot correction.
SCLK	4	1	I	Serial data shift clock for GS shift register and DC shift register. Schmitt buffer input. The shift register is selected by the DCSEL pin. Data present on the SIN pin are shifted into the shift register selected by DCSEL with the rising edge of the SCLK pin. Data in the selected shift register are shifted to the MSB side by 1-bit synchronizing to the rising edge of SCLK. The MSB data of the selected register appears on SOUT.
XLAT	3	32	I	Data in the GS and DC shift register are moved to the respective data latch with a low-to-high transition of this pin.
DCSEL	6	3	I	Shift register and data latch select. When DCSEL is low, SCLK/XLAT/SOUT are connected to the GS shift register and data latch. When DCSEL is high, SCLK/XLAT/SOUT are connected to the DC shift register and data latch. DCSEL should not be changed while SCLK is high.
GSCLK	25	24	I	Reference clock for grayscale PWM control. If BLANK is low, then each rising edge of GSCLK increments the grayscale counter for PWM control.
BLANK	2	31	I	Blank (all constant current outputs off). When BLANK is high, all constant current outputs (OUT0 through OUT15) are forced off, the grayscale counter is reset to '0', and the grayscale PWM timing controller is initialized. When BLANK is low, all constant current outputs are controlled by the grayscale PWM timing controller.
IREF	27	26	I/O	Constant current value setting. OUT0 through OUT15 sink constant current is set to the desired value by connecting an external resistor between IREF and GND.
SOUT	24	23	O	Serial data output for GS, DC, and status information data (SID). This output is connected to the MSB of the shift register selected by DCSEL.
XERR	23	22	O	Error output. Open-drain output. XERR goes low when LOD or TEF are set. XERR is in high impedance when error free.
OUT0	7	4	O	Constant current output. Each output can be tied to other outputs to increase the constant current.
OUT1	8	5	O	Constant current output
OUT2	9	6	O	Constant current output
OUT3	10	7	O	Constant current output
OUT4	11	8	O	Constant current output
OUT5	12	9	O	Constant current output
OUT6	13	10	O	Constant current output
OUT7	14	11	O	Constant current output
OUT8	15	14	O	Constant current output
OUT9	16	15	O	Constant current output
OUT10	17	16	O	Constant current output
OUT11	18	17	O	Constant current output
OUT12	19	18	O	Constant current output
OUT13	20	19	O	Constant current output
OUT14	21	20	O	Constant current output
OUT15	22	21	O	Constant current output
VCC	28	27	—	Power-supply voltage
VUP	26	25	—	Pre-charge FET power supply
GND	1	30	—	Power ground
NC	—	12, 13, 28, 29	—	No internal connection

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PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

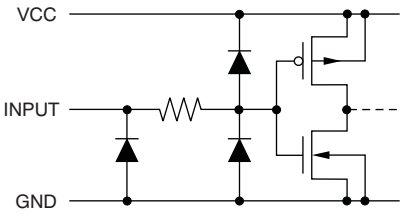


Figure 1. SIN, SCLK, XLAT, DCSEL, BLANK, GSCLK

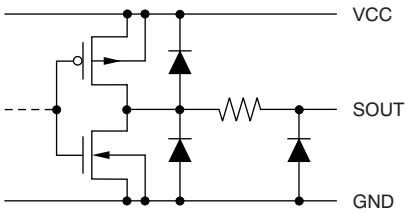


Figure 2. SOUT

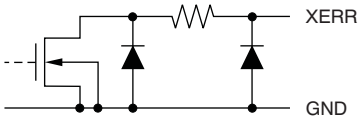


Figure 3. XERR

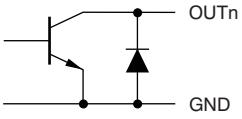
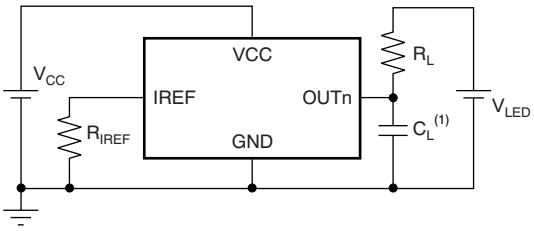


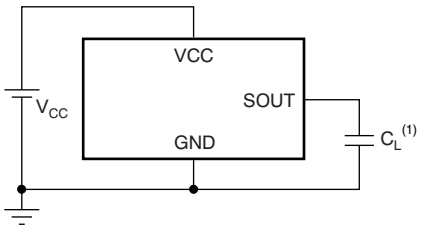
Figure 4. OUT0 Through OUT15

TEST CIRCUITS



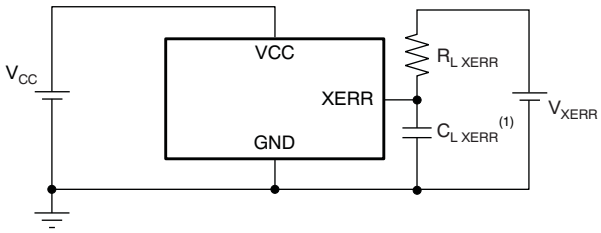
(1) C_L includes measurement probe and jig capacitance.

Figure 5. Rise Time and Fall Time Test Circuit for OUTn



(1) C_L includes measurement probe and jig capacitance.

Figure 6. Rise Time and Fall Time Test Circuit for SOUT



(1) $C_{L\ XERR}$ includes measurement probe and jig capacitance.

Figure 7. Fall Time Test Circuit for XERR

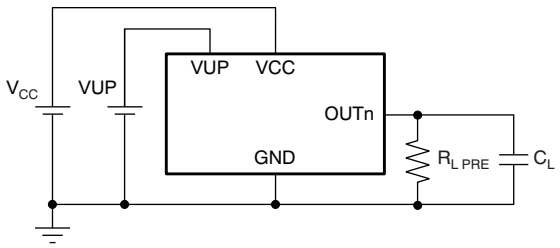


Figure 8. Delay Time Test Circuit for Pre-Charge FET

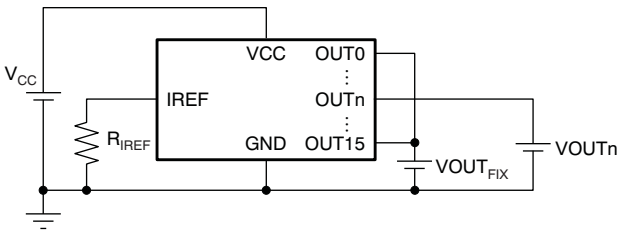


Figure 9. Constant Current Test Circuit for OUTn

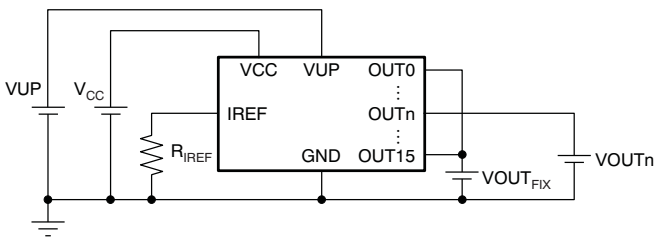
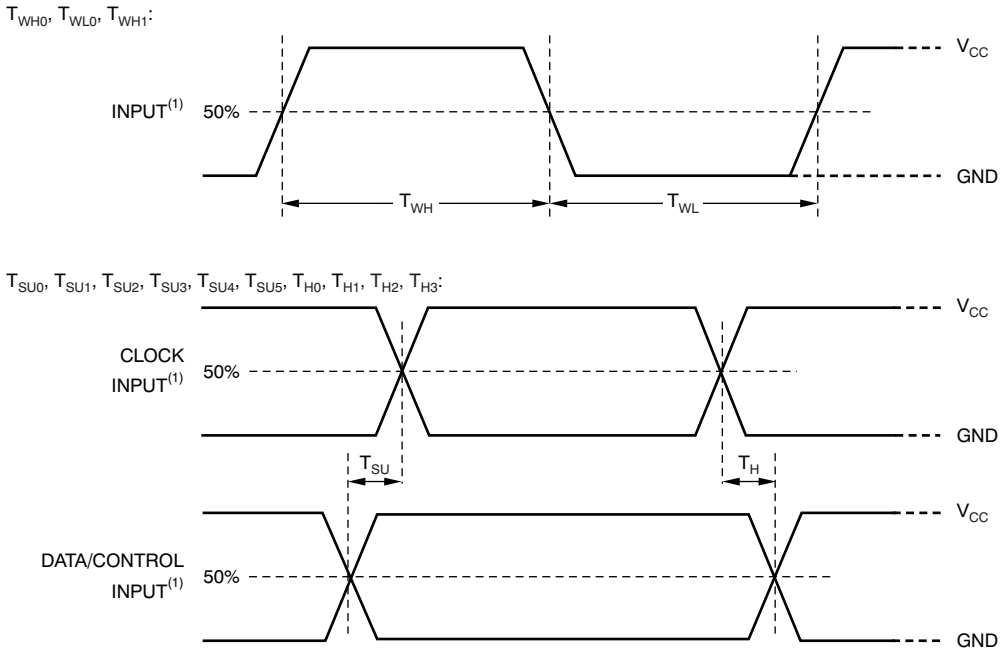


Figure 10. Leakage Current of Pre-Charge FET Test Circuit for OUTn

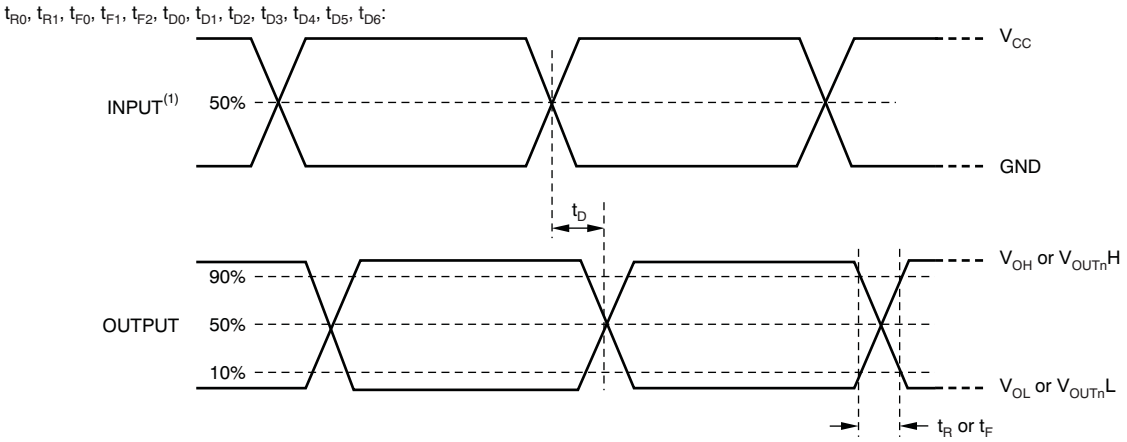
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TIMING DIAGRAMS



(1) Input pulse rise and fall time is 1 ns to 3 ns.

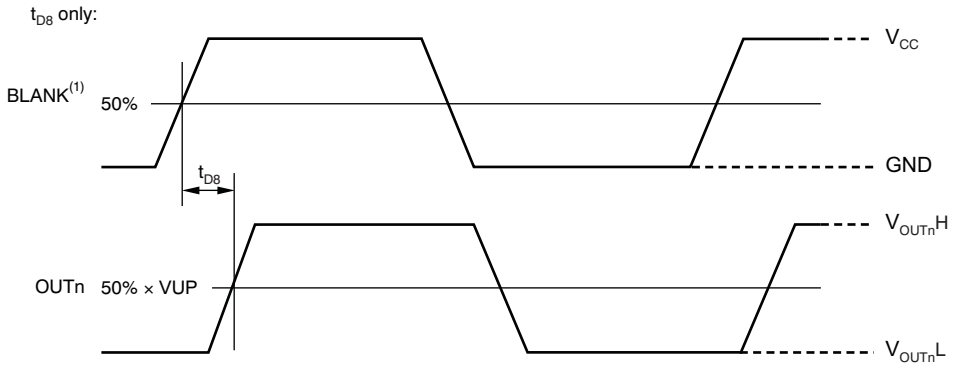
Figure 11. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 12. Output Timing

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(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 13. Output Timing (Pre-Charge FET)

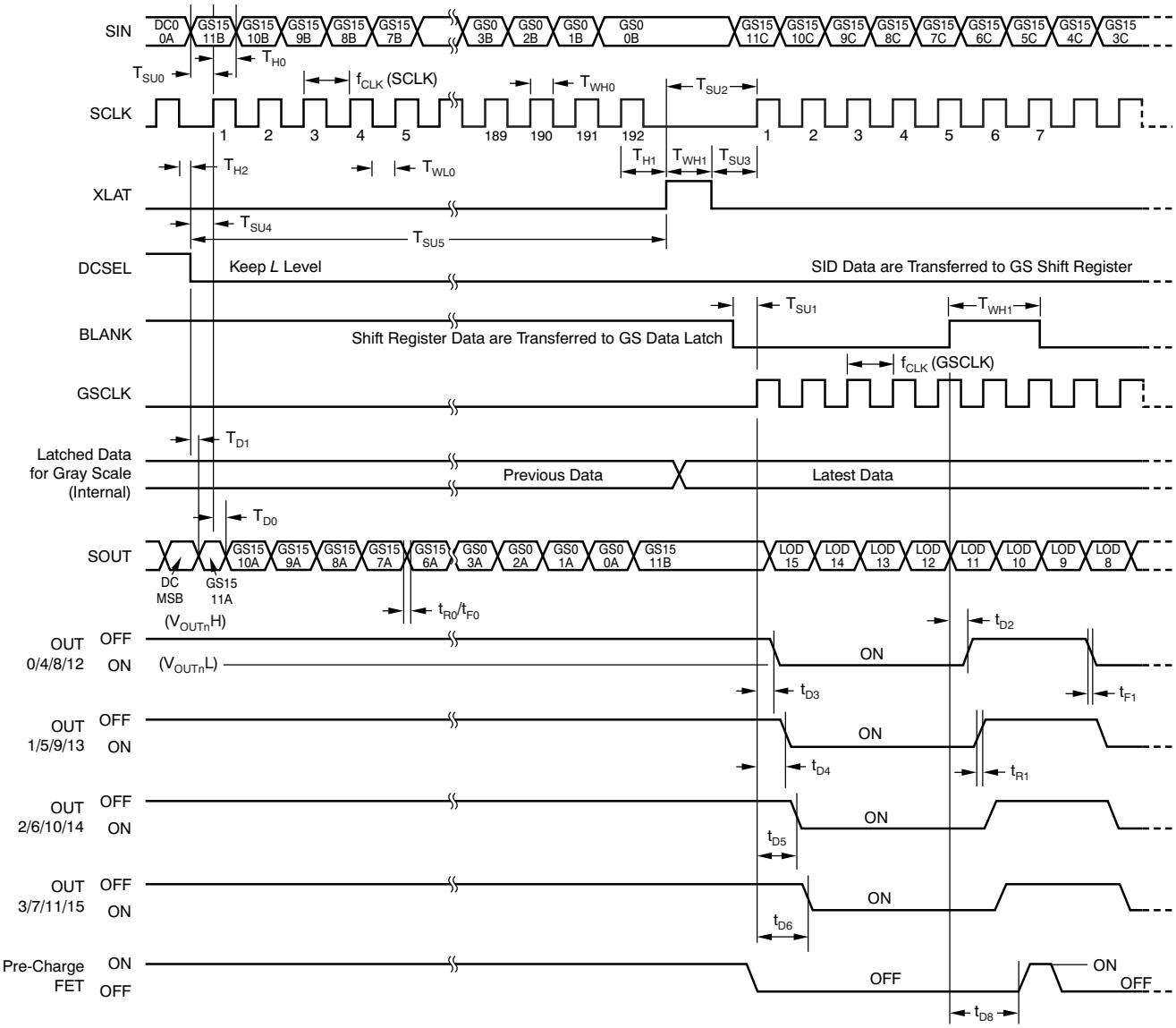


Figure 14. Grayscale Data Write Timing

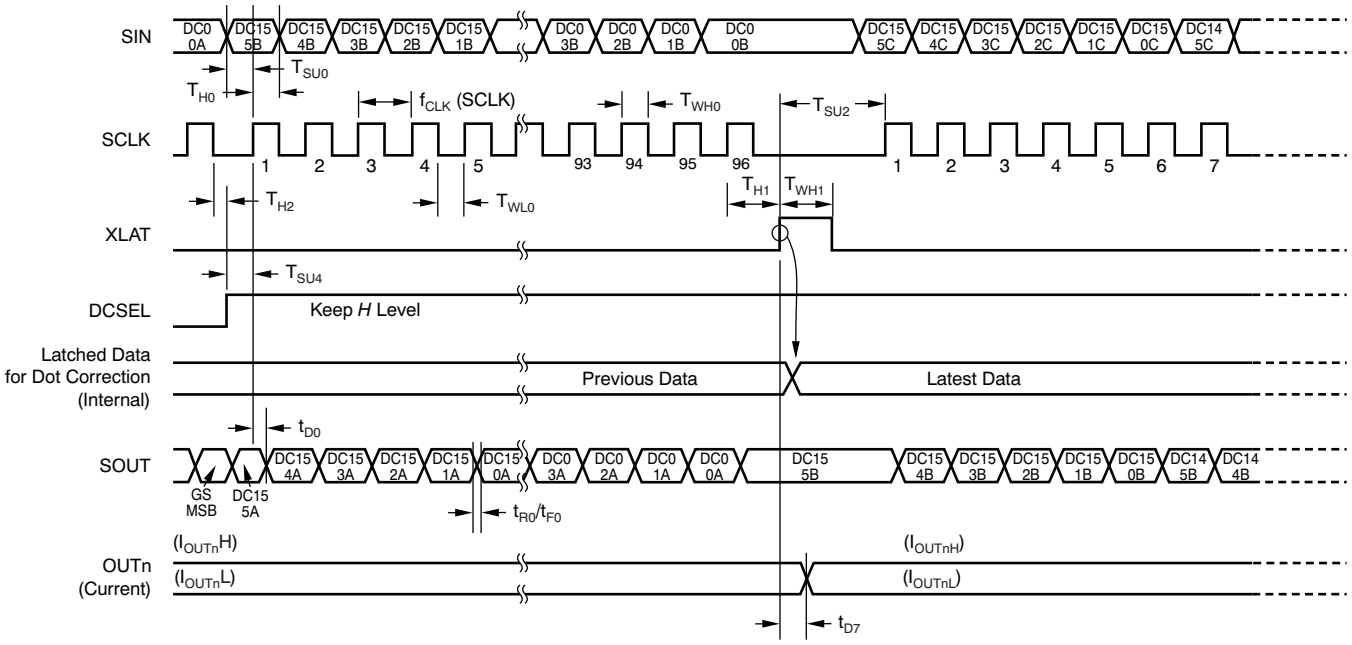
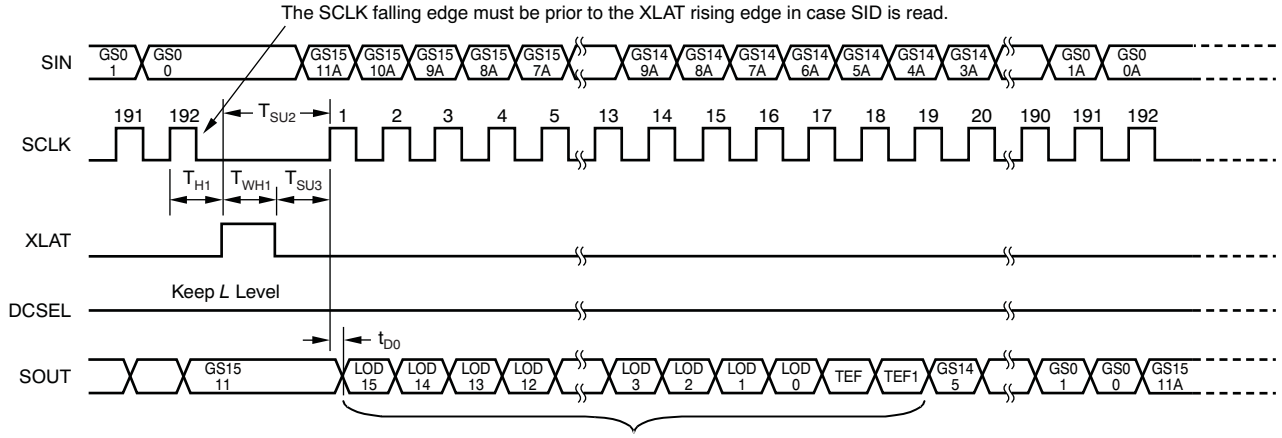


Figure 15. Dot Correction Data Write Timing



SID are entered in GS shift register at the first rising edge of SCLK with low level of DCSEL after XLAT. The SID readout consists of the saved LOD result at the 33rd GSCLK rising edge in the previous display period and the saved TEF data and TEF1 at the rising edge of the first of SCLK after XLAT goes low.

Figure 16. Status Information Data Read Timing

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TYPICAL CHARACTERISTICS

At V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

REFERENCE RESISTOR vs OUTPUT CURRENT

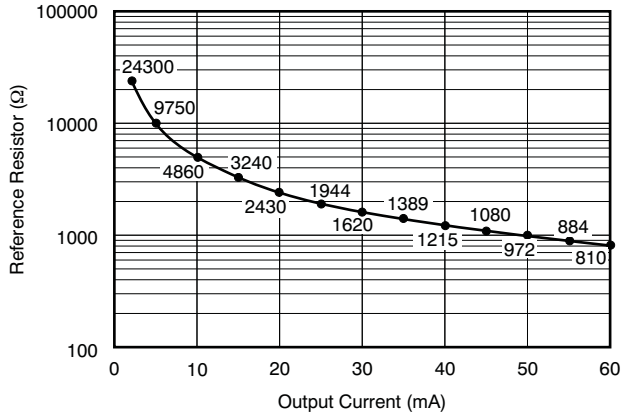


Figure 17.

POWER DISSIPATION RATE vs FREE-AIR TEMPERATURE

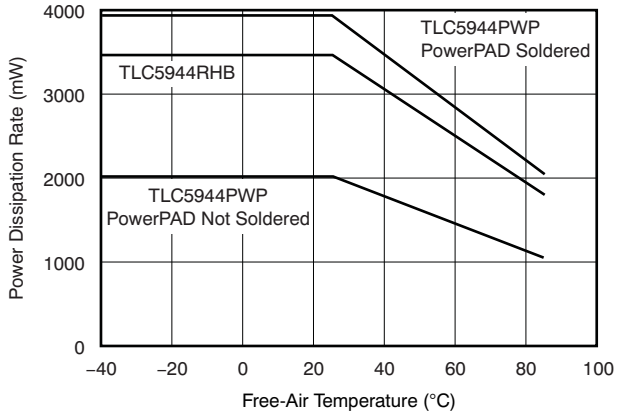
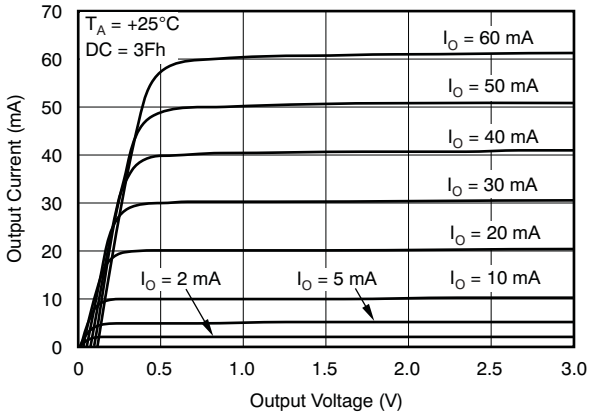


Figure 18.

OUTPUT CURRENT vs OUTPUT VOLTAGE(1)



(1) When the output voltage is less than the maximum voltage of the LED open detection threshold (V_{LOD} = 0.4 V_{MAX}) while the LED is on, the LED is forced off by the auto output off function.

Figure 19.

OUTPUT CURRENT vs OUTPUT VOLTAGE

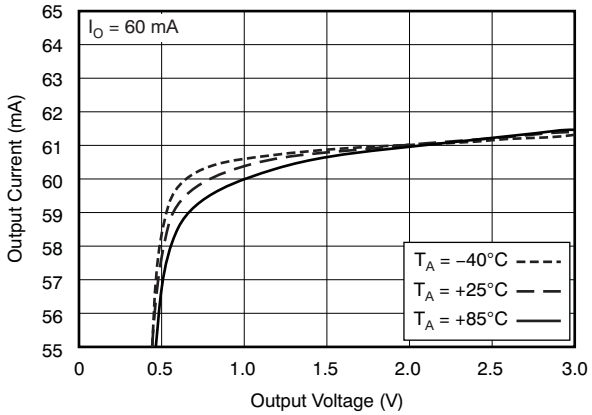


Figure 20.

ΔI_{OLC} vs AMBIENT TEMPERATURE

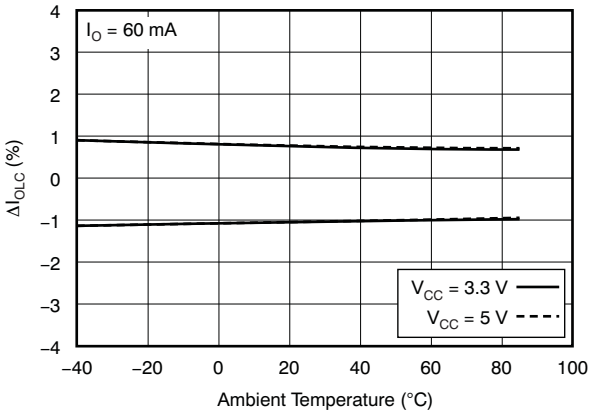


Figure 21.

ΔI_{OLC} vs OUTPUT CURRENT

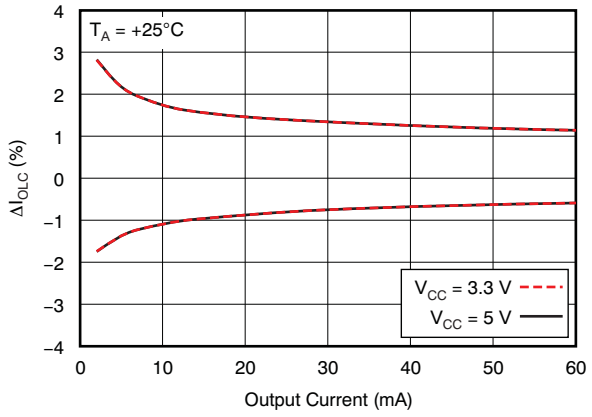


Figure 22.

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TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

ΔI_{OLC} vs OUTPUT CURRENT

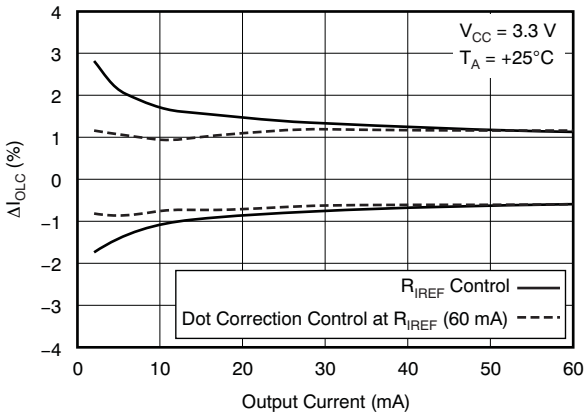


Figure 23.

DOT CORRECTION LINEARITY (ABS Value)

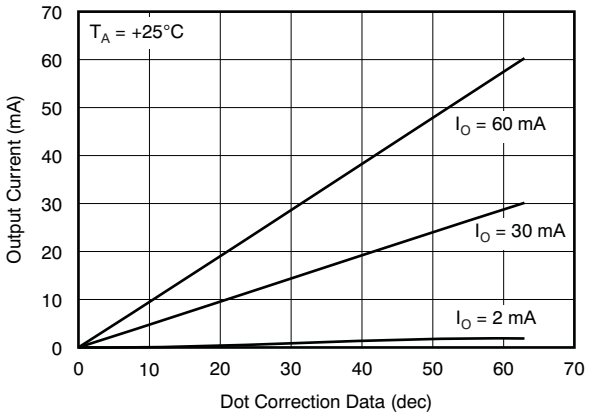


Figure 24.

DOT CORRECTION LINEARITY (ABS Value)

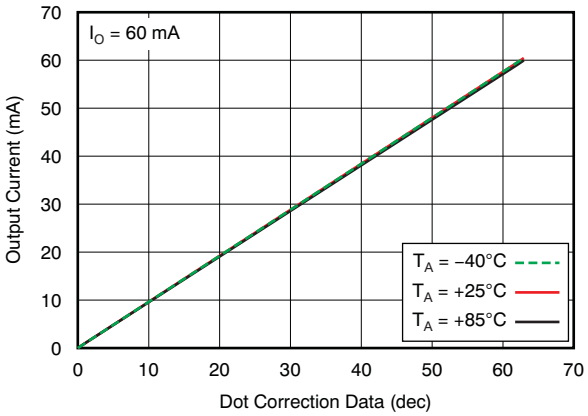


Figure 25.

CONSTANT CURRENT OUTPUT VOLTAGE WAVEFORM

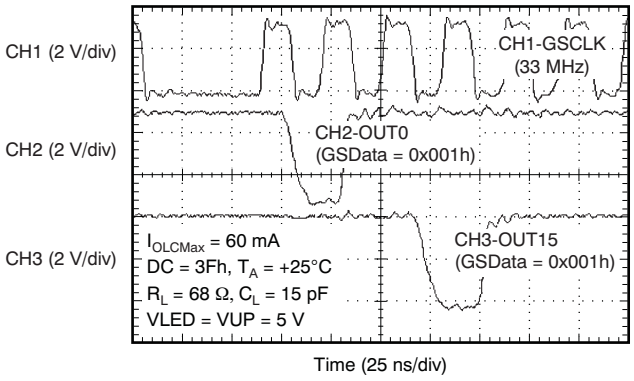


Figure 26.

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DETAILED DESCRIPTION

Setting for the Maximum Constant Sink Current Value

On the TLC5944, the maximum constant current sink value for each channel, I_{OLCMax}, is determined by an external resistor, R_{IREF}, and GND pins. The R_{IREF} resistor value is calculated with Equation 1:

$$R_{IREF}\ (k\Omega) = \frac{V_{IREF}\ (V)}{I_{OLCMax}\ (mA)} \times 40.5 \quad (1)$$

Where:

- V_{IREF} = the internal reference voltage on the IREF pin (typically 1.20 V)

I_{OLCMax} is the largest current for all outputs. Each output sinks the I_{OLCMax} current when it is turned on and the dot correction is set to the maximum value of 3Fh (63d). The sink current for each output can be reduced by lowering the respective output dot correction data.

R_{IREF} must be between 810 Ω (typ) and 24.3 kΩ (typ) in order to keep I_{OLCMax} between 2 mA and 60 mA. The output may become unstable when I_{OLCMax} is set lower than 2 mA. However, output currents lower than 2 mA can be achieved by setting I_{OLCMax} to 2 mA or higher, and then using dot correction to lower the output current.

Figure 17 in the Typical Characteristics and Table 1 show the characteristics of the constant sink current versus the external resistor, R_{IREF}.

Table 1. Maximum Constant Current Output versus External Resistor Value

I_{OLCMax} (mA, Typical)	R_{IREF} (Ω)
60	810
55	884
50	972
45	1080
40	1215
35	1389
30	1620
25	1944
20	2430
15	3240
10	4860
5	9720
2	24300

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Dot Correction (DC) Function

The TLC5944 is able to individually adjust the output current of each channel (OUT0 to OUT15). This function is called *dot correction* (DC). The DC function allows users to individually adjust the brightness and color deviations of LEDs connected to the outputs OUT0 to OUT15. Each respective channel output current can be adjusted in 64 steps from 0% to 100% of the maximum output current, I_{OLCMax}. Dot correction data are entered into the TLC5944 via the serial interface.

Equation 2 determines the sink current for each output (OUTn):

$$I_{OUTn}\ (mA) = I_{OLCMax}\ (mA) \times \frac{DCn}{63d} \quad (2)$$

Where:

- I_{OLCMax} = the maximum channel current for each channel determined by R_{IREF}
- DCn = the programmed dot correction value for OUTn (DCn = 0 to 63d)

When the IC is powered on, the data in the dot correction shift register and data latch are not set to any default values. Therefore, DC data must be written to the DC latch before turning on the constant current output.

Table 2 summarizes the DC data versus current ratio and set current value.

Table 2. DC Data versus Current Ratio and Set Current Value

DC DATA (Binary)	DC DATA (Decimal)	DC DATA (Hex)	SET CURRENT RATIO TO MAX CURRENT (%)	OUTPUT CURRENT (mA, Typical) AT I_{OLCMax} = 60 mA	OUTPUT CURRENT (mA, Typical) AT I_{OLCMax} = 2 mA
00 0000	0	00	0.0	0.0	0.000
00 0001	1	01	1.6	0.4	0.032
00 0010	2	02	3.2	0.8	0.064
—	—	—	—	—	—
11 1101	61	3D	96.8	58.1	1.937
11 1110	62	3E	98.4	59.0	1.968
11 1111	63	3F	100.0	60.0	2.000

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Grayscale (GS) Function (PWM Operation)

The pulse width modulation (PWM) operation is controlled by a 12-bit grayscale counter that is clocked on each rising edge of the grayscale reference clock (GSCLK). The counter is reset to zero when BLANK is high. The counter value is held at zero while BLANK is high, even if the GSCLK input is toggled high and low. After the falling edge of BLANK, the counter increments with each rising edge of GSCLK. Any constant current sink output (OUT0 through OUT15) with a nonzero value in the corresponding grayscale latch starts to sink current after the first rising edge of GSCLK following a high-to-low transition of BLANK. The internal counter keeps track of the number of GSCLK pulses. Each output channel stays on as long as the internal counter is equal to or less than the respective output GSCLK. Each channel turns off at the rising edge of GSCLK when the grayscale counter value is larger than the grayscale latch value.

For example, an output that has a grayscale latch value of '1' turns on at the first rising edge of GSCLK after BLANK goes low. It turns off at the second rising edge of GSCLK. Figure 27 shows the PWM timing diagram.

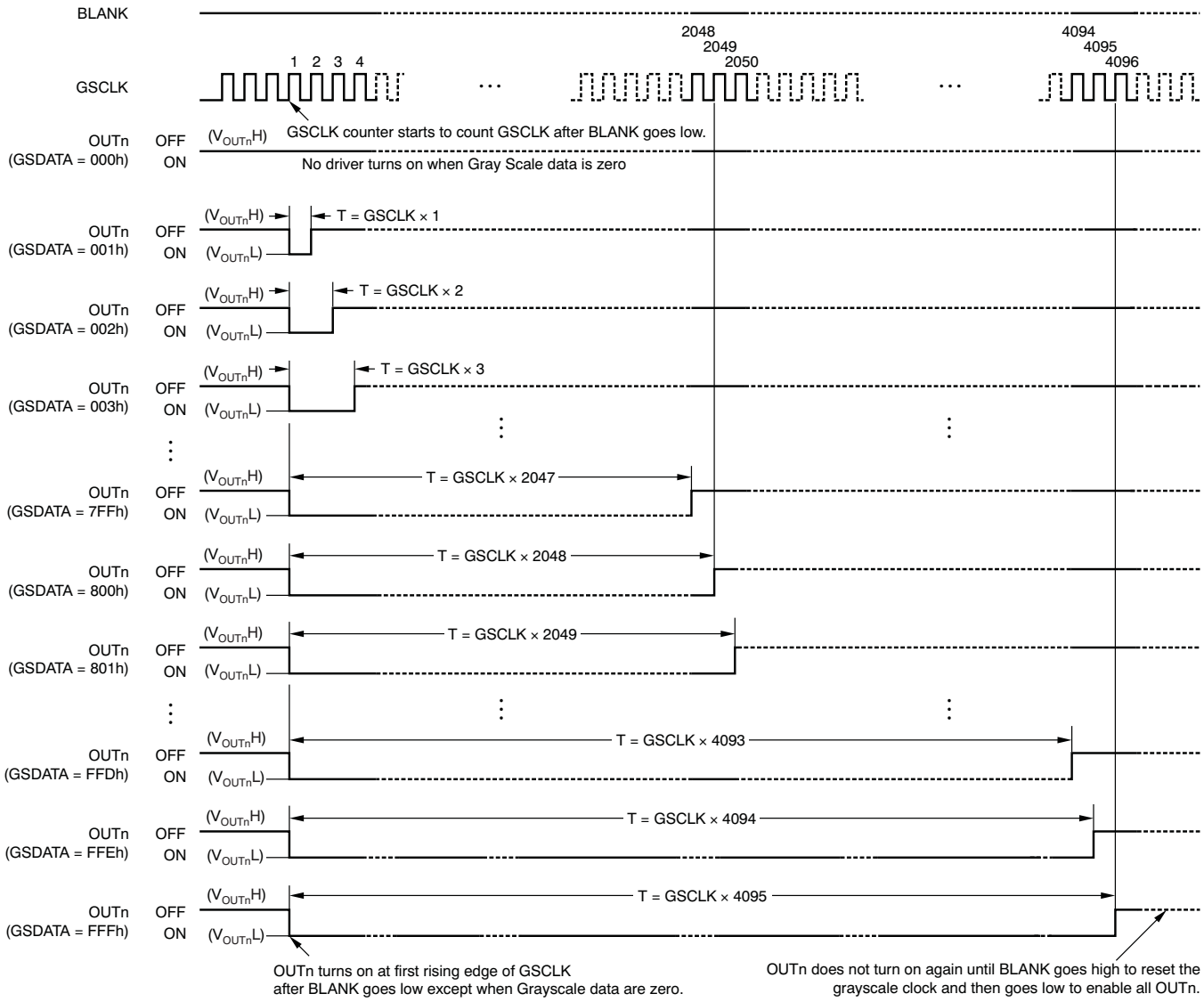


Figure 27. PWM Operation Timing

When the IC powers on, the data in the grayscale shift register and latch are not set to any default value. Therefore, grayscale data must be written to the grayscale latch before turning on the constant current output. Additionally, BLANK should be held high when the device turns on, to prevent the outputs from turning on before the proper grayscale and dot correction values can be written. All constant current outputs are forced off when BLANK is high. Equation 3 determines the on time (t_{OUTON}) for each output (OUTn).

$$t_{OUTON}\ (ns) = t_{GSCLK}\ (ns) \times GSn \quad (3)$$

Where:

- T_{GSCLK} = the period of GSCLK
- GSn = the programmed grayscale value for OUTn (GSn = 0 to 4095d)

If GS data change during a display period because XLAT goes high, and latches new GS data, the internal data latch registers are immediately updated. This action can cause the outputs to turn on or off unexpectedly. For proper operation, GS data should only be latched into the IC at the end of a display period when BLANK is high. Table 3 summarizes the GS data versus OUTn on duty and on time.

Table 3. GS Data versus OUTn On Duty and OUTn On Time

GS DATA (Binary)	GS DATA (Decimal)	GS DATA (Hex)	OUTn ON DUTY RATIO TO MAXIMUM CODE (%)	OUTn ON-TIME (ns, Typical) AT 33-MHz GSCLK
0000 0000 0000	0	000	0.00	0
0000 0000 0001	1	001	0.02	30
0000 0000 0010	2	002	0.05	61
0000 0000 0011	3	003	0.07	91
—	—	—	—	—
0111 1111 1111	2047	7FF	49.99	62030
1000 0000 0000	2048	800	50.01	62061
1000 0000 0001	2049	801	50.04	62091
—	—	—	—	—
1111 1111 1101	4093	FFD	99.95	124030
1111 1111 1110	4094	FFE	99.98	124061
1111 1111 1111	4095	FFF	100.00	124091

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Grayscale (GS) Shift Register and Data Latch

The grayscale (GS) shift registers and data latches are each 192 bits in length, and set the PWM timing for each constant current driver. See Table 3 for the ON time duty of each GS data bit. Figure 28 shows the shift register and latch configuration. Refer to Figure 14 for the timing diagram for writing data into the GS shift register and latch.

The driver on time is controlled by the data in the GS data latch. GS data present on the SIN pin are clocked into the GS shift register with each rising edge of the GSCLK pin when DCSEL is low. Data are shifted in MSB first. Data are latched from the shift register into the GS data latch with a rising edge on the XLAT pin. A DCSEL level change is allowed when SCLK is low and 100 ns after the rising edge of XLAT.

When the device powers up, the data in the GS shift register and latches are not set to any default value. Therefore, GS data must be written to the GS latch before turning on the constant current output. Also, BLANK should be at a high level when powering on the device, because the constant current may be turned on as well. All constant current output is off when BLANK is at a high level. The status information data (SID) byte is overwritten on the most significant 18 bits of the grayscale shift register at the first rising edge of GSCLK after XLAT goes low.

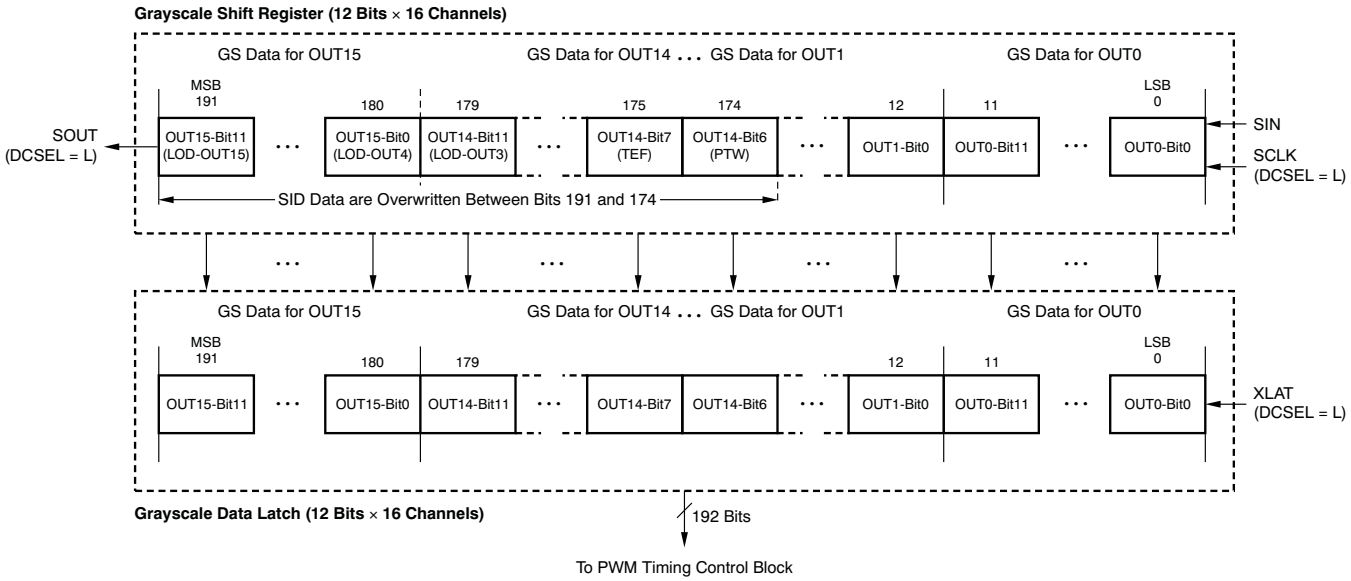


Figure 28. Grayscale Shift Register and Data Latch Configuration

Dot Correction (DC) Shift Register and Data Latch

The dot correction (DC) shift register and latches are each 96 bits long and are used to individually adjust the constant current value for each constant current driver. Each channel can be adjusted from 0% to 100% of the maximum LED current with 6-bit resolution. Table 2 describes the percentage of maximum current for each dot correction data. Figure 29 shows the shift register and latch configuration for DC data. Figure 15 illustrates the timing for writing data into the DC shift registers and latches. Each LED channel current is dot-corrected by the percentage value that corresponds to the data in the respective DC data latch. DC data present on the SIN pin are clocked, MSB first, into the DC shift register at each rising edge of the SCLK pin when DCSEL is high. Data are latched from the shift register into the DC data latch with a rising edge on the XLAT pin when DCSEL is high. A DCSEL level change is allowed when SCLK is low and 100 ns after the rising edge of XLAT.

When the IC is powered on, the data in the DC shift register and data latch are not set to any default value. Therefore, dot correction data must be written to the DC latch before turning on the constant current output.

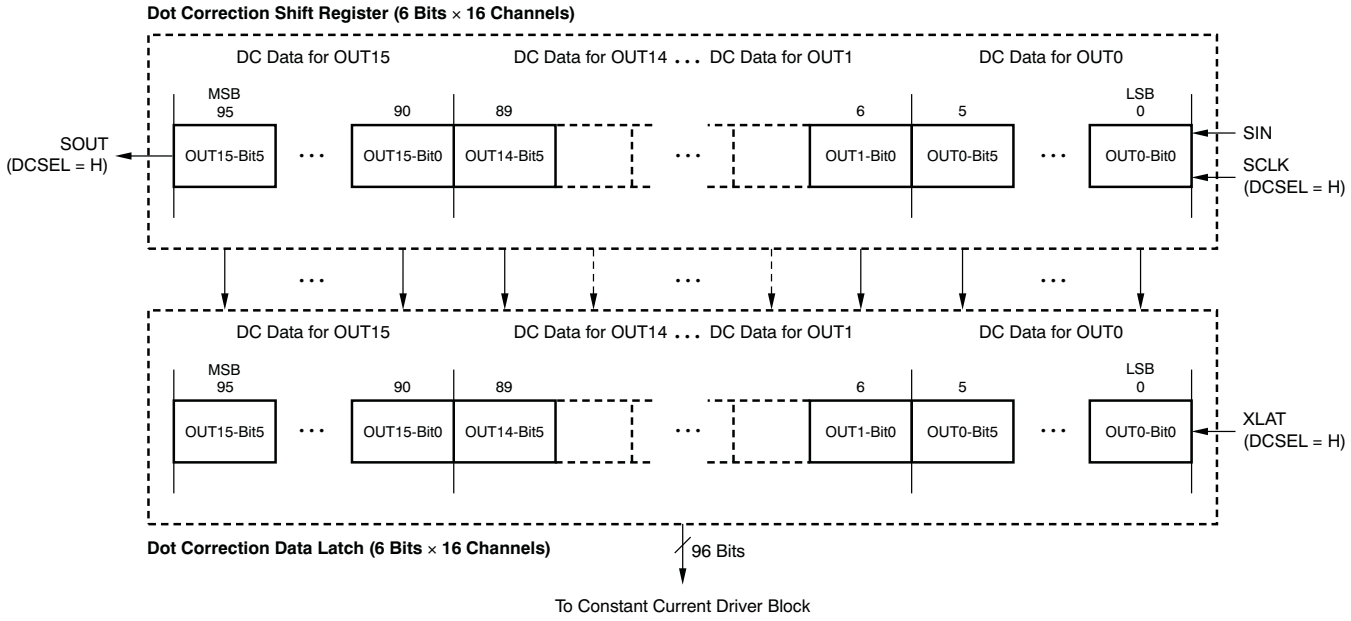


Figure 29. Dot Correction Shift Register and Latch Configuration

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Status Information Data (SID)

Status information data (SID) are 18-bit, read-only data. The 16-bit LED open detection (LOD) error, the thermal error flag (TEF), and the pre-thermal warning (PTW) are shifted out onto the SOUT pin with each rising edge of the serial data shift clock, SCLK. The 16 LOD bits for each channel and the two TEF bits are written into the 18 most significant bits of the grayscale shift register at the rising edge of the first SCLK after XLAT goes low. As a result, the previous data in the 18 most significant bits of the grayscale information are lost at the same time. No data are loaded into the other 174 bits. Figure 30 shows the bit assignments. Figure 16 illustrates the read timing for the status information data.

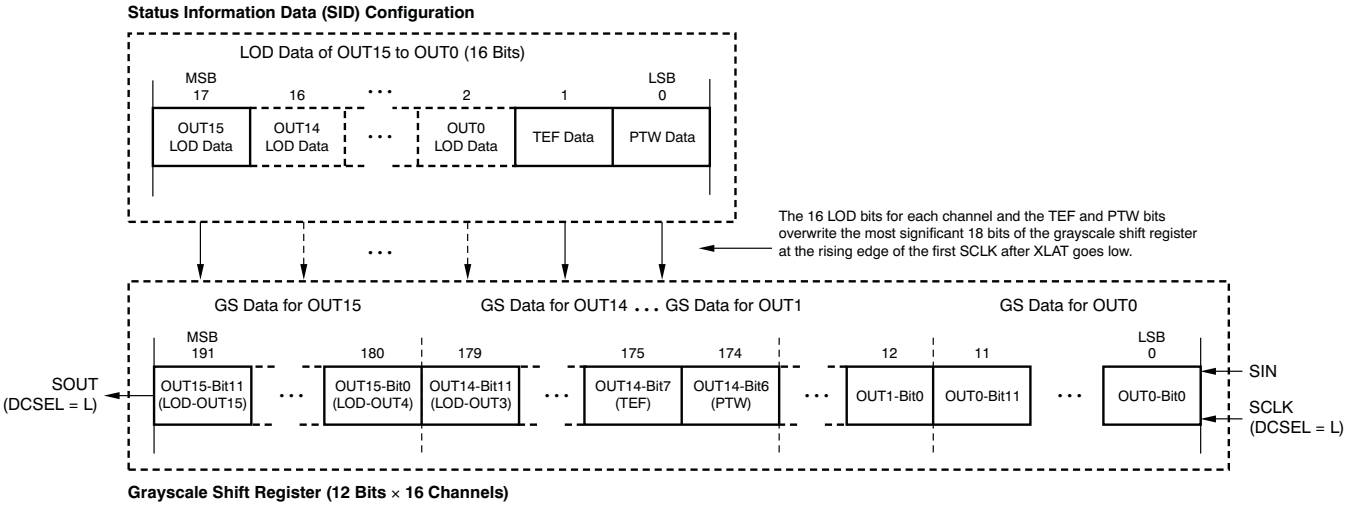


Figure 30. Status Information Data Configuration

The LOD data update at the rising edge of the next 33rd GSCLK of the subsequent PWM cycle; the LOD data are retained until the next 33rd GSCLK. LOD data are only checked for outputs that are turned on during the rising edge of the 33rd GSCLK pulse. A '1' in an LOD bit indicates an open LED condition for the corresponding channel. A '0' indicates normal operation. It is possible for LOD data to show a '0' even if the LED is open when the grayscale data are less than 20h (32d).

The PTW and TEF bits indicate that the IC temperature is high and too high, respectively. The TEF flag also indicates that the IC has turned off all drivers to avoid damage by overheating the device. A '1' in the TEF bit means that the IC temperature has exceeded the detect temperature threshold of high side ($T_{(TEF)}$) and the driver is forced off. A '0' in the TEF bit indicates the driver has not exceeded the high temperature. The PTW flag indicates that the IC temperature has exceeded the detect temperature threshold, but does not force the driver off. A '1' in the PTW bit indicates that the IC temperature has exceeded the pre-thermal warning threshold ($T_{(PTW)}$) but does not force the driver off. A '0' in the PTW bit indicates normal operation with low-side temperature conditions. When the PTW is set, the IC temperature should be reduced by lowering the power dissipated in the driver to avoid a forced shutdown by the thermal shutdown circuit. This reduction can be accomplished by lowering the values of the GS or DC data.

When the IC powers on, LOD data do not show correct values. Therefore, LOD data must be read from the 33rd GSCLK pulse input after BLANK goes low. Table 4 shows a truth table for both LOD and TEF.

Table 4. LOD and TEF Truth Table

SID DATA	CONDITION		
	LED OPEN DETECTION (LODn)	THERMAL ERROR FLAG (TEF)	PRE-THERMAL WARNING (PTW)
0	LED is connected ($V_{OUTn} > V_{LOD}$)	Device temperature is lower than the high-side detect temperature (temp ≤ $T_{(TEF)} - T_{(HYST)}$)	Device temperature is lower than the low-side detect temperature (temp < $T_{(PTW)} - T_{(HYSP)}$)
1	LED is open or shorted to GND ($V_{OUTn} \le V_{LOD}$)	Device temperature is higher than the high-side detect temperature and the driver is forced off (temp > $T_{(TEF)}$)	Device temperature is higher than the low-side detect temperature (temp ≥ $T_{(PTW)}$)

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Continuous Base LED Open Detection

At the rising edge of the 33rd GSCLK after the falling edge of BLANK, the LED open detection (LOD) circuit checks the voltage of each constant current output (OUT0 through OUT15 = OUTn) that is turned on to detect open LEDs and short LEDs to GND. The channels corresponding to the LOD bit in the status information data (SID) register are set to '1' if the voltage of the OUTn pin (V_{OUTn}) is less than the LED open detection threshold (V_{LOD} = 0.3 V_{TYP}). This status information can be read from the SOUT pin when DCSEL is low. No special test sequence is required for LED open detection.

The LOD function automatically checks for open LEDs and short LEDs to GND during each grayscale PWM cycle. The SID information of LOD is latched into the LED open detection data latch and does not change until the rising edge of the 33rd GSCLK pulse following the next falling edge of BLANK. To eliminate false detection of open LEDs, the LED driver design must ensure that the TLC5944 output voltage is greater than V_{LOD} when the outputs are on. The GS data must be 21h (33d) or more to get the LOD result. Figure 31 shows the LED open detection timing.

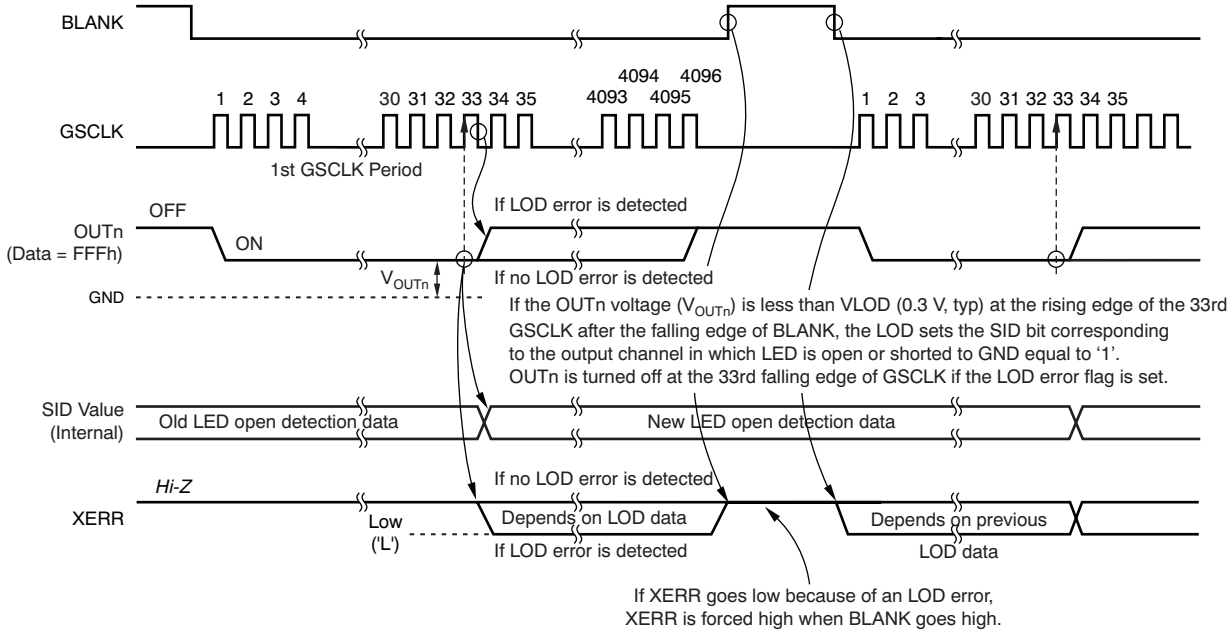


Figure 31. LED Open Detection (LOD) Timing

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Thermal Shutdown and Thermal Error Flag

The thermal shutdown (TSD) function turns off all of the constant current outputs on the IC immediately when the junction temperature (T_J) exceeds the threshold ($T_{(TEF)}$ = +162°C, typ) and sets the thermal error flag (TEF) to '1'. All outputs are latched off when TEF is set to '1'; TEF and PTW remain off until the next grayscale cycle after T_J drops below ($T_{(TEF)} – T_{(HYST)}$). TEF is set to '0' once T_J drops below ($T_{(TEF)} – T_{(HYST)}$), but the output does not turn on until the first GSCLK after BLANK goes low while TEF is set to '0'. Figure 32 illustrates the TEF/TSD/XERR timing sequence.

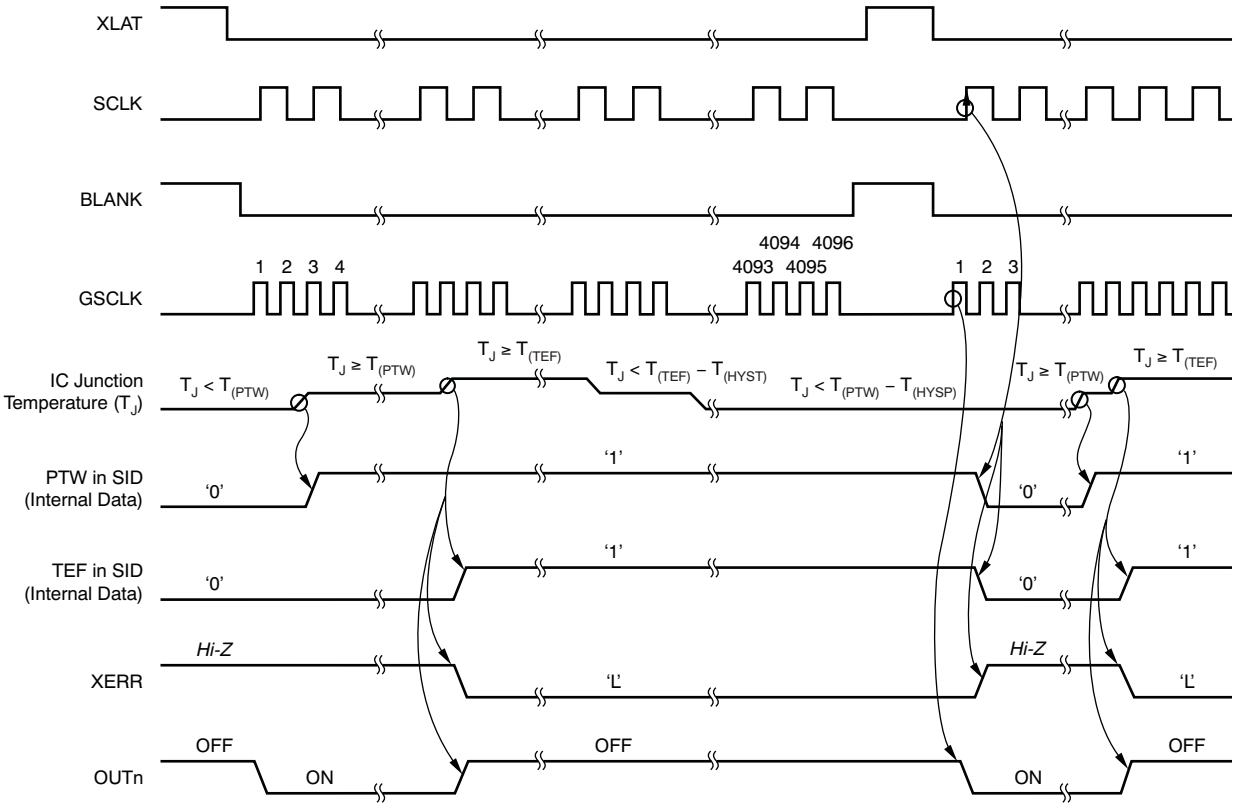


Figure 32. TEF/TSD/XERR Timing

Internal Pre-Charge FET

The internal pre-charge FET can prevent ghosting of multiplexed LED modules. One cause of this phenomenon is the charging current for parasitic capacitance of the constant current output line and driver through the LED. One of the mechanisms is shown in Figure 33.

In Figure 33, the constant current driver turns LED0-0 on at (1) and off at (2). After LED0-0 is turned off, OUT0 voltage is pulled up to V_{CHG} by LED0-0. This OUT0 node has some parasitic capacitance (such as the constant current driver output capacitance, and the board layout capacitance shown as C0-2). After LED0-0 turns off, SWPMOS0 is turned off and SWNMOS0 is turned on for LINE0, then LINE0 is pulled down to GND. Because there is a parasitic capacitance between LINE0 and OUT0, OUT0 voltage is also pulled down to GND. After that, SWPMOS1 is turned on for next line (LINE1). When SWPMOS1 turns on, OUT0 voltage is pulled up from the ground voltage to $V_{LED} – V_F$. The charge current (I_{CHRG}) flows to the parasitic capacitor (C0) through LED1-0, causing the LED to briefly turn on and creating the ghosting effect of LED1-0.

The TLC5944 has an internal pre-charge FET to prevent ghosting. The power supply of the pre-charge FET must be connected to V_{LED} (LED anode voltage). After a small delay after BLANK goes high, this FET pulls OUTn (OUT0 to OUT15) up to V_{LED}. The charge current does not flow to C0 through LED1-0 when SWMOS1 is turned on and the ghosting is eliminated at (3). The pre-charge FET turns off as soon as BLANK goes low to avoid current flowing from V_{LED} through the pre-charge FET.

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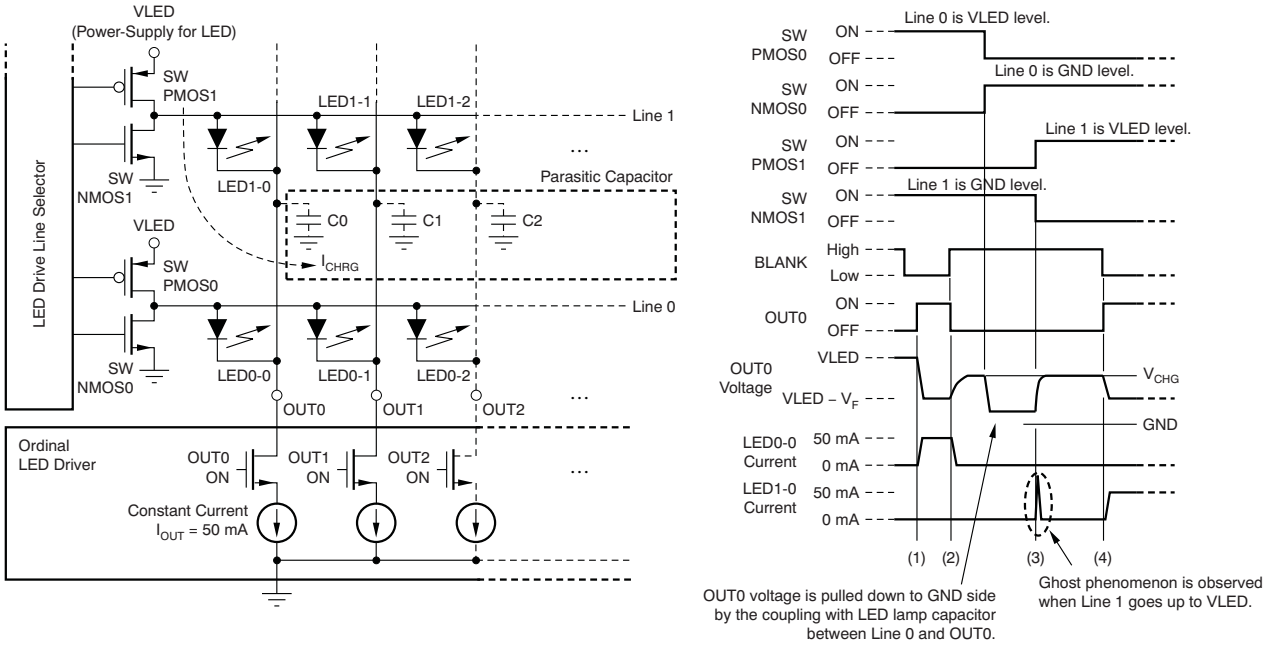


Figure 33. LED Ghost-Lighting Phenomenon Mechanism

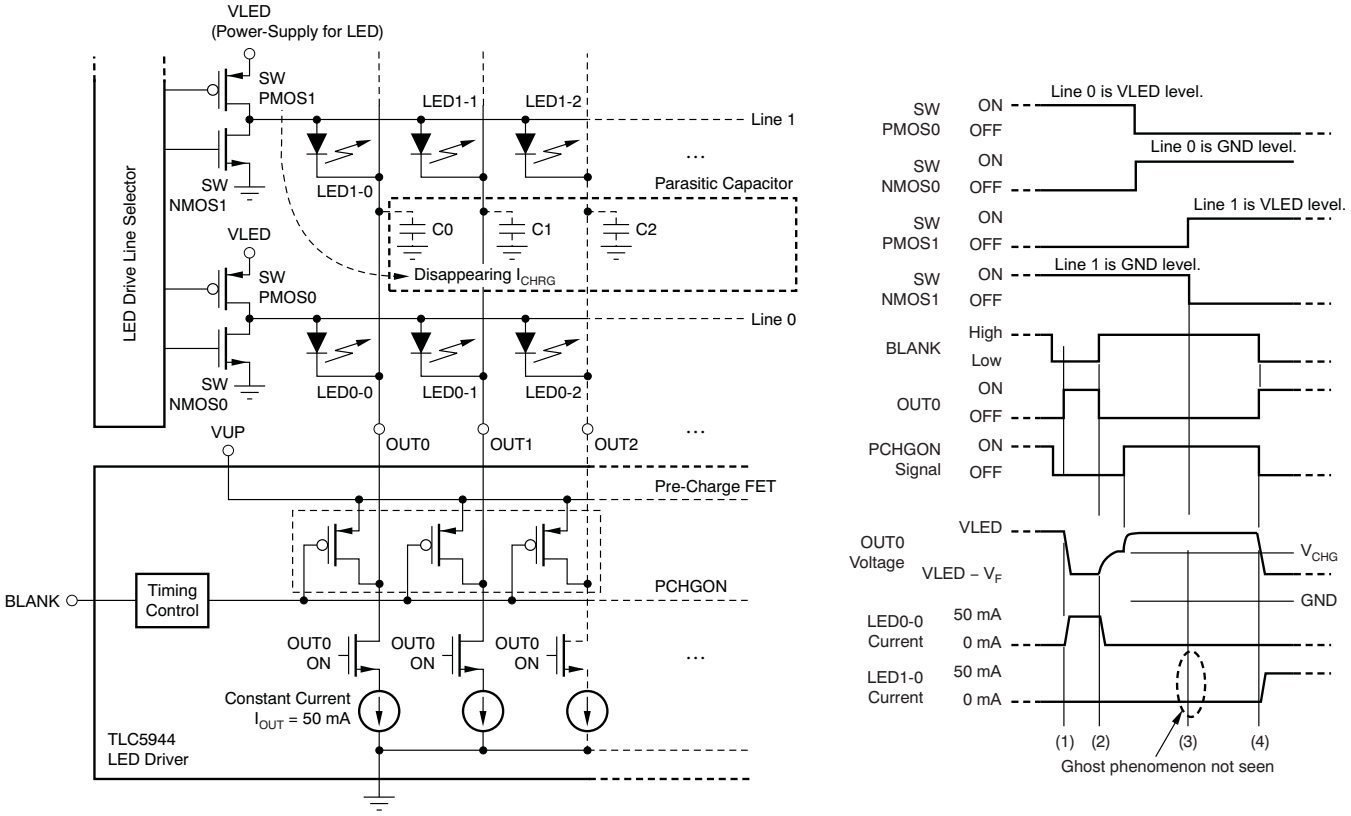


Figure 34. LED Ghost-Lighting Mechanism by Pre-Charge FET

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Auto Output Off

The TLC5944 current consumption increases if any output (OUTn) is turned on and no LED is connected, the LED is an open circuit, or the output is shorted to GND. The TLC5944 has the auto output off function to reduce consumption current in these cases. This function turns off any OUTn where LED open has been detected to reduce the current into the VCC pin during error conditions. Figure 35 illustrates the auto output off function. Therefore, the LED anode voltage must be held over the LED forward voltage (V_F) plus the maximum voltage of the LED open detection threshold (V_{LOD} = 0.4 V_{MAX}) while the LED is on, in any case. Otherwise, the LED is forced off by the auto output off function.

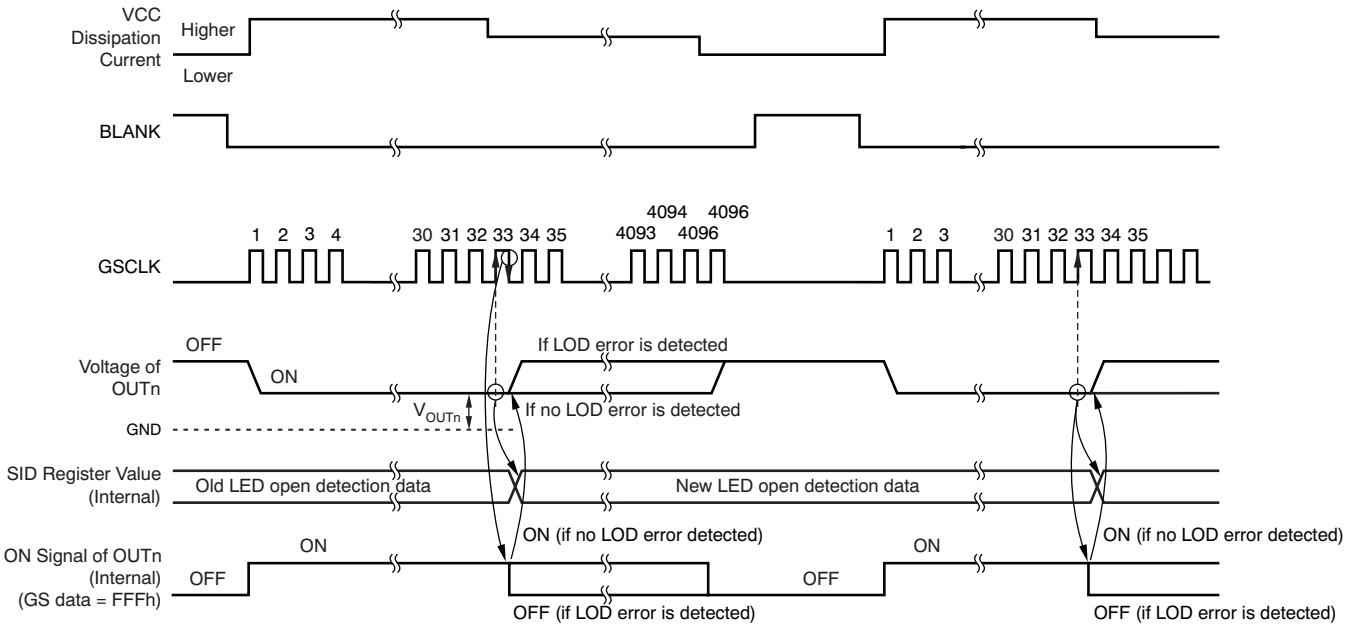


Figure 35. Auto Output Off Function

Noise Reduction

Large surge currents may flow through the IC and the printed circuit board (PCB) on which the device is mounted if all 16 LED channels turn on simultaneously at the start of each grayscale cycle. This large current surge could introduce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC5944 turns on the LED channels in a series delay to provide a circuit soft-start feature. The output current sinks are grouped into four groups of four channels each. The first group is OUT0/4/8/12; the second group is OUT1/5/9/13; the third group is OUT2/6/10/14; and the fourth group is OUT3/7/11/15. Each group is turned on sequentially with a small delay between groups; Figure 14 shows this delay. Both turn-on and turn-off are delayed.

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POWER DISSIPATION CALCULATION

The device power dissipation must be below the power dissipation rate of the device package (illustrated in Figure 18) to ensure correct operation. Equation 4 calculates the power dissipation of the device:

$$P_D = (V_{CC} \times I_{CC}) + \left(V_{OUT} \times I_{OLCMax} \times N \times \frac{DCn}{63d} \times d_{PWM} \right) \quad (4)$$

Where:

- V_{CC} = device supply voltage
- I_{CC} = device supply current
- V_{OUT} = OUTn voltage when driving LED current
- I_{MAX} = LED current adjusted by R_{IREF} resistor
- DCn = maximum DC value for OUTn
- N = number of OUTn driving LED at the same time
- d_{PWM} = duty ratio defined by BLANK pin or GS PWM value

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2008) to Revision A	Page
• Changed Figure 14	11
• Changed Figure 34	24

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5944PWP	ACTIVE	HTSSOP	PWP	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5944	Samples
TLC5944PWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5944	Samples
TLC5944PWPRG4	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5944	Samples
TLC5944RHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5944	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

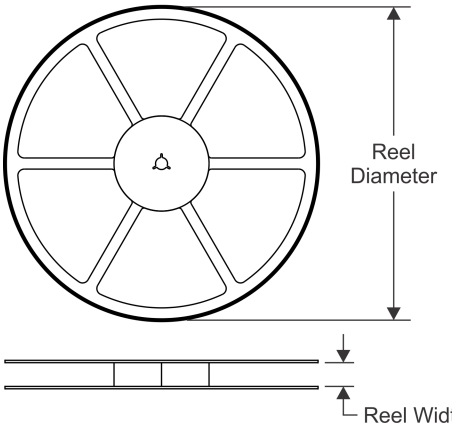
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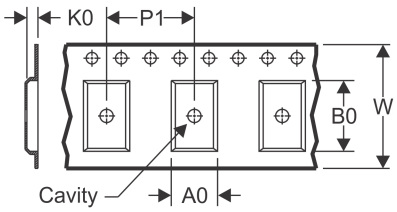
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

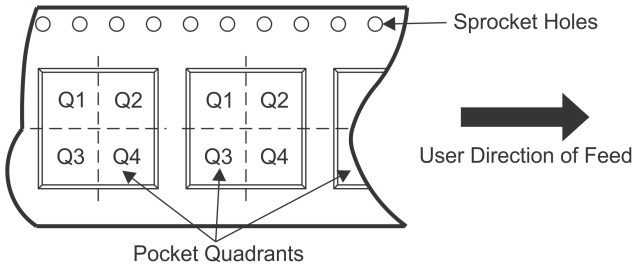


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

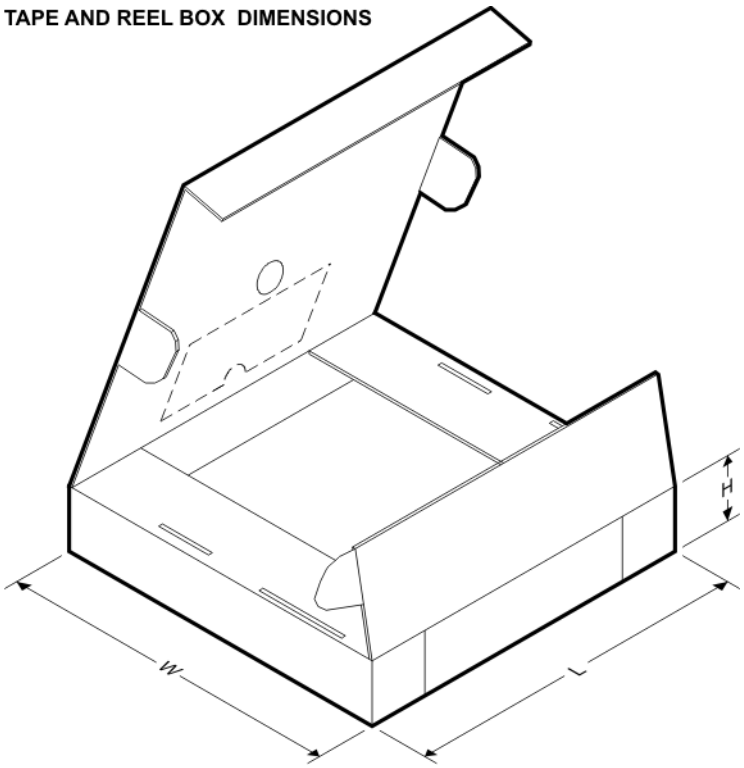
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5944PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TLC5944RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

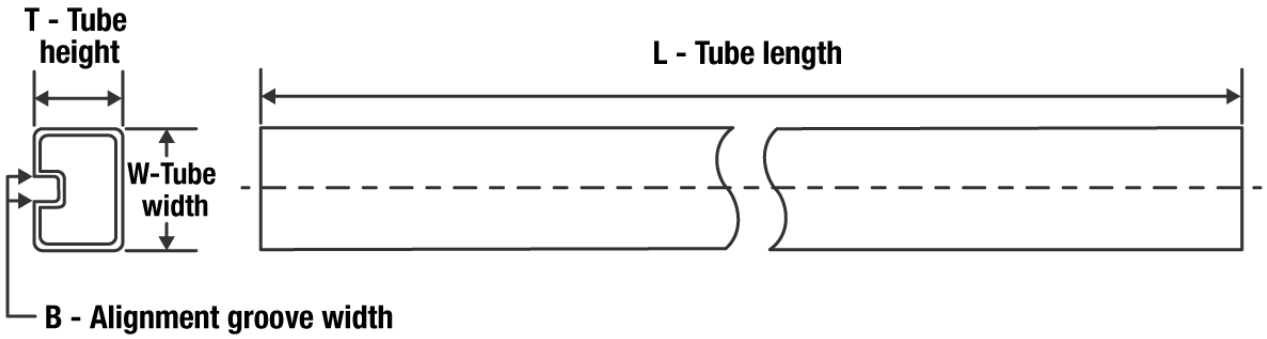
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5944PWPR	HTSSOP	PWP	28	2000	853.0	449.0	35.0
TLC5944RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC5944PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5

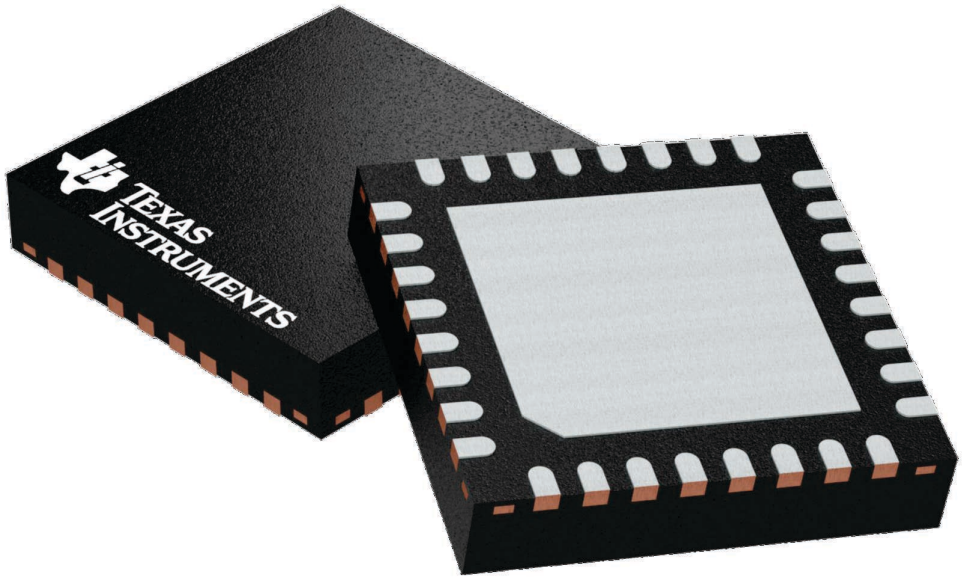
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

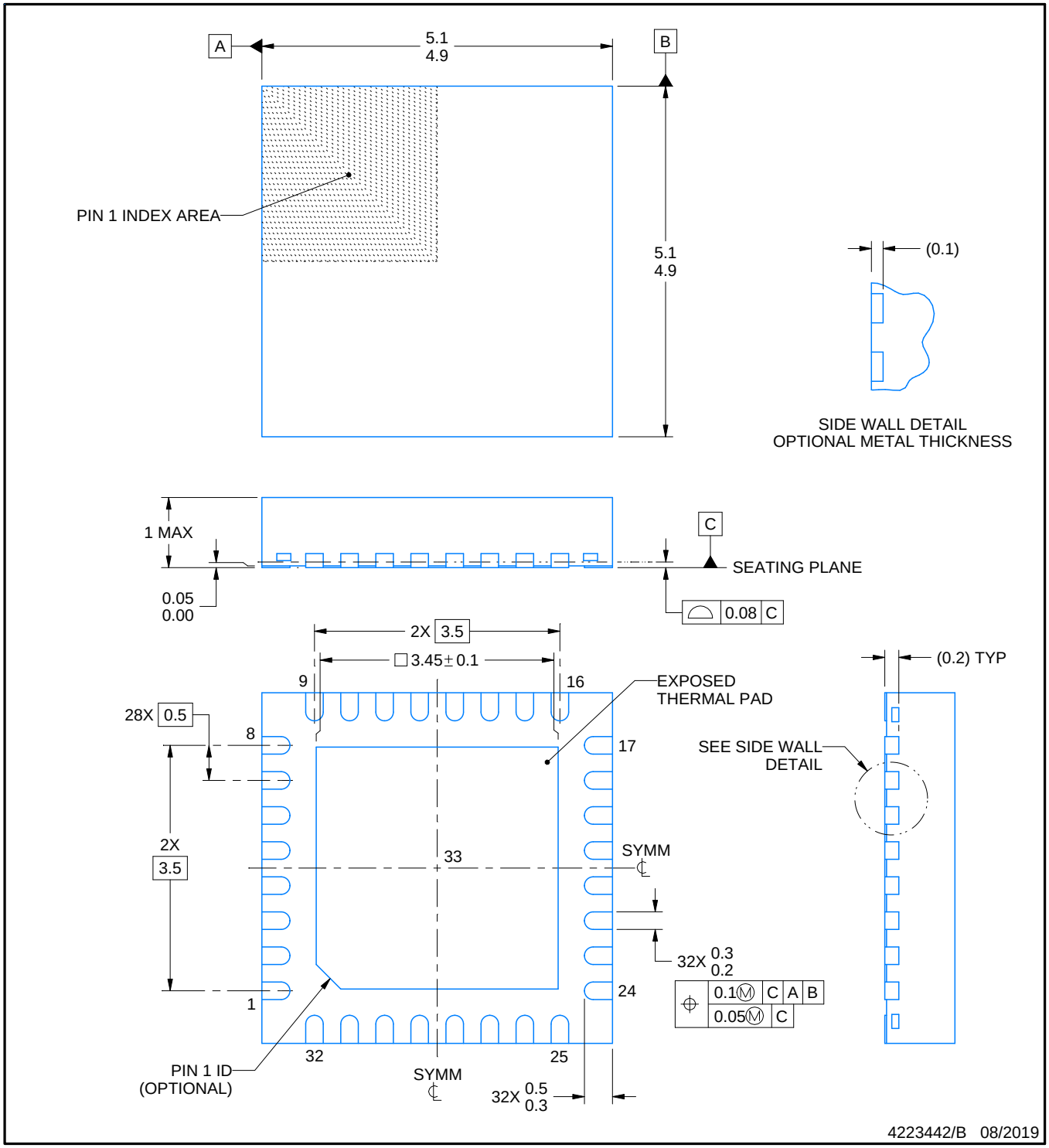
4224745/A

RHB0032E

PACKAGE OUTLINE

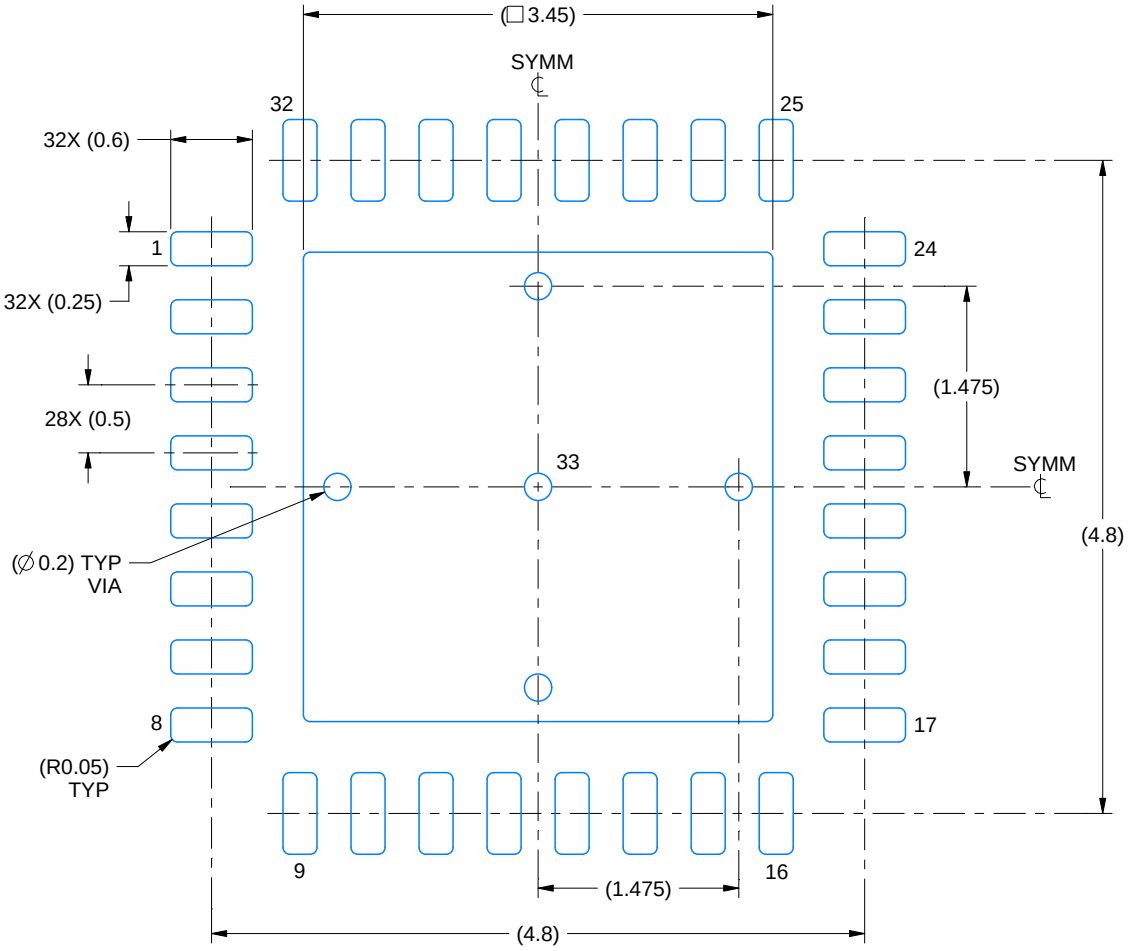
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

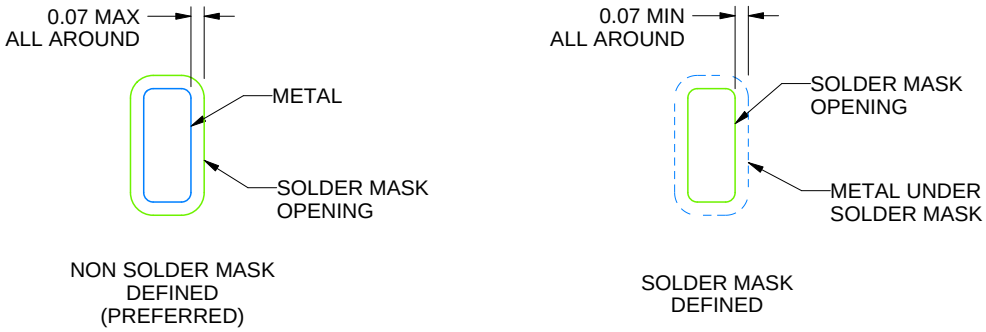


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

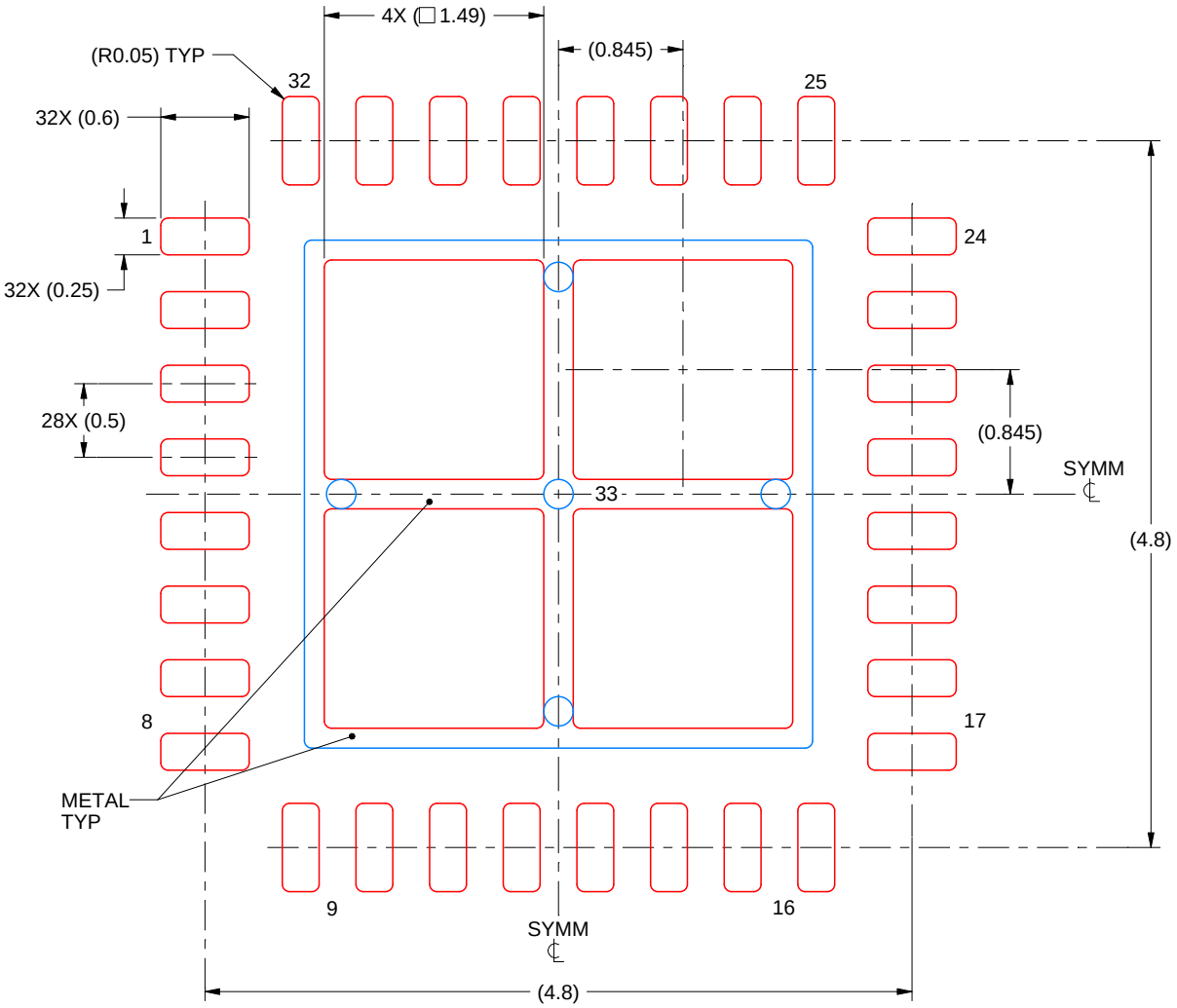


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

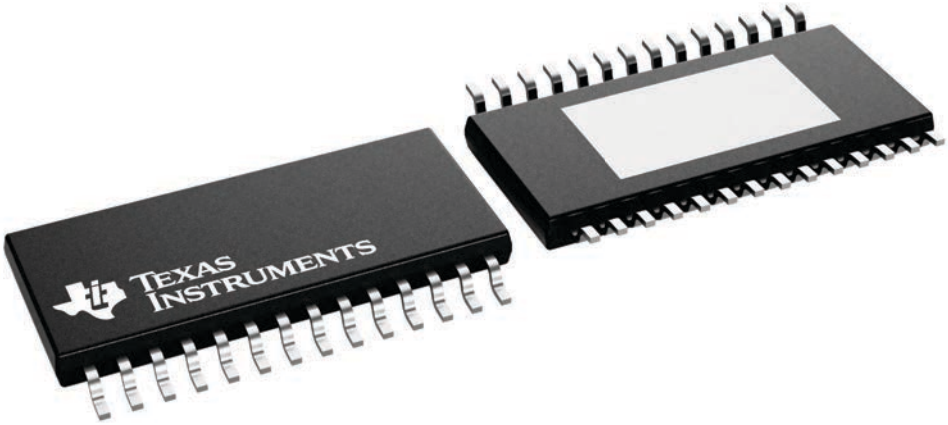
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

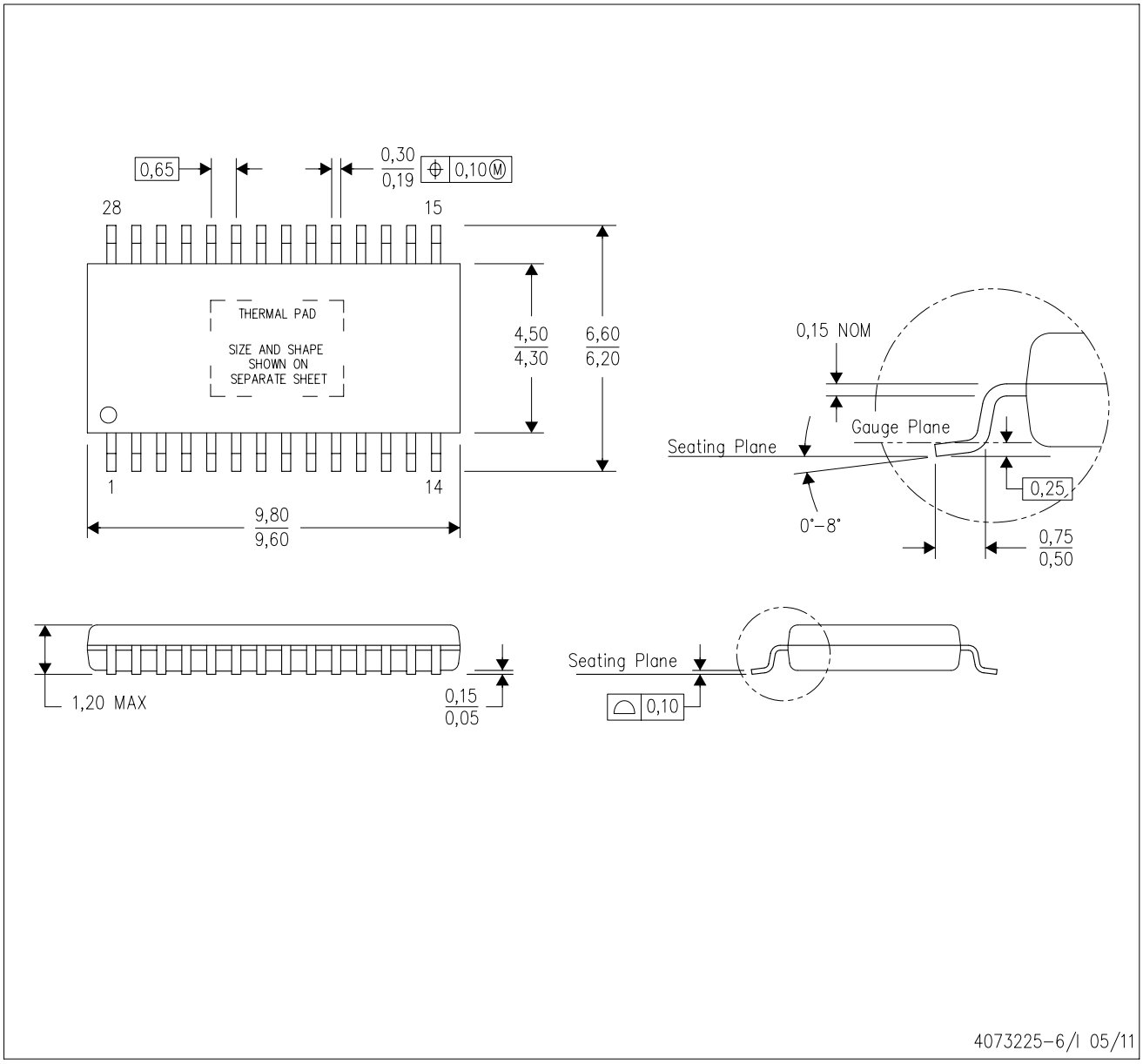
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

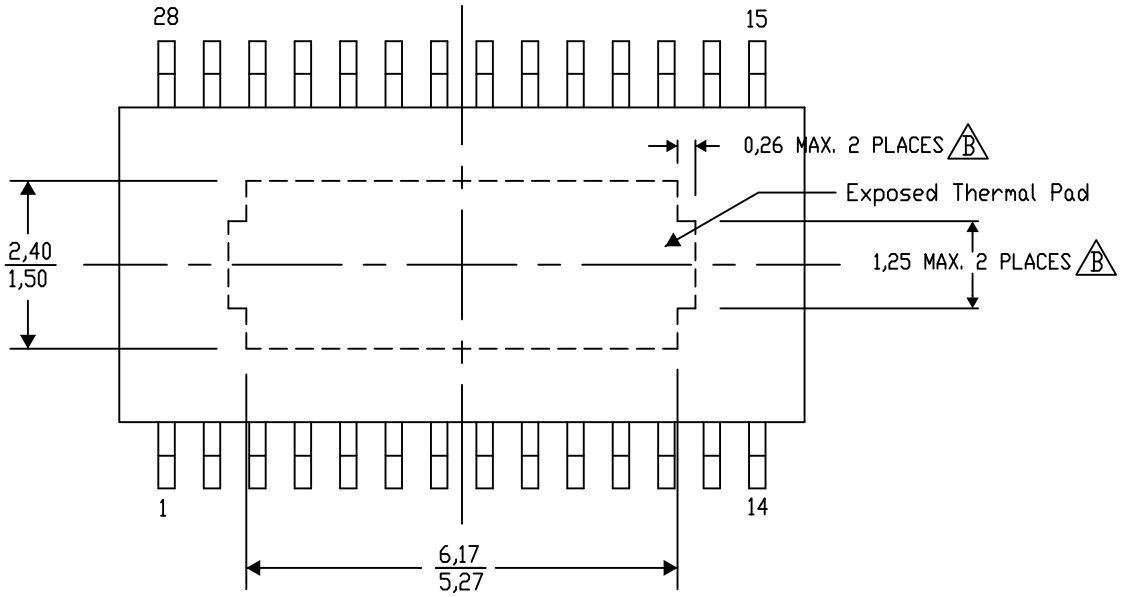
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

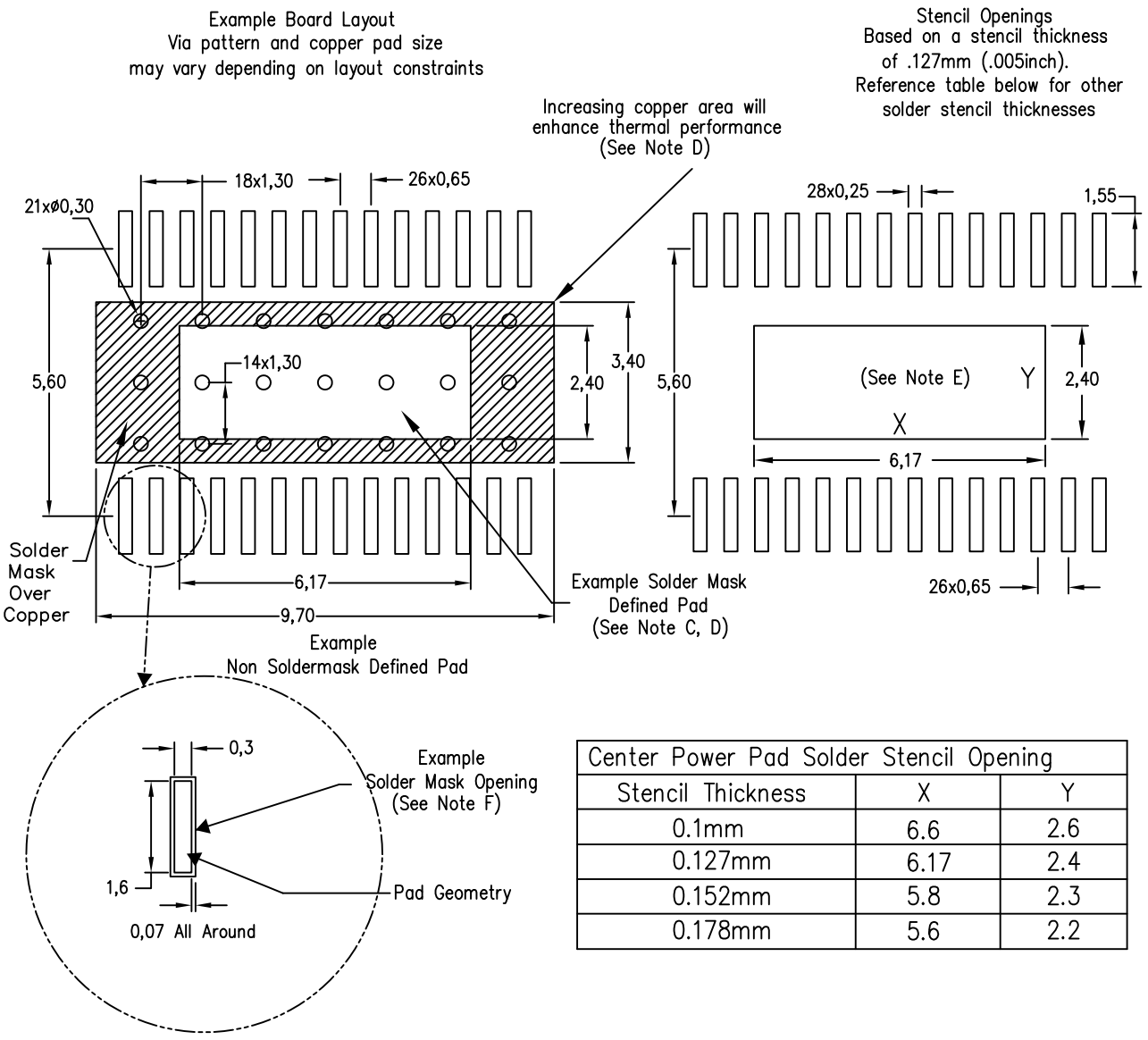
4206332–33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

4207609–19/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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