# TPS715xx-Q1 50-mA, 24-V, 3.2-µA Supply Current Low-Dropout Linear Regulators in SC70 Package

## 1 Features

- Qualified for Automotive Applications
  - Automotive Grade 1 (Q-temperature Range)
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- 24-V Maximum Input Voltage
- Low 3.2-µA Quiescent Current at 50 mA
- Stable With Any Capacitor (> 0.47 µF)
- 50-mA Low-Dropout Regulator
- Available in 2.5 V, 3 V, 3.3 V, 5 V, and Adjustable (1.2 V to 15 V)
- Minimum and Maximum Specified Current Limit
- 5-Pin SC70 and SOT (DCK) Package
- –40°C to 125°C Specified Junction Temperature Range

## 2 Applications

- Ultra-Low-Power Microcontrollers
- Cellular and Cordless Handsets
- Portable- and Battery-Powered Equipment

## 3 Description

The TPS715xx-Q1 low-dropout (LDO) voltage regulators offer the benefits of high input voltage, LDO voltage, low-power operation, and miniaturized packaging. The devices, which operate over an input range of 2.5 V to 24 V, are stable with any capacitor (>0.47 µF). The LDO voltage and low quiescent current allow operations at extremely low power levels. Therefore, the devices are ideal for powering battery-management ICs. Specifically, since the devices are enabled as soon as the applied voltage reaches the minimum input voltage, the output is quickly available to power continuously operating battery-charging ICs.

The usual PNP pass transistor has been replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the LDO voltage, typically 415 mV at 50 mA of load current, is directly proportional to the load current. The low quiescent current (3.2 µA typical) is stable over the entire range of output load current (0 mA to 50 mA).

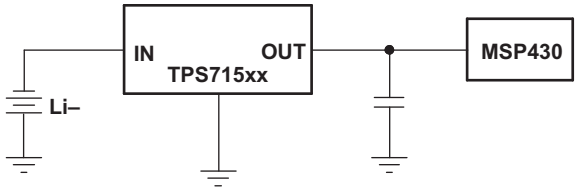
**Table 1. Device Information(1)(2)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS715xx-Q1 | SC70 (5) | 2.00 mm × 1.25 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Contact Texas Instruments for other voltage options between 1.25 V and 5.85 V.

**Simplified Schematic**



## Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision G (July 2013) to Revision H** — **Page**

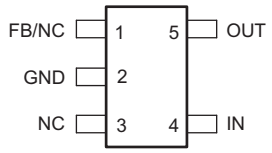
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation*section, *Power Supply Recommendations*section, *Layout*section, *Device and Documentation Support*section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

**Changes from Revision F (August 2011) to Revision G** — **Page**

- Added Grade 1 and HBM and CDM classification to features list ... 1
- Changed CDM absolute maximum value from 500 to 750 ... 3
- Added ESD classifications for HBM and CDM models in *ABSOLUTE MAXIMUM RATINGS* table ... 3
- Added additional test condition to Output current limit in *ELECTRICAL CHARACTERISTICS* table, and added $V_{IN}$ value to condition to differentiate conditions ... 4

# 5 Pin Configuration and Functions

**DCK Package**
**5-Pin SC70**
**Top View**




**Pin Functions**

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | SC70 | | | |
| | FIXED | ADJ. | | |
| FB | | 1 | Input | Adjustable version only. This terminal is used to set the output voltage. |
| NC | 1 | | NC | No connection |
| GND | 2 | 2 | GND | Ground |
| NC | 3 | 3 | NC | No connection |
| IN | 4 | 4 | Input | Input supply. |
| OUT | 5 | 5 | Output | Output of the regulator, any output capacitor ≥ 0.47 µF can be used for stability. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)(2)

| | MIN | MAX | UNIT |
|---|---|---|---|
| $V_{IN}$ | –0.3 | 24 | V |
| $V_{OUT}$ | –0.3 | 16.5 | V |
| Peak output current | Internally limited | | |
| Continuous total power dissipation | See *Thermal Information* | | |
| Junction temperature, $T_J$ | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 — All pins | ±500 | |
| | | Charged-device model (CDM), per AEC Q100-011 — Corner pins (1, 3, 4, and 5) | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 2.5 | 24 | V |
| $V_O$ | Output voltage | 1.2 | 15 | V |
| $I_O$ | Output current | | 50 | mA |
| $C_O$ | Output capacitor | 0.47 | | µF |
| $T_J$ | Operating junction temperature | –40 | 150 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TPS715xx-Q1 DCK (SC70) 5 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 261.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 71.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 48.5 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 47.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

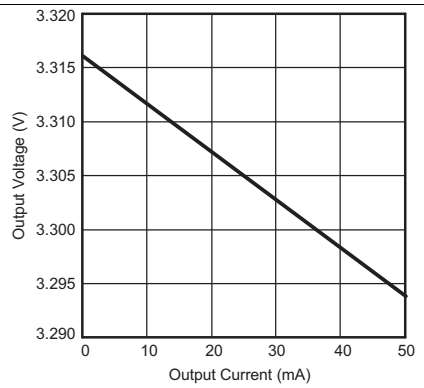
## 6.5 Electrical Characteristics

over operating junction temperature range ($T_J$ = –40°C to 125°C), $V_{IN}$ = $V_{OUT(NOM)}$ + 1 V, $I_{OUT}$ = 1 mA, $C_{OUT}$ = 1 µF, unless otherwise noted. Typical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage(1) | $I_O$ = 10 mA | 2.5 | | 24 | V |
| | | $I_O$ = 50 mA | 3 | | 24 | |
| | $V_{OUT}$ voltage range (TPS71501) | | 1.2 | | 15 | V |
| | $V_{OUT}$ accuracy(1) over $V_{IN}$, $I_{OUT}$, and T | $V_{IN}$ + 1 V ≤ $V_{IN}$ ≤ 24 V , 100 µA ≤ $I_{OUT}$ ≤ 50 mA | –4% | | 4% | |
| $I_{GND}$ | Ground-pin current | 0 mA ≤ $I_{OUT}$ ≤ 50 mA | | 3.2 | 12 | µA |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation | $I_{OUT}$ = 100 µA to 50 mA | | 22 | | mV |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Output voltage line regulation (1) | $V_{OUT}$ + 1 V < $V_{IN}$ ≤ 24 V | | 20 | 60 | mV |
| $V_n$ | Output noise voltage | BW = 200 Hz to 100 kHz, $C_{OUT}$ = 10 µF, $I_{OUT}$ = 50 mA | | 575 | | µVrms |
| $I_{CL}$ | Output current limit | $V_{OUT}$ = 0 V, $V_{IN}$ ≥ 3.5 V | 125 | | 750 | mA |
| | | $V_{OUT}$ = 0 V, $V_{IN}$ < 3.5 V | 90 | | 750 | |
| PSRR | Power-supply ripple rejection | f = 100 kHz, $C_{OUT}$ = 10 µF | | 60 | | dB |
| $V_{DO}$ | Dropout voltage, $V_{IN}$ = $V_{OUT(NOM)}$ – 1 V | $I_{OUT}$ = 50 mA | | 415 | 750 | mV |

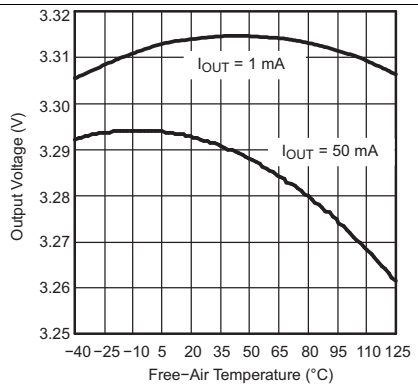
(1) Minimum $V_{IN}$ = $V_{OUT}$ + $V_{DO}$ or the value shown for input voltage in this table, whichever is greater.

## 6.6 Typical Characteristics



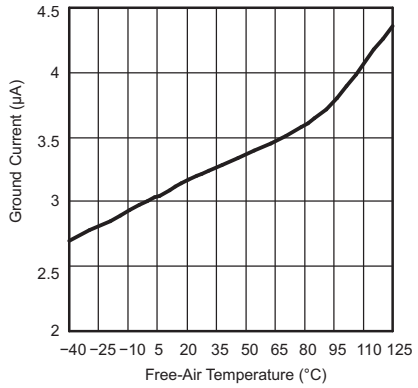

$V_{IN}$ = 4.3 V $C_{OUT}$ = 1 µF $T_J$ = 25°C

**Figure 1. Output Voltage vs Output Current**



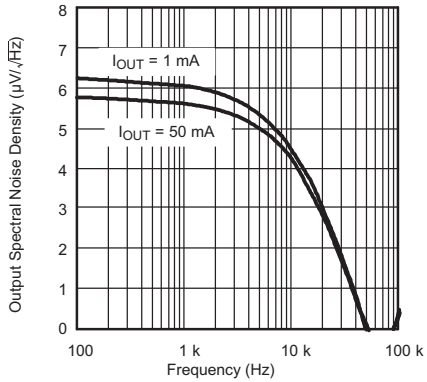

$V_{IN}$ = 4.3 V $C_{OUT}$ = 1 µF

**Figure 2. Output Voltage vs Free-air Temperature**



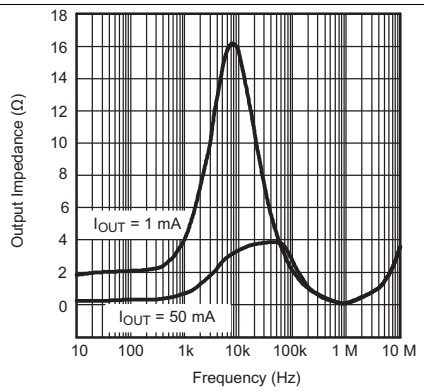

$V_{IN}$ = 4.3 V $V_{OUT}$ = 3.3 V $I_{OUT}$ = 1 µF

**Figure 3. Quiescent Current vs Free-air Temperature**



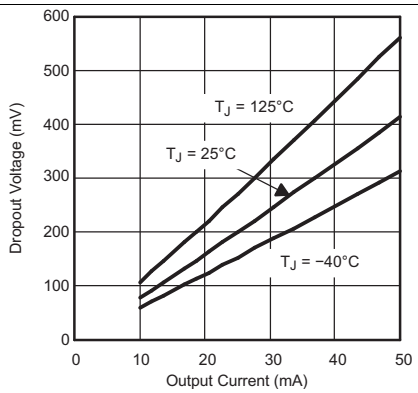

$V_{IN}$ = 4.3 V $V_{OUT}$ = 3.3 V $C_{OUT}$ = 1 µF

**Figure 4. Output Spectral Noise Density vs Frequency**




$V_{IN}$ = 4.3 V $V_{OUT}$ = 3.3 V $C_{OUT}$ = 1 µF
$T_J$ = 25°C

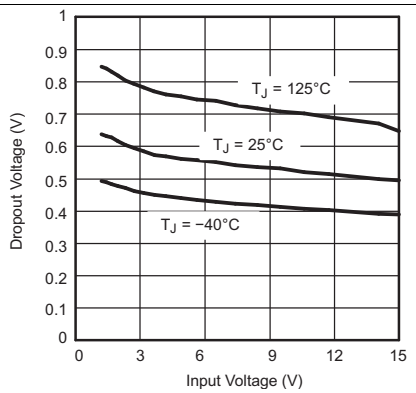
**Figure 5. Output Impedance vs Frequency**




$V_{IN}$ = 3.2 V $C_{OUT}$ = 1 µF

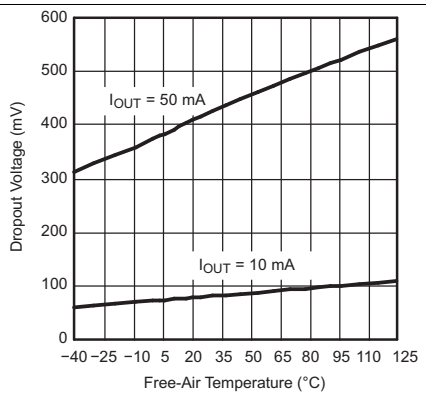
**Figure 6. Dropout Voltage vs Output Current**

## Typical Characteristics (continued)



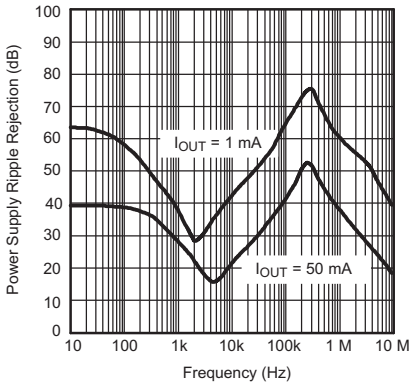

$I_{OUT}$ = 50 mA

**Figure 7. TPS71501 Dropout Voltage vs Input Voltage**



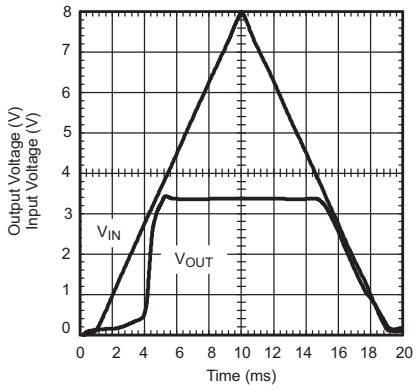

$V_{IN}$ = 3.2 V

**Figure 8. Dropout Voltage vs Free-air Temperature**



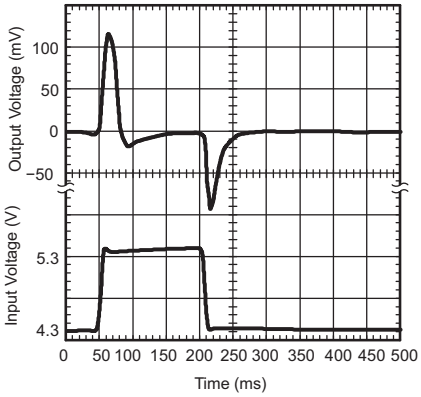

$V_{IN}$ = 4.3 V $V_{OUT}$ = 3.3 V $C_{OUT}$ = 10 µF
$T_J$ = 25°C

**Figure 9. Power-supply Ripple Rejection vs Frequency**



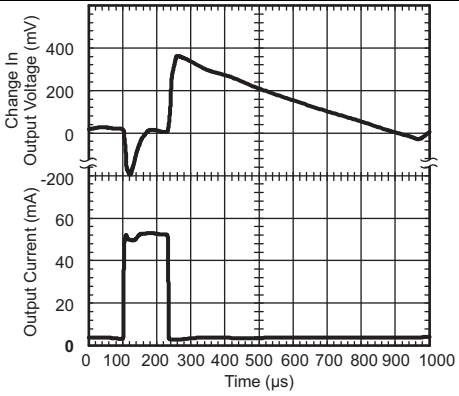

$V_{OUT}$ = 3.3 V $R_L$ = 66 Ω $C_{OUT}$ = 10 µF

**Figure 10. Power Up and Power Down**




$V_{OUT}$ = 3.3 V $I_{OUT}$ = 50 mA $C_{OUT}$ = 10 µF

**Figure 11. Line Transient Response**




$V_{IN}$ = 4.3 V $V_{OUT}$ = 3.3 V $C_{OUT}$ = 10 µF

**Figure 12. Load Transient Response**

# 7 Detailed Description

## 7.1 Overview

The TPS715xx-Q1 series of low-dropout (LDO) voltage regulators offer the benefits of high input voltage, LDO voltage, low-power operation, and miniaturized packaging. The devices, which operate over an input range of 2.5 V to 24 V, are stable with any capacitor (> 0.47 µF). The LDO voltage and low quiescent current allow operations at extremely low power levels. Therefore, the devices are ideal for powering battery-management ICs. Specifically, since the devices are enabled as soon as the applied voltage reaches the minimum input voltage, the output is quickly available to power continuously operating battery-charging ICs.

## 7.2 Functional Block Diagram

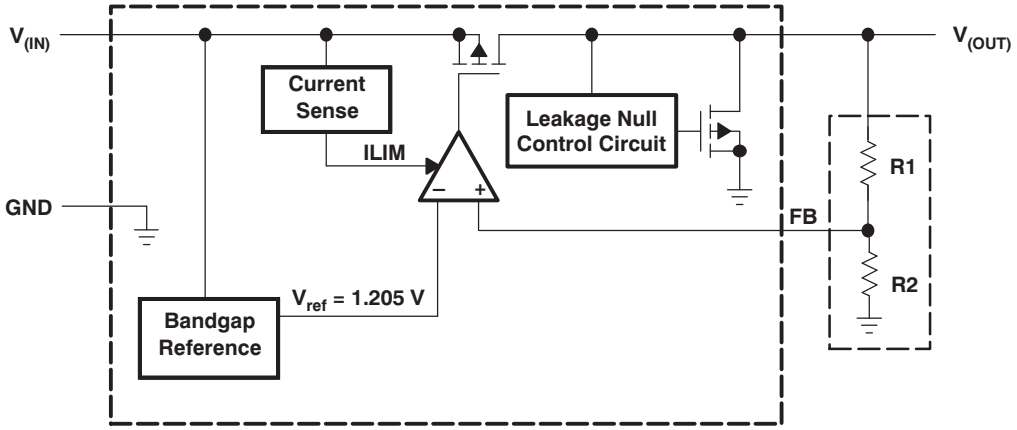



**Figure 13. Functional Block Diagram—Adjustable Version**

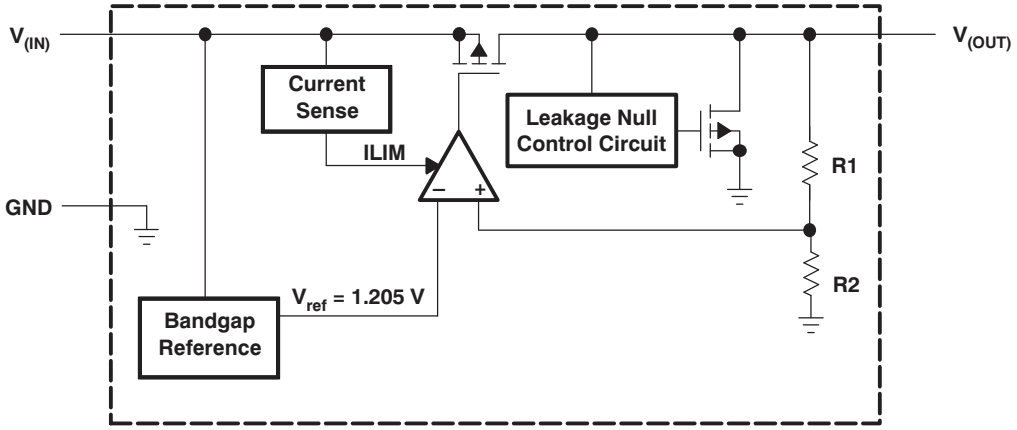



**Figure 14. Functional Block Diagram—Fixed Version**

## 7.3 Feature Description

### 7.3.1 Regulator Protection

The TPS715xx-Q1 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

## Feature Description (continued)

### 7.3.2 Current Limit

The TPS715xx-Q1 features internal current limiting. During normal operation, the TPS715xx-Q1 limits output current to approximately 500 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Take care not to exceed the power dissipation ratings of the package.

### 7.3.3 Adjustable Output Voltage

TPS715xx-Q1 provides both fixed output version and adjustable output version. 2.5 V, 3 V, 3.3 V, and 5 V outputs are available for fixed output version. The range for adjustable output is from 1.2 V to 15 V. This can be realized by adjusting the resistor divider on the FB pin.

## 7.4 Device Functional Modes

Table 2 provides a quick comparison between the normal, dropout, and disabled modes of operation.

**Table 2. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | |
|---|---|---|
| | $V_{IN}$ | $I_{OUT}$ |
| Normal | VIN > $V_{OUT(nom)}$ + $V_{DO}$ | $I_{OUT}$ < $I_{CL}$ |
| Dropout | VIN < $V_{OUT(nom)}$ + $V_{DO}$ | $I_{OUT}$ < $I_{CL}$ |
| Disabled | — | — |

### 7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage (VOUT(nom) + VDO).
- The output current is less than the current limit ($I_{OUT}$ < $I_{CL}$).
- The device junction temperature is less than 125°C.

### 7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPS715xx-Q1 family of LDO regulators has been optimized for ultra-low power applications such as the MSP430 microcontroller. Its ultralow supply current maximizes efficiency at light loads and its high input voltage range makes it suitable for supplies such as unconditioned solar panels.

### 8.1.1 Programming the TPS71501 Adjustable LDO Regulator

The output voltage of the TPS71501 adjustable regulator is programmed using an external resistor divider as shown in Figure 15. The output voltage is calculated using Equation 1.

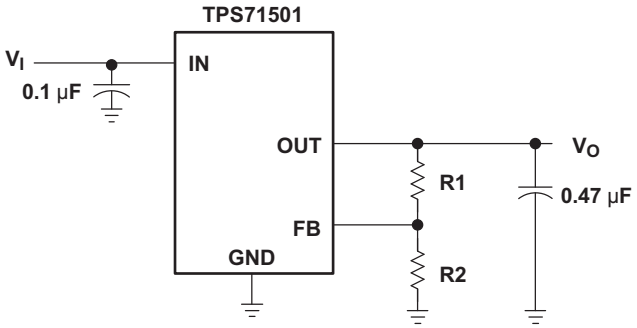
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where

- $V_{REF}$ = 1.205 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 1.5-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases $V_O$. The recommended design procedure is to choose R2 = 1 MΩ to set the divider current at 1.5 µA and then calculate R1 using Equation 2.

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$




**OUTPUT VOLTAGE PROGRAMMING GUIDE**

| OUTPUT VOLTAGE | R1 | R2 |
|---|---|---|
| 1.8 V | 0.499 MΩ | 1 MΩ |
| 2.8 V | 1.33 MΩ | 1 MΩ |
| 5 V | 3.16 MΩ | 1 MΩ |

**Figure 15. TPS71501 Adjustable LDO Regulator Programming**

## 8.2 Typical Application

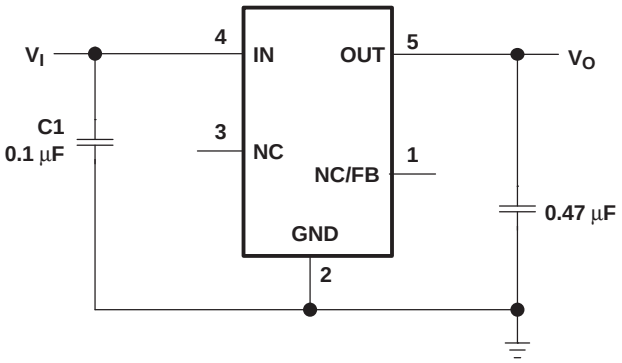



**Figure 16. Typical Application Circuit (Fixed Voltage Version)**

### 8.2.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

**Table 3. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUES |
|---|---|
| Input voltage range | 4.3-24 V |
| Input capacitor | 0.1 µF |
| Output voltage | 3.3 V |
| Output current rating | 50 mA |
| Output capacitor range | 0.47 µF |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 External Capacitor Requirements*

Although not required, a 0.047-µF or larger input bypass capacitor, connected between IN and GND and located close to the device, is recommended to improve transient response and noise rejection of the power supply as a whole. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

The TPS715xx-Q1 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. Any capacitor (including ceramic and tantalum) ≥0.47 µF properly stabilizes this loop.

### 8.2.3 Application Curves

Figure 17 shows the input voltage ramp from 0 to just below 24 V (CH1), the 3.3-V regulated output voltage (CH3), and the 50-mA output current (CH4). The scale on CH4 is 50 mA/div.

Figure 18 shows the load transient waveform of the TPS71533-Q1, output current is switched between 0 mA and 50 mA (CH4). Input voltage is set at 4.3 V(CH1). Output voltage DC (CH3) and output voltage AC(CH2) are also shown in the waveform.

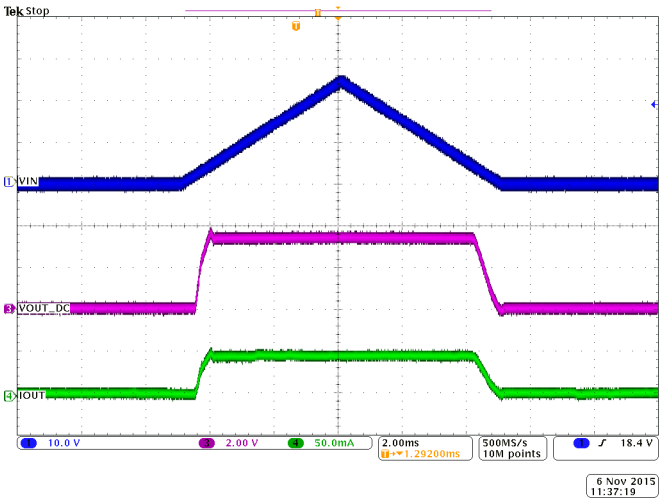



**Figure 17. TPS71533-Q1 Power Up and Power Down Waveform**

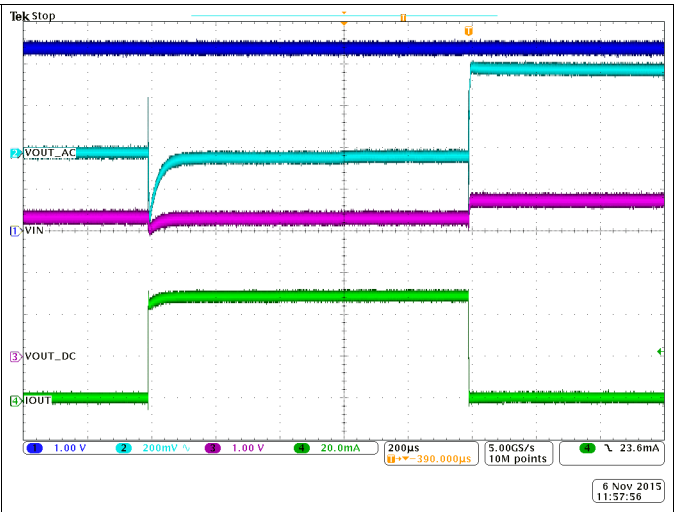



**Figure 18. TPS71533-Q1 Load Transient Waveform**

## 9 Power Supply Recommendations

The device is designed to operate from a max 24V input voltage supply. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS715xx-Q1 device, it is recommended to add an µF level bulk capacitor and an nF level ceramic bypass capacitor at the input.

## 10 Layout

### 10.1 Layout Guidelines

For the LDO power supply, layout is an important step. If layout is not carefully designed, the regulator could not deliver enough output current because of the thermal limitation. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, it is recommended to spread the ground copper as large as possible. Figure 19 shows an example layout.

### 10.2 Layout Example

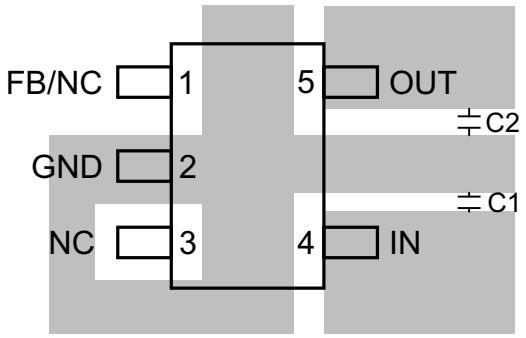



**Figure 19. TPS715xx-Q1 Layout Example**

### 10.3 Power Dissipation and Junction Temperature

To ensure reliable operation, worst-case junction temperature should not exceed 125°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, $P_D$, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using Equation 3.

## Power Dissipation and Junction Temperature (continued)

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

where

- $T_J$max = Maximum allowable junction temperature
- $R_{\theta JA}$ = Thermal resistance junction-to-ambient for the package (see the Dissipation Ratings table)
- $T_A$ = Ambient temperature (3)

The regulator dissipation is calculated using Equation 4.

$$P_D = \left(V_I - V_O\right) \times I_O \quad (4)$$

Power dissipation resulting from quiescent current is negligible.

# 11 Device and Documentation Support

## 11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 4. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TPS71501-Q1 | Click here | Click here | Click here | Click here | Click here |
| TPS71525-Q1 | Click here | Click here | Click here | Click here | Click here |
| TPS71530-Q1 | Click here | Click here | Click here | Click here | Click here |
| TPS71533-Q1 | Click here | Click here | Click here | Click here | Click here |
| TPS71550-Q1 | Click here | Click here | Click here | Click here | Click here |

## 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71501QDCKRQ1 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | ANS | Samples |
| TPS71525QDCKRQ1 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | ANU | Samples |
| TPS71530QDCKRQ1 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | ANV | Samples |
| TPS71533QDCKRQ1 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | ANW | Samples |
| TPS71550QDCKRQ1 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | ANX | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF TPS715-Q1 :**

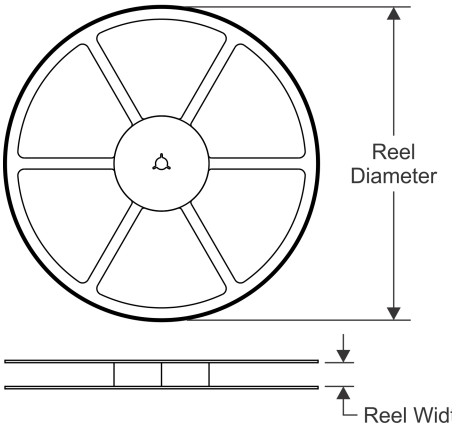
- Catalog: TPS715

NOTE: Qualified Version Definitions:

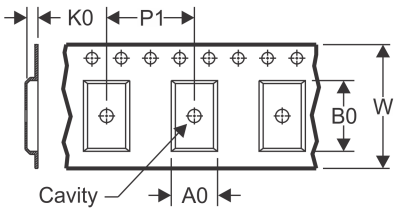
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

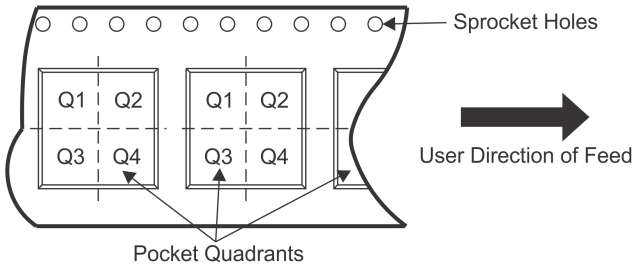



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

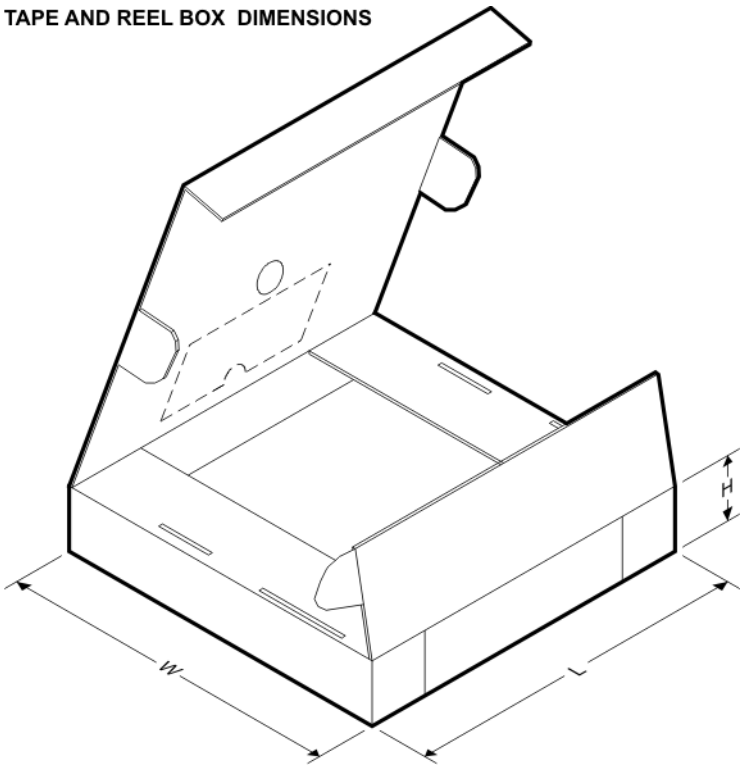
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71501QDCKRQ1 | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71525QDCKRQ1 | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71533QDCKRQ1 | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |

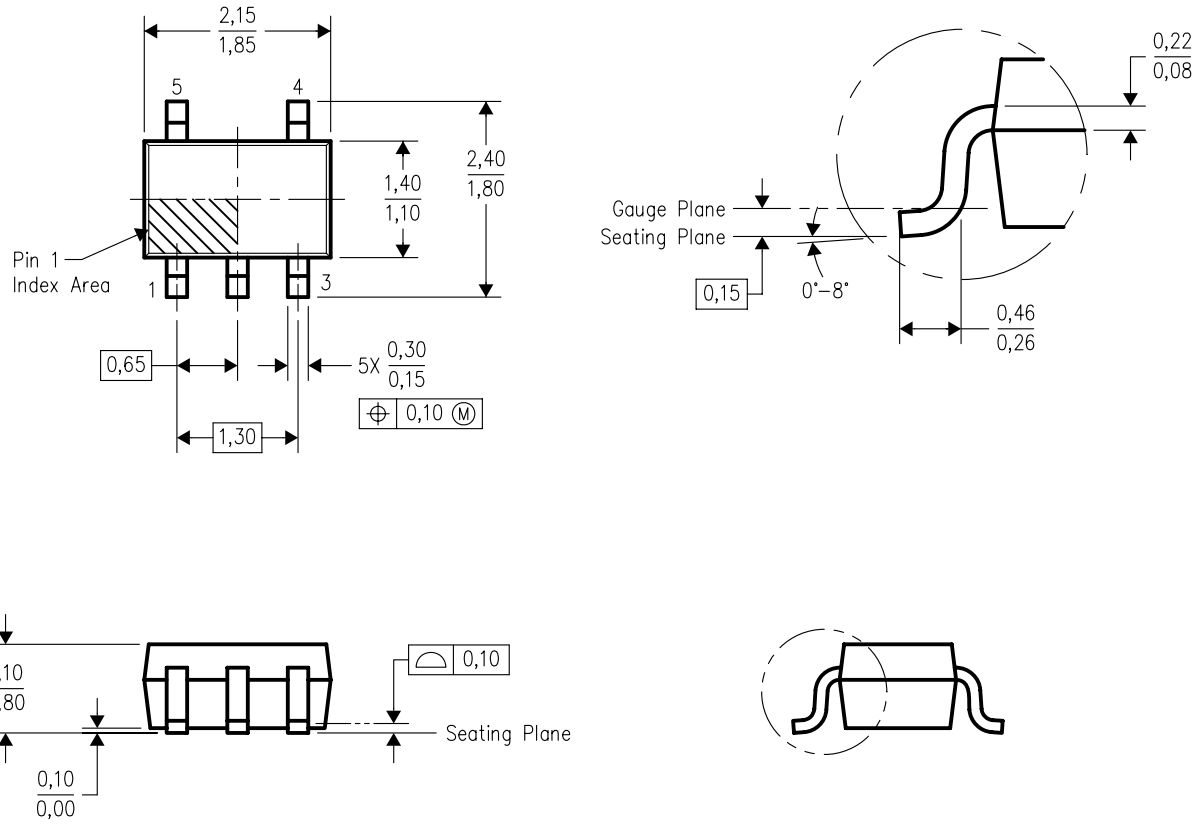
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS71501QDCKRQ1 | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71525QDCKRQ1 | SC70 | DCK | 5 | 3000 | 340.0 | 340.0 | 38.0 |
| TPS71533QDCKRQ1 | SC70 | DCK | 5 | 3000 | 340.0 | 340.0 | 38.0 |

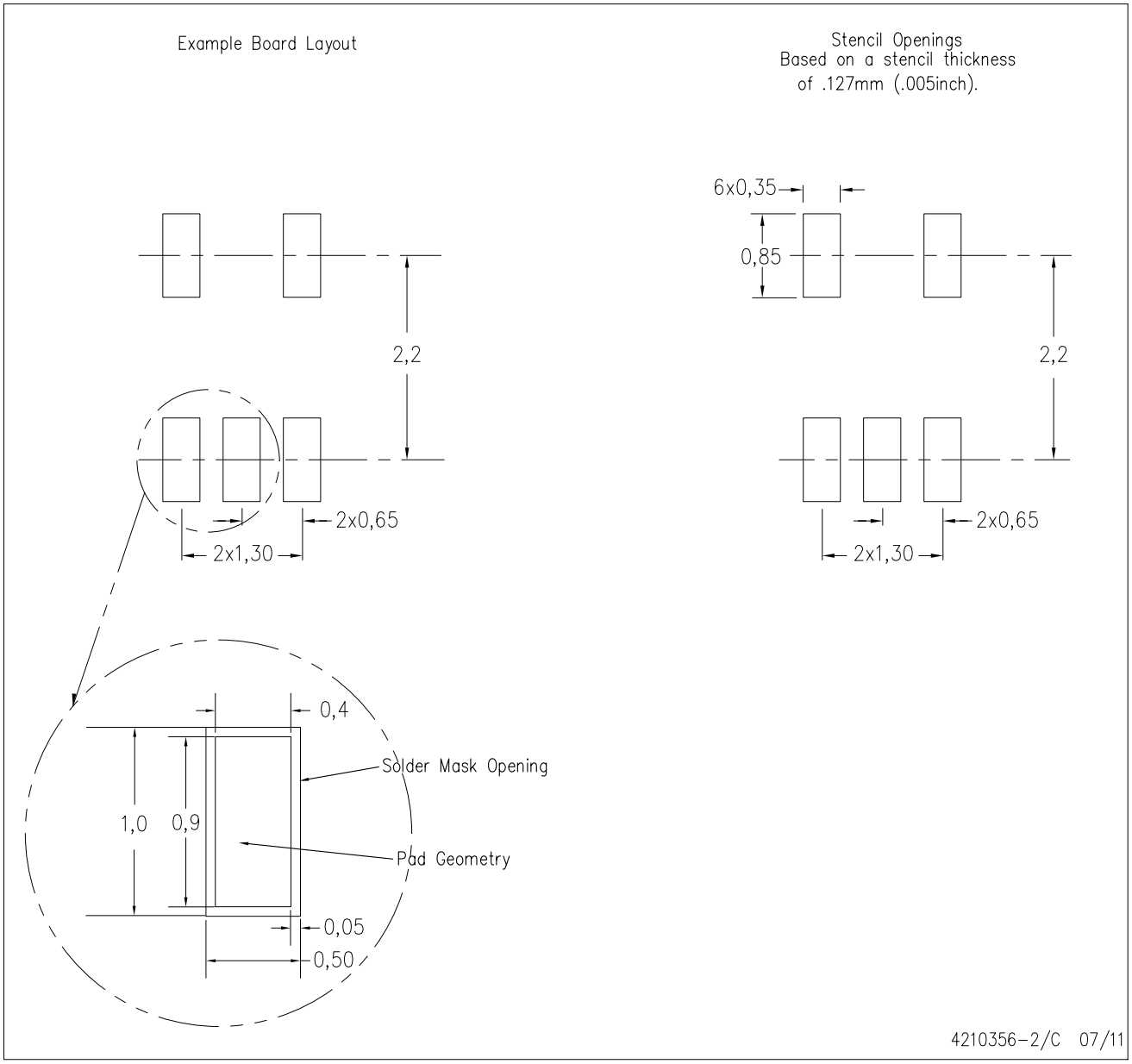
## DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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