TAS576xM 2x50-W/4-Ω PurePath™智能放大器

1 特性

- PurePath 智能放大器：
  - 优化和保护动圈式扬声器
  - 低音 Q 补偿和频率扩展：音量更高、低音增强、清晰度更佳且保真度更高。
  - 热量和偏移限制。
- 立体声 D 类放大器：
  - 宽电源范围：4.5V 至 26.4V
  - 宽负载范围：2Ω 至 8Ω
  - 高输出电流：2x 7.5A
  - 峰值输出功率 2x 50W/4Ω
  - 连续功率：2x 20W（不使用散热器）
  - 电源、静音和待机开/关时无喀哒声和噼啪声
  - 低输出噪声：<60µVrms（12V 供电时）；<90µVrms（24V 供电时）
  - 低总谐波失真和噪声 (THD+N)：< 0.02%（1W/4Ω、1kHz 时）
  - 热保护、过流保护和短路保护
- 可配置的数字音频处理器。
  - 降频混频和具有 10 个 BiQuad 的定制 EQ
- 数字音频接口：I^2S 或时分复用 (TDM) 输入
  - 44.1kHz 和 48kHz 快速 (FS)
  - 可配置的数字输出
- 多段数模转换器 (DAC)，去抖动性能出色
- 集成高性能音频锁相环 (PLL)
- I^2C 控制
- 48 引脚 PowerPAD™散热薄型小外形尺寸 (HTSSOP) 或超薄型四方扁平无引线 (VQFN) 封装

2 应用

- 音频接口盒
- 条形音箱
- 笔记本电脑
- 一体化计算机
- 数字电视

3 说明

TAS576xM PurePath 智能放大器不仅可增强低音效果和音质保真度，还可提供更高的音量，同时将扬声器驱动至其热限值和机械限值。

TAS576xM 包含两个桥接负载 (BTL) D 类放大器，峰值功率高达 2x50W/4Ω。在热保护方面，该放大器针对典型扬声器而设计，可处理扬声器音圈升温期间的高温峰值，然后将其平均功率降至安全限值。

该器件具有 4.5V 至 26.4V 宽电源范围，支持从双节锂离子电池到固定 24V 电源各类不同的电源选项。

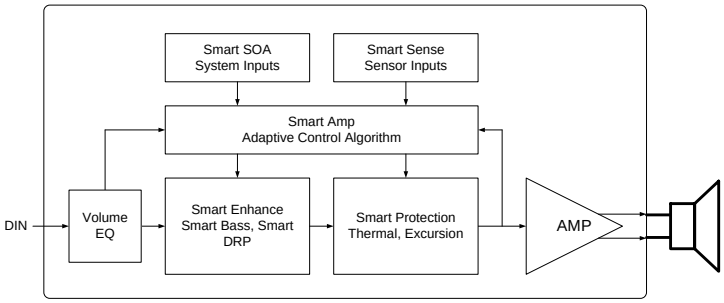
凭借德州仪器 (TI) 的 PurePath Smart Amp 技术，可更多地以峰值功率（而非平均额定功率）来驱动扬声器，且不必担心因偏移或热过载而损坏扬声器。

器件信息(1)

器件编号	封装	封装尺寸（标称值）
TAS5766M	HTSSOP (48)	12.50mm x 6.10mm
TAS5768M	VQFN (48)	7.00mm x 5.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

智能放大器概览



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (September 2014) to Revision D — **Page**

- Added paragraph to clarify the 3-wire mode of I2S operation ... 41

Changes from Revision B (September 2014) to Revision C — **Page**

- Added NOTE and additional descriptive text to Applications and Implementation section. ... 39
- Moved Detailed Register Map Descriptions section ... 51

Changes from Revision A (June 2014) to Revision B — **Page**

- Added descriptions for CDST[5] through CDST[0] in Register 94 (Hex 0x5E); and changed Bit 6 description from CDST[6:0] to CDST[6]. ... 69

Changes from Original (September 2013) to Revision A — **Page**

- 将数据表更改为最新格式；将器件信息表添加到了第一页。 ... 1
- 添加了 TAS5768M 器件 ... 1
- 添加了 RMT 封装选项 ... 1

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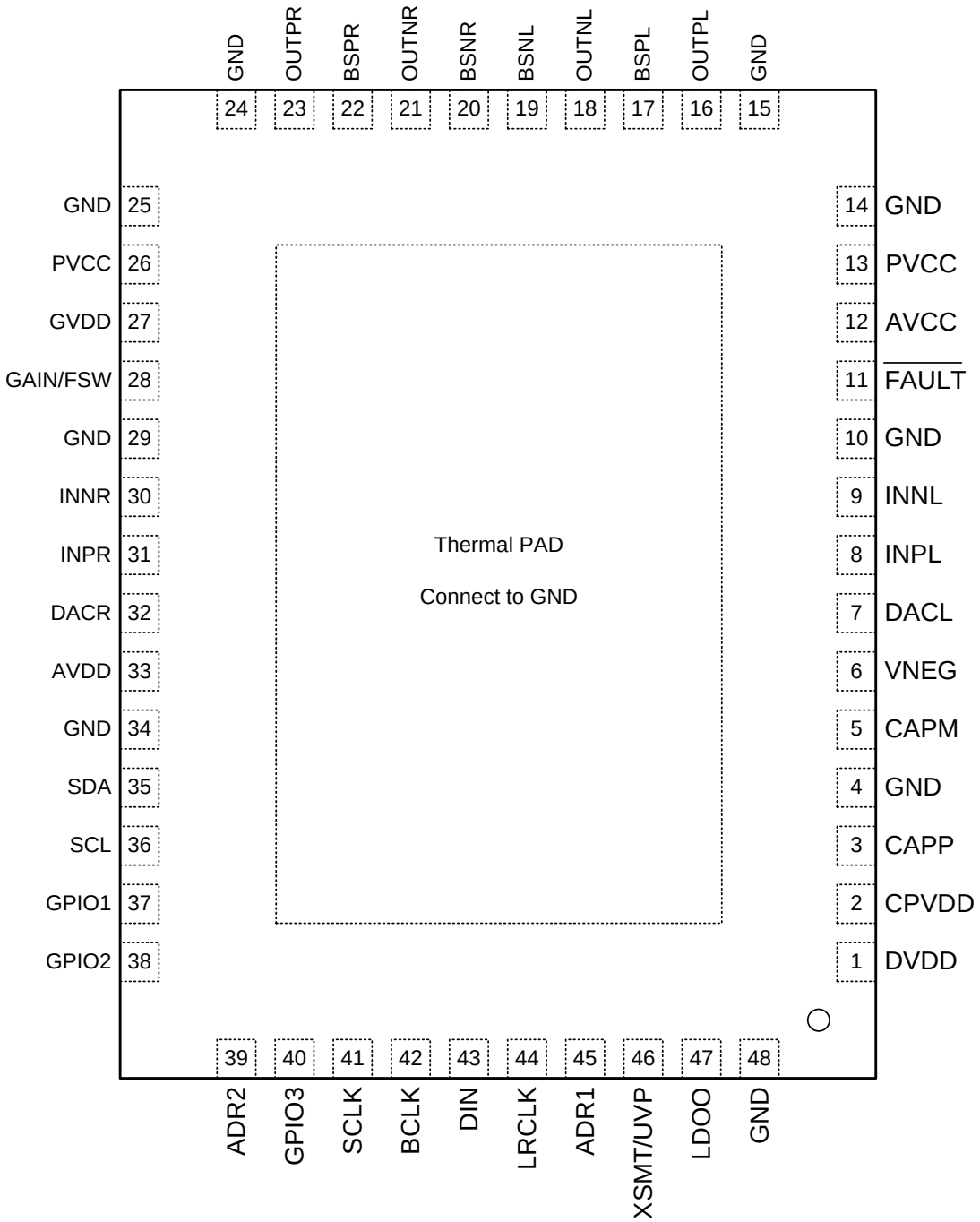
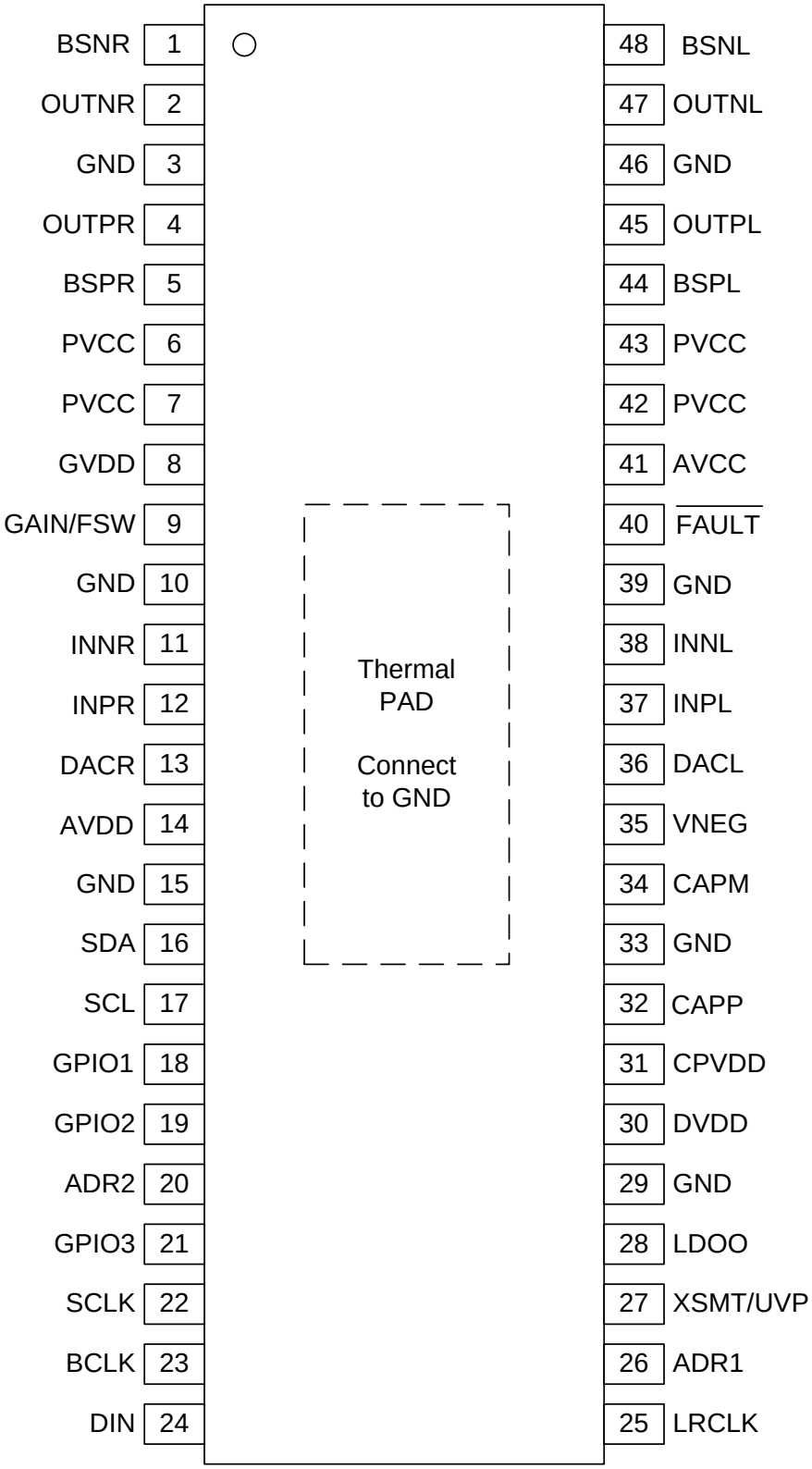
5 Pin Configuration and Functions

RMT Package
48-Pin VQFN
Top View



DCA Package
48-Pin HTSSOP
Top View



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Pin Functions

SYMBOL	HTTSOP PIN No.	VQFN PIN No.	TYPE(1)	DESCRIPTION
ADR1	26	45	I	LSB address select bit for I^2C
ADR2	20	39	I	2nd LSB address select bit for I^2C
AVCC	41	12	PI	Analog Supply – connect to PVCC
AVDD	14	33	PI	Analog Supply
BCLK	23	42	I	Audio data bit clock input
BSNL	48	19	BST	Boot strap negative Left channel output, connect to 220 nF X7R ceramic cap to OUTNL
BSNR	1	20	BST	Boot strap negative Right channel output, connect to 220 nF X7R ceramic cap to OUTNR
BSPL	44	17	BST	Boot strap positive Left channel output, connect to 220 nF X7R ceramic cap to OUTPL
BSPR	5	22	BST	Boot strap positive Right channel output, connect to 220 nF X7R ceramic cap to OUTPR
CAPM	34	5		Charge pump flying capacitor pin for negative rail
CAPP	32	3		Charge pump flying capacitor pin for positive rail
CPVDD	31	2	PI	Charge pump power supply, 3.3 V
DACL	36	7	O	Analog output from DAC left channel, ground centered
DACR	13	32	O	Analog output from DAC Right channel, ground centered
DIN	24	43	I	Audio data input
DVDD	30	1	PI	Digital power supply, 3. 3 V
$\overline{\text{FAULT}}$	40	11	OD	General fault reporting, Open Drain, High = normal operation, Low = fault condition
GAIN/FSW	9	28	I	Sets power stage Gain and selects output switching frequency
GND	3, 10, 15, 29, 33, 39, 46	4, 10, 14, 15, 24, 25, 29, 34, 48	G	Ground
GPIO1	18	37	I/O	General purpose digital input and output port
GPIO2	19	38	I/O	General purpose digital input and output port
GPIO3	21	40	I/O	General purpose digital input and output port
GVDD	8	27	PBY	Internal Gate drive supply, connect 1uF to GND
INNL	38	9	I	Negative audio input for Left channel. Internally biased at 3 V
INNR	11	30	I	Negative audio input for Right channel. Internally biased at 3 V
INPL	37	8	I	Positive audio input for Left channel. Internally biased at 3 V
INPR	12	31	I	Positive audio input for Right channel. Internally biased at 3 V
LDOO	28	47	PBY	Internal logic supply rail pin for decoupling, 1.8 V, connect 1 µF to GND
LRCLK	25	44	I	Audio data word clock input
OUTNL	47	18	PO	Negative Left channel output
OUTNR	2	21	PO	Negative Right channel output
OUTPL	45	16	PO	Positive Left channel output
OUTPR	4	23	PO	Positive Right channel output
PVCC	6, 7, 42, 43	13, 26	PI	4.5-V to 26.4-V Power supply
SCL	17	36	I	Input clock for I^2C
SCLK	22	41	I	System clock input (also referred to as master clock input)
SDA	16	35	I/O	Input data for I^2C
Thermal pad	49	49	G	Connect Thermal Pad to Ground
VNEG	35	6	PO	Negative charge pump rail pin for decoupling –3.3 V
XSMT/UVP	27	46	I	Soft mute control : Soft mute (Low) / soft un-mute (High)

(1) TYPE: BST=Boot Strap, PO=Power Output, G = General Ground, I= Input, O= Output, I/O = Input or Output, , PBY=Power Bypass, , PI=Power Input,.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage: PVCC, AVCC	–0.3	30	V
	AVDD, DVDD, CPVDD	–0.3	3.9	V
V_I	Input Voltage: INPL, INNL, INPR, INNR	–0.3	6.3	V
	Input Voltage: GAIN/FSW, $\overline{FAULT}$	–0.3	GVDD+0.3	V
	Digital Input Voltage: DVDD=3.3V	–0.3	3.9	V
T_A	Operating free-air temperature	–40	85	°C
T_J	Operating Junction temperature, digital die	–40	125	°C
	Operating Junction temperature, power die	–40	150	°C
Storage temperature, T_{stg}		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (2)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (3)	±500	

(1) Electrostatic discharge (ESD) measures device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
Vcc	Supply Voltage	PVCC, AVCC	4.5		26.4	V
Vdd		AVDD, DVDD, CPVDD	3	3.3	3.6	
V_{IH}	High level input voltage		2			V
V_{IL}	Low level input voltage				0.8	V
V_{OL}	Low level output voltage	$\overline{FAULT}$, R_{pullup} = 100 kΩ, PVCC = 26 V			0.8	V
R_L	Minimum load impedance	PVCC = 24 V	3.2	4		Ω
		PVCC = 18 V	2.5	3		
		PVCC = 12 V	1.8	2		
		PVCC = 6 V	0.9	1		
R_{L_PBTL}	PBTL Minimum load impedance	PVCC = 24 V	1.8	2.2		Ω
		PVCC = 18 V	1.4	1.6		
		PVCC = 12 V	1.0	1.2		
		PVCC = 6 V	0.5	0.6		
Lo	Output filter inductance	Minimum output filter inductance under short-circuit condition	1	4.7		µH

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6.4 Thermal Information

THERMAL METRIC[1]		TAS576xM		UNIT
		RMT (48 PINS)	DCA (48 PINS)	
		4 LAYER PCB[2]	2 LAYER PCB[3]	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30	30	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15	14	
$R_{\theta JB}$	Junction-to-board thermal resistance	6	13	
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.6	
ψ_{JB}	Junction-to-board characterization parameter	6	13	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.9	0.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For the PCB layout see the TAS576xMRMTEVM User Guide. A 4 layer 60x60mm 1oc PCB was used
(3) For the PCB layout see the TAS576xMDCAEVM User Guide. A 2 layer 60x60mm 1oc PCB was used

6.5 DC Electrical Characteristics

All specifications at T_A = 25°C, AVDD = CPVDD = DVDD = 3.3 V, f_S = 48 kHz, system clock = 512 f_S and 24-bit data, V_{CC} = 12 V to 24 V, R_L = 4 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
| VOS |	Class-D output offset voltage (measured differentially) Input is Bipolar Zero data	PV_{CC} = 12 V, gain set to 14 dB		1	10	mV
		PV_{CC} = 24 V, gain set to 20 dB		1.5	15	mV
$R_{DS(on)}$	Drain-source on-state resistance, measured pin to pin	VCC = 24 V, I_{out} = 500 mA, T_J = 25°C		120		mΩ
G	Analog Gain from INxx to OUTxx	Gain pin voltage < 3 V	13	14	15	dB
		Gain pin voltage > 3.3 V	19	20	21	dB
t_{on}	Turn-on time	XSMT = 2 V		1.5		ms
t_{OFF}	Turn-off time	XSMT = 0.8 V		0.8		ms
GVDD	Gate Drive Supply Voltage	IGVDD ≤ 200 µA		6.9		V

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6.6 AC Electrical Characteristics

All specifications at T_A = 25°C, AVDD = CPVDD = DVDD = 3.3V, f_S = 48kHz, system clock = 512f_S and 24-bit data, V_{CC} = 12V to 24V, R_L = 4 Ω unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Power supply ripple rejection	200 mV_{PP} ripple at 1 kHz, gain = 20 dB, zero input signal		–60		dB
P_O	Peak output power	THD+N = 10%, 1 kHz, 24-V supply, 8-Ω load		30		W
		THD+N = 10%, 1 kHz, 24-V supply, 4-Ω load		50		W
F_{sw}	Output switch frequency multiple of FS Gain set to 14 dB	Ra = 100 kΩ, Rb = open		8		
		Ra = 20 kΩ, Rb = 100 kΩ		10		
		Ra = 39 kΩ, Rb = 100 kΩ		12		
		Ra = 47 kΩ, Rb = 75 kΩ		16		
F_{sw}	Output switch frequency multiple of FS Gain set to 20 dB	Ra = 51 kΩ, Rb = 51 kΩ		8		
		Ra = 75 kΩ, Rb = 47 kΩ		10		
		Ra = 100 kΩ, Rb = 39 kΩ		12		
		Ra = 100kΩ, Rb = 20 kΩ		16		
THD+N	Total Harmonic Distortion + Noise	1W, 1 kHz, 4R load, 12 V supply		0.05%		
		1W, 1 kHz, 8R load, 24 V supply		0.05%		
V_N	Output integrated noise	20-22 kHz, A-weighted, 14 dB gain, 12 V supply		60		µV
		20-22 kHz, A-weighted, 20 dB gain, 24 V supply		85		µV
SNR	Signal to Noise Ratio	20-22 kHz, A-weighted, 14 dB gain, 12 V supply		103		dB
		20-22 kHz, A-weighted, 20 dB gain, 24 V supply		106		dB
	Crosstalk	V_O = 1 V_{rms}, 20 dB gain, 1 kHz, 4-Ω load		–90		dB
I_P	Peak output current	1 kHz, 10 ms, 3-Ω load, 24-V supply		7.5		A

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6.7 Electrical Characteristics

All specifications at T_A = 25°C, AVDD = CPVDD = DVDD = 3.3 V, f_S = 48 kHz, system clock = 512 f_S and 24-bit data, V_{CC} = 12 V to 24 V, R_L = 4 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		16	24	32	Bits
DATA FORMAT (PCM MODE)						
	Audio data interface format		I2S, left justified, right justified and TDM			
	Audio data bit length		16, 24, 32-bit acceptable			
	Audio data format		MSB First, 2s Complement			
f_S	Sampling frequency		8		48	kHz
CLOCKS						
	System clock frequency		64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, or 3072 F_{SCLK}, up to 50MHz			
	PLL input frequency /SCL Clock Frequency 400kHz)	Clock divider uses fractional divide D>0, P=1	6.7		20	MHz
		Clock divider uses integer divide D=0, P=1	1		20	MHz
DIGITAL INPUT/OUTPUT						
Logic Family: 3.3V LVCMOS compatible						
V_{IH}	High level input voltage		0.7xDV_{DD}			V
V_{IL}	low level input voltage				0.3 x DV_{DD}	V
I_{IH}	High level input current	V_{IN} = V_{DD}			10	µA
I_{IL}	low level input current	V_{IN} = 0 V			–10	µA
V_{OH}	High level output voltage	I_{OH} = –4 mA	0.8xDV_{DD}			V
V_{OL}	low level output voltage	I_{OL} = 4 mA			0.22 x DV_{DD}	V
DAC DYNAMIC PERFORMANCE, MEASURED ON DACL and DACR						
	THD+N at –1dB			–90		dB
	Dynamic range			109		dB
	Signal to noise ratio			109		dB
	Channel separation			109		dB
DAC ANALOG OUTPUT, MEASURED ON DACL and DACR						
	Output voltage			2.1		Vrms
	Gain error	| % | of FSR		2%	6%	
	Gain mismatch, channel to channel	| % | of FSR		1/2%	6%	
	Bipolar zero error	|At bipolar zero|		1	5	mV
POWER SUPPLY REQUIREMENTS						
DV_{DD}	Digital Supply Voltage		3	3.3	3.6	V
AV_{DD}	Analog Supply Voltage		3	3.3	3.6	V
	Charge-pump supply voltage		3	3.3	3.6	V
I_{DD}	DV_{DD} supply current at 3.3V	f_s = 48 kHz, Input is Bipolar Zero data		12	15	mA
		f_s = 48 kHz, Input is 1 kHz -1 dBFS data		12	15	mA
		f_s = N/A, power Down Mode		0.5	0.8	mA
I_{CC}	AVDD/ CPVDD supply current at 3.3V	f_s = 48 kHz, Input is Bipolar Zero data		11	16	mA
		f_s = 48 kHz, Input is 1kHz -1 dBFS data		24	32	mA
		f_s = N/A, power Down Mode		0.2	0.4	mA
	PVCC Quiescent supply current	XSMT = 2 V, no load, PV_{CC} = 12 V		20	35	mA
		XSMT = 2 V, no load, PV_{CC} = 24 V		32	50	mA
$I_{CC(SD)}$	PVCC Quiescent supply current in shutdown mode	XSMT = 0.8 V, no load, P_{VCC} = 12 V		30		µA
		XSMT = 0.8 V, no load, PV_{CC} = 24 V		50	400	µA

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6.8 Timing Requirements - I²C Bus Timing

			MIN	MAX	UNIT
t_{SCL}	SCL clock frequency	Standard		100	kHz
		Fast		400	
t_{BUF}	Bus free time between a STOP and START condition	Standard	4.7		µs
		Fast	1.3		
t_{LOW}	Low period of the SCL clock	Standard	4.7		µs
		Fast	1.3		
t_{HI}	High period of th eSCL clock	Standard	4		µs
		Fast	0.6		
t_{RS-SU}	Setup time for (repeated) START condition	Standard	4.7		µs
		Fast	0.6		
t_{S-HD} / t_{RS-HD}	Hold time for (repeated) START condition	Standard	4		µs
		Fast	0.6		
t_{D-SU}	Data setup time	Standard	0.25		µs
		Fast	0.1		
t_{D-HD}	Data hold time	Standard	0	0.9	µs
		Fast	0	0.9	
t_{SCL-R}	Rise time of SCL signal	Standard	$20+ 0.1C_B$	1	µs
		Fast	$20+ 0.1C_B$	0.3	
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard	$20+ 0.1C_B$	1	µs
		Fast	$20+ 0.1C_B$	0.3	
t_{SCL-F}	Fall time of SCL signal	Standard	$20+ 0.1C_B$	1	µs
		Fast	$20+ 0.1C_B$	0.3	
t_{SDA-R}	Rise time of SDA signal	Standard	$20+ 0.1C_B$	1	µs
		Fast	$20+ 0.1C_B$	0.3	
t_{SDA-F}	Fall time of SDA signal	Standard	$20+ 0.1C_B$	1	µs
		Fast	$20+ 0.1C_B$	0.3	
t_{P-SU}	Setup time for STOP condition	Standard	4		µs
		Fast	0.6		
C_B	Capacitive load for SDA and SCL line			400	pF
t_{SP}	Pulse width of spike suppressed	Fast		50	ns
V_{NH}	Noise margin at high level for each connected device (including hysteresis)		$0.2\ V_{DD}$		V

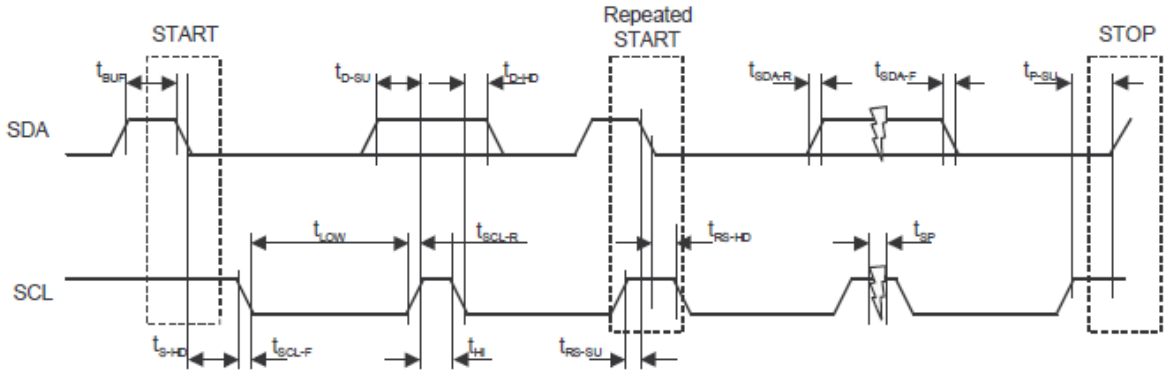

Figure 1. Register Access Timing

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6.9 Typical Characteristics

All measurements taken at 1kHz, unless otherwise noted. Measurements were made using the TAS5766MDCA EVM.

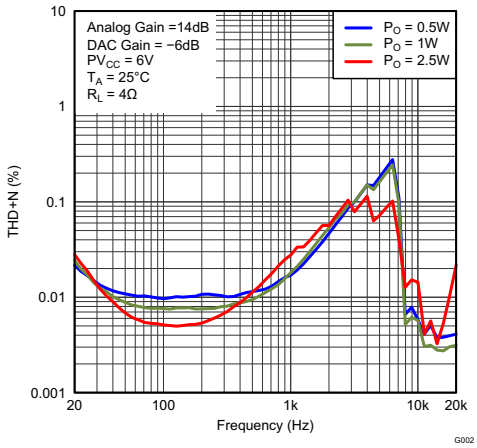

Figure 2. Total Harmonic Distortion + Noise vs Frequency

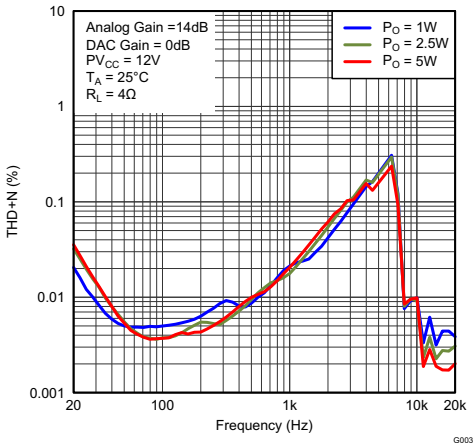

Figure 3. Total Harmonic Distortion + Noise vs Frequency

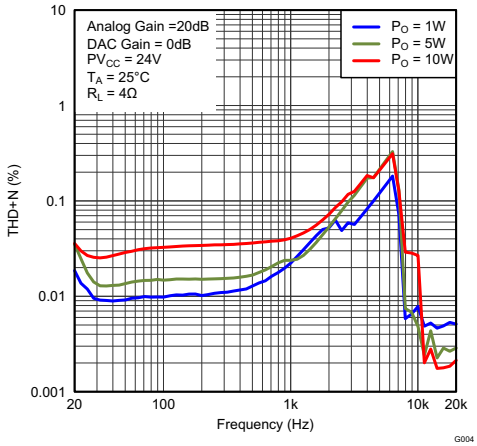

Figure 4. Total Harmonic Distortion + Noise vs Frequency

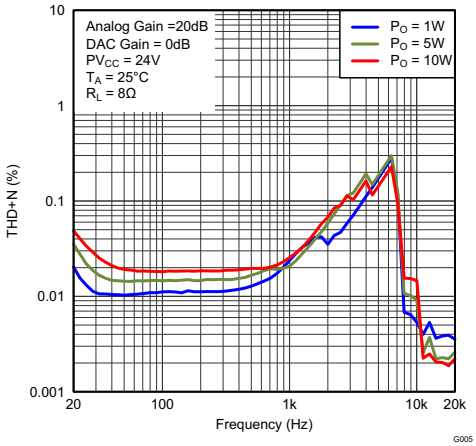

Figure 5. Total Harmonic Distortion + Noise vs Frequency

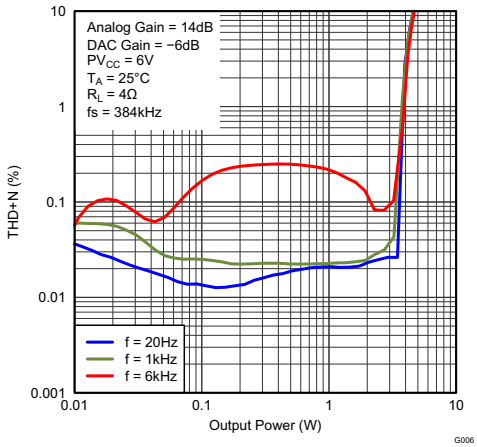

Figure 6. Total Harmonic Distortion + Noise vs Power

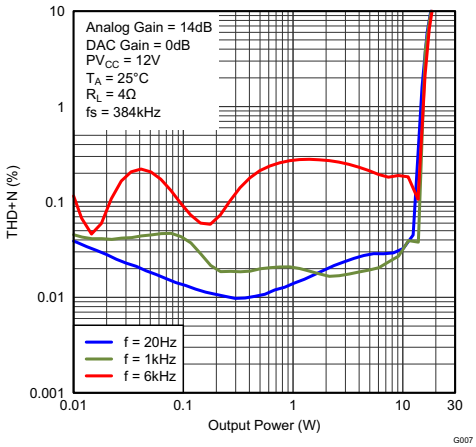

Figure 7. Total Harmonic Distortion + Noise vs Power

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Typical Characteristics (continued)

All measurements taken at 1kHz, unless otherwise noted. Measurements were made using the TAS5766MDCA EVM.

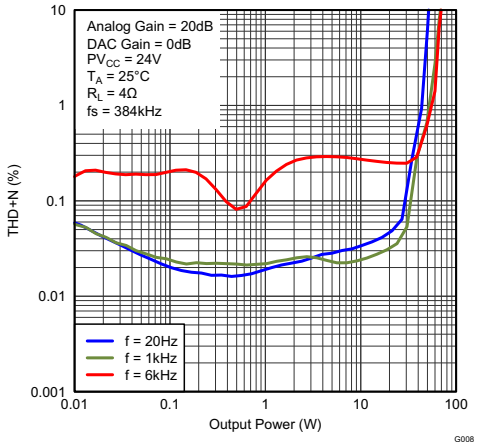

Figure 8. Total Harmonic Distortion + Noise vs Power

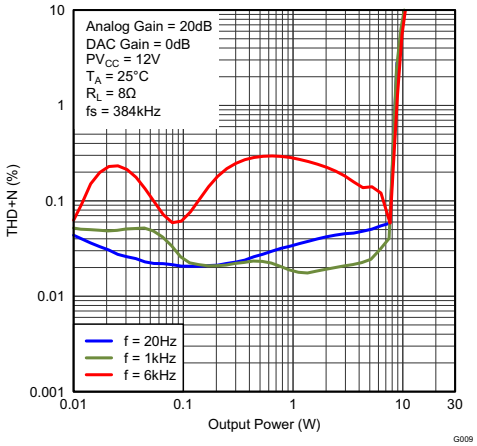

Figure 9. Total Harmonic Distortion + Noise vs Power

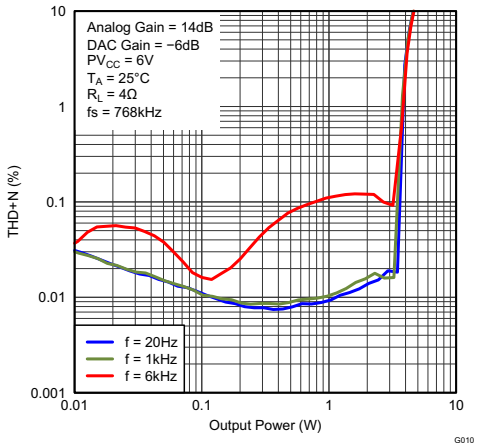

Figure 10. Total Harmonic Distortion + Noise vs Power

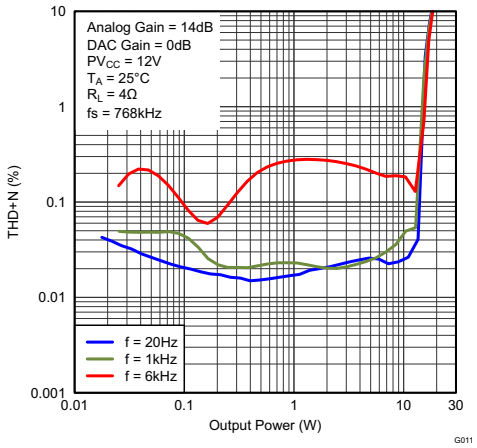

Figure 11. Total Harmonic Distortion + Noise vs Power

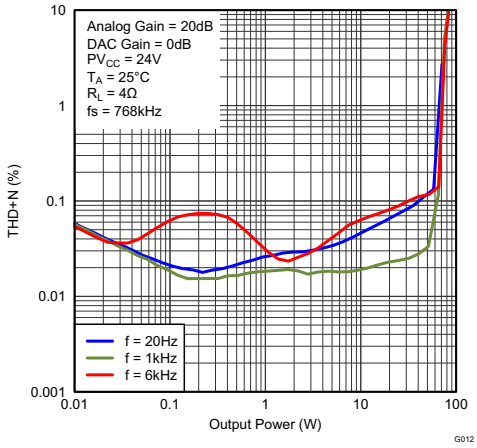

Figure 12. Total Harmonic Distortion + Noise vs Power

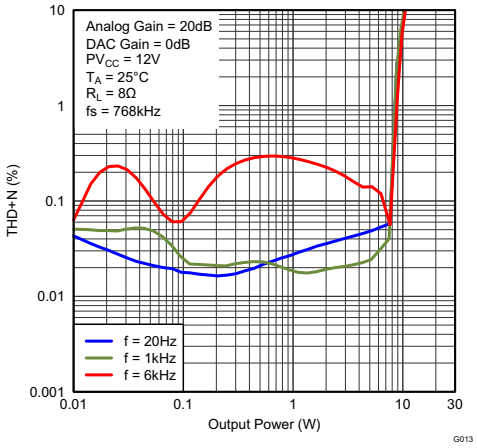

Figure 13. Total Harmonic Distortion + Noise vs Power

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Typical Characteristics (continued)

All measurements taken at 1kHz, unless otherwise noted. Measurements were made using the TAS5766MDCA EVM.

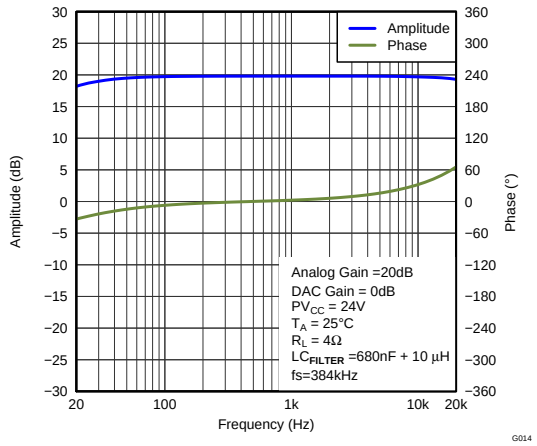


Figure 14. Gain/Phase vs Frequency

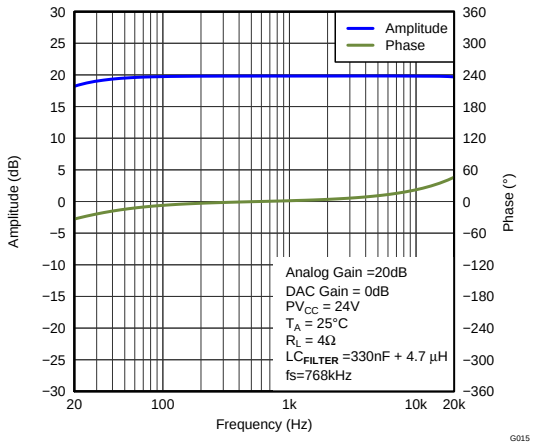
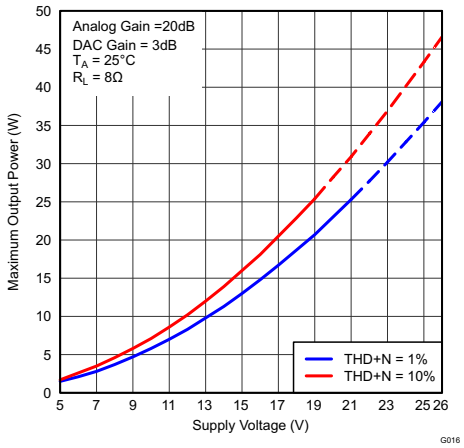
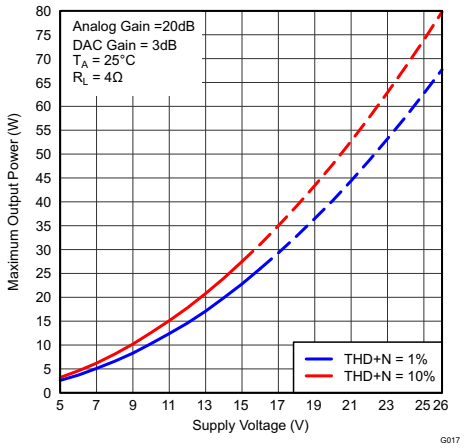


Figure 15. Gain/Phase vs Frequency



Thermally limited for dashed lines

Figure 16. Maximum Output Power vs Supply Voltage



Thermally limited for dashed lines

Figure 17. Maximum Output Power vs Supply Voltage

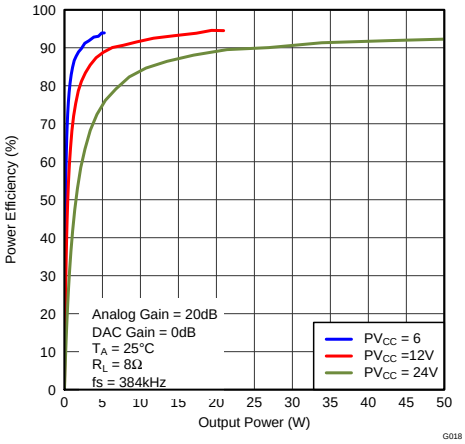


Figure 18. Power Efficiency vs Output Power

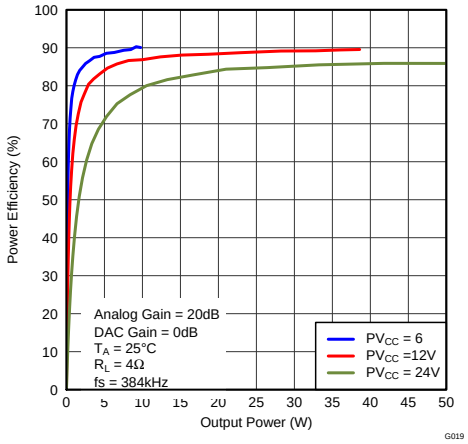


Figure 19. Power Efficiency vs Output Power

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Typical Characteristics (continued)

All measurements taken at 1kHz, unless otherwise noted. Measurements were made using the TAS5766MDCA EVM.

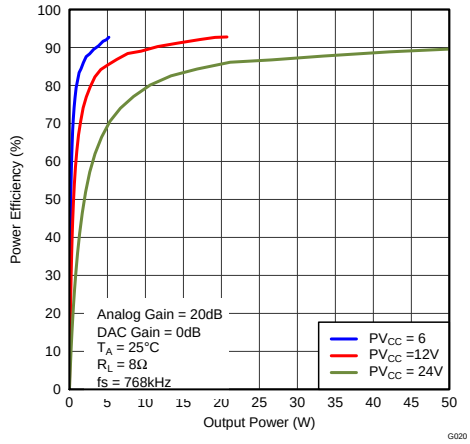


Figure 20. Power Efficiency vs Output Power

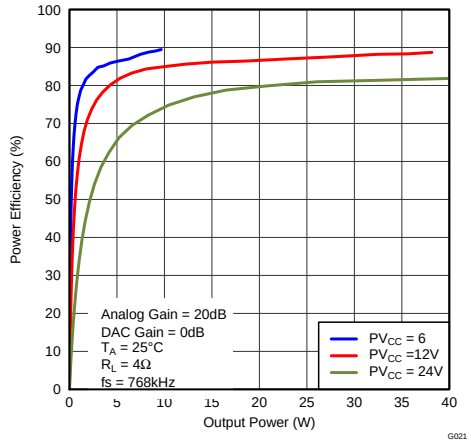


Figure 21. Power Efficiency vs Output Power

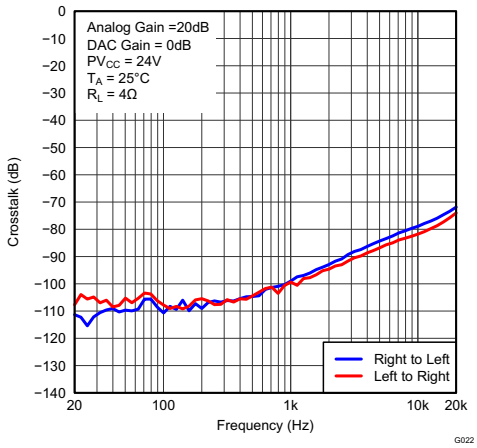


Figure 22. Crosstalk vs Frequency

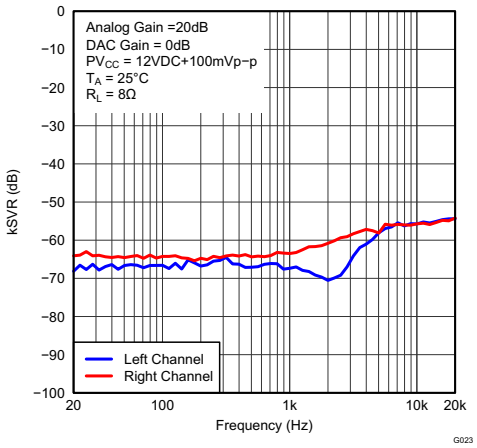


Figure 23. Supply Ripple Rejection vs Frequency

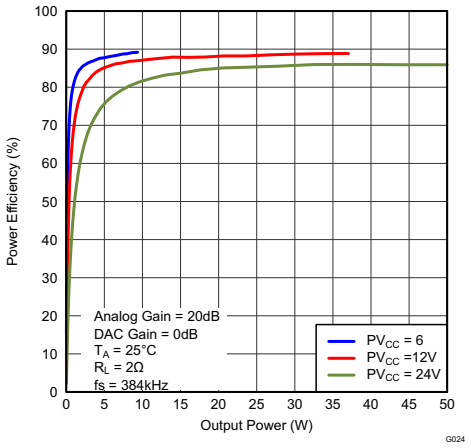
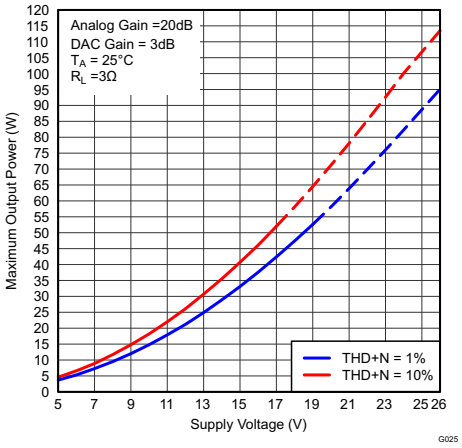


Figure 24. Power Efficiency (PBTL) vs Output Power



Thermally limited for dashed lines

Figure 25. Maximum Output Power vs Supply Voltage

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Typical Characteristics (continued)

All measurements taken at 1kHz, unless otherwise noted. Measurements were made using the TAS5766MDCA EVM.

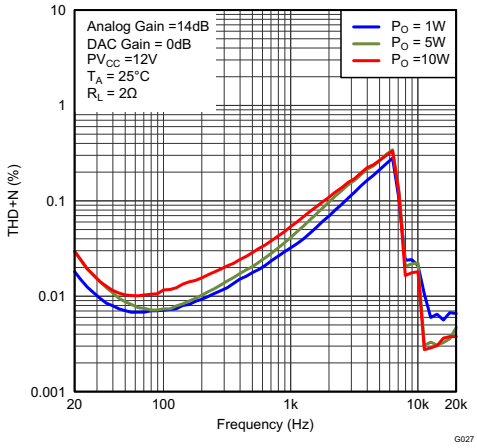


Figure 26. Total Harmonic Distortion + Noise (PBTL) vs Frequency

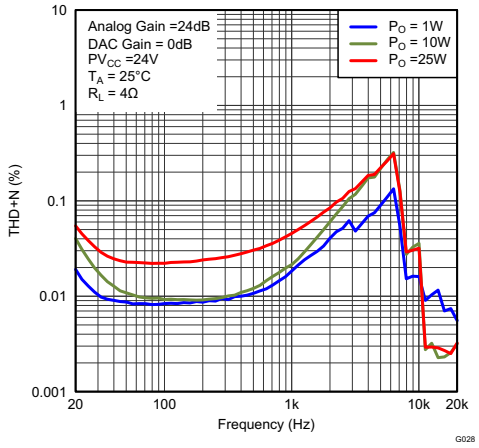


Figure 27. Total Harmonic Distortion + Noise (PBTL) vs Frequency

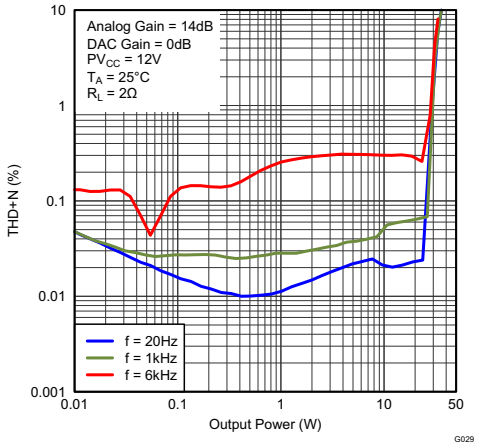


Figure 28. Total Harmonic Distortion + Noise (PBTL) vs Power

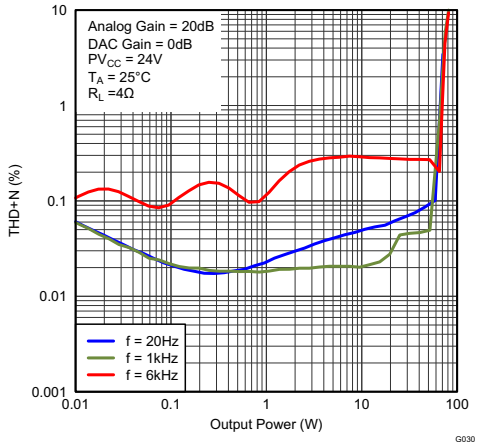


Figure 29. Total Harmonic Distortion + Noise (PBTL) vs Power

7 Detailed Description

7.1 Overview

The TAS576xM PurePath Smart Amp enhance the bass, sound fidelity and increased loudness by driving the speaker to its thermal and mechanical limits.

The TAS576xM contains two BTL class-D amplifiers that supply up to 2 x 50W peak power into 4 Ω. The amplifier is thermally designed to match the typical speaker so it can withstand high peaks for the time it takes the speaker voice-coil to heat up; it then lowers the average power to safe operating limits.

The wide supply range of 4.5 V to 26.4 V enables the use of different power supply options from 2-cell Li-Ion batteries to fixed 24-V supply.

The Smart Amp is available with two different class-D amplifier modulations: BD-mode in the TAS576**6**M; and, 1SPW-mode in the TAS576**8**M.

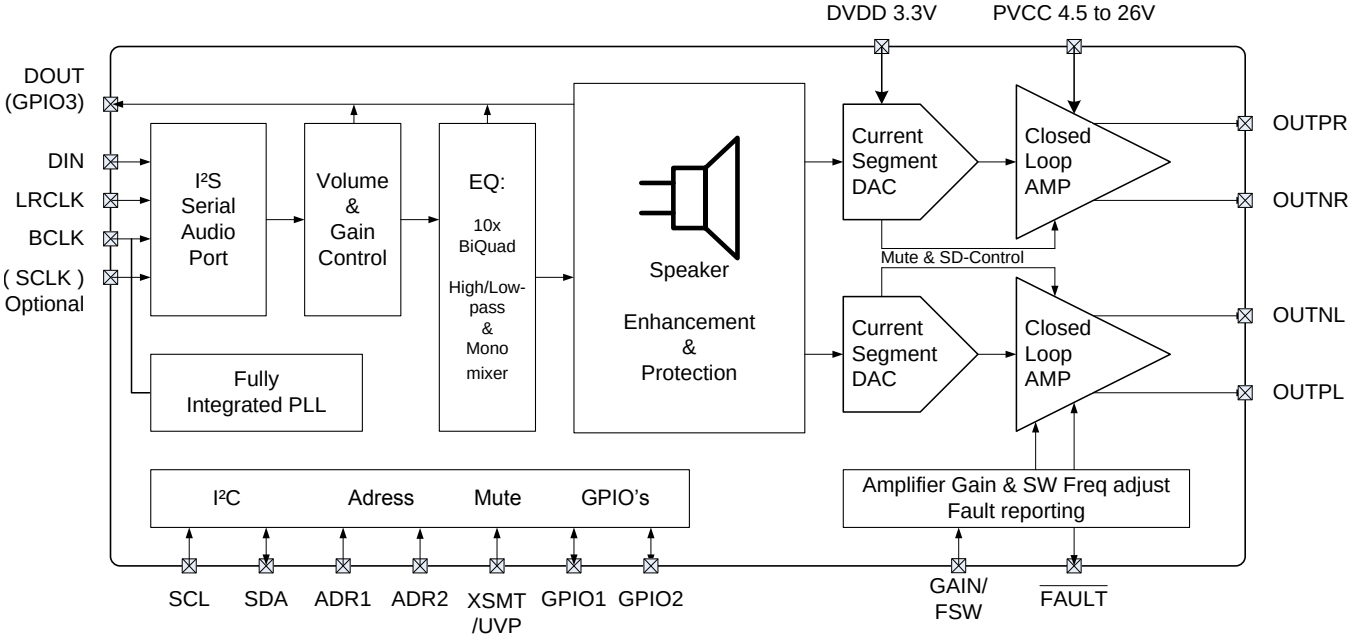
TI's PurePath Smart Amp technology allows speakers to be driven with more peak power than their average-power rating, without damage to the speaker by voice coil over excursion or thermal overload.

Sophisticated speaker models (electro-mechanical-thermal) are used as a foundation for the protection and enhancement of the system. This is done by modeling the loudspeaker in the on-chip miniDSP and running an adaptive algorithm that modifies the output based on the modeled conditions of the speaker.

TI provides a PurePath Console (PPC) GUI, including a TI learning board that measures the loudspeaker parameters. The PPC GUI generates the code for download to the device on boot-up.

Smart Amp technology in the TAS576xM uses information from the SOA (Safe Operating Area) characterization details for the loudspeaker, as well as real-world temperature, and uses this data in an adaptive control algorithm in order to control Smart Bass and Smart DRP (Dynamic Range Preservation). The protection side of the algorithm is also used for thermal protection and mechanical voice coil excursion protection.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Smart SOA

The "Safe Operating Area" (SOA) for a loudspeaker is based on its electro-mechanical-thermal model. Depending on a speaker's inefficiency, some of the power is dissipated as heat rather than mechanical/acoustic energy. By understanding the characteristics of the speaker, Smart Amp is able to drive the speaker harder, without causing the speaker to thermally overload; or, suffer voice coil over-exclusion and fail. SMART SOA are parameters that are differentiated by a PPC GUI into coefficients that the algorithm uses.

7.3.2 Smart BASS

Smart Bass is an intelligent True Bass Alignment algorithm. Smart Bass uses the combination of the speaker model and a desired target response selected by the user to equalize the speaker in the bass region. This target response is critical for the sound character and the user can apply the same target response to very different speakers and get the same sound.

In conventional adaptive Bass Boost Algorithms, designers need to vary the amount of bass boost whenever the output volume is changed. This approach is very much an "open loop" process. Smart Bass is a new proprietary algorithm that combines: True bass extension (in bandwidth and amplitude) and Psycho-acoustic bass extension, with a smart adaptive control.

Smart Bass varies the mix of True Bass extension and Psycho-acoustic bass extension in real time, depending on the loudspeakers position in its SOA.

Smart Bass dynamically switches between True Bass and Psycho-acoustic extension based on a number of parameters such as:

- Capabilities and properties of the speaker, including Q compensation
- Music type
- Volume setting
- Temperature
- User preferences
- Designer preferences

7.3.3 Smart Protection

The two main failure mechanisms for loudspeakers are over temperature and over excursion. By modeling the current state of the speaker, Smart Protection adaptively changes various settings in Smart Amplifier to avoid over temperature and over excursion. Design engineers must first provide details of the loudspeaker (driver and enclosure) into the GUI. From there the appropriate coefficients are generated for the algorithm.

7.3.4 Implementing a Real World Design

Traditionally, system developers and hardware engineers use graphic equalizers in trial-and-error fashion to boost the bass for each new speaker until the sound is right (or "good enough" in many cases). However, this typically results in a strange combined response with too much phase shift. This process must be repeated every time a new speaker is selected. The Smart Bass concept uses the GUI to select a desired target response takes the speaker out of the equation. By this approach users can obtain a target response with minimum phase warp and time domain ringing which gives a speedy and tight bass. Conversely, users can select a target response that has lots of ringing to give a classical heavy ‘oomph’ bass.

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Feature Description (continued)

7.3.5 Modulation Schemes

7.3.5.1 BD-Modulation

The TAS576**6**M uses this modulation, it is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

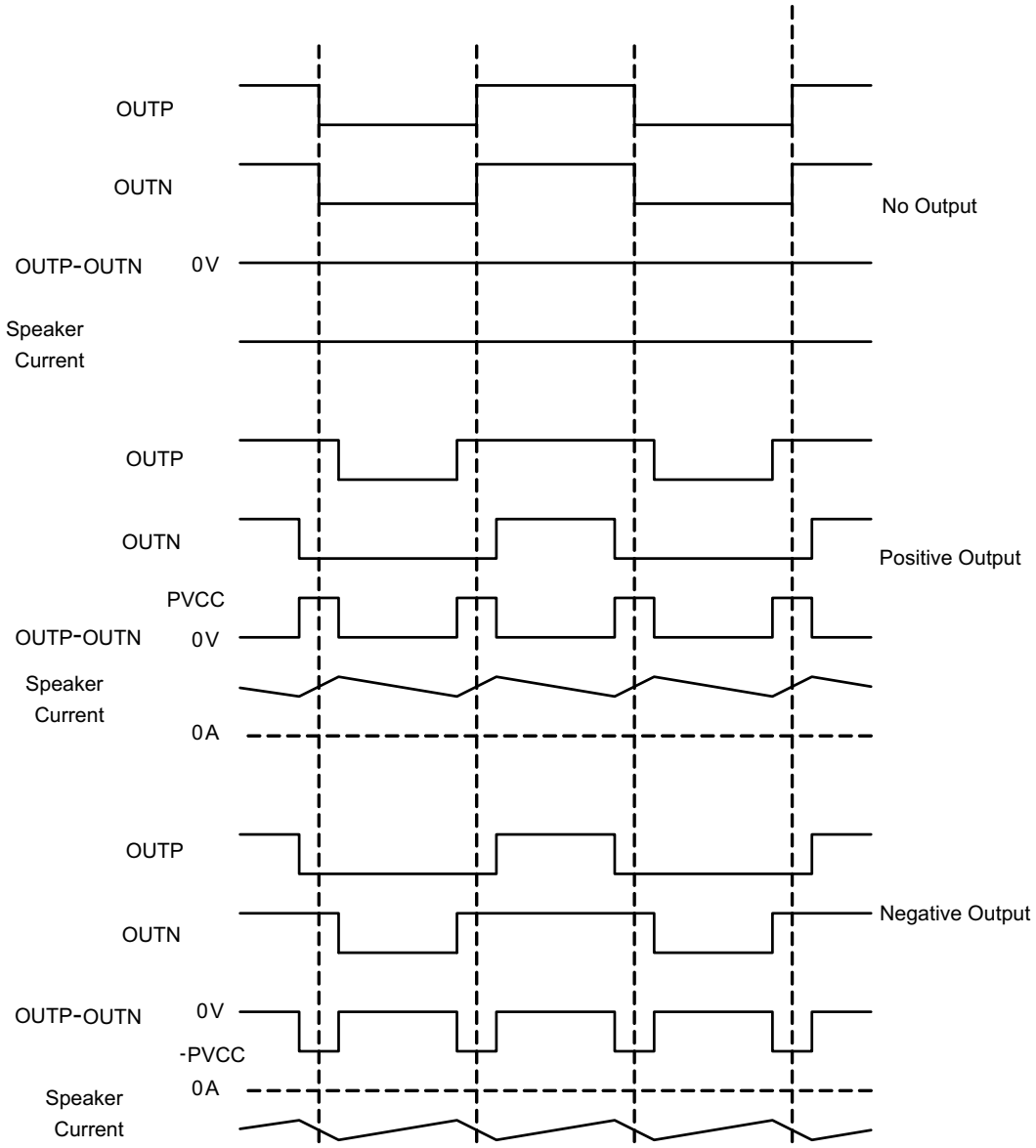

Figure 30. BD-Modulation

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Feature Description (continued)

7.3.5.2 1SPW-Modulation

The TAS576**8**M uses this modulation, the 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In 1SPW mode the outputs operate at ~15% modulation during idle conditions. When an audio signal is applied one output will decrease and one will increase. The decreasing output signal will quickly rail to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses. The THD penalty in 1SPW mode is minimized by the high performance feedback loop. The resulting audio signal at each half output has a discontinuity each time the output rails to GND. This can cause ringing in the audio reconstruction filter unless care is taken in the selection of the filter components and type of filter used.

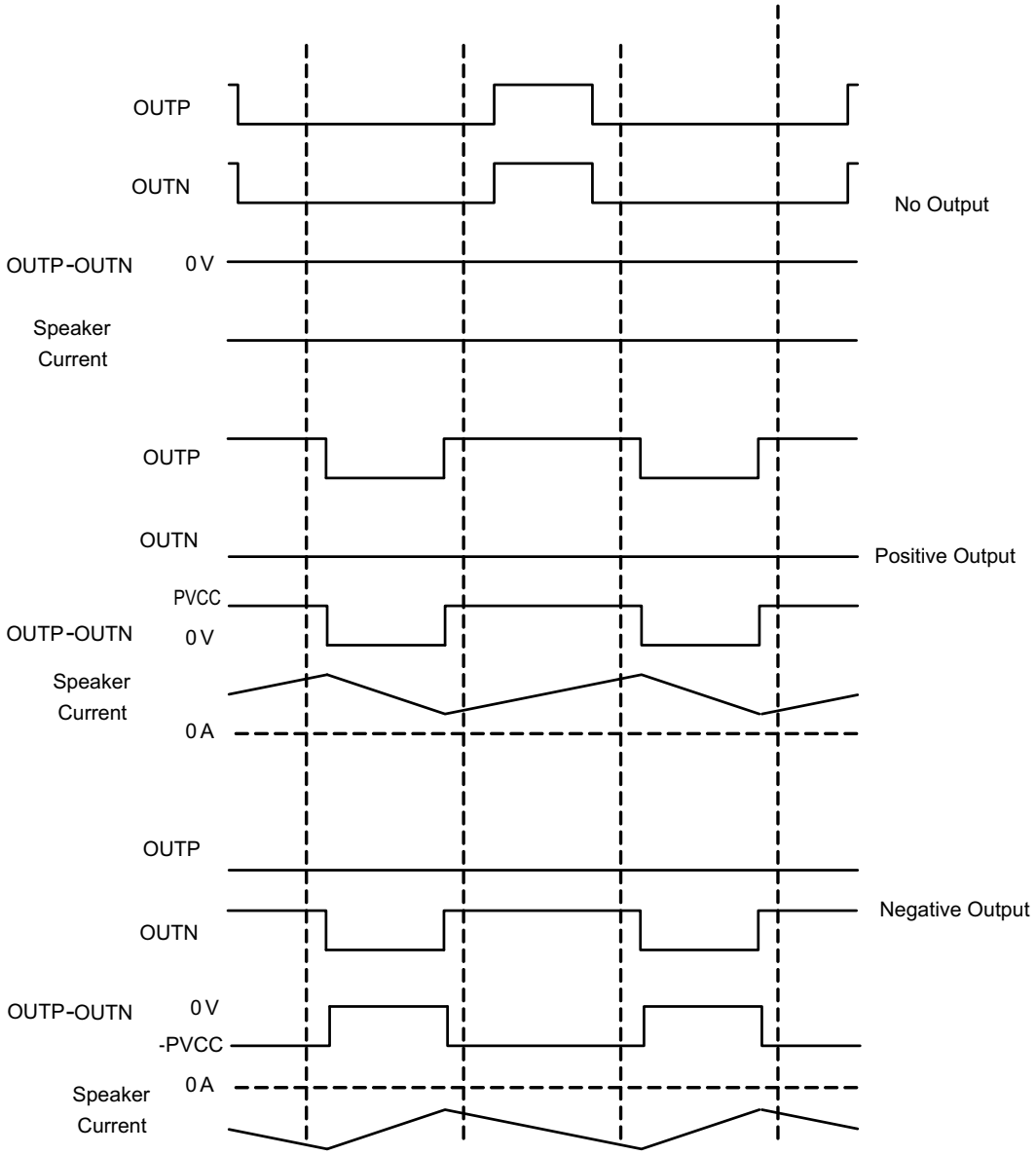

Figure 31. 1SPW-Modulation

7.4 Device Functional Modes

7.4.1 Device Protection System

The TAS576xM contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overload, over temperature, and under-voltage. If an error is detected, the $\overline{\text{FAULT}}$ pin signals according to Table 1.

Table 1. TAS576xM Device Protections

FAULT	TRIGGERING CONDITION (TYPICAL VALUE)	$\overline{\text{FAULT}}$	ACTION	LATCHED/ SELF-CLEARING
Over Current	Output short or short to PVCC or GND	Low	Output high impedance	Self-clearing
Over Temperature	T_J > 150°C	Low	Output high impedance	Self-clearing
Too High DC offset	DC output voltage	Low	Output high impedance	Self-clearing
Under Voltage on PVCC	PVCC < 4.5 V	High	Output high impedance	Self-clearing
Over voltage on PVCC	PVCC > 27 V	High	Output high impedance	Self-clearing

7.4.1.1 Over Current Protection

The TAS576xM has protection from over current conditions caused by a short circuit or over load on the output stage. The fault is reported on the $\overline{\text{FAULT}}$ pin as a low state. The amplifier outputs are switched to a high impedance state when the over current is detected. The outputs are automatically re-engaged after a 1.3s off time.

7.4.1.2 Thermal Protection

Thermal protection on the TAS576xM prevents damage to the device when the internal die temperature exceeds 150°C. There is a 15°C hysteresis on this trip point. When the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are put in high impedance mode. The outputs are automatically re-engaged after a 1.3s off time if the temperature is below the trip point.

7.4.1.3 DC Protection

DC protection on the TAS576xM prevents damage to the attached speaker when the output DC voltage exceeds 20% of supply voltage. When the voltage exceeds the trip point, the device enters into the shutdown state and the outputs are put in high impedance mode. The outputs are automatically re-engaged after a 0.65 s off time if the voltage is below the trip point.

7.4.2 Reset and System Clock Functions

7.4.2.1 Power-On Reset Function

The TAS576xM includes a power-on reset function shown in Figure 32. With DVDD > 2.8 V, the power-on reset function is enabled. After the initialization period, the TAS576xM is set to its default reset state.

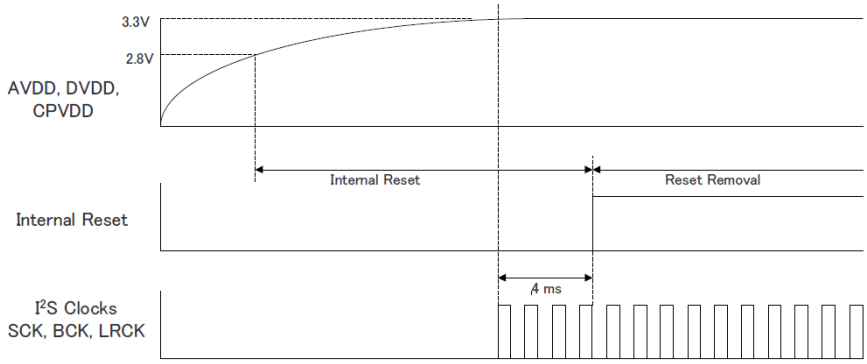

Figure 32. Power-On Reset Timing, DVDD = 3.3V

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7.4.2.2 System Clock Input

The TAS576xM requires a system clock to operate the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCLK input (pin 12) and supports up to 50MHz. The TAS576xM system-clock detection circuit automatically senses the system-clock frequency. The Smart AMP processing block only supports 44.1 kHz and 48kHz sampling rates even though the hardware supports all the common audio sampling frequencies in the bands of 8 kHz, 16 kHz, (32 kHz–44.1 kHz–48kHz), (88.2 kHz–96 kHz), (176.4 kHz–192 kHz), and 384 kHz with ±4% tolerance.

Values in the parentheses are "grouped" when detected, e.g. 88.2 kHZ and 96 kHz are detected as "double rate", 32 kHz, 44.1 kHz and 48 kHz will be detected as "single rate". The sampling frequency detector sets the clock for the digital filter, Delta Sigma Modulator (DSM) and the Negative Charge Pump (NCP) automatically. Table 2 shows examples of system clock frequencies for common audio sampling rates.

SCLK rates that are not common to standard audio clocks, between 1 MHz and 50 MHz, are only supported in software mode by configuring various PLL and clock-divider registers. This programmability allows the device to become a clock master and drive the host serial port with LRCLK and BCLK, from a non-audio related clock (for example, using 12 MHz to generate 44.1 kHz (LRCLK) and 2.8224 MHz (BCLK))

Figure 33 shows the timing requirements for the system clock input. For optimal performance, use a clock source with low phase jitter and noise.

Table 2. System Master Clock Inputs for Audio Related Clocks

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)						
	128 fs	192 f_s	256 f_s	384 f_s	512 f_s	768 f_s	1024 f_s
44.1 kHz	5.6488	8.4672	11.2896	16.9344	22.5792	33.8688	45.1584
48 kHz	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640	49.1520

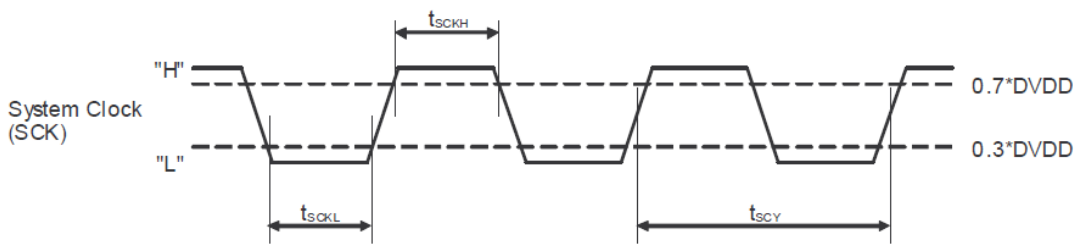

Figure 33. Timing Requirement for SCLK Input

Table 3. Timing Requirements for SCLK Input

		MIN	MAX	UNIT
t_{SCY}	System clock pulse cycle time	20	1000	ns
t_{SCLKH}	System clock pulse width, High	8		ns
t_{SCLKL}	System clock pulse width, Low	9		ns

7.4.3 System Clock PLL Mode

The system clock PLL mode allows designers to use a simple 3-wire I^2S audio source when driving the output. The 3-wire source reduces the need for a high frequency SCLK, making PCB layout easier, and reduces high frequency electromagnetic interference.

The user must set all the PLL registers and clock divider registers for referencing BCLK. See *Clock Generation and PLL* for more information.

Table 4. BCLK Rates (MHz) by LRCLK Sample Rate for PLL Operation

Sample f (kHz)	BCLK (f_S)	
	32	64
44.1	1.4112	2.8224
48	1.536	3.072

7.4.4 Clock Generation and PLL

The TAS576xM supports a wide range of options to generate the required clocks for the DAC section as well as interface and other control blocks as shown in Figure 34.

The clocks for the PLL require a source reference clock. This clock is sourced as the incoming BCLK or SCLK. The source reference clock for the PLL reference clock is selected by programming the SRCREF value on Page 0, Register 13, D(6:4). The PLL reference clock can then be routed through highly-flexible clock dividers shown in Table 5 to generate the various clocks required for the DAC, Negative Charge Pump (NCP), Internal modulator and sections. The TAS576xM provides several programmable clock dividers to achieve a variety of sampling rates for the DAC and clocks for the NCP, OSR, and the OSRCK for OSR must be set at 16fS frequency by DOSR on Page0, Register 30, D(6:0).

If PLL functionality isn't required, set the PLLEN value on Page 0, Register 4, D(0) to 0. In this situation, an external SCLK is required.

Table 5. PLL Configuration Registers

CLOCK MULTIPLEXER	FUNCTION	BITS
SRCREF	PLL Reference	Page 0, Register 13, D(6:4)
DIVIDER	**FUNCTION**	**BITS**
DDSP	Clock divider	Page 0, Register 27, D(6:0)
DDAC	DAC clock divider	Page 0, Register 28, D(6:0)
DNCOP	NCP clock divider	Page 0, Register 29, D(6:0)
DOSR	OSR clock divider	Page 0, Register 30, D(6:0)
DBCLK	External BCLK Div	Page 0, Register 32, D(6:0)
DLRK	External LRCLK Div	Page 0, Register 33, D(7:0)

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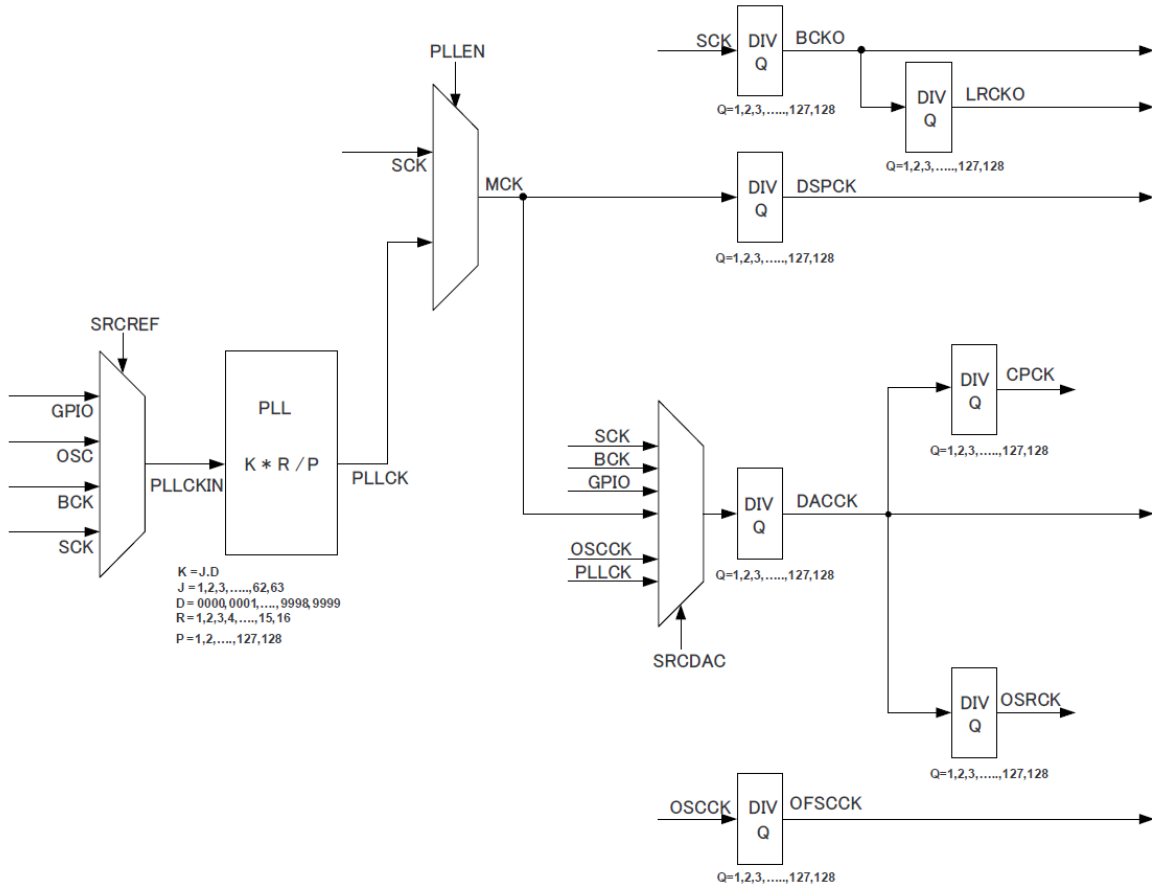

Figure 34. PLL Clock Source and Clock Distribution

7.4.5 PLL Calculation

The TAS576xM has an on-chip PLL with fractional multiplication to generate the clock frequency needed by the audio DAC, Negative Charge Pump, Modulator and Digital Signal Processing blocks. The programmability of the PLL allows operation from a wide variety of clocks that may be available in the system. The PLL input (PLLCKIN) supports clock frequencies from 512 kHz to 50 MHz and is register programmable to enable generation of required sampling rates with fine precision.

The PLL is enabled by default. The PLL can be turned on by writing to Page 0, Register 4, D(0). When the PLL is enabled, the PLL output clock PLLCK is given by Equation 1:

$$PLLCK = \frac{PLLCKIN \times R \times J.D}{P} \quad \text{or} \quad PLLCK = \frac{PLLCKIN \times R \times K}{P} \tag{1}$$

R = 1, 2, 3,4, … 15, 16
J = 0 4,5,6, … 63 and D = 0000, 0001, 0002, … 9999
K = [J value].[D value]
P 0 1, 2, 3, … 15
R, J, D and P are programmable. J is the integer portion of K (the number to the left of the decimal point) while D is the fraction portion of K (the number to the right of the decimal point, assuming four digits of precision).

Examples:

- If K = 8.5, then J = 8, D = 5000
- If K = 7.12, then J = 7, D = 1200
- If K = 14.03, then J = 14, D = 0300

- If K = 6.0004, then J = 6, D = 0004

When the PLL is enabled and D = 0000, the following conditions must be satisfied:

- 1 MHz ≤ (PLLCKIN / P) ≤20 MHz
- 64 MHz ≤ (PLLCKIN x K x R / P) ≤ 100 MHz
- 1 ≤ J ≤ 63

When the PLL is enabled and D ≠ 0000, the following conditions must be satisfied:

- 6.667 MHz ≤ PLLCLKIN / P ≤ 20 MHz
- 64 MHz ≤ (PLLCKIN x K x R / P) ≤ 100 MHz
- 4 ≤ J ≤ 11
- R = 1

When the PLL is enabled:

- fS = (PLLCLKIN × K × R) / (2048 × P)
- The value of N is selected so that fS × N = PLLCLKIN x K x R / P is in the allowable range.

Example: MCLK = 12 MHz and fS = 44.1 kHz, (N=2048)
Select P = 1, R = 1, K = 7.5264, which results in J = 7, D = 5264

Example: MCLK = 12 MHz and fS = 48.0 kHz, (N=2048)
Select P = 1, R = 1, K = 8.192, which results in J = 8, D = 1920

Values are written to the registers in Table 6.

Table 6. PLL Registers

DIVIDER	FUNCTION	BITS
PLLE	PLL enable	Page 0, Register 4, D(0)
PPDV	PLL P	Page 0, Register 20, D(3:0)
PJDV	PLL J	Page 0, Register 21, D(5:0)
PDDV	PLL D	Page 0, Register 22, D(5:0)
		Page 0, Register 23, D(7:0)
PRDV	PLL R	Page 0, Register 24, D(3:0)

Table 7. PLL Configuration Recommendations

COLUMN	DESCRIPTION
f_S (kHz)	Sampling frequency
RSCLK	Ration between sampling frequency and SCLK frequency (SCLK frequency = RSCLK x sampling frequency)
SCLK (MHz)	System master clock frequency at SCLK input (pin 22)
PLL VCO (MHz)	PLL VCO frequency as PLLCK
P	One of the PLL coefficients
PLL REF (MHz)	Internal reference clock frequency which is produced by SCLK / P
M = K × R	The final PLL multiplication factor computed from K and R as described in Equation 1
K = J.D	One of the PLL coefficients
R	One of the PLL coefficients
PLL f_S	Ratio between fS and PLL VCO frequency (PLL VCO / fS)
DSP f_S	Ratio between operating clock rate and fS (PLL fS / NMAC)
NMAC	The clock divider value in Table 4
DSP CLK (MHz)	The operating frequency as DSPCK in *Clock Generation and PLL*
MOD fS	Ratio between DAC operating clock frequency and fS (PLL fS / NDAC)
MOD f(kHz)	DAC operating frequency as DACCK in *Clock Generation and PLL*
NDAC	DAC clock divider value in Table 4
DOSR	OSR clock divider value in Table DOSR 7 for generating OSRCK in Clock Generation and PLL. DOSR must be chosen so that MOD fS / DOSR = 16 for correct operation.

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Table 7. PLL Configuration Recommendations (continued)

COLUMN	DESCRIPTION
NCP	NCP (negative charge pump) clock divider value in Table 4
CP f	Negative charge pump clock frequency (fS × MOD fS / NCP)
% Error	Percentage of error between PLL VCO / PLL fS and fS (mismatch error). ● This number is typically zero but can be non-zero especially when K is not an integer (D is % Error not zero). ● This number may be non-zero only when the TAS576xM acts as a master

Table 8. Recommended Clock Divider Settings for PLL as Master Clock

44.1 kHz									
RSCLK	32	64	128	192	256	384	512	768	1024
SCLK (MHz)	1.4112	2.8224	5.6448	8.4672	11.2896	16.9344	22.5792	33.8688	45.1584
PLL VCO (MHz)	90.3168	90.3168	90.3168	90.3168	90.3168	90.3168	90.3168	90.3168	90.3168
P	1	1	1	3	2	3	3	3	3
PLL REF (MHz)	1.4112	2.8224	5.6448	2.8224	5.6448	5.6448	7.526	11.29	15.053
M = K×R	64	32	16	32	16	16	12	8	6
K = J.D	32	16	16	32	16	16	12	8	6
R	2	2	1	1	1	1	1	1	1
PLL f_S	2048	2048	2048	2048	2048	2048	2048	2048	2048
DSP f_S	1024	1024	1024	1024	1024	1024	1024	1024	1024
NMAC	2	2	2	2	2	2	2	2	2
DSP CLK (MHz)	45.1584	45.1584	45.1584	45.1584	45.1584	45.1584	45.1584	45.1584	45.1584
MOD f_S	128	128	128	128	128	128	128	128	128
MOD f (kHz)	5644.8	5644.8	5644.8	5644.8	5644.8	5644.8	5644.8	5644.8	5644.8
NDAC	16	16	16	16	16	16	16	16	16
DOSR	8	8	8	8	8	8	8	8	8
% ERROR	0	0	0	0	0	0	0	0	0
NCP	4	4	4	4	4	4	4	4	4
CP f (kHz)	1411.2	1411.2	1411.2	1411.2	1411.2	1411.2	1411.2	1411.2	1411.2
48kHz									
RSCLK	32	64	128	192	256	384	512	768	1024
SCLK (MHz)	1.536	3.072	6.144	9.216	12.288	18.432	24.576	36.864	49.152
PLL VCO (MHz)	98.304	98.304	98.304	98.304	98.304	98.304	98.304	98.304	98.304
P	1	1	1	3	2	3	3	3	3
PLL REF (MHz)	1.536	3.072	6.144	3.072	6.144	6.144	8.192	12.288	16.384
M = K×R	64	32	16	32	16	16	12	8	6
K = J.D	32	16	16	32	16	16	12	8	6
R	2	2	1	1	1	1	1	1	1
PLL fS	2048	2048	2048	2048	2048	2048	2048	2048	2048
DSP f_S	1024	1024	1024	1024	1024	1024	1024	1024	1024
NMAC	2	2	2	2	2	2	2	2	2
DSP CLK (MHz)	49.152	49.152	49.152	49.152	49.152	49.152	49.152	49.152	49.152
MOD f_S	128	128	128	128	128	128	128	128	128
MOD f (kHz)	6144	6144	6144	6144	6144	6144	6144	6144	6144
NDAC	16	16	16	16	16	16	16	16	16
DOSR	8	8	8	8	8	8	8	8	8
% ERROR	0	0	0	0	0	0	0	0	0
NCP	4	4	4	4	4	4	4	4	4
CP f (kHz)	1536	1536	1536	1536	1536	1536	1536	1536	1536

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7.4.6 Audio Data Interface

7.4.6.1 Audio Serial Interface

The audio interface port is a 3-wire serial port with the signals LRCLK (pin 15), BCLK (pin 13), and DIN (pin 14). BCLK is the serial audio bit clock, used to clock the serial data present on DIN into the serial shift register of the audio interface. Serial data is clocked into the TAS576xM on the rising edge of BCLK. LRCLK is the serial audio left/right word clock.

Table 9. TAS576xM Audio Data Formats, Bit Depths and Clock rates

FORMAT	DATA BITS	LRCLK	SCH RATE	BCLK RATE
I^2S/LJ	32, 24, 20, 16	44.1 or 48 kHz	128–3072	64, 48, 32
TDM	32, 24, 20, 16	44.1 or 48 kHz	128–3072	128, 265

The TAS576xM requires the synchronization of LRCLK and system clock, but does not require a specific phase relation between LRCLK and system clock.

If the relationship between LRCLK and system clock changes more than ±5 SCLK, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until resynchronization between LRCLK and system clock is completed.

7.4.6.2 PCM Audio Data Formats and Timing

The TAS576xM supports industry-standard audio data formats, including standard I2S and left-justified. Data formats are selected via Register (Pg0Reg40). All formats require binary 2s-complement, MSB-first audio data, up to 32-bit audio data is accepted.

The TAS576xM also supports right-justified and TDM. I2S, LJ, RJ, and TDM are selected using Register (Pg0Reg40). All formats require binary 2s complement, MSB-first audio data. Up to 32 bits are accepted. Default setting is I2S and 24 bit word length. The I2S slave timing is shown in Figure 35.

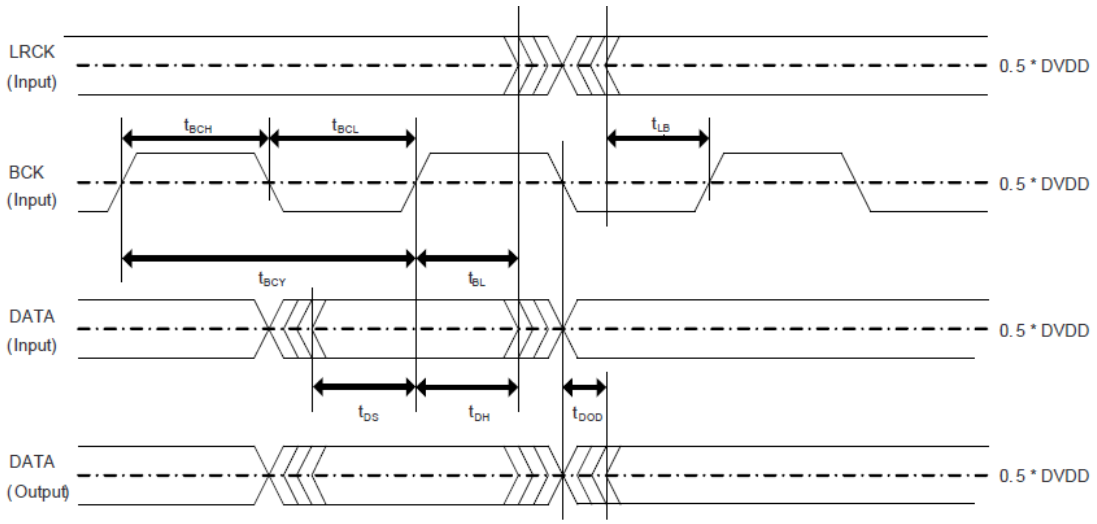

Figure 35. TAS576xM Serial Audio Timing – Slave

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Table 10. Audio Interface Slave Timing

		MIN	MAX	UNIT
t_{BCY}	BCLK pulse Cycle Time	40		ns
t_{BCL}	BCLK pulse Width LOW	16		ns
t_{BCH}	BCLK pulse Width HIGH	16		ns
t_{BL}	BCLK Rising Edge to LRCLK Edge	8		ns
t_{BCLK}	BCLK frequency at DVDD = 3.3V		24.576	MHz
t_{LB}	LRCLK Edge to BCLK Rising Edge	8		ns
t_{DS}	DATA set Up time	8		ns
t_{DH}	DATA Hold Time	8		ns
t_{DOD}	DATA delay time from BCLK falling edge		15	ns

The TAS576xM can act as an I^{2}S master, generating BCLK and LRCLK as outputs from the SCLK input.

Table 11. I^{2}S Master Mode Registers

REGISTER	FUNCTION
Page 0, register 9, D(0), D(4) and D85)	I^{2}S master Mode select
Register 32, D(6:0)	BCLK divider and LRCLK divider
Register 33, D(7:0)	

The I^{2}S master timing is shown in Figure 36 and Table 12.

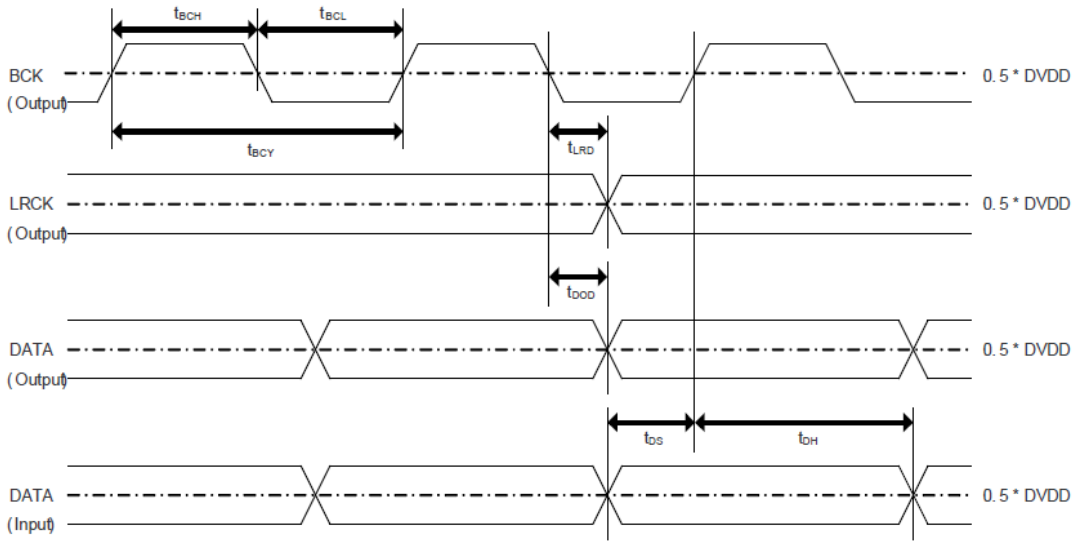

Figure 36. TAS576xM Serial Audio Timing - Master

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Table 12. Audio Interface Master Timing

		MIN	MAX	UNIT
t_{BCY}	BCLK pulse Cycle Time	40		ns
t_{BCL}	BCLK pulse Width LOW	16		ns
t_{BCH}	BCLK pulse Width HIGH	16		ns
t_{BL}	BCLK Rising Edge to LRCLK Edge	8		ns
t_{BCLK}	BCLK frequency at DVDD = 3.3V		24.576	MHz
t_{LB}	LRCLK Edge to BCLK Rising Edge	8		ns
t_{DS}	DATA set Up time	8		ns
t_{DH}	DATA Hold Time	8		ns
t_{DOD}	DATA delay time from BCLK falling edge		15	ns

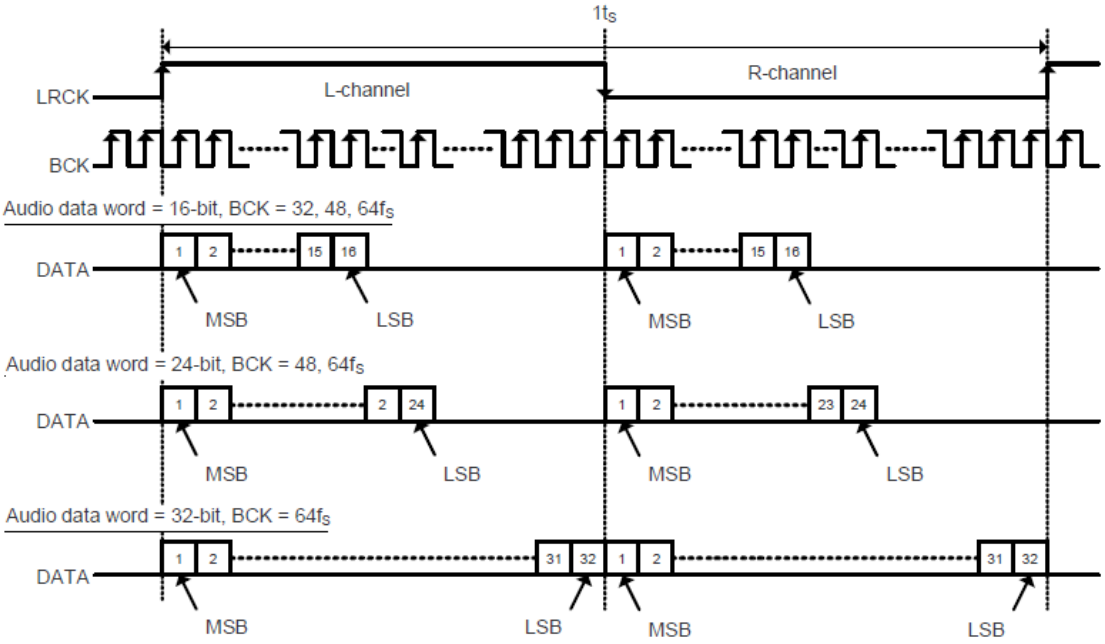

Figure 37. Left Justified Audio Data Format

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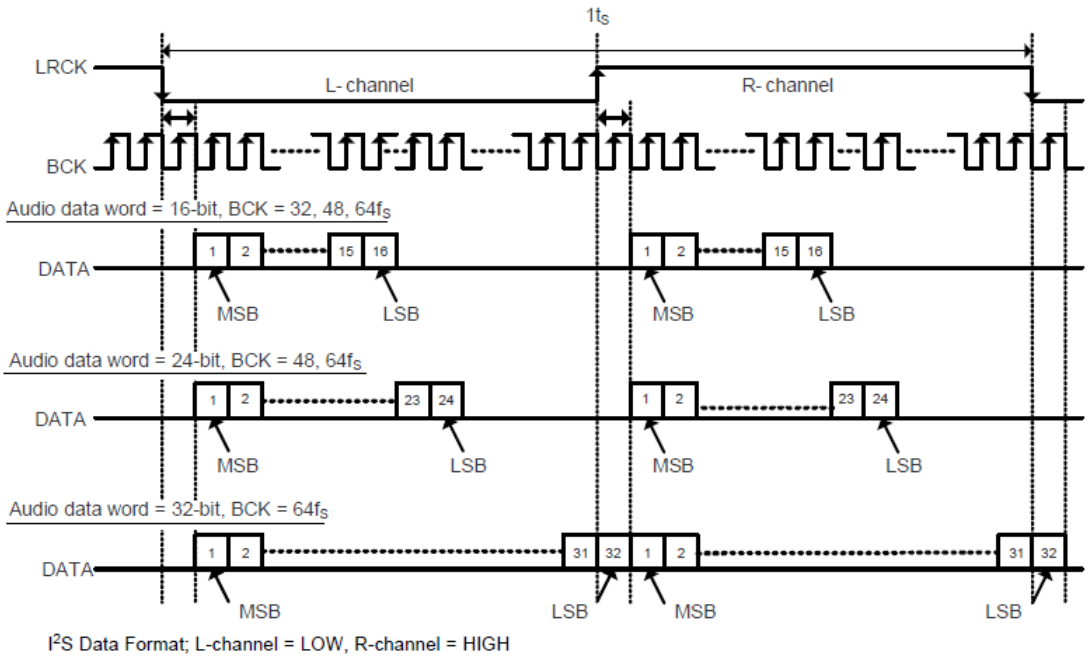

Figure 38. I²S Audio Data Format

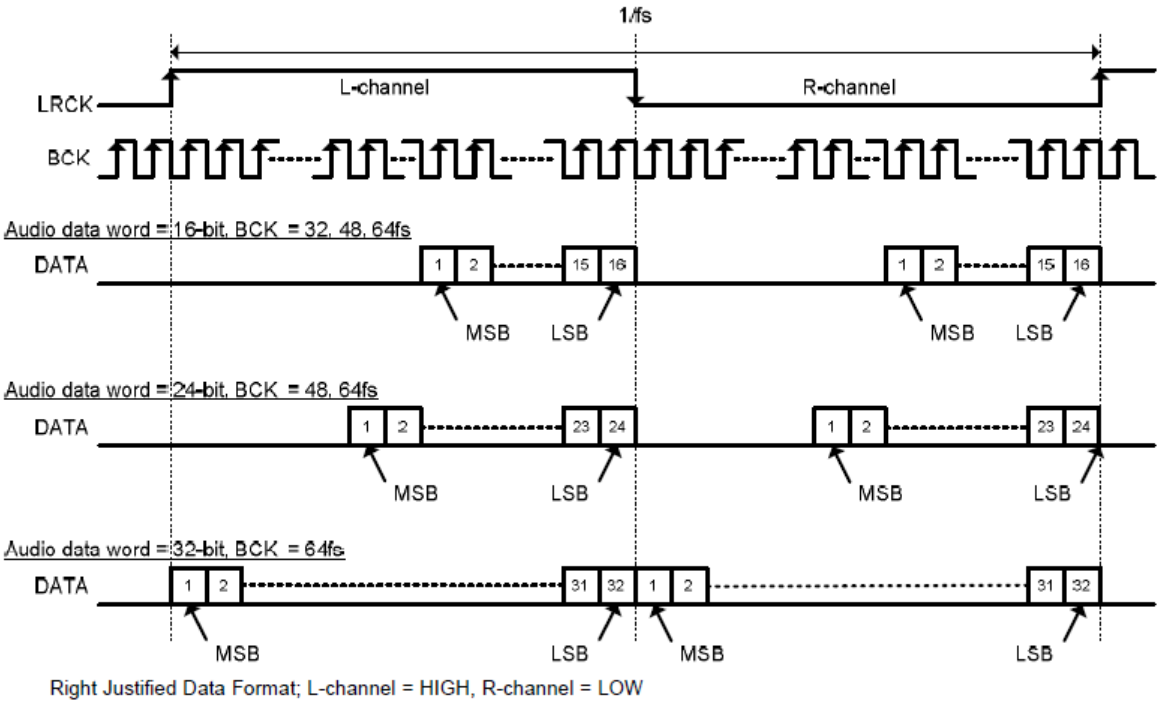

Figure 39. Right Justified Audio Data Format

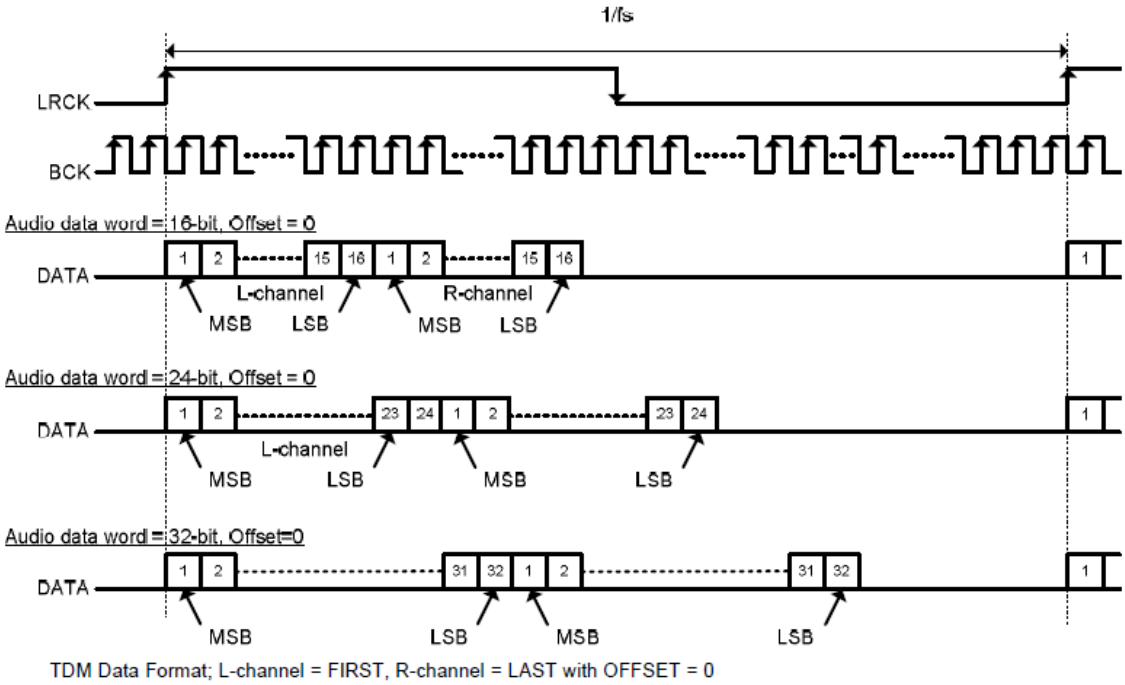

Figure 40. TDM Audio Data Format

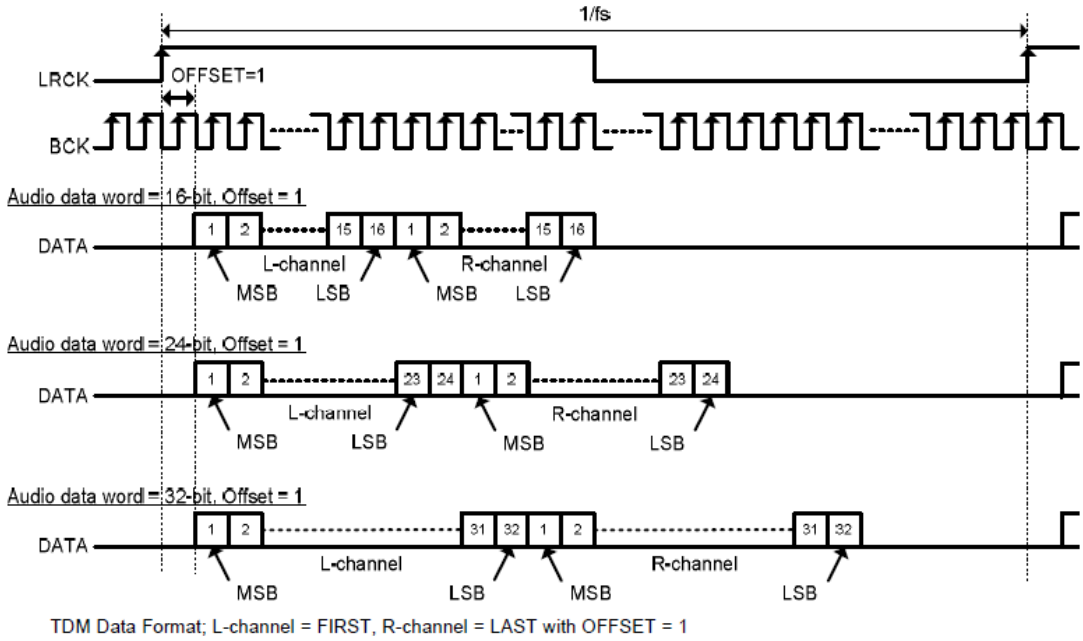

Figure 41. TDM 2 Audio Data Format

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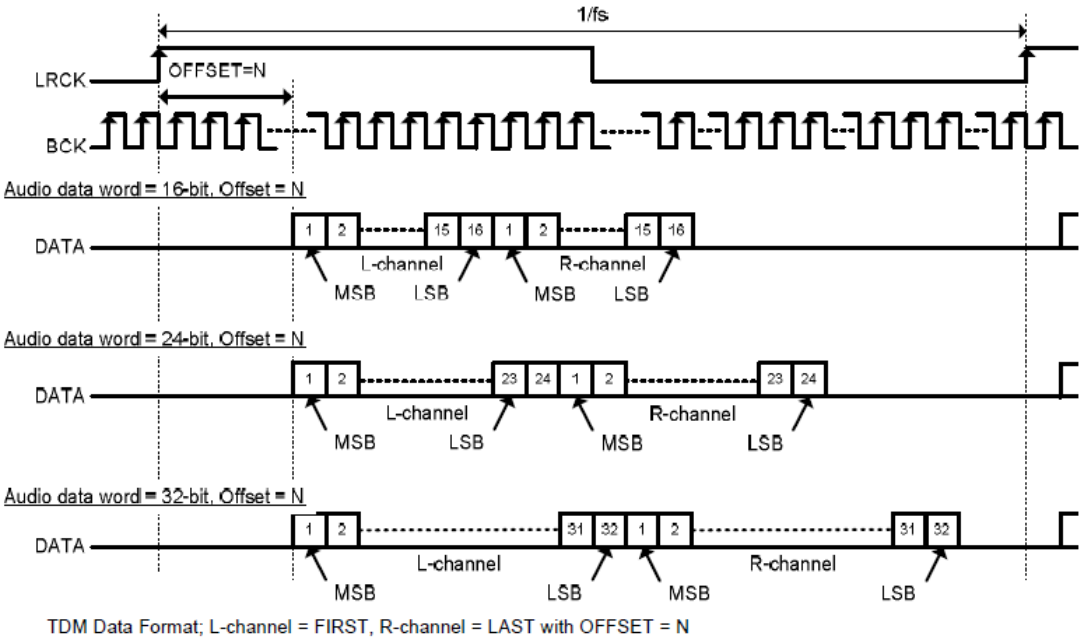

Figure 42. TDM 3 Audio Data Format

7.4.7 TAS576xM Audio Processing Options

7.4.7.1 Overview

The TAS576xM features a configurable miniDSP core. The algorithms for the miniDSP are loaded into the device after power up. The miniDSP has direct access to the digital stereo audio stream, offering the possibility for advanced DSP algorithms with very low group delay. The miniDSP can run up to 1024 instructions on every audio sample at a 48 kHz sample rate.

The TAS576xM Smart Amplifier uses a mix of code sources. ROM based process flow and RAM based process flow. In the program, different algorithms are called from ROM – such as EQ, DRC and Zero Crossing volume control enabling a faster program load.

7.4.7.2 miniDSP Instruction Register

Registers on Register Pages 152-169 are 25-bit instructions for the miniDSP engine. For details, see Table 21. Seven (7) bits of Instr(32:25) in Base register +0 are reserved bits. 1 bit of Instr(24) – (LSB) in Base register +0 is MSB bit of 25-bit instruction. These instructions control miniDSP operation. When the fully programmable miniDSP mode is enabled and the DAC channel is powered up, the read and write access to these registers is disabled

7.4.7.3 Digital Output

The TAS576xM supports an SDOUT output. This can be selected within the process flow, and driven out of a GPIO pin selected in the register map (e.g. Page 0 / Register 80). The I2S output can be fed back to the signal host and used for echo cancellation.

7.4.7.4 Software

Software selection for the TAS576xM is supported through TI's comprehensive PurePath Console Development Environment; a powerful, easy-to-use tool designed specifically to simplify development on the TAS576xM platform. Visit the TAS576xM product folder on www.ti.com to learn more about PurePath Console and the latest status on available, ready-to-use DSP algorithms.

7.4.7.5 Process Flow

An example of the default Process Flow available for the TAS576xM in the PurePath Console target is shown below:

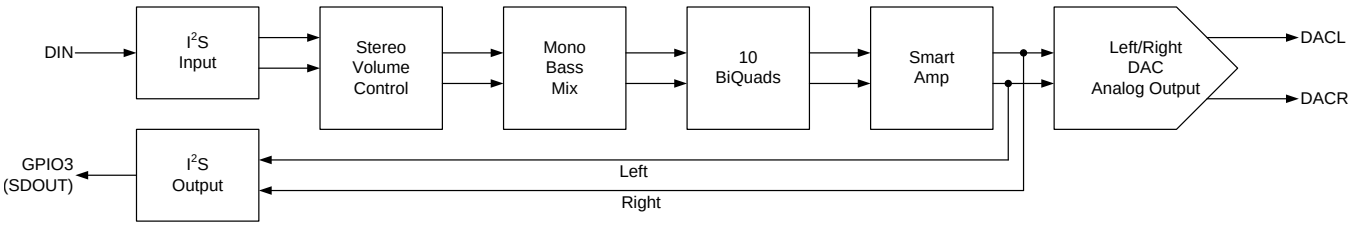

Figure 43. Example Process Flow

This process flow has from input to output:

- Volume block, from -110 db to +6 dB with 0.5 dB steps, including a fixed gain block of 0dB to 12 dB gain
- monobass mixer – mixes the bass into mono below the set frequency, useful for systems where left and right speaker shares the same cabinet volume, bypassed when not needed.
- 10 Biquads for filtering and EQ. The PPC GUI have an advanced biquad control where various filter and eq options can be set and controlled.
- SmartAmp block, containing all the blocks for bass Q compensation, bass alignment, excursion control and power limited
- Digital monitor output enabled on GPIO3

7.4.7.6 Zero Data Detect

The TAS576xM has a zero-detect function. When the device detects the continuous zero data for both L-ch and R-cn, or separate L-cn and R-ch, Analog mutes are set to both OUTL and OUTR, or separate OUTL and OUTR. These are controlled by Page0, Register 65, D(2:1) as shown in Table 13.

Continuous Zero data cycles are counted by LRCLK, and the threshold of decision for analog mute can be set by Page 0, Register 59, D(6:4) for L-ch, and D(2:0) for Rch as shown in Table 14. Default values are 0 for both channels.

Table 13. Zero Detection Mode

ATMUTECTL	VALUE	FUNCTION
Bit:2	0	Independently L-ch or R-ch are zero data for zero detection
	1 (Default)	Both L-ch and R-ch have to be zero data for zero detection
Bit:1	0	Zero detection and analog mute are disabled for R-ch
	1 (Default)	Zero detection and analog mute are enabled for R-ch
Bit:0	0	Zero detection and analog mute are disabled for L-ch
	1 (Default)	Zero detection and analog mute are enabled for L-ch

Table 14. Zero Data Detection Time

ATMUTETIML /ATMUTETIMR	NUMBER of LRCLKs	TIME at 48 kHz
0 0 0	1024	21 ms
0 0 1	5120	106 ms
0 1 0	10240	213 ms
0 1 1	25600	533 ms
1 0 0	51200	1.07 sec
1 0 1	102400	2.13 sec
1 1 0	256000	5.33 sec
1 1 1	512000	10.66 sec

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7.4.7.7 Power Save Modes

The TAS576xM offers two power-save modes; standby and power-down.

When a clock error (SCLK, BCLK, and LRCLK) or clock halt is detected, the TAS576xM automatically enters standby mode. The DAC and power amplifier are also powered down. The device can also be placed in standby mode via software command.

When BCLK and LRCLK remain at a low level for more than 1 second, the TAS576xM automatically enters power-down mode. Power-down mode disables the negative charge pump and bias/reference circuit, in addition to those disabled in standby mode. The device can also be placed in power-down mode via I^2C command.

When expected Audio clocks (SCLK, BCLK, LRCLK) are applied to the TAS576xM, the device starts its power-up sequence automatically.

Table 15. Power Save Parameter Programming

REGISTER	DESCRIPTION
Page 0, register 2, D(4)	I^2C standby-mode command
Page 0, register 2, D(0)	I^2C power-down command
Page 0, register 2, D(4) and D(0)	I^2C power-up sequence command (required after I^2C standby or power-down command)
Page 0, register 44, D(2:0)	Detection time of BCLK and LRCLK halt

7.4.7.8 XSMT Pin (Soft Mute/Soft Un-Mute)

An external digital host controls the TAS576xM soft mute function by driving the XSMT pin with a specific minimum rise time (tr) and fall time (tf) for soft mute and soft un-mute. The TAS576xM requires tr and tf times of less than 20ns. In the majority of applications, this is no problem, however, traces with high capacitance may have issues.

When the XSMT pin is shifted from high to low (3.3V to 0V), a soft digital attenuation ramp begins. –1dB attenuation is then applied every sample time from 0dBFS to –104dBFS.

When the XSMT pin is shifted from low to high (0V to 3.3V), a soft digital “un-mute” is started. 1dB gain steps are applied every sample time from –104dBFS to 0dBFS.

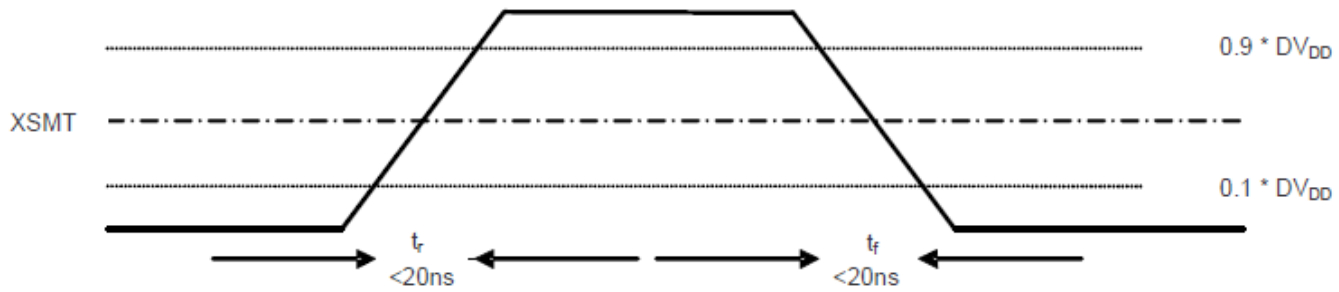

Figure 44. XSMT Timing for Soft Mute and Soft Un-Mute

7.4.7.9 External Power Sense Undervoltage Protection Mode

The XSMT pin can also be used to monitor a system voltage, such as the 24-VDC LCD TV back light, or 12-VDC system supply using a voltage divider created with two resistors. See Figure 45.

* If the XSMT pin makes a transition from “1” to “0” over 6ms or more, the device switches into external undervoltage protection mode. This mode uses two trigger levels.
* When the XSMT pin level reaches 2 V, soft mute process begins.
* When the XSMT pin level reaches 1.2 V, analog mute engages, regardless of digital audio level, and analog shutdown begins. (DAC and related circuitry powers down).

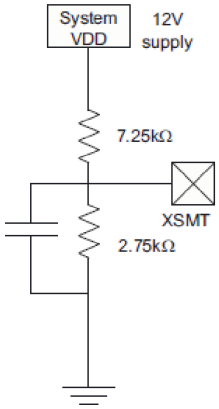

Figure 45. External Power Sense

A timing diagram describing this is shown in Figure 46.

NOTE

The XSMT input pin voltage range is from –0.3 V to DVDD + 0.3 V.The ratio of external resistors must produce a voltage within this input range. Any increase in power supply (such as power supply positive noise or ripple) can pull the XSMT pin higher than DVDD +0.3V.

For example, if the TAS576xM is monitoring a 12 V input, and dividing the voltage by 4, then the voltage at XSMT during ideal power supply conditions is 3 V. A voltage spike higher than 14.4 V causes a voltage greater than 3.6 V (DVDD+0.3) on the XSMT pin, potentially damaging the device. Providing the divider is set appropriately, any DC voltage can be monitored.

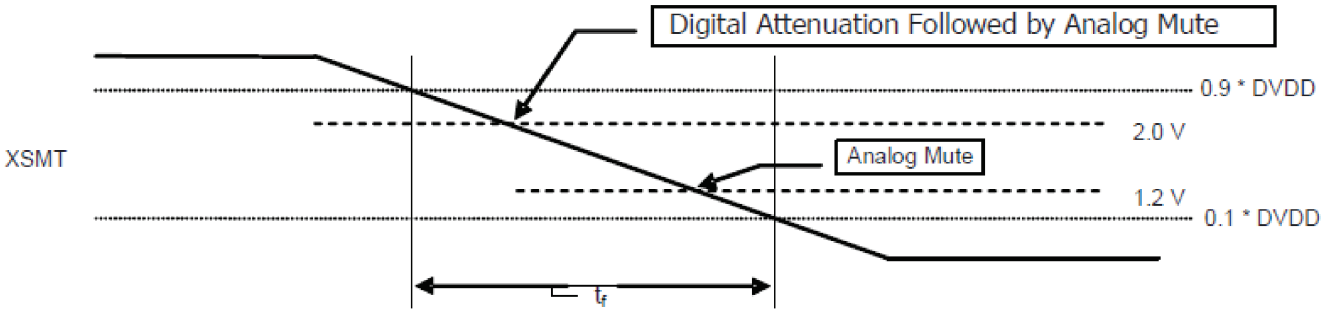

Figure 46. XSMT Timing for Undervoltage Protection

7.4.7.10 Recommended Power Down Sequence

With inadequate system design, the TAS576xM can exhibit pop on power down. Pops are caused by the device not having enough time to detect power loss and start the muting process.

The TAS576xM evaluation board avoids audible pop with an electrolytic decoupling capacitor. This capacitor provides enough time between data loss from USB or S/PDIF and power supply loss for the muting process to take place.

The TAS576xM has two auto-mute functions to mute the device upon power loss (intentional or unintentional).

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7.4.7.10.1 XSMT = 0

When the XSMT pin is pulled low, the incoming PCM data is attenuated to 0, then closely followed by a hard analog mute. This process takes 150 sample times (t_S) + 0.2 mS.

7.4.7.10.2 Clock Error Detect

When clock error is detected on the incoming data clock, the TAS576xM family switches to an internal oscillator, and continues to the drive the output, while attenuating the data from the last known value. Once this process is complete, the TAS576xM outputs are pulled to ground with 30kΩ.

7.4.7.10.3 Planned Shutdown

These auto-muting processes can be manipulated by system designs to mute before power loss in the following ways: Assert XSMT low 150t_s + 0.2 ms before power is removed, shown in Figure 47.

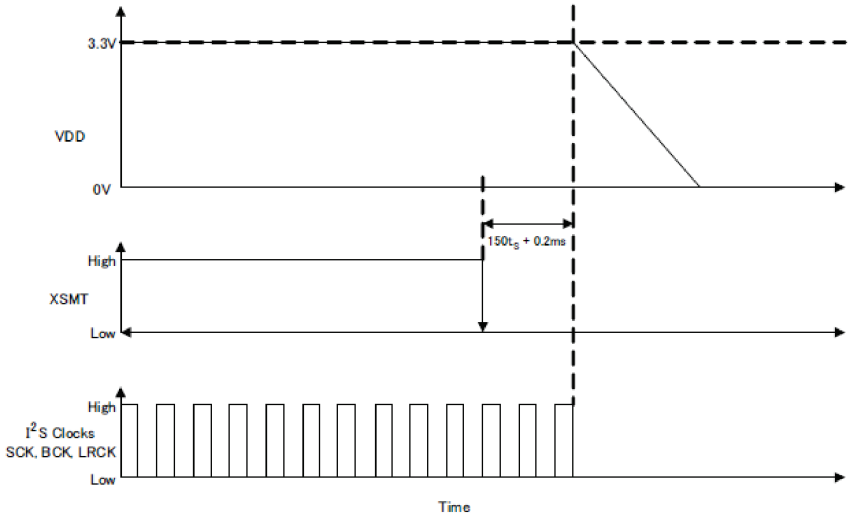

Figure 47. Assert XSMT Low Example

Stop I^{2}S clocks (SCLK, BCLK, LRCLK) 3ms before power down as shown in Figure 48 below:

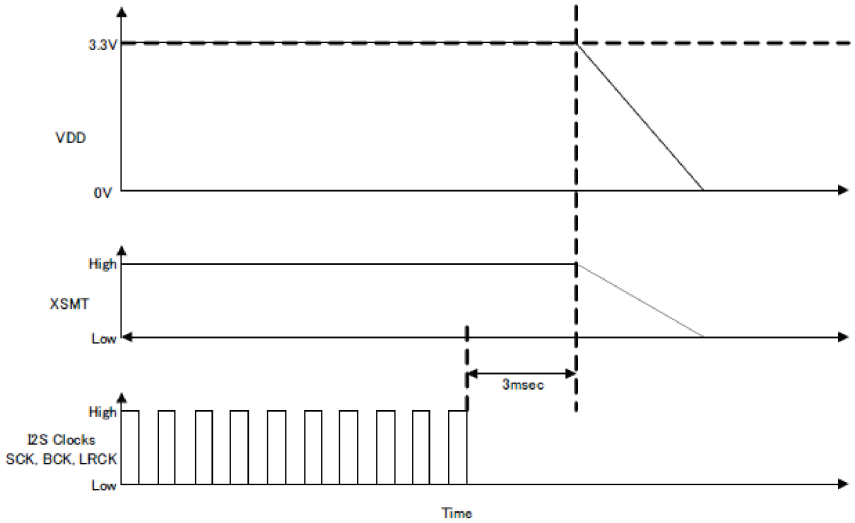

Figure 48. Stop I^{2}S Clocks Example

7.5 Programming

7.5.1 I²C Interface and Slave Address

The TAS576xM supports the I²C serial bus and the data transmission protocol for standard and fast mode as a slave device.

Table 16. I²C pins and Functions

SIGNAL	PIN	I/O	DESCRIPTION
SDA	16	I/O	I2C data
SCL	17	I	I2C clock
ADR2	20	I	I2C address 2
ADR1	26	I	I2C address 1

7.5.2 Slave Address

Table 17. I²C Slave Address

Address	D7	D6	D5	D4	D3	ADR2	ADR1	R/W
0x98	1	0	0	1	1	0	0	x
0x9A						0	1	
0x9C						1	0	
0x9E						1	1	

The TAS576xM has 7 bits for its own slave address. The first five bits (MSBs) of the slave address are factory preset to 10011 (0x9x). The next two bits of the address byte are the device select bits which can be user defined by the ADR1 and ADR0 pins. A maximum of four TAS576xMs can be connected on the same bus at one time. This gives a range of 0x98, 0x9A, 0x9C and 0x9E. Each TAS576xM responds when it receives its own slave address.

7.5.3 Register Address Auto-Increment Mode

Auto-increment mode allows multiple sequential register locations to be written to or read back in a single operation, and is especially useful for block write and read operations.

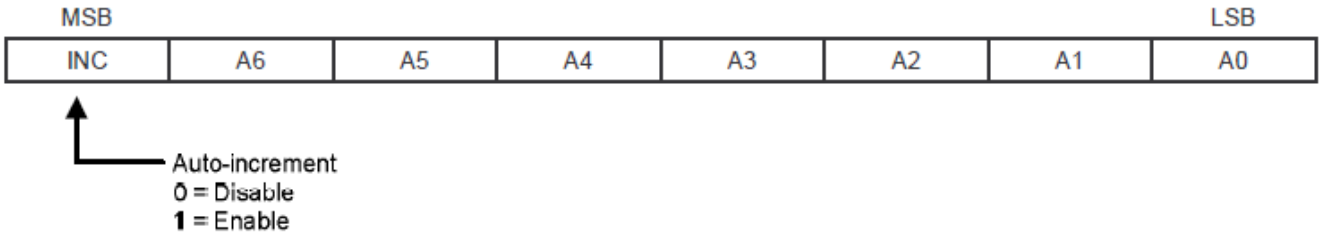

Figure 49. Auto Increment Mode

7.5.4 Packet Protocol

A master device must control packet protocol, which consists of start condition, slave address, read/write bit, data if write or acknowledge if read, and stop condition. The TAS5766M supports only slave receivers and slave transmitters.

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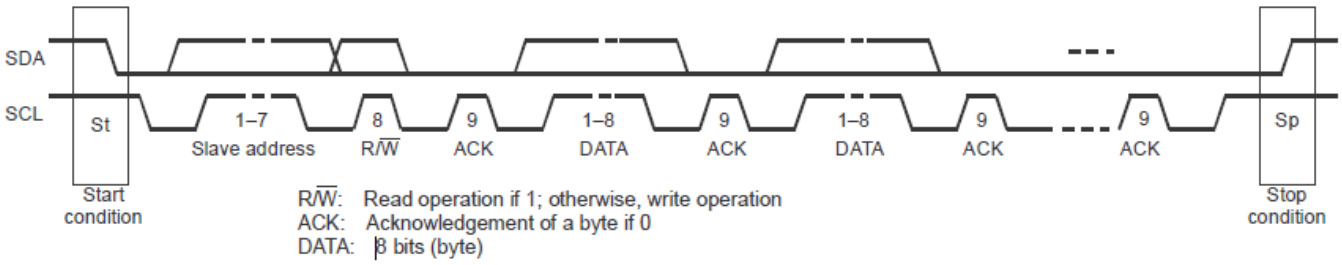

Figure 50. Packet Protocol

Table 18. Read / Write Operation – Basic I²C Framework

Transmitter Write	**M**	**M**	**M**	**S**	**M**	**S**	**M**	**S**		**S**	**M**
Data Type	St	Slave address	W/	ACK	DATA	ACK	DATA	ACK		**ACK**	Sp
Transmitter Read	**M**	**M**	**M**	**S**	**S**	**M**	**S**	**M**		**M**	**S**
Data Type	St	Slave address	R/	ACK	DATA	ACK	DATA	ACK		**NACK**	Sp
M = Master Device; S = Slave Device; St = Start Condition; Sp = Stop Condition											

7.5.5 Write Register

A master can write to any TAS576xM registers using single or multiple accesses. The master sends a TAS576xM slave address with a write bit, a register address with auto-increment bit, and the data. If auto-increment is enabled, the address is that of the starting register, followed by the data to be transferred. When the data is received properly, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x0. The following table shows the write operation.

Table 19. Write Operation

Transmitter	**M**	**M**	**M**	**S**	**M**		**S**	**M**	**S**	**M**	**S**		**S**	**M**
Data Type	St	Slave addr	W	ACK	inc	reg addr	ACK	Write data1	ACK	Write data2	ACK		ACK	Sp
M = Master Device; S = Slave Device; St = Start Condition; Sp = Stop Condition; W = Write; ACK = Acknowledge														

7.5.5.1 Read Register

A master can read the TAS576xM register. The value of the register address is stored in a indirect index register in advance. The master sends a TAS576xM slave address with a read bit after storing the register address. Then the TAS576xM transferes the data which the index points to. When auto-increment is enabled, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x0. The following table shows the read operation.

Table 20. Read Operation

Transmitter	**M**	**M**	**M**	**S**	**M**		**S**	**M**	**M**	**M**	**S**	**S**	**M**		**M**	**M**
Data Type	St	Slave addr	W	ACK	inc	reg addr	ACK	Sr	Slave addr	R	ACK	data	ACK		NACK	Sp
M = Master Device; S = Slave Device; St = Start Condition; Sr = Repeated start condition; Sp = Stop Condition; W = Write; R 0 read; NACK = Acknowledge																

7.6 Register Maps

In any page, register 0 is the Page Select Register. The register value selects the Register Page from 0 to 255 for next read or write command.

Table 21. Register Map Summary(1)

Register No	Description		Register No	Description
Page 0			44	Clock missing detection period
0	Page Select register		59	Auto mute time
1	Analog control register		60-64	Reserved
2	Standby, Powerdown requests		65-66	Auto mute enable and delay
3	Mute		67-82	Reserved
4	PLL Lock Flag, PLL enable		83-85	GPIOn output selection
5	Reserved		86,87	GPIO control
6	Reserved		88,89	Reserved
7	De-emphasis enable, SDOUT select		90	DSP overflow
8	GPIO enables & Mute Control		91-94	Sample rate status
9	BCLK, LRCLK configuration		95-107	Reserved
10	DSP GPIO Input		108	Analog mute monitor
11	Reserved		109-118	Reserved
12	Master Mode BCLK, LRCLK reset		119	GPIO input
13	PLL clock source select		120	Auto mute flags
14-19	Reserved		121-125	Reserved
20-24	PLL dividers		**Page 1**	
25,26	Reserved		1	Reserved
27	DSP clock divider		2	Analog gain control
28	DAC clock divider		3,4	Reserved
29	NCP clock divider		5	Undervoltage protection
30	OSR clock divider		6	Analog mute control
31	Reserved		7	Analog gain boost
32,33	Master mode dividers		8	REF BG Fast
34	FS speed mode		9-15	Reserved
35,36	IDAC number of DSP clock cycles available in one audio frame)		**Page 44**	
37	Ignore various errors		1	Coefficient memory (CRAM) control
38,39	Reserved		Pages 44-52	Coefficient buffer – A (256 coeffs x 24 bits)
40,41	I2S configuration		Pages 62-70	Coefficient buffer – B (256 coeffs x 24 bits)
42	DAC data path		Pages 152-186	Instruction buffer (1024 instruction x 24 bits), I512 – I1023 are reserved
43	Reserved		Pages 187-255	Reserved

(1) See *Detailed Register Map Descriptions*.

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8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

One of the most significant benefits of the TAS5766M device is the ability to be used in a variety of applications. This section details the information needed to configure the device for several popular configurations and provides guidance on integrating the TAS5766M device into the larger system.

8.1.1 External Component Selection Criteria

The Supporting Component Requirements table in each application description section lists the details of the supporting required components in each of the System Application Schematics.

Where possible, the supporting component requirements have been consolidated to minimize the number of unique components which are used in the design. Component list consolidation is a method to reduce the number of unique part numbers in a design, to ease inventory management, and reduce the manufacturing steps during board assembly. For this reason, some capacitors are specified at a higher voltage than what would normally be required. An example of this is a 50-V capacitor may be used for decoupling of a 3.3-V power supply net.

In this example, a higher voltage capacitor can be used even on the lower voltage net to consolidate all caps of that value into a single component type. Similarly, a several unique resistors, having all the same size and value but with different power ratings can be consolidated by using the highest rated power resistor for each instance of that resistor value.

While this consolidation may seem excessive, the benefits of having fewer components in the design may far outweigh the trivial cost of a higher voltage capacitor. If lower voltage capacitors are already available elsewhere in the design, they can be used instead of the higher voltage capacitors. In all situations, the voltage rating of the capacitors must be at least 1.45 times the voltage of the voltage which appears across them. The power rating of the capacitors should be 1.5 times to 1.75 times the power dissipated in it during normal use case.

8.1.2 Component Selection Impact on Board Layout, Component Placement, and Trace Routing

Because the layout is important to the overall performance of the circuit, the package size of the components shown in the component list were intentionally chosen to allow for proper board layout, component placement, and trace routing. In some cases, traces are passed in between two surface mount pads or ground plane extends from the TAS5766M device between two pads of a surface mount component and into to the surrounding copper for increased heat-sinking of the device. While components may be offered in smaller or larger package sizes, it is highly recommended that the package size remain identical to that used in the application circuit as shown. This consistency ensures that the layout and routing can be matched very closely, optimizing thermal, electromagnetic, and audio performance of the TAS5766M device in circuit in the final system.

8.1.3 Amplifier Output Filtering

The TAS5766M device is often used with a low-pass filter, which is used to filter out the carrier frequency of the PWM modulated output. This filter is frequently referred to as the L-C Filter, due to the presence of an inductive element L and a capacitive element C to make up the 2-pole filter.

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Application Information (continued)

The L-C filter removes the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which is drawn from the power supply. The presence and size of the L-C filter is determined by several system level constraints. In some low-power use cases that do not have other circuits which are sensitive to EMI, a simple ferrite bead or ferrite bead and capacitor can replace the traditional large inductor and capacitor that are commonly used. In other high-power applications, large toroid inductors are required for maximum power and film capacitors may be preferred due to audio characteristics. Refer to the application report SLOA119 for a detailed description on proper component selection and design of an L-C filter based upon the desired load and response.

8.2 Typical Applications

8.2.1 Stereo Application

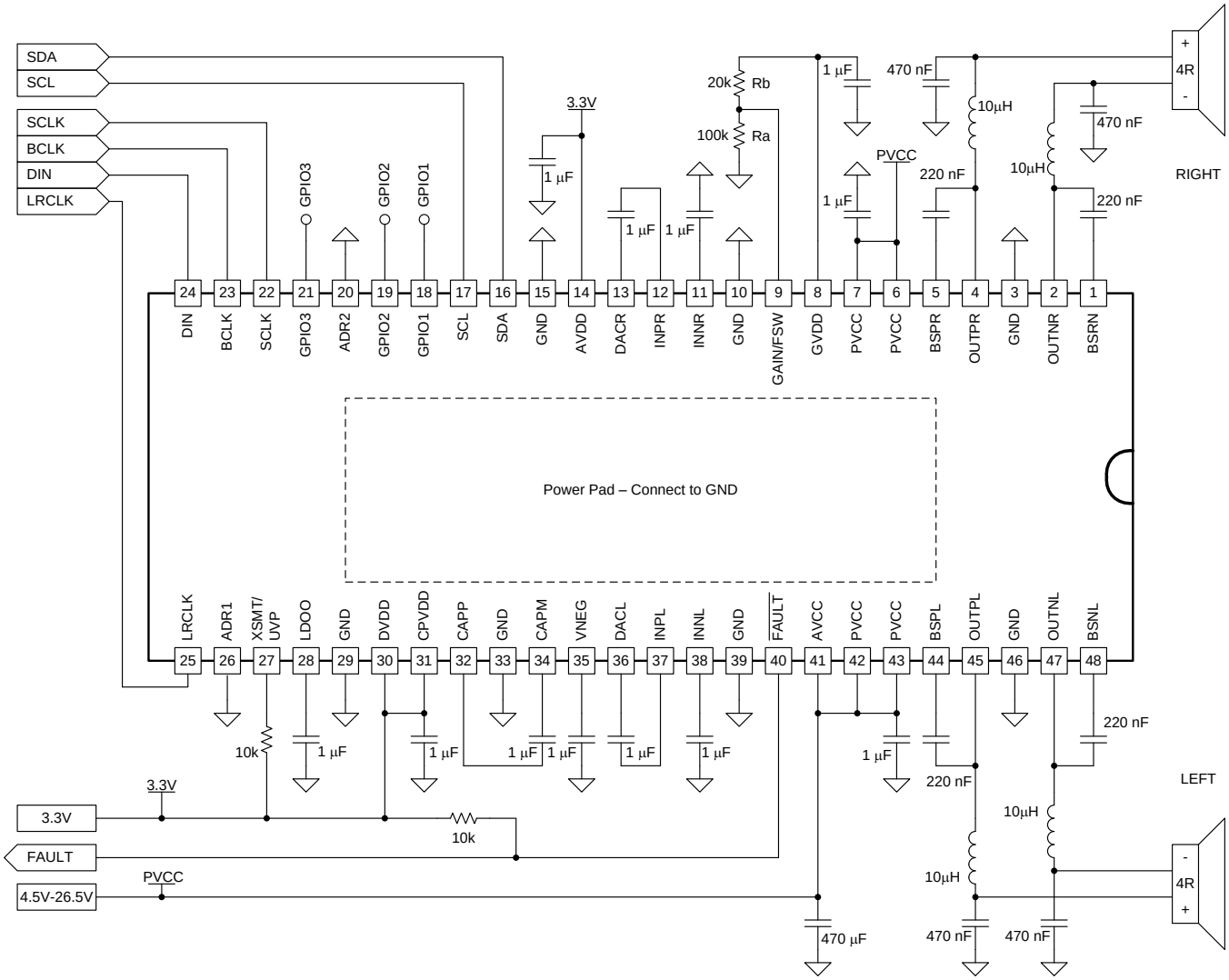

Figure 51. Typical Stereo Application

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Typical Applications (continued)

8.2.1.1 Design Requirements

The device is configured to have 20 dB analog gain and switch at 768kHz, by the resistor network on the GAIN/FSW pin 9.

I^2C slave address is set to default 0x98, as a result of the two address pins (ADR1, pin 26 and ADR2, pin 20) set to ground.

In this setup a master clock is supplied to the device on pin 22 (SCLK). the device can also run with 3-wire I2S by setting the PLL registers as shown in the *Clock Generation and PLL* section.

When the device is configured to operate in 3-wire mode of operation where BCLK is used as reference to PLL (NO SCLK), TI recommends shorting PIN23 (BCLK) and PIN22 (SCLK) and configuring the device to use SCLK as PLL reference.

8.2.1.2 Detailed Design Procedure

For the stereo (BTL) PCB layout, see examples in the *Layout* section.

A 2.0 system generally refers to a system in which there are two full range speakers without a separate amplifier path for the speakers which reproduce the low-frequency content. In this system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers. In some cases, the amplified signal is further separated based upon frequency by a passive crossover network after the L-C filter. Even so, the application is considered 2.0.

Most commonly, the two channels are a pair of signals called a stereo pair, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While certainly the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

It is important to note that the SmartAmp Flows which have been developed for specifically for stereo applications will apply the same equalizer curves to the left channel and the right channel. This minimizes the needed RAM capabilities of the SmartAmp.

When two signals that are not two separate signals, but instead are derived from a single signal which is separated into low frequency and high frequency by the signal processor, the application is commonly referred to as 1.1 or Bi-Amped systems. The 2.0 (Stereo BTL) System application is shown in Figure 51.

8.2.1.2.1 Gain Setting and Output Switch Frequency

The analog class-D amplifier gain of the TAS576xM is set by the voltage divider connected to the GAIN/FSW control pin. Output Stage switch frequency multiplication is also controlled by the same pin, giving a ratio of 8, 10, 12 or 16x the I2S input sample rate. An internal ADC is used to detect the 8 input states. The first four stages sets the GAIN to 14 dB, while the next four stages sets the GAIN to 20 dB.

A gain setting of 14 dB is recommended for supply voltages of 12V and lower, while a gain of 20 dB is recommended for supply voltages up to 26.4 V. Table 22 shows the recommended resistor values and the state and gain:

Table 22. Gain and FSW

Ra (to GND)	Rb (to GVDD)	INPUT IMPEDANCE	GAIN	FSW – RATIO TO LRCLK	FSW w. 44.1 kHz	FSW w. 48 kHz
10 0kΩ	OPEN	120 kΩ	14 dB	8	353 kHz	384 kHz
20 kΩ	100 kΩ	120 kΩ	14 dB	10	441 kHz	480 kHz
38 kΩ	100 kΩ	120 kΩ	14 dB	12	529 kHz	576 kHz
47 kΩ	75 kΩ	120 kΩ	14 dB	16	706 kHz	768 kHz
51 kΩ	51 kΩ	60 kΩ	20 dB	8	353 kHz	384 kHz
75 kΩ	47 kΩ	60 kΩ	20 dB	10	441 kHz	480 kHz
100 kΩ	39 kΩ	60 kΩ	20 dB	12	529 kHz	576 kHz
100 kΩ	20 kΩ	60 kΩ	20 dB	16	706 kHz	768 kHz

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8.2.1.2.2 Gain Setting and Supply Voltage

If the TAS576xM is to be used in systems operating below 6 V it is recommended to change the maximum DAC output voltage from the nominal 2 Vrms FS(0 dB) to 1 Vrms FS (–6 dB), by setting register 2 on page 1 D4(Lch) / D0(Rch), Table 23.

Table 23. GAIN and Supply Voltage

SUPPLY VOLTAGE RANGE	GAIN (via GAIN/FSW pin)	DAC OUTPUT at FS	Page 1 / Register 2
4.5 V – 6 V	14 dB	1 V_{rms}	00010001
6 V – 12 V	14 dB	2 V_{rms}	default
12 V – 26 V	20 dB	2 V_{rms}	default

8.2.1.2.3 DAC to AMP AC Coupling

The TAS576xM uses an external ac-coupling capacitor between DACx output and AMP INPx input and a capacitor from INNx to ground for minimum dc-offset and click & pop during power on/off. Shown as C13, C14, C19 & C20 in the drawing here.

The AMP INNPx and INNMx input stage is a fully differential input stage and the input impedance changes with the gain setting from 120 kΩ at 14 dB gain to 60 kΩ at 20 dB gain. The tolerance of the input resistor value is ±20%.

The input ac-coupling capacitor together with the input impedance forms a high-pass filter with the following cut-off frequency:

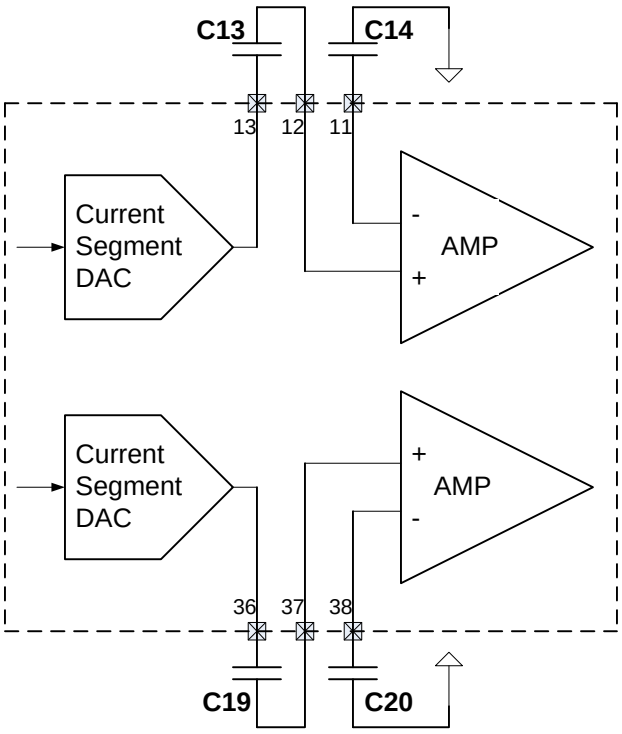

Figure 52. DAC to AMP AC Coupling

If a flat bass response is required down to 20Hz the recommended cut-off frequency is a tenth of that, 2 Hz.

Table 24 lists the recommended ac-coupling capacitors for the two gain step over a range of desired system high pass filter frequency.

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Table 24. F3dB Versus Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	0.1 µF	0.22 µF	0.33 µF	0.47 µF	1 µF	2.2 µF
14 dB	120 kΩ	13 Hz	6 Hz	4 Hz	3 Hz	1.3 Hz	0.6 Hz
20 dB	60 kΩ	26 Hz	12 Hz	8 Hz	6 Hz	2.7 Hz	1.2 Hz

The input capacitors used should be a type with low leakage, like film or quality ceramic X5R or X7R with high voltage rating. If a polarized type is used the negative connection should face the DACx output pins. INPx and INMx are biased at 3Vdc.

8.2.1.2.4 Bootstrap Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor, rated for at least 16 V, must be connected from each output to its corresponding bootstrap input. See the application circuit diagram in *智能放大器概览*.

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

8.2.1.3 BTL Application Curves

The following graphs shows the frequency response with different output filter configurations: Figure 53: 4-Ω load with 680 nF and 10-µH output filter, Figure 54: 4-Ω load with 330 nF and 4.7-µH inductor. Both setups are using 220 nF for the DAC-to-amp AC coupling capacitor.

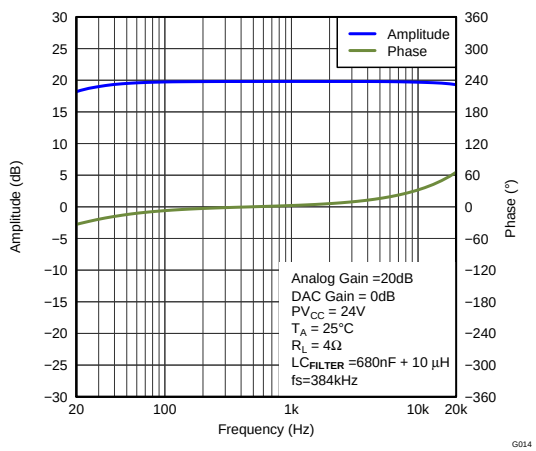

Figure 53. Gain/Phase vs Frequency

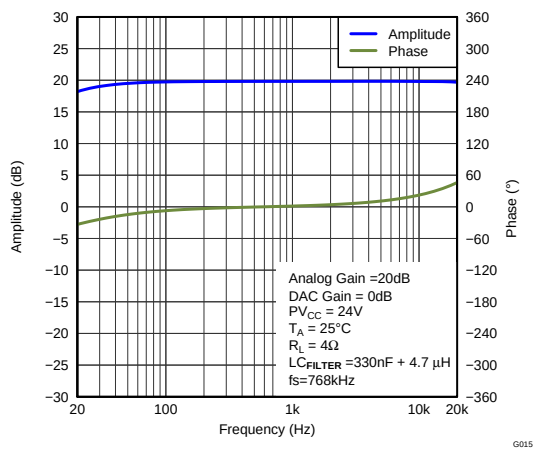

Figure 54. Gain/Phase vs Frequency

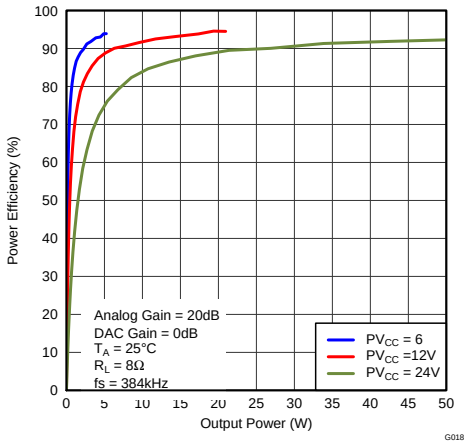

Figure 55. Power Efficiency vs Output Power

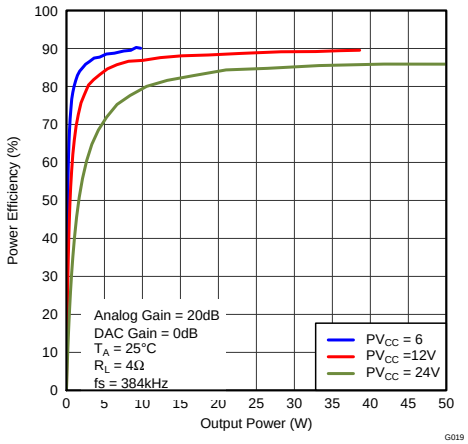

Figure 56. Power Efficiency vs Output Power

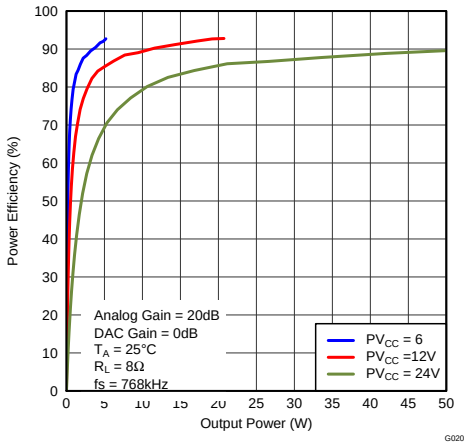

Figure 57. Power Efficiency vs Output Power

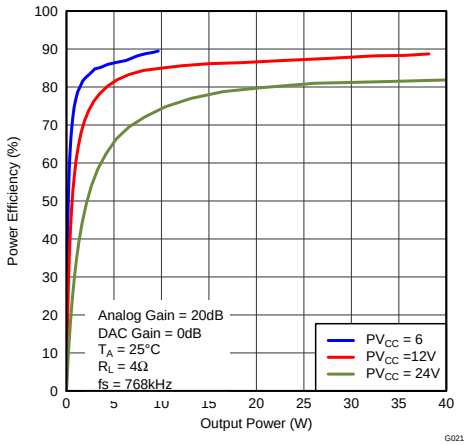

Figure 58. Power Efficiency vs Output Power

8.2.2 Mono/PBTL Application

The TAS576xM can be configured in MONO mode enabling up to 100 W peak output power into 2-Ω speaker. This is done by:

- Connect INPL and INNL directly to GND (without capacitors) this sets the device in Mono mode during power up.
- Connect OUTNR and OUTPR together for the positive speaker terminal and OUTPL and OUTNL together for the negative terminal

In mono mode the right DAC channel, DACR, is used as input for the speaker amplifier, INPR. The left channel DACL can be used for a external AMP if more channels and power is needed.

The combined output can source up to 15A – so be careful to select inductors that can handle that level of current, if inductors with that high saturation current is not available, the PBTL connection can be made after the inductors, this setup is shown in the PBTL application section.

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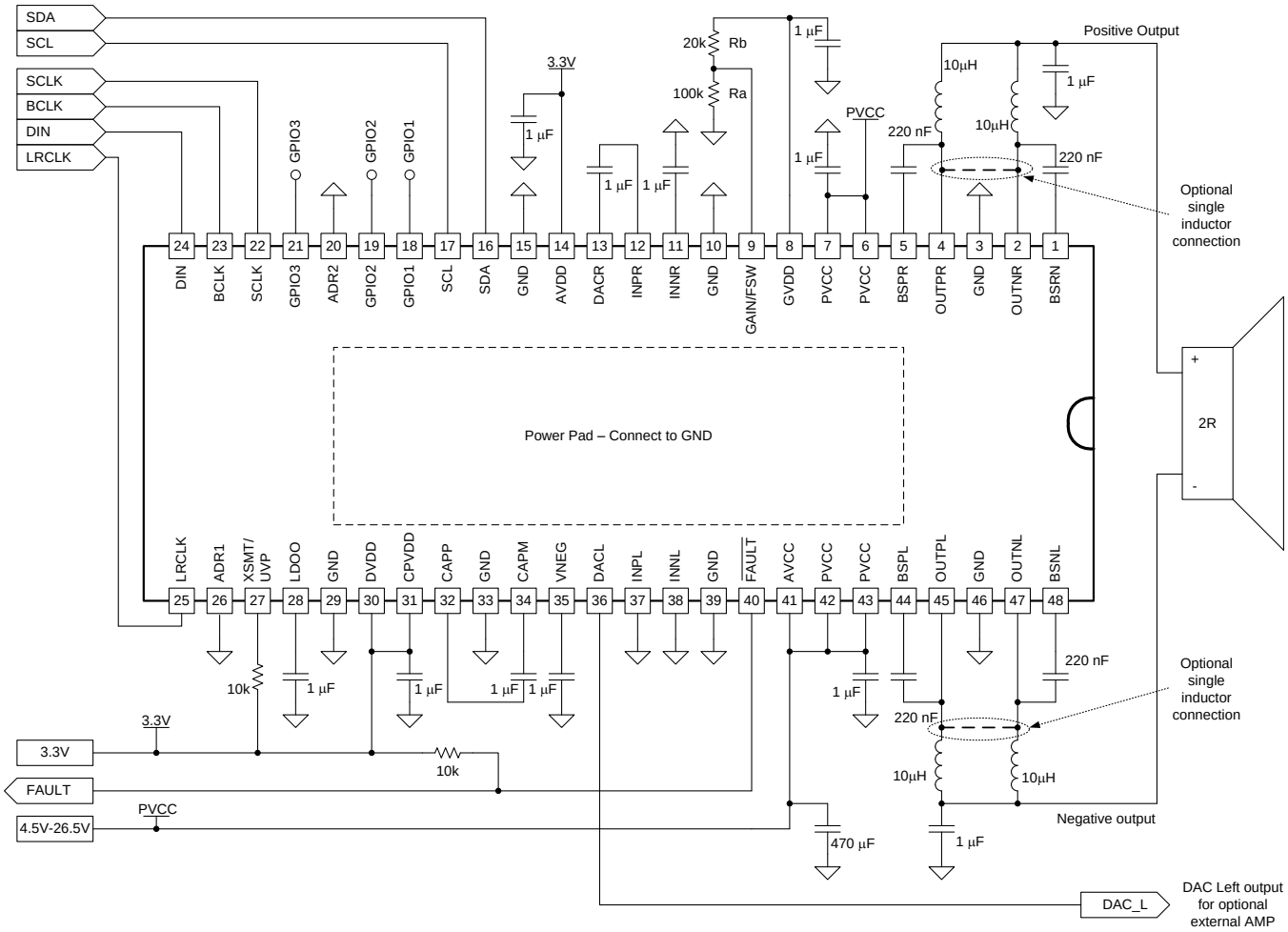

Figure 59. Mono/PBTL Application

8.2.2.1 Design Requirements

See Stereo Application *Design Requirements*.

8.2.2.2 PBTL Application Curves

Figure 60 shows power efficiency of the TAS5766MDCAEVM configured in PBTL mode as described in section *Mono/PBTL Application*.

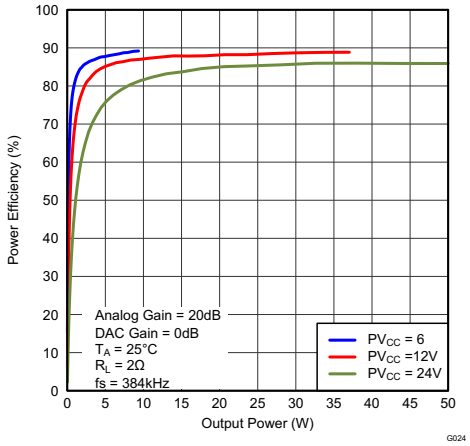

Figure 60. Power Efficiency (PBTL) vs Output Power

8.2.3 QFN BTL Application Diagram

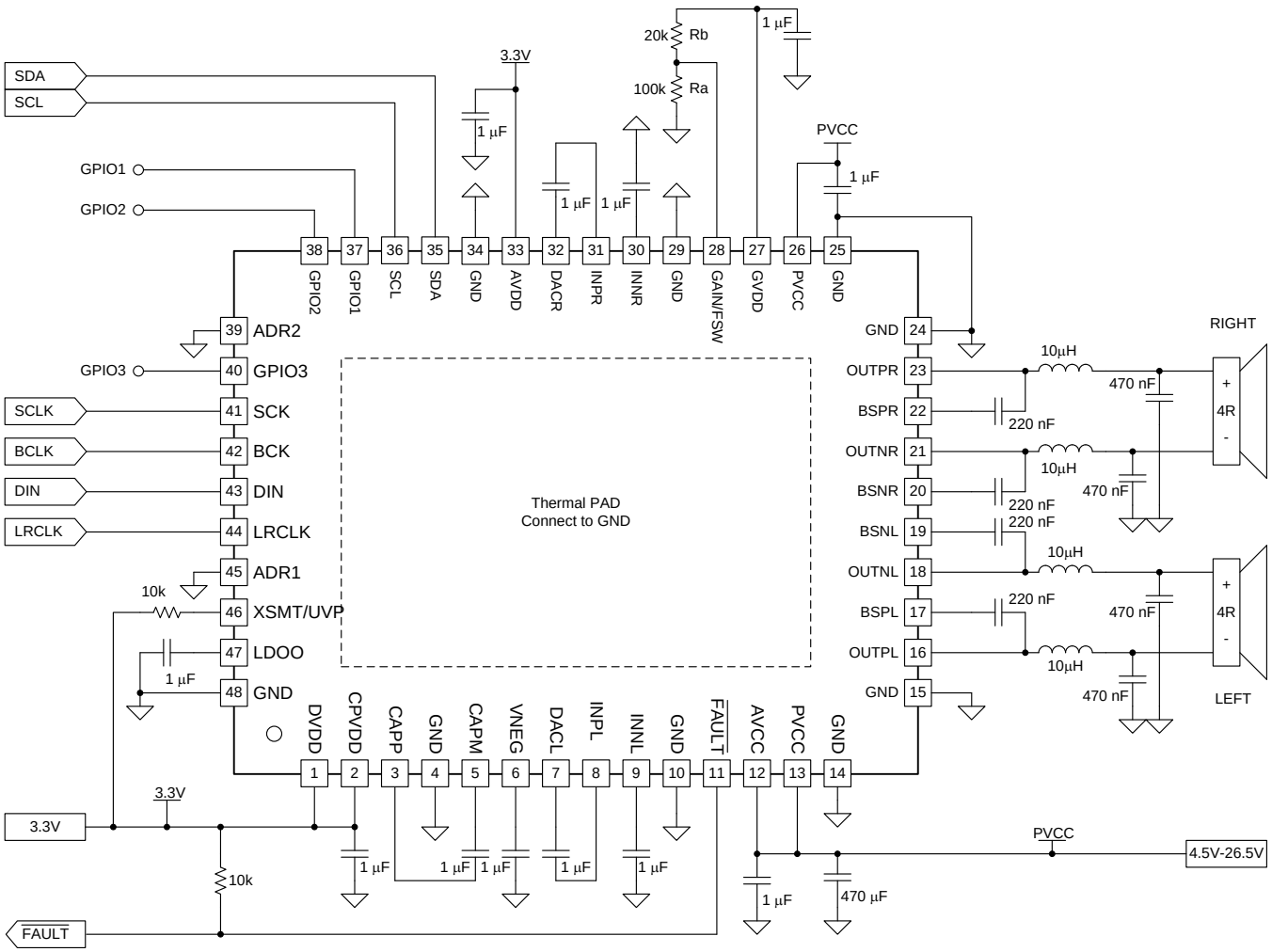

Figure 61. QFN BTL Application

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8.2.3.1 Design Requirements

See the Stereo *Design Requirements* section.

9 Power Supply Recommendations

The TAS576xM requires two power supplies; a low voltage 3.3 V nominal for the pins, AVDD, DVDD and CPVDD and a high power supply, 4.5 V to 26.5 V for the pins PVCC and AVCC.

There is no requirement for sequencing of DVDD and PVCC, either supplies can ramp first.

9.1 AVDD, DVDD, CPVDD Supply

The AVDD Supply is used to power the DAC analog output stage, and needs a well regulated and filtered 3.3-V supply voltage. The DVDD Supply is used to power the digital circuitry for I2S input, I2C input, GPIO blocks and the audio DSP. DVDD needs a well regulated and filtered 3.3-V supply voltage.

9.2 GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. It is also used to supply the GAIN/FSW voltage divider. Decouple GVDD with a X7R ceramic 1-µF capacitor to GND. The GVDD supply is not intended to be used for external supply. It is recommended to limit the current consumption by using resistor voltage dividers for GAIN/FSW of 100 kΩ or more.

9.3 PVCC, AVCC Power Supply

The TAS576xM high performance class-D audio system requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) and noise is as low as possible.

Optimum decoupling is achieved by placing a good quality low equivalent-series-resistance (ESR) ceramic capacitor larger than 220nF as close to the device PVCC pins and system ground plane as possible.

For filtering lower frequency signals and handling the switching ripple current, a larger aluminum electrolytic capacitor of 470µF or greater placed near the audio power amplifier is recommended. The 470-µF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs.

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10 Layout

10.1 Layout Guidelines

The TAS576xM can be used with a small, inexpensive ferrite bead output filter when speaker are placed with short internal wires and supply voltages are 12 V or lower, for systems with longer wires or higher than 12V supply voltage LC filtering is recommended.

Class-D switching edges are fast and swithced currents are high so it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet audio, thermal and EMC requirements

- TAS576xM uses the PCB for heatsinking therefore the powerPad need to be soldered to the PCB and adquate cobber area and cobber via's connecting the top, bottom and internal layers should be used.
- Decoupling capacitors — The high-frequency decoupling capacitors should be placed as close to the PVDD and AVCC pins as possible, on the TAS576xM a 1-µF high-quality ceramic capacitor is used. Large (470 µF or greater) bulk power supply decoupling capacitors should be placed near the TAS576xM on the PVDD supplies. Local, high-frequency bypass capacitors should be placed as close to the DVDD, AVDD and CPVDD pins as possible.
- Keep the current loop from each of the outputs through the output inductor and the small filter cap and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding — A big common GND plane is recommended. The PVDD decoupling capacitors should connect to GND. The TAS576xM power pad should be connected to GND
- Output filter — remember to select inductors that can handle the high short circuit current of the device. The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded

The EVM user guide available on www.ti.com shows both schematic, bill of material and more detailed layout plots including gerber files.

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10.2 Layout Examples

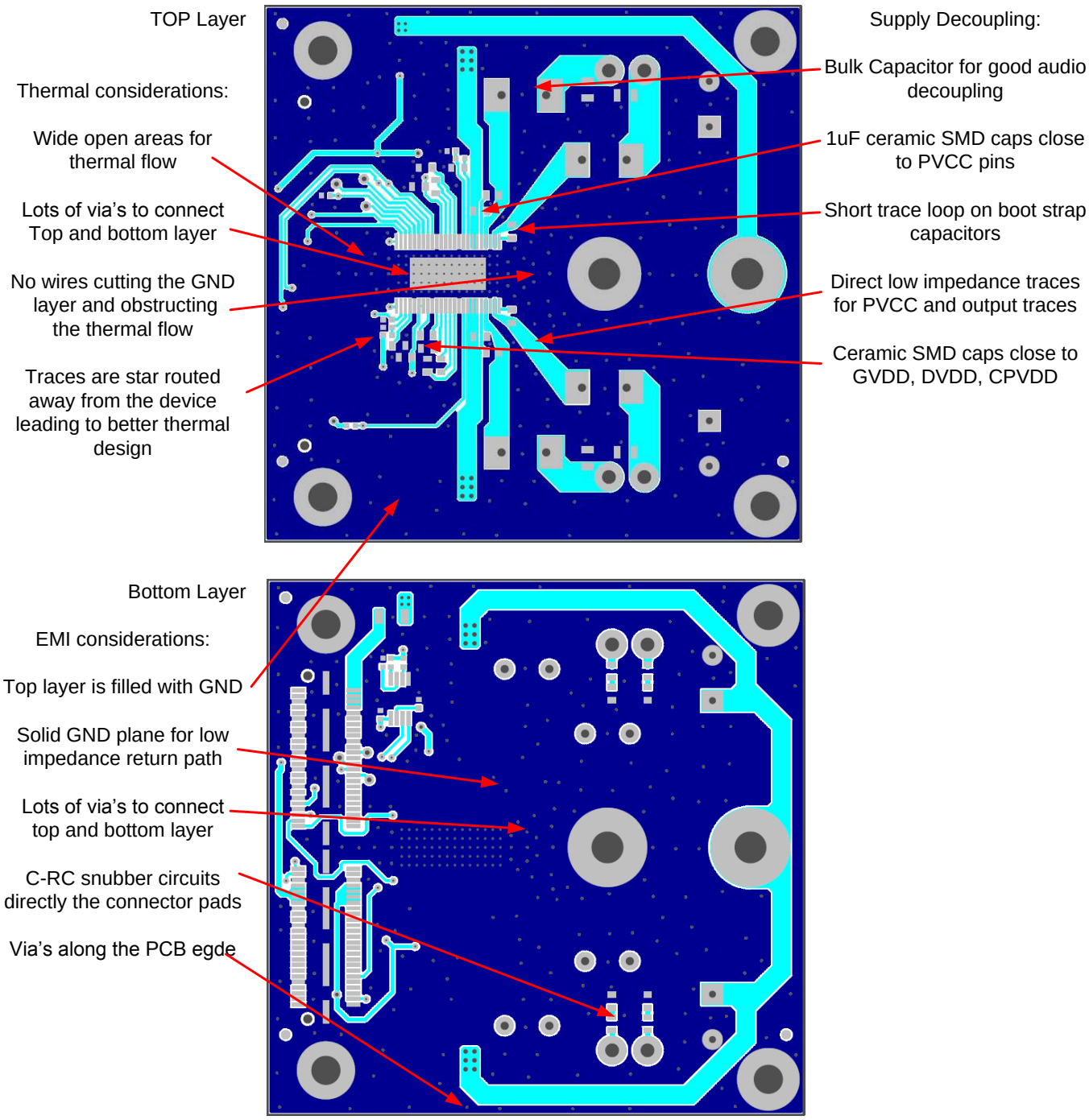

Figure 62. HTTSOP PCB Layout Example

Layout Examples (continued)

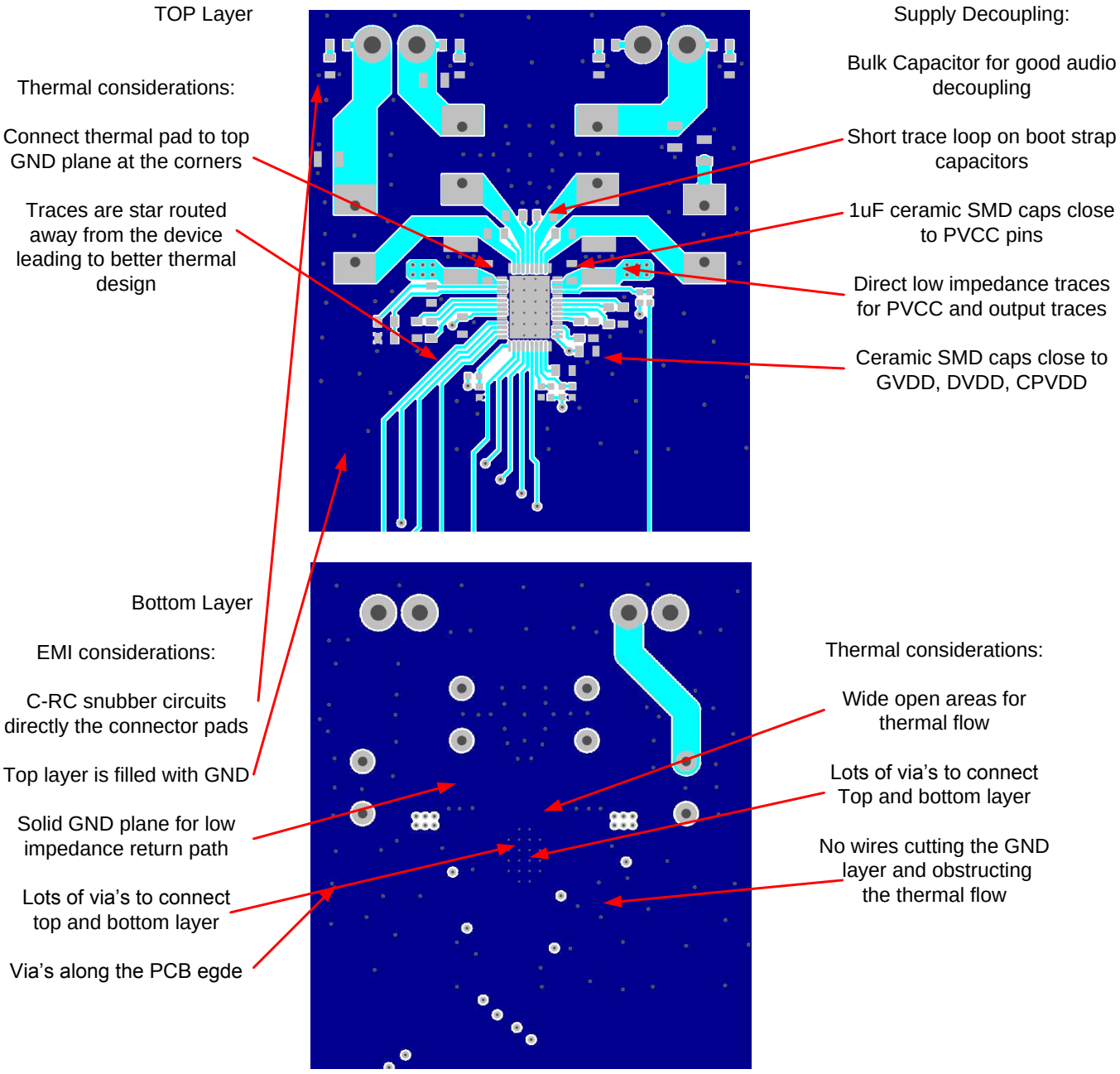

Figure 63. VQFN PCB Layout Example

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11 Register Map Information

11.1 Detailed Register Map Descriptions

Register Map Summary

Page 0									
Dec	**Hex**	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
1	0x01	RSV	RSV	RSV	RSTM	RSV	RSV	RSV	RSTR
2	0x02	RSV	RSV	RSV	RQST	RSV	RSV	RSV	RQPD
3	0x03	RSV	RSV	RSV	RQML	RSV	RSV	RSV	RQMR
4	0x04	RSV	RSV	RSV	PLCK	RSV	RSV	RSV	PLLE
7	0x07	RSV	RSV	RSV	DEMP	RSV	RSV	RSV	SDSL
8	0x08	RSV	RSV	G3OE	MUTEOE	G1OE	G2OE	RSV	RSV
9	0x09	RSV	RSV	BCKP	BCKO	RSV	RSV	RSV	LRKO
10	0x0A	DSPG7	DSPG6	DSPG5	DSPG4	DSPG3	DSPG2	DSPG1	DSPG0
12	0x0C	RSV	RSV	RSV	RSV	RSV	RSV	RBCK	RLRK
13	0x0D	RSV	RSV	RSV	SREF	RSV	RSV	RSV	RSV
20	0x14	RSV	RSV	RSV	RSV	PPDV3	PPDV2	PPDV1	PPDV0
21	0x15	RSV	RSV	PJDV5	PJDV4	PJDV3	PJDV2	PJDV1	PJDV0
22	0x16	RSV	RSV	PDDV5	PDDV4	PDDV3	PDDV2	PDDV1	PDDV0
23	0x17	PDDV7	PDDV6	PDDV5	PDDV4	PDDV3	PDDV2	PDDV1	PDDV0
24	0x18	RSV	RSV	RSV	RSV	PRDV3	PRDV2	PRDV1	PRDV0
27	0x1B	RSV	DDSP6	DDSP5	DDSP4	DDSP3	DDSP2	DDSP1	DDSP0
28	0x1C	RSV	DDAC6	DDAC5	DDAC4	DDAC3	DDAC2	DDAC1	DDAC0
29	0x1D	RSV	DNCP6	DNCP5	DNCP4	DNCP3	DNCP2	DNCP1	DNCP0
30	0x1E	RSV	DOSR6	DOSR5	DOSR4	DOSR3	DOSR2	DOSR1	DOSR0
32	0x20	RSV	DBCK6	DBCK5	DBCK4	DBCK3	DBCK2	DBCK1	DBCK0
33	0x21	DLRK7	DLRK6	DLRK5	DLRK4	DLRK3	DLRK2	DLRK1	DLRK0
34	0x22	RSV	RSV	RSV	I16E	RSV	RSV	FSSP1	FSSP0
35	0x23	IDAC_MSB7	IDAC_MSB6	IDAC_MSB5	IDAC_MSB4	IDAC_MSB3	IDAC_MSB2	IDAC_MSB1	IDAC_MSB0
36	0x24	IDAC_LSB7	IDAC_LSB6	IDAC_LSB5	IDAC_LSB4	IDAC_LSB3	IDAC_LSB2	IDAC_LSB1	IDAC_LSB0
37	0x25	RSV	IDFS	IDBK	IDSK	IDCH	IDCM	DCAS	IPLK
40	0x28	RSV	RSV	AFMT1	AFMT0	RSV	RSV	ALEN1	ALEN0
41	0x29	AOFS7	AOFS6	AOFS5	AOFS4	AOFS3	AOFS2	AOFS1	AOFS0
42	0x2A	RSV	RSV	AUPL1	AUPL0	RSV	RSV	AUPR1	AUPR0
43	0x2B	RSV	RSV	RSV	PSEL4	PSEL3	PSEL2	PSEL1	PSEL0
44	0x2C	RSV	RSV	RSV	RSV	RSV	CMDP2	CMDP1	CMDP0
59	0x3B	RSV	AMTL2	AMTL1	AMTL0	RSV	AMTR2	AMTR1	AMTR0
65	0x41	RSV	RSV	RSV	RSV	RSV	ACTL	AMLE	AMRE
66	0x42	ADLY7	ADLY6	ADLY5	ADLY4	ADLY3	ADLY2	ADLY1	ADLY0
82	0x52	RSV	RSV	RSV	RSV	G2SL3	G2SL2	G2SL1	G2SL0
83	0x53	RSV	RSV	RSV	RSV	G1SL3	G1SL2	G1SL1	G1SL0
84	0x54	RSV	RSV	RSV	RSV	MTSL3	MTSL2	MTSL1	MTSL0
85	0x55	RSV	RSV	RSV	RSV	G3SL3	G3SL2	G3SL1	G3SL0
86	0x56	RSV	RSV	GOUT5	GOUT4	GOUT3	GOUT2	RSV	RSV
87	0x57	RSV	RSV	GINV5	GINV4	GINV3	GINV2	RSV	RSV
90	0x5A	RSV	RSV	RSV	L1OV	R1OV	L2OV	R2OV	SFOV
91	0x5B	RSV	DTFS2	DTFS1	DTFS0	DTSR3	DTSR2	DTSR1	DTSR0
92	0x5C	RSV	RSV	RSV	RSV	RSV	RSV	RSV	DTBR_MSB
93	0x5D	DTBR_LSB7	DTBR_LSB6	DTBR_LSB5	DTBR_LSB4	DTBR_LSB3	DTBR_LSB2	DTBR_LSB1	DTBR_LSB0
94	0x5E	RSV	CDST6	CDST5	CDST4	CDST3	CDST2	CDST1	CDST0
95	0x5F	RSV	RSV	RSV	LTSH	RSV	CKMF	CSRF	CERF
108	0x6C	RSV	RSV	ADLM	ADRM	RSV	RSV	AMLM	AMRM
118	0x76	BOTM	RSV	RSV	RSV	PSTM3	PSTM2	PSTM1	PSTM0
119	0x77	RSV	RSV	GPIN5	RSV	3	2	RSV	RSV
120	0x78	RSV	RSV	RSV	AMFL	RSV	RSV	RSV	AMFR
121	0x79	RSV	RSV	RSV	RSV	RSV	RSV	RSV	DAMD

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Detailed Register Map Descriptions (continued)

Register Map Summary (continued)

Page 1									
Dec	**Hex**	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
2	0x02	RSV	RSV	RSV	LAGN	RSV	RSV	RSV	RAGN
5	0x05	RSV	RSV	RSV	RSV	RSV	RSV	UEPD	UIPD
6	0x06	RSV	RSV	RSV	RSV	RSV	RSV	RSV	AMCT
7	0x07	RSV	RSV	RSV	AGBL	RSV	RSV	RSV	AGBR
8	0x08	RSV	RSV	RSV	RBGF	RSV	RSV	RSV	RSV
Page 44									
Dec	**Hex**	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
1	0x01	RSV	RSV	RSV	RSV	ACRM	AMDC	ACRS	ACSW

11.1.1 Page 0 Registers

Page 0 / Register 1 (Hex 0x01)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
1	0x01	RSV	RSV	RSV	RSTM	RSV	RSV	RSV	RSTR
Reset Value					0				0

RSV	**Reserved** Reserved. Do not access.
RSTM	**Reset Modules** This bit resets the interpolation filter and the DAC modules. Since the DSP is also reset, the coeffient RAM content will also be cleared by the DSP. This bit is auto cleared and can be set only in standby mode. Default value: 0 0: Normal 1: Reset modules
RSTR	**Reset Registers** This bit resets the mode registers back to their initial values. The RAM content is not cleared, but the execution source will be back to ROM. This bit is auto cleared and must be set only when the DAC is in standby mode (resetting registers when the DAC is running is prohibited and not supported). Default value: 0 0: Normal 1: Reset mode registers

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Page 0 / Register 2 (Hex 0x02)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
2	0x02	RSV	RSV	RSV	RQST	RSV	RSV	RSV	RQPD
Reset Value					0				0

RSV	**Reserved** Reserved. Do not access.
RQST	**Standby Request** When this bit is set, the DAC will be forced into a system standby mode, which is also the mode the system enters in the case of clock errors. In this mode, most subsystems will be powered down but the charge pump and digital power supply. Default value: 0 0: Normal operation 1: Standby mode
RQPD	**Powerdown Request** When this bit is set, the DAC will be forced into powerdown mode, in which the power consumption would be minimum as the charge pump is also powered down. However, it will take longer to restart from this mode. This mode has higher precedence than the standby mode, i.e. setting this bit along with bit 4 for standby mode will result in the DAC going into powerdown mode. Default value: 0 0: Normal operation 1: Powerdown mode

Page 0 / Register 3 (Hex 0x03)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
3	0x03	RSV	RSV	RSV	RQML	RSV	RSV	RSV	RQMR
Reset Value					0				0

RSV	**Reserved** Reserved. Do not access.
RQML	**Mute Left Channel** This bit issues soft mute request for the left channel. The volume will be smoothly ramped down/up to avoid pop/click noise. Default value: 0 0: Normal volume 1: Mute
RQMR	**Mute Right Channel** This bit issues soft mute request for the right channel. The volume will be smoothly ramped down/up to avoid pop/click noise. Default value: 0 0: Normal volume 1: Mute

Page 0 / Register 4 (Hex 0x04)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
4	0x04	RSV	RSV	RSV	PLCK	RSV	RSV	RSV	PLLE
Reset Value									1

RSV	**Reserved** Reserved. Do not access.
PLCK	**PLL Lock Flag (Read Only)** This bit indicates whether the PLL is locked or not. When the PLL is disabled this bit always shows that the PLL is not locked.

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	0: The PLL is locked 1: The PLL is not locked
PLLE	**PLL Enable** This bit enables or disables the internal PLL. When PLL is disabled, the master clock will be switched to the SCK. Default value: 1 0: Disable PLL 1: Enable PLL

Page 0 / Register 7 (Hex 0x07)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
7	0x07	RSV	RSV	RSV	DEMP	RSV	RSV	RSV	SDSL
Reset Value					0				0

RSV	**Reserved** Reserved. Do not access.
DEMP	**De-Emphasis Enable** This bit enables or disables the de-emphasis filter. The default coefficients are for 44.1kHz sampling rate, but can be changed by reprogramming the appropriate coeffients in RAM. Default value: 0 0: De-emphasis filter is disabled 1: De-emphasis filter is enabled
SDSL	**SDOUT Select** This bit selects what is being output as SDOUT via GPIO pins. Default value: 0 0: SDOUT is the DSP output (post-processing) 1: SDOUT is the DSP input (pre-processing)

Page 0 / Register 8 (Hex 0x08)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
8	0x08	RSV	RSV	G3OE	MUTEOE	G1OE	G2OE	RSV	RSV
Reset Value				0	0	0	0		

RSV	**Reserved** Reserved. Do not access.
G3OE	**GPIO3 Output Enable** This bit sets the direction of the GPIO3 pin Default value: 0 0: GPIO3 is input 1: GPIO3 is output
MUTEOE	**MUTE Control Enable** This bit enables MUTE of speaker amplifier Default value: 0 0: MUTE control disable 1: MUTE control enable
G1OE	**GPIO1 Output Enable** This bit sets the direction of the GPIO1 pin Default value: 0 0: GPIO1 is input 1: GPIO1 is output
G2OE	**GPIO2 Output Enable**

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	This bit sets the direction of the GPIO2 pin Default value: 0 0: GPIO2 is input 1: GPIO2 is output

Page 0 / Register 9 (Hex 0x09)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
9	0x09	RSV	RSV	BCKP	BCKO	RSV	RSV	RSV	LRKO
Reset Value				0	0				0

RSV	**Reserved** Reserved. Do not access.
BCKP	**BCK Polarity** This bit sets the inverted BCK mode. In inverted BCK mode, the DAC assumes that the LRCK and DIN edges are aligned to the rising edge of the BCK. Normally they are assumed to be aligned to the falling edge of the BCK. Default value: 0 0: Normal BCK mode 1: Inverted BCK mode
BCKO	**BCK Output Enable** This bit sets the BCK pin direction to output for I2S master mode operation. In I2S master mode the device outputs the reference BCK and LRCK, and the external source device provides the DIN according to these clocks. Use Page 0 / Register 32 to program the division factor of the SCK to yield the desired BCK rate (normally 64FS) Default value: 0 0: BCK is input (I2S slave mode) 1: BCK is output (I2S master mode)
LRKO	**LRCLK Output Enable** This bit sets the LRCK pin direction to output for I2S master mode operation. In I2S master mode the device outputs the reference BCK and LRCK, and the external source device provides the DIN according to these clocks. Use Page 0 / Register 33 to program the division factor of the BCK to yield 1FS for LRCK. Default value: 0 0: LRCK is input (I2S slave mode) 1: LRCK is output (I2S master mode)

Page 0 / Register 10 (Hex 0x0A)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
10	0x0A	DSPG7	DSPG6	DSPG5	DSPG4	DSPG3	DSPG2	DSPG1	DSPG0
Reset Value		0	0	0	0	0	0	0	0

DSPG[7:0]	**DSP GPIO Input** The DSP accepts a 24-bit external control signals input. The value set in this register will go to bit 16:8 of this external input. Default value: 00000000

Page 0 / Register 12 (Hex 0x0C)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
12	0x0C	RSV	RSV	RSV	RSV	RSV	RSV	RBCK	RLRK
Reset Value								0	0

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RSV	**Reserved** Reserved. Do not access.
RBCK	**Master Mode BCK Divider Reset** This bit, when set to 0, will reset the SCK divider to generate BCK clock for I2S master mode. To use I2S master mode, the divider must be enabled and programmed properly. Default value: 0 0: Master mode BCK clock divider is reset 1: Master mode BCK clock divider is functional
RLRK	**Master Mode LRCK Divider Reset** This bit, when set to 0, will reset the BCK divider to generate LRCK clock for I2S master mode. To use I2S master mode, the divider must be enabled and programmed properly. Default value: 0 0: Master mode LRCK clock divider is reset 1: Master mode LRCK clock divider is functional

Page 0 / Register 13 (Hex 0x0D)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
13	0x0D	RSV	RSV	RSV	SREF	RSV	RSV	RSV	RSV
Reset Value					0				

RSV	**Reserved** Reserved. Do not access.
SREF	**PLL Reference** This bit select the source clock for internal PLL. This bit is ignored and overriden in clock auto set mode. Default value: 0 0: The PLL reference clock is SCK 1: The PLL reference clock is BCK

Page 0 / Register 20 (Hex 0x14)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
20	0x14	RSV	RSV	RSV	RSV	PPDV3	PPDV2	PPDV1	PPDV0
Reset Value						0	0	0	0

RSV	**Reserved** Reserved. Do not access.
PPDV[3:0]	**PLL P** These bits set the PLL divider P factor. These bits are ignored in clock auto set mode. Default value: 0000 0000: P=1 0001: P=2 ... 1110: P=15 1111: Prohibited (do not set this value)

Page 0 / Register 21 (Hex 0x15)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
21	0x15	RSV	RSV	PJDV5	PJDV4	PJDV3	PJDV2	PJDV1	PJDV0
Reset Value				0	0	0	0	0	0

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RSV	**Reserved** Reserved. Do not access.
PJDV[5:0]	**PLL J** These bits set the J part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode. Default value: 000000 000000: Prohibited (do not set this value) 000001: J=1 000010: J=2 ... 111111: J=63

Page 0 / Register 22 (Hex 0x16)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
22	0x16	RSV	RSV	PDDV5	PDDV4	PDDV3	PDDV2	PDDV1	PDDV0
Reset Value				0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
PDDV[5:0]	**PLL D (MSB)** Most-significant 6 bits to set the D part of the overall PLL multiplication factor J.D * R These bits are ignored in clock auto set mode. Default value: 000000 0 (in decimal): D=0000 1 (in decimal): D=0001 ... 9999 (in decimal): D=9999 others: Prohibited (do not set)

Page 0 / Register 23 (Hex 0x17)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
23	0x17	PDDV7	PDDV6	PDDV5	PDDV4	PDDV3	PDDV2	PDDV1	PDDV0
Reset Value		0	0	0	0	0	0	0	0

PDDV[7:0]	**PLL D (LSB)** Least-significant 8 bits to set the D part of the overall PLL multiplication factor J.D * R. Default value: 00000000 0 (in decimal): D=0000 1 (in decimal): D=0001 ... 9999 (in decimal): D=9999 others: Prohibited (do not set)

Page 0 / Register 24 (Hex 0x18)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
24	0x18	RSV	RSV	RSV	RSV	PRDV3	PRDV2	PRDV1	PRDV0
Reset Value						0	0	0	0

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RSV	**Reserved** Reserved. Do not access.
PRDV[3:0]	**PLL R** These bits set the R part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode. Default value: 0000 0000: R=1 0001: R=2 ... 1111: R=16

Page 0 / Register 27 (Hex 0x1B)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
27	0x1B	RSV	DDSP6	DDSP5	DDSP4	DDSP3	DDSP2	DDSP1	DDSP0
Reset Value			0	0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
DDSP[6:0]	**DSP Clock Divider** These bits set the source clock divider value for the DSP clock. These bits are ignored in clock auto set mode. Default value: 0000000 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

Page 0 / Register 28 (Hex 0x1C)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
28	0x1C	RSV	DDAC6	DDAC5	DDAC4	DDAC3	DDAC2	DDAC1	DDAC0
Reset Value			0	0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
DDAC[6:0]	**DAC Clock Divider** These bits set the source clock divider value for the DAC clock. These bits are ignored in clock auto set mode. Default value: 0000000 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

Page 0 / Register 29 (Hex 0x1D)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
29	0x1D	RSV	DNCP6	DNCP5	DNCP4	DNCP3	DNCP2	DNCP1	DNCP0
Reset Value			0	0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
DNCP[6:0]	**NCP Clock Divider** These bits set the source clock divider value for the CP clock. These bits are ignored in clock auto set mode. Default value: 0000000

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	0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

Page 0 / Register 30 (Hex 0x1E)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
30	0x1E	RSV	DOSR6	DOSR5	DOSR4	DOSR3	DOSR2	DOSR1	DOSR0
Reset Value			0	0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
DOSR[6:0]	**OSR Clock Divider** These bits set the source clock divider value for the OSR clock. These bits are ignored in clock auto set mode. Default value: 0000000 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

Page 0 / Register 32 (Hex 0x20)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
32	0x20	RSV	DBCK6	DBCK5	DBCK4	DBCK3	DBCK2	DBCK1	DBCK0
Reset Value			0	0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
DBCK[6:0]	**Master Mode BCK Divider** These bits set the SCK divider value to generate I2S master BCK clock. Default value: 0000000 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

Page 0 / Register 33 (Hex 0x21)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
33	0x21	DLRK7	DLRK6	DLRK5	DLRK4	DLRK3	DLRK2	DLRK1	DLRK0
Reset Value		0	0	0	0	0	0	0	0

DLRK[7:0]	**Master Mode LRCK Divider** These bits set the I2S master BCK clock divider value to generate I2S master LRCK clock. Default value: 00000000 00000000: Divide by 1 00000001: Divide by 2 ... 11111111: Divide by 256

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Page 0 / Register 34 (Hex 0x22)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
34	0x22	RSV	RSV	RSV	I16E	RSV	RSV	FSSP1	FSSP0
Reset Value					0			0	0

RSV	**Reserved** Reserved. Do not access.
I16E	**16x Interpolation** This bit enables or disables the 16x interpolation mode Default value: 0 0: 8x interpolation 1: 16x interpolation
FSSP[1:0]	**FS Speed Mode** These bits select the FS operation mode, which must be set according to the current audio sampling rate. These bits are ignored in clock auto set mode. Default value: 00 00: Single speed (FS ≤ 48 kHz) 01: Double speed (48 kHz < FS ≤ 96 kHz) 10: Quad speed (96 kHz < FS ≤ 192 kHz) 11: Octal speed (192 kHz < FS ≤ 384 kHz)

Page 0 / Register 35 (Hex 0x23)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
35	0x23	IDAC_MSB7	IDAC_MSB6	IDAC_MSB5	IDAC_MSB4	IDAC_MSB3	IDAC_MSB2	IDAC_MSB1	IDAC_MSB0
Reset Value		0	0	0	0	0	0	0	1

IDAC_MSB[7:0]	**IDAC (MSB)** Most-significant 8 bits to specify the number of DSP clock cycles available in one audio frame. The value should match the DSP clock FS ratio. These bits are ignored in clock auto set mode. Default value: 00000001

Page 0 / Register 36 (Hex 0x24)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
36	0x24	IDAC_LSB7	IDAC_LSB6	IDAC_LSB5	IDAC_LSB4	IDAC_LSB3	IDAC_LSB2	IDAC_LSB1	IDAC_LSB0
Reset Value		0	0	0	0	0	0	0	0

IDAC_LSB[7:0]	**IDAC (LSB)** Least-significant 8 bits to specify the number of DSP clock cycles available in one audio frame. Default value: 00000000

Page 0 / Register 37 (Hex 0x25)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
37	0x25	RSV	IDFS	IDBK	IDSK	IDCH	IDCM	DCAS	IPLK
Reset Value			0	0	0	0	0	0	0

RSV	**Reserved** Reserved. Do not access.
IDFS	**Ignore FS Detection** This bit controls whether to ignore the FS detection. When ignored, FS error will not cause a clock error. Default value: 0 0: Regard FS detection

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	1: Ignore FS detection
IDBK	**Ignore BCK Detection** This bit controls whether to ignore the BCK detection against LRCK. The BCK must be stable between 32FS and 256FS inclusive or an error will be reported. When ignored, a BCK error will not cause a clock error. Default value: 0 0: Regard BCK detection 1: Ignore BCK detection
IDSK	**Ignore SCK Detection** This bit controls whether to ignore the SCK detection against LRCK. Only some certain SCK ratios within some error margin are allowed. When ignored, an SCK error will not cause a clock error. Default value: 0 0: Regard SCK detection 1: Ignore SCK detection
IDCH	**Ignore Clock Halt Detection** This bit controls whether to ignore the SCK halt (static or frequency is lower than acceptable) detection. When ignored an SCK halt will not cause a clock error. Default value: 0 0: Regard SCK halt detection 1: Ignore SCK halt detection
IDCM	**Ignore LRCK/BCK Missing Detection** This bit controls whether to ignore the LRCK/BCK missing detection. The LRCK/BCK need to be in low state (not only static) to be deemed missing. When ignored an LRCK/BCK missing will not cause the DAC go into powerdown mode. Default value: 0 0: Regard LRCK/BCK missing detection 1: Ignore LRCK/BCK missing detection
DCAS	**Disable Clock Divider Autoset** This bit enables or disables the clock auto set mode. When dealing with uncommon audio clock configuration, the auto set mode must be disabled and all clock dividers must be set manually. Addtionally, some clock detectors might also need to be disabled. Default value: 0 0: Enable clock auto set 1: Disable clock auto set
IPLK	**Ignore PLL Lock Detection** This bit controls whether to ignore the PLL lock detection. When ignored, PLL unlocks will not cause a clock error. The PLL lock flag at Page 0 / Register 4, bit 4 is always correct regardless of this bit. Default value: 0 0: PLL unlocks raise clock error 1: PLL unlocks are ignored

Page 0 / Register 40 (Hex 0x28)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
40	0x28	RSV	RSV	AFMT1	AFMT0	RSV	RSV	ALEN1	ALEN0
Reset Value				0	0			1	0

RSV	**Reserved** Reserved. Do not access.
AFMT[1:0]	**I2S Data Format** These bits control both input and output audio interface formats for DAC operation. Default value: 00 00: I2S 01: DSP

	10: RTJ 11: LTJ
ALEN[1:0]	**I2S Word Length** These bits control both input and output audio interface sample word lengths for DAC operation. Default value: 10 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits

Page 0 / Register 41 (Hex 0x29)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
41	0x29	AOFS7	AOFS6	AOFS5	AOFS4	AOFS3	AOFS2	AOFS1	AOFS0
Reset Value		0	0	0	0	0	0	0	0

AOFS[7:0]	**I2S Shift** These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCK from the starting (MSB) of audio frame to the starting of the desired audio sample. Default value: 00000000 00000000: offset = 0 BCK (no offset) 00000001: ofsset = 1 BCK 00000010: offset = 2 BCKs ... 11111111: offset = 256 BCKs

Page 0 / Register 42 (Hex 0x2A)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
42	0x2A	RSV	RSV	AUPL1	AUPL0	RSV	RSV	AUPR1	AUPR0
Reset Value				0	1			0	1

RSV	**Reserved** Reserved. Do not access.
AUPL[1:0]	**Left DAC Data Path** These bits control the left channel audio data path connection. Default value: 01 00: Zero data (mute) 01: Left channel data 10: Right channel data 11: Reserved (do not set)
AUPR[1:0]	**Right DAC Data Path** These bits control the right channel audio data path connection. Default value: 01 00: Zero data (mute) 01: Right channel data 10: Left channel data 11: Reserved (do not set)

Page 0 / Register 43 (Hex 0x2B)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
43	0x2B	RSV	RSV	RSV	PSEL4	PSEL3	PSEL2	PSEL1	PSEL0
Reset Value					0	0	0	0	1

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RSV	**Reserved** Reserved. Do not access.
PSEL[4:0]	**DSP Program Selection** These bits select the DSP program to use for audio processing. Default value: 00001 00000: Reserved (do not set) 00001: 8x/4x/2x FIR interpolation filter with de-emphasis 00010: Reserved (do not set) 00011: Reserved (do not set) 00100: Reserved (do not set) 00101: Reserved (do not set) 00110: Reserved (do not set) 00111: Reserved (do not set) 01000: Reserved (do not set) 11111: User program in RAM others: Reserved (do not set)

Page 0 / Register 44 (Hex 0x2C)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
44	0x2C	RSV	RSV	RSV	RSV	RSV	CMDP2	CMDP1	CMDP0
Reset Value							0	0	0

RSV	**Reserved** Reserved. Do not access.
CMDP[2:0]	**Clock Missing Detection Period** These bits set how long both BCK and LRCK keep low before the audio clocks deemed missing and the DAC transitions to powerdown mode. Default value: 000 000: about 1 second 001: about 2 seconds 010: about 3 seconds ... 111: about 8 seconds

Page 0 / Register 59 (Hex 0x3B)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
59	0x3B	RSV	AMTL2	AMTL1	AMTL0	RSV	AMTR2	AMTR1	AMTR0
Reset Value			0	0	0		0	0	0

RSV	**Reserved** Reserved. Do not access.
AMTL[2:0]	**Auto Mute Time for Left Channel** These bits specify the length of consecutive zero samples at left channel before the channel can be auto muted. The times shown are for 48 kHz sampling rate and will scale with other rates. Default value: 000 000: 21 ms 001: 106 ms 010: 213 ms 011: 533 ms 100: 1.07 sec 101: 2.13 sec

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	110: 5.33 sec 111: 10.66 sec
AMTR[2:0]	**Auto Mute Time for Right Channel** These bits specify the length of consecutive zero samples at right channel before the channel can be auto muted. The times shown are for 48 kHz sampling rate and will scale with other rates. Default value: 000 000: 21 ms 001: 106 ms 010: 213 ms 011: 533 ms 100: 1.07 sec 101: 2.13 sec 110: 5.33 sec 111: 10.66 sec

Page 0 / Register 65 (Hex 0x41)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
65	0x41	RSV	RSV	RSV	RSV	RSV	ACTL	AMLE	AMRE
Reset Value							1	0	0

RSV	**Reserved** Reserved. Do not access.
ACTL	**Auto Mute Control** This bit controls the behavior of the auto mute upon zero sample detection. The time length for zero detection is set with Page 0 / Register 59. Default value: 1 0: Auto mute left channel and right channel independently. 1: Auto mute left and right channels only when both channels are about to be auto muted.
AMLE	**Auto Mute Left Channel** This bit enables or disables auto mute on right channel. Note that when right channel auto mute is disabled and the Page 0 / Register 65, bit 2 is set to 1, the left channel will also never be auto muted. Default value: 0 0: Disable right channel auto mute 1: Enable right channel auto mute
AMRE	**Auto Mute Right Channel** This bit enables or disables auto mute on left channel. Note that when left channel auto mute is disabled and the Page 0 / Register 65, bit 2 is set to 1, the right channel will also never be auto muted. Default value: 0 0: Disable left channel auto mute 1: Enable left channel auto mute

Page 0 / Register 66 (Hex 0x42)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
66	0x42	ADLY7	ADLY6	ADLY5	ADLY4	ADLY3	ADLY2	ADLY1	ADLY0
Reset Value		0	0	0	1	0	1	0	0

ADLY[7:0]	**AMUTE Delay** These bits control the delay before the complete digital mute to the assertion of analog mute. This is to allow the non-mute audio samples to completely flow out through analog parts before the assertion of the analog mute. Default value: 00010100 00000000: No delay

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	00000001: 1 LRCK delay 00000010: 2 LRCK delay ... 11111111: 255 LRCK delay

Page 0 / Register 82 (Hex 0x52)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
82	0x52	RSV	RSV	RSV	RSV	G2SL3	G2SL2	G2SL1	G2SL0
Reset Value						0	0	0	0

RSV	**Reserved** Reserved. Do not access.
G2SL[3:0]	**GPIO2 Output Selection** These bits select the signal to output to GPIO2. To actually output the selected signal, the GPIO2 must be set to output mode at Page 0 / Register 8. Default value: 0000 0000: off (low) 0001: DSP GPIO2 output 0010: Register GPIO2 output (Page 0 / Register 86, bit 2) 0011: Auto mute flag (asserted when both L and R channels are auto muted) 0100: Auto mute flag for left channel 0101: Auto mute flag for right channel 0110: Clock invalid flag (clock error or clock changing or clock missing) 0111: Serial audio interface data output (SDOUT) 1000: Analog mute flag for left channel (low active) 1001: Analog mute flag for right channel (low active) 1010: PLL lock flag 1011: Charge pump clock 1100: DAC clock 1101: MiniDSP clock/4 1110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD 1111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD

Page 0 / Register 83 (Hex 0x53)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
83	0x53	RSV	RSV	RSV	RSV	G1SL3	G1SL2	G1SL1	G1SL0
Reset Value						0	0	0	0

RSV	**Reserved** Reserved. Do not access.
G1SL[3:0]	**GPIO1 Output Selection** These bits select the signal to output to GPIO1. To actually output the selected signal, the GPIO1 must be set to output mode at Page 0 / Register 8. Default value: 0000 0000: off (low) 0001: DSP GPIO1 output 0010: Register GPIO1 output (Page 0 / Register 86, bit 3) 0011: Auto mute flag (asserted when both L and R channels are auto muted) 0100: Auto mute flag for left channel 0101: Auto mute flag for right channel 0110: Clock invalid flag (clock error or clock changing or clock missing)

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	0111: Serial audio interface data output (SDOUT) 1000: Analog mute flag for left channel (low active) 1001: Analog mute flag for right channel (low active) 1010: PLL lock flag 1011: Charge pump clock 1100: DAC clock 1101: MiniDSP clock/4 1110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD 1111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD

Page 0 / Register 84 (Hex 0x54)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
84	0x54	RSV	RSV	RSV	RSV	MTSL3	MTSL2	MTSL1	MTSL0
Reset Value						0	0	0	0

RSV	**Reserved** Reserved. Do not access.
MTSL[3:0]	**MUTE Output Selection** These bits select the signal to output to MUTE. To actually output the selected signal, the MUTE must be set to output mode at Page 0 / Register 8. Default value: 0000 0000: off (low) 0001: DSP MUTE output 0010: Register MUTE output (Page 0 / Register 86, bit 4) 0011: Auto mute flag (asserted when both L and R channels are auto muted) 0100: Auto mute flag for left channel 0101: Auto mute flag for right channel 0110: Clock invalid flag (clock error or clock changing or clock missing) 1110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD 1111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD

Page 0 / Register 85 (Hex 0x55)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
85	0x55	RSV	RSV	RSV	RSV	G3SL3	G3SL2	G3SL1	G3SL0
Reset Value						0	0	0	0

RSV	**Reserved** Reserved. Do not access.
G3SL[3:0]	**GPIO3 Output Selection** These bits select the signal to output to GPIO3. To actually output the selected signal, the GPIO3 must be set to output mode at Page 0 / Register 8. Default value: 0000 0000: off (low) 0001: DSP GPIO3 output 0010: Register GPIO3 output (Page 0 / Register 86, bit 5) 0011: Auto mute flag (asserted when both L and R channels are auto muted) 0100: Auto mute flag for left channel 0101: Auto mute flag for right channel 0110: Clock invalid flag (clock error or clock changing or clock missing) 0111: Serial audio interface data output (SDOUT)

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	1000: Analog mute flag for left channel (low active) 1001: Analog mute flag for right channel (low active) 1010: PLL lock flag 1011: Charge pump clock 1100: DAC clock 1101: MiniDSP clock/4 1110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD 1111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD

Page 0 / Register 86 (Hex 0x56)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
86	0x56	RSV	RSV	GOUT5	GOUT4	GOUT3	GOUT2	RSV	RSV
Reset Value				0	0	0	0		

RSV	**Reserved** Reserved. Do not access.
GOUT[5:0]	**GPIO Output Control** This bit controls the GPIO3 output when the selection at Page 0 / Register 85 is set to 0010 (register output) Default value: 000000 0: Output low 1: Output high

Page 0 / Register 87 (Hex 0x57)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
87	0x57	RSV	RSV	GINV5	GINV4	GINV3	GINV2	RSV	RSV
Reset Value				0	0	0	0		

RSV	**Reserved** Reserved. Do not access.
GINV[5:0]	**GPIO Output Inversion** This bit controls the polarity of GPIO3 output. When set to 1, the output will be inverted for any signal being selected. Default value: 000000 0: Non-inverted 1: Inverted

Page 0 / Register 90 (Hex 0x5A)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
90	0x5A	RSV	RSV	RSV	L1OV	R1OV	L2OV	R2OV	SFOV
Reset Value									

RSV	**Reserved** Reserved. Do not access.
L1OV	**Left1 Overflow (Read Only)** This bit indicates whether the left channel of DSP first output port has overflow. This bit is sticky and is cleared when read. 0: No overflow 1: Overflow occurred
R1OV	**Right1 Overflow (Read Only)** The bit indicates whether the right channel of DSP first output port has overflow. This bit is sticky and is cleared when read.

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	0: No overflow 1: Overflow occurred
L2OV	**Left2 Overflow (Read Only)** This bit indicates whether the left channel of DSP second output port has overflow. This bit is sticky and is cleared when read. 0: No overflow 1: Overflow occurred
R2OV	**Right2 Overflow (Read Only)** The bit indicates whether the right channel of DSP second output port has overflow. This bit is sticky and is cleared when read. 0: No overflow 1: Overflow occurred
SFOV	**Shifter Overflow (Read Only)** This bit indicates whether overflow occurred in the DSP shifter (possible sample corruption). This bit is sticky and is cleared when read. 0: No overflow 1: Overflow occurred

Page 0 / Register 91 (Hex 0x5B)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
91	0x5B	RSV	DTFS2	DTFS1	DTFS0	DTSR3	DTSR2	DTSR1	DTSR0
Reset Value									

RSV	**Reserved** Reserved. Do not access.
DTFS[2:0]	**Detected FS (Read Only)** These bits indicate the currently detected audio sampling rate. 000: Error (Out of valid range) 001: 8 kHz 010: 16 kHz 011: 32-48 kHz 100: 88.2-96 kHz 101: 176.4-192 kHz 110: 384 kHz
DTSR[3:0]	**Detected SCK Ratio (Read Only)** These bits indicate the currently detected SCK ratio. Note that even if the SCK ratio is not indicated as error, clock error might still be flagged due to incompatible combination with the sampling rate. Specifically the SCK ratio must be high enough to allow enough DSP cycles for minimal audio processing when PLL is disabled. The absolute SCK frequency must also be lower than 50 MHz. 0000: Ratio error (The SCK ratio is not allowed) 0001: SCK = 32 FS 0010: SCK = 48 FS 0011: SCK = 64 FS 0100: SCK = 128 FS 0101: SCK = 192 FS 0110: SCK = 256 FS 0111: SCK = 384 FS 1000: SCK = 512 FS 1001: SCK = 768 FS 1010: SCK = 1024 FS 1011: SCK = 1152 FS 1100: SCK = 1536 FS

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	1101: SCK = 2048 FS 1110: SCK = 3072 FS

Page 0 / Register 92 (Hex 0x5C)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
92	0x5C	RSV	RSV	RSV	RSV	RSV	RSV	RSV	DTBR_MSB
Reset Value									

RSV	**Reserved** Reserved. Do not access.
DTBR_MSB	**Detected BCK Ratio (MSB) (Read Only)** Most significant of 9 bits that indicate the currently detected BCK ratio, that is, the number of BCK clocks in one audio frame. Note that for extreme case of BCK = 1 FS (which is not usable anyway), the detected ratio will be unreliable.

Page 0 / Register 93 (Hex 0x5D)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
93	0x5D	DTBR_LSB7	DTBR_LSB6	DTBR_LSB5	DTBR_LSB4	DTBR_LSB3	DTBR_LSB2	DTBR_LSB1	DTBR_LSB0
Reset Value									

DTBR_LSB[7:0]	**Detected BCK Ratio (LSB) (Read Only)** Least significant of 8 bits that indicate the currently detected BCK ratio.

Page 0 / Register 94 (Hex 0x5E)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
94	0x5E	RSV	CDST6	CDST5	CDST4	CDST3	CDST2	CDST1	CDST0
Reset Value									

RSV	**Reserved** Reserved. Do not access.
CDST[6]	**Clock Detector Status (Read Only)** This bit indicates whether the SCK clock is present or not. 0: SCK is present 1: SCK is missing (halted)
CDST[5]	**Clock Detector Status (Read Only)** This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled. 0: PLL is locked 1: PLL is unlocked
CDST[4]	**Clock Detector Status (Read Only)** This bit indicates whether the both LRCK and BCK are missing (tied low) or not. 0: LRCK and/or BCK is present 0: LRCK and BCK are missing
CDST[3]	**Clock Detector Status (Read Only)** This bit indicates whether the combination of current sampling rate and SCK ratio is valid for clock auto set. 0: The combination of FS/SCK ratio is valid 1: Error (clock auto set is not possible)
CDST[2]	**Clock Detector Status (Read Only)** This bit indicates whether the SCK is valid or not. The SCK ratio must be detectable to be valid. There is a limitation with this flag; that is, when the low period of LRCK is less than or equal to 5 BCKs, this flag will be asserted (SCK invalid reported). 0: SCK is valid

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	1: SCK is invalid
CDST[1]	**Clock Detector Status (Read Only)** This bit indicates whether the BCK is valid or not. The BCK ratio must be stable and in the range of 32-256FS to be valid. 0: BCK is valid 1: BCK is invalid
CDST[0]	**Clock Detector Status (Read Only)** This bit indicates whether the audio sampling rate is valid or not. The sampling rate must be detectable to be valid. There is a limitation with this flag; that is, when this flag is asserted and $0/37$ is set to ignore all asserted error flags such that the DAC recovers, this flag will be de-asserted (sampling rate invalid not reported anymore). 0: Sampling rate is valid 1: Sampling rate is invalid

Page 0 / Register 95 (Hex 0x5F)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
95	0x5F	RSV	RSV	RSV	LTSH	RSV	CKMF	CSRF	CERF
Reset Value									

RSV	**Reserved** Reserved. Do not access.
LTSH	**Latched Clock Halt (Read Only)** This bit indicates whether SCK halt has occurred. The bit is cleared when read. 0: SCK halt has not occurred 1: SCK halt has occurred since last read
CKMF	**Clock Missing (Read Only)** This bit indicates whether the LRCK and BCK are missing (tied low). 0: LRCK and/or BCK is present 1: LRCK and BCK are missing
CSRF	**Clock Resync Request (Read Only)** This bit indicates whether the clock resynchronization is in progress. 0: Not resynchronizing 1: Clock resynchronization is in progress
CERF	**Clock Error (Read Only)** This bit indicates whether a clock error is being reported. 0: Clock is valid 1: Clock is invalid (Error)

Page 0 / Register 108 (Hex 0x6C)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
108	0x6C	RSV	RSV	ADLM	ADRM	RSV	RSV	AMLM	AMRM
Reset Value									

RSV	**Reserved** Reserved. Do not access.
ADLM	**AMUTEZ dummy left monitor (Read Only)** This bit is a monitor for left channel dummy output analog mute status. 0: Mute 1: Unmute
ADRM	**AMUTEZ dummy right monitor (Read Only)** This bit is a monitor for right channel dummy output analog mute status.

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	0: Mute 1: Unmute
AMLM	**Left Analog Mute Monitor (Read Only)** This bit is a monitor for left channel analog mute status. 0: Mute 1: Unmute
AMRM	**Right Analog Mute Monitor (Read Only)** This bit is a monitor for right channel analog mute status. 0: Mute 1: Unmute

Page 0 / Register 118 (Hex 0x76)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
118	0x76	BOTM	RSV	RSV	RSV	PSTM3	PSTM2	PSTM1	PSTM0
Reset Value									

RSV	**Reserved** Reserved. Do not access.
BOTM	**DSP Boot Done Flag (Read Only)** This bit indicates whether the DSP boot is completed. 0: DSP is booting 1: DSP boot completed
PSTM[3:0]	**Power State (Read Only)** These bits indicate the current power state of the DAC. 0000: Powerdown 0001: Wait for CP voltage valid 0010: Calibration 0011: Calibration 0100: Volume ramp up 0101: Run (Playing) 0110: Reserved 0111: Volume ramp down 1000: Standby

Page 0 / Register 119 (Hex 0x77)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
119	0x77	RSV	RSV	GPIN5	RSV	3	2	RSV	RSV
Reset Value									

RSV	**Reserved** Reserved. Do not access.
GPIN[5:0]	**GPIO Input States (Read Only)** This bit indicates the logic level at GPIO3 pin. 0: Low 1: High

Page 0 / Register 120 (Hex 0x78)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
120	0x78	RSV	RSV	RSV	AMFL	RSV	RSV	RSV	AMFR
Reset Value									

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RSV	**Reserved** Reserved. Do not access.
AMFL	**Auto Mute Flag for Left Channel (Read Only)** This bit indicates the auto mute status for left channel. 0: Not auto muted 1: Auto muted
AMFR	**Auto Mute Flag for Right Channel (Read Only)** This bit indicates the auto mute status for right channel. 0: Not auto muted 1: Auto muted

Page 0 / Register 121 (Hex 0x79)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
121	0x79	RSV	RSV	RSV	RSV	RSV	RSV	RSV	DAMD
Reset Value									0

RSV	**Reserved** Reserved. Do not access.
DAMD	**DAC Mode** This bit controls the DAC mode. Default value: 0 0: Mode1 1: Mode2

11.1.2 Page 1 Registers

Page 1 / Register 2 (Hex 0x02)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
2	0x02	RSV	RSV	RSV	LAGN	RSV	RSV	RSV	RAGN
Reset Value					0				0

RSV	**Reserved** Reserved. Do not access.
LAGN	**Analog Gain Control for Left Channel** This bit controls the left channel analog gain. Default value: 0 0: 0 dB 1:-6 dB
RAGN	**Analog Gain Control for Right Channel** This bit controls the right channel analog gain. Default value: 0 0: 0 dB 1: -6 dB

Page 1 / Register 5 (Hex 0x05)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
5	0x05	RSV	RSV	RSV	RSV	RSV	RSV	UEPD	UIPD
Reset Value								0	0

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RSV	**Reserved** Reserved. Do not access.
UEPD	**External UVP Control** This bit enables or disables detection of power supply drop via XSMUTE pin (External Under Voltage Protection). Default value: 0 0: Enabled 1: Disabled
UIPD	**Internal UVP Control** This bit enables or disables internal detection of AVDD voltage drop (Internal Under Voltage Protection). Default value: 0 0: Enabled 1: Disabled

Page 1 / Register 6 (Hex 0x06)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
6	0x06	RSV	RSV	RSV	RSV	RSV	RSV	RSV	AMCT
Reset Value									1

RSV	**Reserved** Reserved. Do not access.
AMCT	**Analog Mute Control** This bit enables or disables analog mute following digital mute. Default value: 1 0: Enabled 1: Disabled

Page 1 / Register 7 (Hex 0x07)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
7	0x07	RSV	RSV	RSV	AGBL	RSV	RSV	RSV	AGBR
Reset Value					0				0

RSV	**Reserved** Reserved. Do not access.
AGBL	**Analog +10% Gain for Left Channel** This bit enables or disables amplitude boost mode for left channel. Default value: 0 0: Normal amplitude 1: +10% (+0.8 dB) boosted amplitude
AGBR	**Analog +10% Gain for Right Channel** This bit enables or disables amplitude boost mode for right channel. Default value: 0 0: Normal amplitude 1: +10% (+0.8 dB) boosted amplitude

Page 1 / Register 8 (Hex 0x08)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
8	0x08	RSV	RSV	RSV	RBGF	RSV	RSV	RSV	RSV
Reset Value					0				

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RSV	**Reserved** Reserved. Do not access.
RBGF	**REF BG Fast** This bit controls the bandgap voltage ramp up speed. Default value: 0 0: Normal ramp up, ~50ms with external capacitance = 1uF 1: Fast ramp up, ~1ms with external capacitance = 1 uF

11.1.3 Page 44 Registers

Page 44 / Register 1 (Hex 0x01)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
1	0x01	RSV	RSV	RSV	RSV	ACRM	AMDC	ACRS	ACSW
Reset Value							0		0

RSV	**Reserved** Reserved. Do not access.
ACRM	**Active CRAM Monitor (Read Only)** This bit indicates which CRAM is being accessed by the DSP when adaptive mode is disabled. When adaptive mode is enabled, this bit has no meaning. 0: CRAM A is being used by the DSP 1: CRAM B is being used by the DSP
AMDC	**Adaptive Mode Control** This bit controls the DSP adaptive mode. When in adaptive mode, only CRAM A is accessible via serial interface when the DSP is disabled (DAC in standby state), while when the DSP is enabled (DAC is run state) the CRAM A can only be accessed by the DSP and the CRAM B can only be accessed by the serial interface, or vice versa depending on the value of CRAMSTAT. When not in adaptive mode, both CRAM A and B can be accessed by the serial interface when the DSP is disabled, but when the DSP is enabled, no CRAM can be accessed by serial interface. The DSP can access either CRAM, which can be monitored at SWPMON. Default value: 0 0: Adaptive mode disabled 1: Adaptive mode enabled
ACRS	**Active CRAM Selection (Read Only)** This bit indicates which CRAM currently serves as the active one. The other CRAM serves as an update buffer, and can accessed by serial interface (SPI/I2C) 0: CRAM A is active and being used by the DSP 1: CRAM B is active and being used by the DSP
ACSW	**Switch Active CRAM** This bit is used to request switching roles of the two buffers, i.e. switching the active buffer role between CRAM A and CRAM B. This bit is cleared automatically when the switching process completed. Default value: 0 0: No switching requested or switching completed 1: Switching is being requested

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12 器件和文档支持

12.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **25.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
TAS5766M	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TAS5768M	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.2 商标

PurePath, PowerPAD are trademarks of Texas Instruments.
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12.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5766MDCA	ACTIVE	HTSSOP	DCA	48	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5766M	Samples
TAS5766MDCAR	ACTIVE	HTSSOP	DCA	48	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5766M	Samples
TAS5766MRMTR	ACTIVE	VQFN	RMT	48	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	5766M	Samples
TAS5766MRMTT	ACTIVE	VQFN	RMT	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	5766M	Samples
TAS5768MDCA	ACTIVE	HTSSOP	DCA	48	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5768M	Samples
TAS5768MDCAR	ACTIVE	HTSSOP	DCA	48	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5768M	Samples
TAS5768MRMTR	ACTIVE	VQFN	RMT	48	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	5768M	Samples
TAS5768MRMTT	ACTIVE	VQFN	RMT	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	5768M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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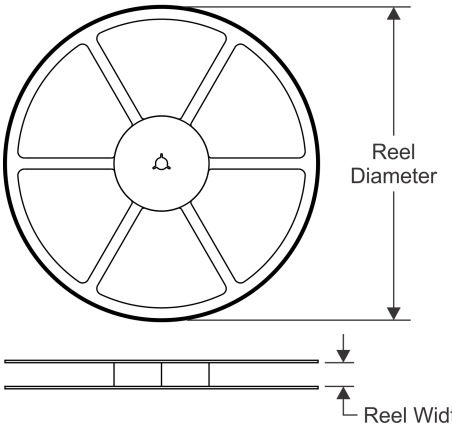
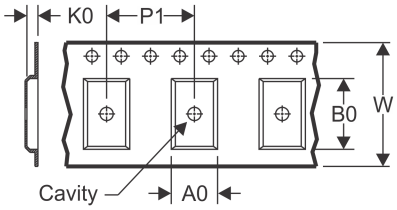
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

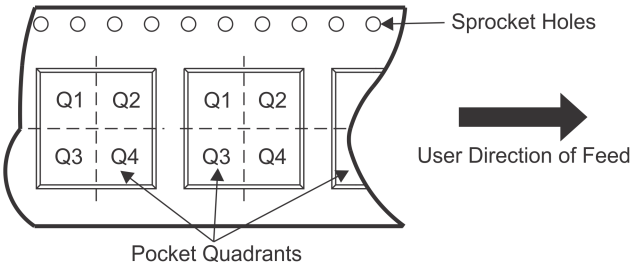


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

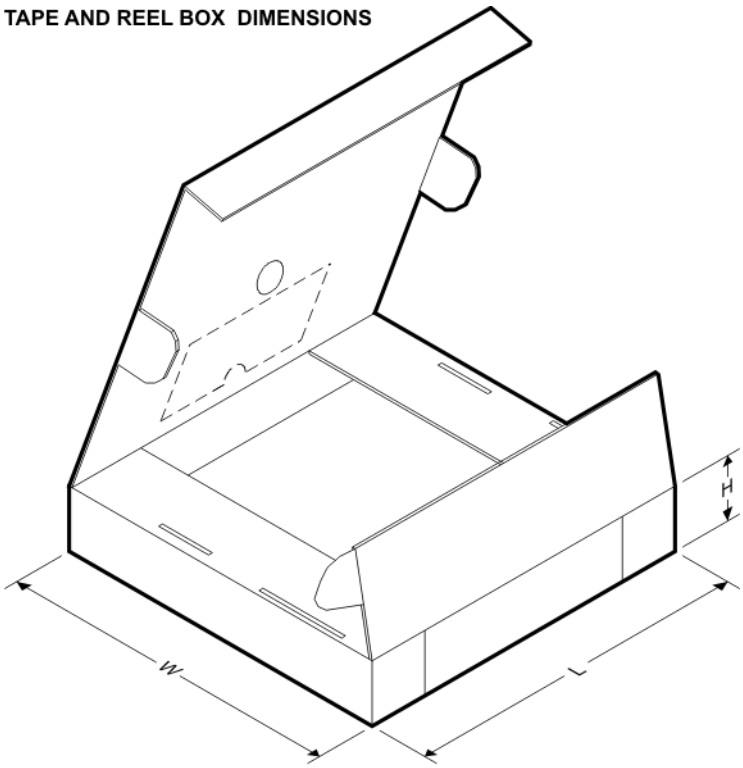
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5766MDCAR	HTSSOP	DCA	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
TAS5766MRMTR	VQFN	RMT	48	3000	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1
TAS5766MRMTT	VQFN	RMT	48	250	180.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1
TAS5768MDCAR	HTSSOP	DCA	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
TAS5768MRMTR	VQFN	RMT	48	3000	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1
TAS5768MRMTT	VQFN	RMT	48	250	180.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1

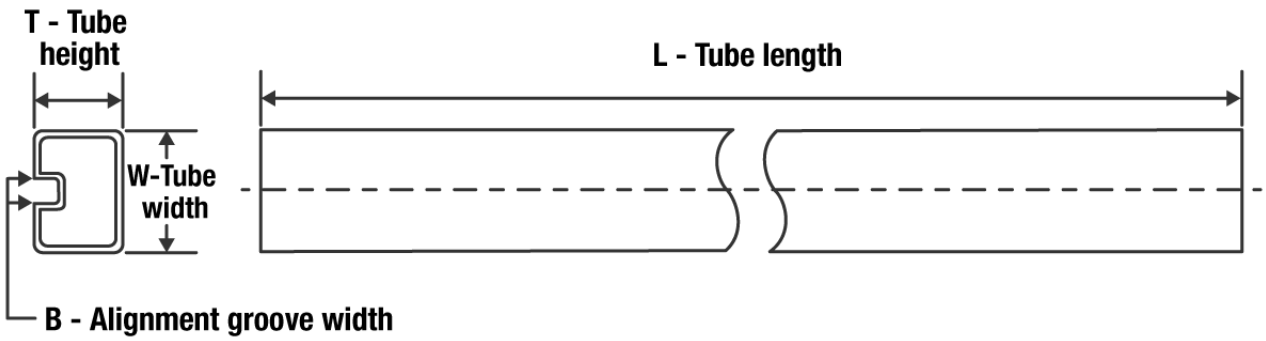
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5766MDCAR	HTSSOP	DCA	48	2000	350.0	350.0	43.0
TAS5766MRMTR	VQFN	RMT	48	3000	367.0	367.0	38.0
TAS5766MRMTT	VQFN	RMT	48	250	210.0	185.0	35.0
TAS5768MDCAR	HTSSOP	DCA	48	2000	350.0	350.0	43.0
TAS5768MRMTR	VQFN	RMT	48	3000	367.0	367.0	38.0
TAS5768MRMTT	VQFN	RMT	48	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

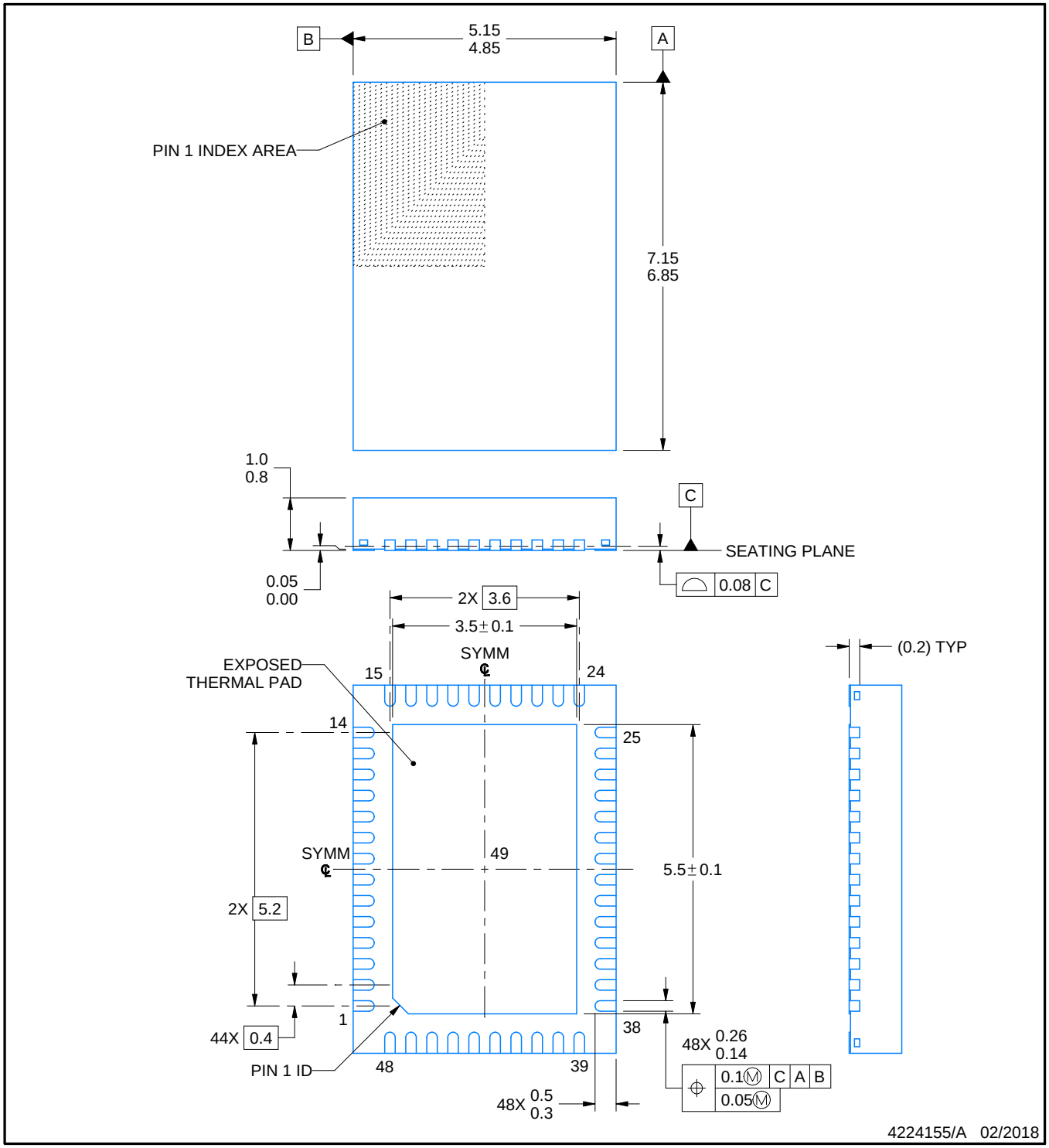
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TAS5766MDCA	DCA	HTSSOP	48	40	530	11.89	3600	4.9
TAS5768MDCA	DCA	HTSSOP	48	40	530	11.89	3600	4.9

PACKAGE OUTLINE

RMT0048A

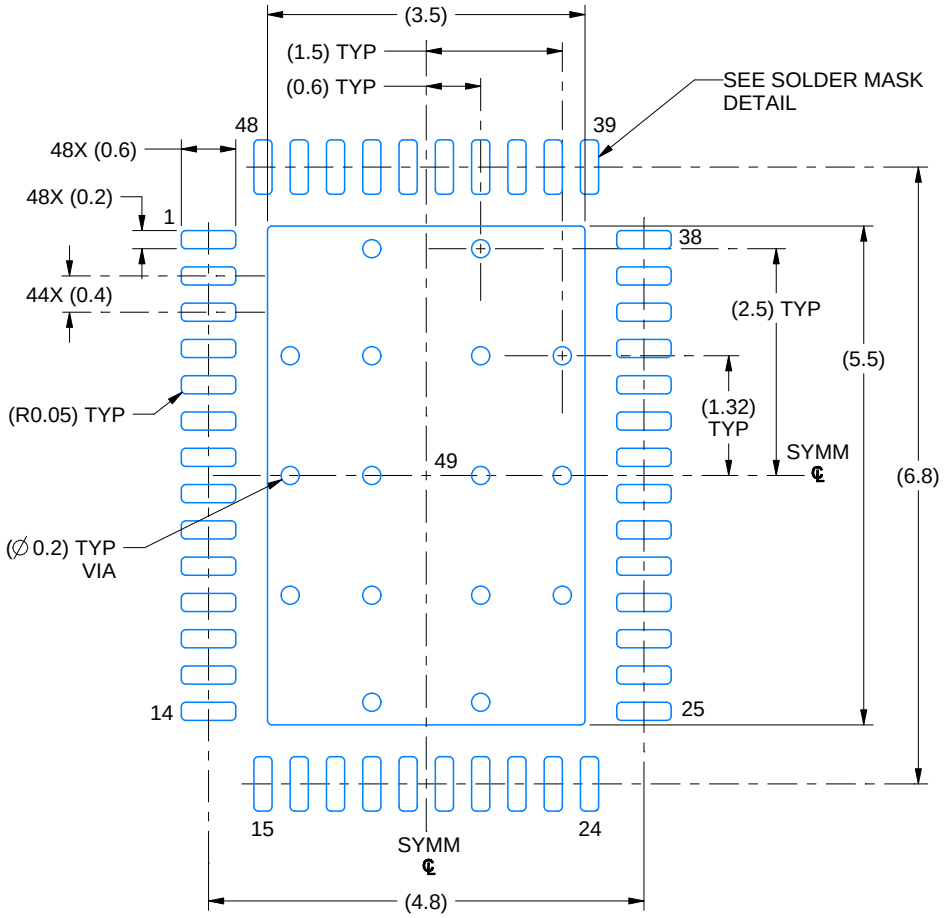
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

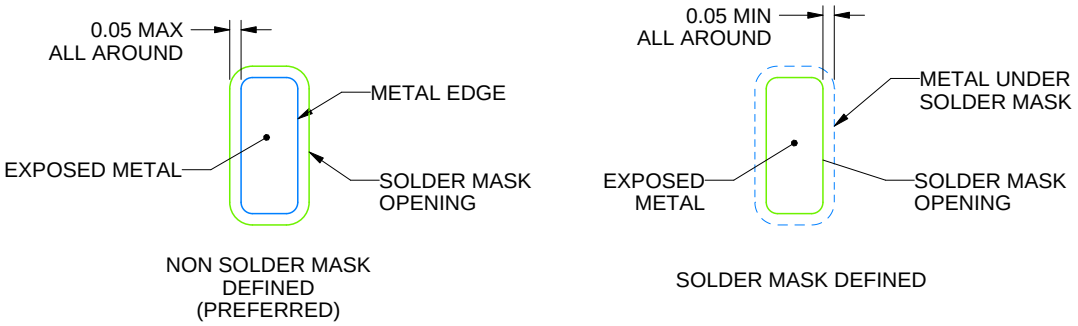


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

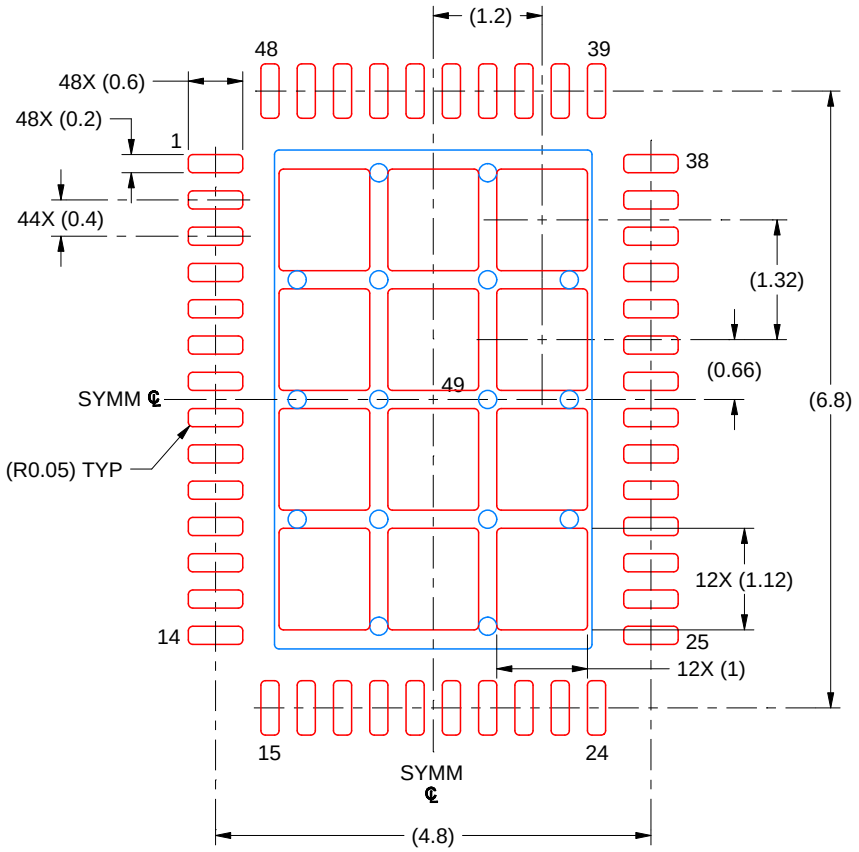


SOLDER MASK DETAILS

4224155/A 02/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

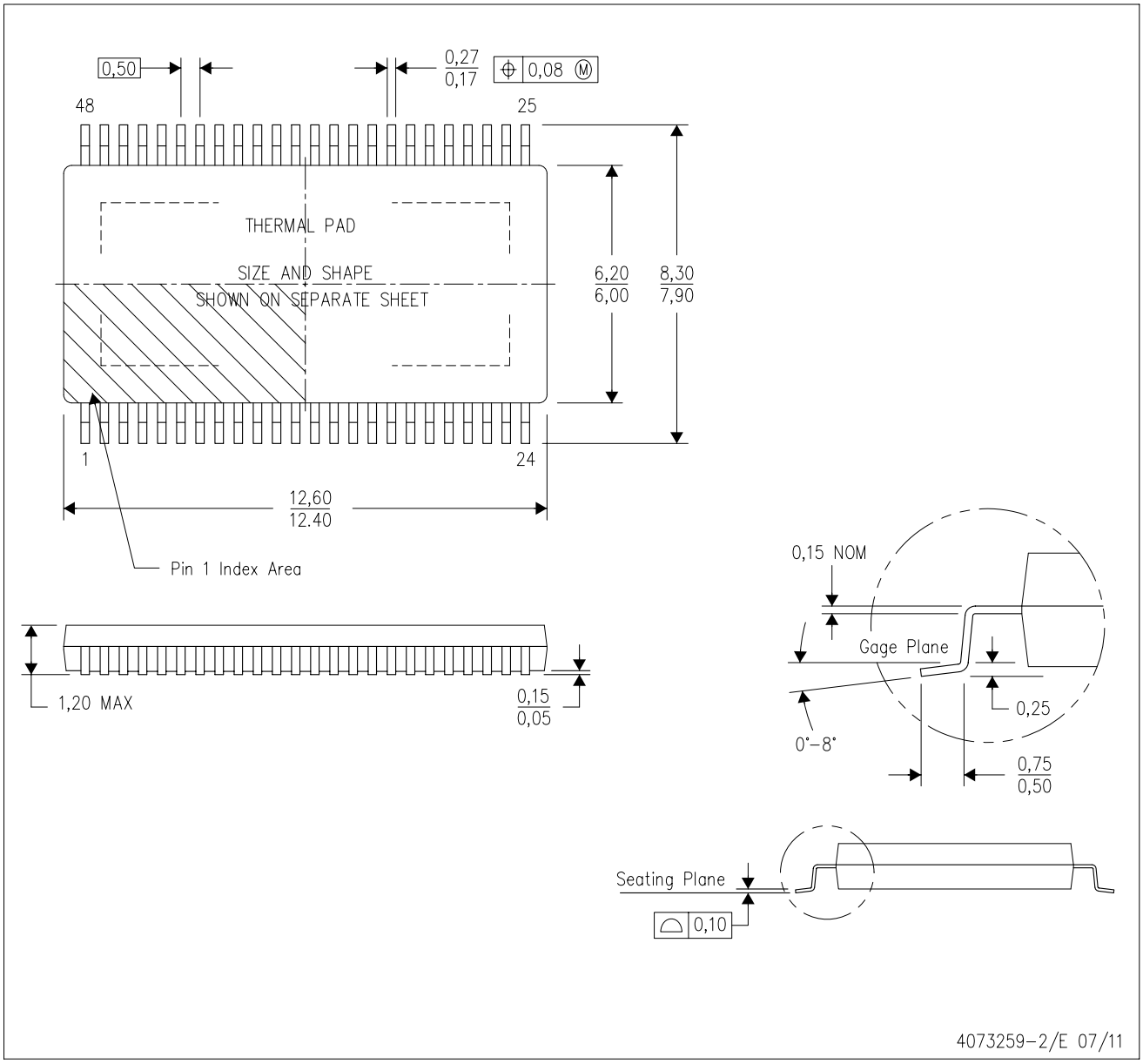
EXPOSED PAD 49
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224155/A 02/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DCA (R-PDSO-G48) PowerPAD™ PLASTIC SMALL-OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

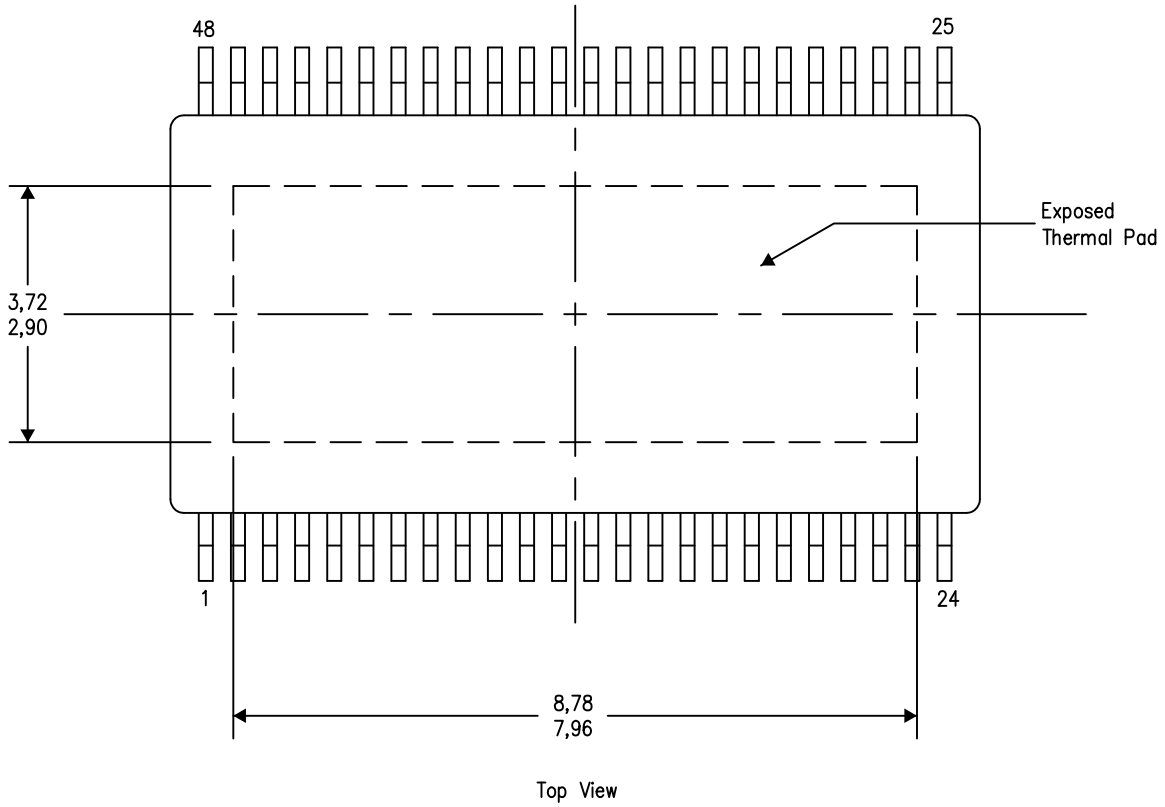
DCA (R-PDSO-G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206320-7/S 11/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

重要声明和免责声明

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