

TLC59291 用于 LED 灯且具有 7 位亮度控制、低静态电流和完全自诊断的 8/16 通道、恒流 LED 驱动器

1 特性

- 8/16 个支持开关控制的恒定灌电流输出通道
- 电流能力:
 - 1mA - 40mA ($V_{CC} \leq 3.6V$)
 - 1mA - 50mA ($V_{CC} > 3.6V$)
- 全局亮度控制: 7 位 (128 色阶)
- 电源电压范围: 3V 至 5.5V
- LED 电源电压: 高达 10V
- 恒定电流精度:
 - 通道间 = $\pm 3\%$ (典型值)
 - 器件间 = $\pm 2\%$ (典型值)
- 低静态电流
- SOUT 可配置为 8 通道或 16 通道输出
- 支持无形检测模式的 LED 开路检测 (LOD)/LED 短路检测 (LSD)
- 输出漏电检测 (OLD) 可检测 $3\mu A$ 漏电
- 预热报警 (PTW)
- 热关断 (T_{SD})
- 电流基准引脚短路标志 (ISF)
- $10\mu A$ 流耗的省电模式
- 欠压锁定可设置默认数据
- 通道间 2ns 延迟开关可最大限度减少浪涌电流
- 运行温度: $-40^{\circ}C$ 至 $85^{\circ}C$

2 应用范围

- 工业用 LED 指示灯
- 照明
- LED 视频显示

3 说明

TLC59291 是一款 8/16 通道恒定灌电流 LED 驱动器。每个通道可通过向内部寄存器写入数据进行开关。所有 16 个通道的恒定电流值均由单个外部电阻设置，并且支持 128 色阶全局亮度控制 (BC)。

TLC59291 具有六类错误标志: LED 开路检测 (LOD)、LED 短路检测 (LSD)、输出漏电检测 (OLD)、基准引脚短路检测 (ISF)、预热报警 (PTW) 以及热故障标志 (TEF)。此外, LOD 和 LSD 功能还具有无形检测模式 (IDM), 可在输出关闭时检测这些故障。故障检测结果可通过串行接口端口读取。

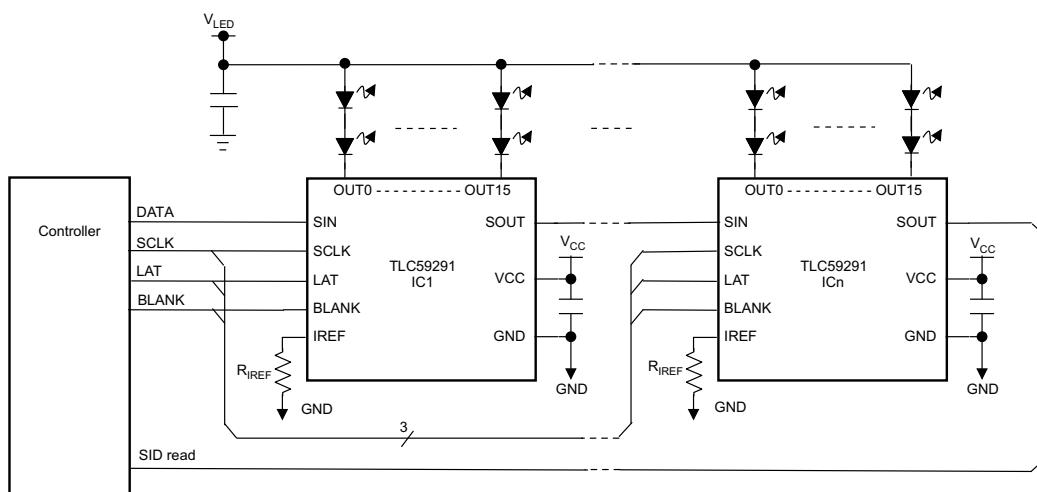
TLC59291 在正常工作模式下拥有低静态电流，并且还可在所有输出关闭时进入省电模式，从而将总电流消耗设为 $10\mu A$ (典型值)。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TLC59291	VQFN (24)	4.00mm x 4.00mm

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

典型应用电路 (以菊花链方式连接的多个 TLC59291)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

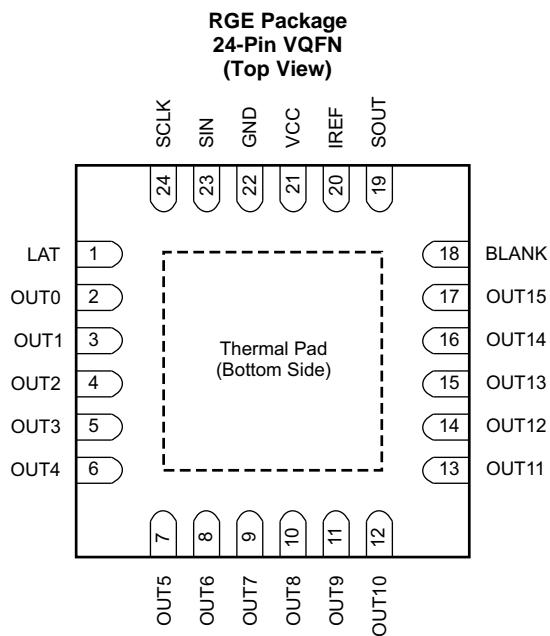
目 录

1	特性	1	8.3	Feature Description	25
2	应用范围	1	8.4	Device Functional Modes	28
3	说明	1	8.5	Register Maps	31
4	修订历史记录	2	9	Application and Implementation	37
5	Pin Configuration and Functions	3	9.1	Application Information	37
6	Specifications	4	9.2	Typical Application	37
6.1	Absolute Maximum Ratings	4	10	Power Supply Recommendations	38
6.2	ESD Ratings	5	11	Layout	39
6.3	Recommended Operating Conditions	5	11.1	Layout Guidelines	39
6.4	Thermal Information	5	11.2	Layout Example	39
6.5	Electrical Characteristics	6	12	器件和文档支持	40
6.6	Switching Characteristics	8	12.1	文档支持	40
6.7	Timing Diagrams	9	12.2	社区资源	40
6.8	Typical Characteristics	21	12.3	商标	40
7	Parameter Measurement Information	23	12.4	静电放电警告	40
8	Detailed Description	24	12.5	Glossary	40
8.1	Overview	24	13	机械、封装和可订购信息	40
8.2	Functional Block Diagram	24			

4 修订历史记录

Changes from Original (September 2015) to Revision A		Page
• 已 特性 从“通道间 = $\pm 1\%$ (典型值) ”更改为“通道间 = $\pm 3\%$ (典型值) ”	1
• Deleted device number TLC5929 From the <i>Electrical Characteristics</i> table	6
• Changed $\Delta I_{OL(C0)}$ Test Condition in <i>Electrical Characteristics</i> From: BC = 7Fh, $R_{REF} = 1.6\text{ k}\Omega$ To: BC = 0Eh, $R_{REF} = 3.6\text{ k}\Omega$,	7
• Changed the $\Delta I_{OL(C1)}$ values in <i>Electrical Characteristics</i> From: TYP = $\pm 2\%$, MAX = $\pm 4\%$ To TYP = 1% , MAX = $\pm 3\%$:	7
• Deleted device number TLC5929 From the <i>Switching Characteristics</i> table	8
• Changed text From: "with the 1-bit data" To: "with the 16-bit data" in the <i>Function Control Data Writing</i> section	34

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BLANK	18	I	<p>BLANK PIN, has two configures: When FC9(BLANK Mode) = 0, Blank pin worked as SOUT select pin:</p> <ul style="list-style-type: none"> a. When BLANK = Low, SOUT is connected to the bit 7 of the 16-bit shift register, worked as 8ch device; b. When BLANK = High, SOUT is connected to the bit 15 of the 16-bit shift register, worked as 16ch device; <p>When FC9(BLANK Mode) = 1, Blank pin worked as OUTPUT enable pin;</p> <ul style="list-style-type: none"> a. When BLANK = Low, all constant current outputs are controlled by the on/off control data in the data latch. b. When BLANK = High, all OUTx are forced off
GND	22	—	Ground
IREF	20	I/O	<p>Maximum current programming terminal. A resistor connected between IREF and GND sets the maximum current for every constant-current output. When this terminal is directly connected to GND, all outputs are forced off. The external resistor should be placed close to the device and must be in the range of 1.32 kΩ to 66 kΩ.</p>
LAT	1	I	<p>Data latch. The rising edge of LAT latches the data from the common shift register into the output on/off data latch. At the same time, the data in the common shift register are replaced with SID, which is selected by SIDLD. See the Output On/Off Data Latch section and Status Information Data (SID) section for more details.</p>

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT0	2	O	Constant-current sink outputs. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output.
OUT1	3	O	
OUT2	4	O	
OUT3	5	O	
OUT4	6	O	
OUT5	7	O	
OUT6	8	O	
OUT7	9	O	
OUT8	10	O	
OUT9	11	O	
OUT10	12	O	
OUT11	13	O	
OUT12	14	O	
OUT13	15	O	
OUT14	16	O	
OUT15	17	O	
SCLK	24	I	Serial data shift clock. Data present on SIN are shifted to the LSB of the 16-bit shift register with the SCKI rising edge. Data in the shift register are shifted toward the MSB at each SCLK rising edge. The MSB data of the common shift register appear on SOUT.
SIN	23	I	Serial data input for the 16-bit common shift register. When SIN is high, a '1' is written to the LSB of the common shift register at the rising edge of SCLK.
SOUT	19	O	Serial data output of the 16-bit common shift register. When FC9(BLANK Mode) = 0 and BLANK = LOW; SOUT is connected to the bit 7 of the 16-bit shift register. Data are clocked out at the SCLK rising edge. In other case: SOUT is connected to the bit 15 of the 16-bit shift register. Data are clocked out at the SCLK rising edge.
VCC	21	—	Power-supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		VALUE		UNIT
		MIN	MAX	
Supply voltage, V_{CC} ⁽²⁾		-0.3	6	V
Input voltage	SIN, SCLK, LAT, BLANK, IREF	-0.3	$V_{CC} + 0.3$	V
Output voltage	SOUT	-0.3	$V_{CC} + 0.3$	V
	OUT0 to OUT15	-0.3	11	V
Output current (DC)	OUT0 to OUT15		65	mA
Operating junction temperature, T_J (max)			150	°C
Storage temperature, T_{STG}		-55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to device ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

At T_A = –40°C to 85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
DC Characteristics: V_{CC} = 3 V to 5.5 V							
V _{CC}	Supply voltage			3	3.3	5.5	V
V _O	Voltage applied to output	OUT0 to OUT15				10	V
V _{IH}	High-level input voltage	SIN, SCLK, LAT, BLANK		0.7 × V _{CC}		V _{CC}	V
V _{IL}	Low-level input voltage	SIN, SCLK, LAT, BLANK		GND	0.3 × V _{CC}		V
I _{OH}	High-level output current	SOUT				–2	mA
I _{OL}	Low-level output current	SOUT				2	mA
I _{OLC}	Constant output sink current	OUT0 to OUT15	3 V ≤ V _{CC} ≤ 3.6 V			40	mA
		OUT0 to OUT15	3.6 V < V _{CC} ≤ 5.5 V			50	mA
T _A	Operating free-air temperature range			–40		85	°C
T _J	Operating junction temperature range			–40		125	°C
AC Characteristics: V_{CC} = 3 V to 5.5 V							
f _{CLK} (SCLK)	Data shift clock frequency	SCLK				33	MHz
t _{W0}	Pulse duration (see Figure 1 and Figure 3)	SCLK		10			ns
t _{W0}		SCLK		10			ns
t _{W1}		LAT		20			ns
t _{W2}		BLANK		40			ns
t _{W2}		BLANK		40			ns
t _{SU0}		SIN to SCLK↑		5			ns
t _{SU1}	(see Figure 1 , Figure 3 and Figure 4)	LAT↑ to SCLK↑		200			ns
t _{SU2}		SCLK↓ to LAT↑		10			ns
t _{H0}		SIN to SCLK↑		3			ns
t _{H1}	(see Figure 1 , Figure 3 , and Figure 13)	LAT↑ to SCLK↑		10			ns
t _{H2}		LAT↑ to SCLK↓		40			ns

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾			TLC59291	UNIT
			RGE (VQFN)	
			24 PINS	
R _{θJA}	Junction-to-ambient thermal resistance		38.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance		45.3	
R _{θJB}	Junction-to-board thermal resistance		16.9	
Ψ _{JT}	Junction-to-top characterization parameter		0.9	
Ψ _{JB}	Junction-to-board characterization parameter		16.9	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance		6.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

At $V_{CC} = 3$ V to 5.5 V and $T_A = -40^\circ\text{C}$ to 85°C . Typical values at $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{OH}	High-level output voltage $I_{OH} = -2$ mA at SOUT	$V_{CC} - 0.4$		V_{CC}	V	
V_{OL}	Low-level output voltage $I_{OL} = 2$ mA at SOUT			0.4	V	
V_{LOD}	LED open detection threshold All OUT n = on	0.25	0.30	0.35	V	
V_{LSD0}	LED short detection threshold All OUT n = on, detection voltage code = 0h	$0.32 \times V_{CC}$	$0.35 \times V_{CC}$	$0.38 \times V_{CC}$	V	
V_{LSD1}		$0.42 \times V_{CC}$	$0.45 \times V_{CC}$	$0.48 \times V_{CC}$	V	
V_{LSD2}		$0.52 \times V_{CC}$	$0.55 \times V_{CC}$	$0.58 \times V_{CC}$	V	
V_{LSD3}		$0.62 \times V_{CC}$	$0.65 \times V_{CC}$	$0.68 \times V_{CC}$	V	
V_{IREF}	Reference voltage output $R_{IREF} = 1.3$ k Ω	1.175	1.205	1.235	V	
I_{IN}	Input current $V_{IN} = V_{CC}$ or GND at SIN, SCLK, LAT, and BLANK	-1		1	μA	
I_{CC0}	Supply current (V_{CC}) SIN/SCLK/LAT = Low, BLANK = High, all OUT n = off, $V_{OUTn} = 0.8$ V, BC = 7Fh, R_{IREF} = open	2	3		mA	
I_{CC1}		5	7		mA	
I_{CC2}		5	7		mA	
I_{CC3}		3	4		mA	
I_{CC4}		9	11		mA	
I_{CC5}		11	14		mA	
I_{CC6}		10	40		μA	
$I_{OL(C0)}$	Constant output sink current (OUT0 to OUT15, see Figure 28)	All OUT n = on, $V_{OUTn} = V_{OUTfix} = 0.8$ V, BC = 7Fh, $R_{IREF} = 1.6$ k Ω	38.5	41.3	44.1	mA
$I_{OL(C1)}$		$V_{CC} = 5$ V, All OUT n = on, $V_{OUTn} = V_{OUTfix} = 1$ V, BC = 7Fh, $R_{IREF} = 1.3$ k Ω	47.3	50.8	54.3	mA
$I_{OL(KG0)}$	Output leakage current (OUT0 to OUT15, see Figure 28)	BLANK = high, $V_{OUTn} = V_{OUTfix} = 10$ V, $R_{IREF} = 1.6$ k Ω	$T_J = 25^\circ\text{C}$		0.1	μA
$I_{OL(KG1)}$			$T_J = 85^\circ\text{C}^{(1)}$		0.2	μA
$I_{OL(KG2)}$			$T_J = 125^\circ\text{C}^{(1)}$		0.3	μA

(1) Not tested; specified by design.

Electrical Characteristics (continued)

At $V_{CC} = 3$ V to 5.5 V and $T_A = -40^\circ\text{C}$ to 85°C . Typical values at $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta I_{OL(C0)}$	Constant-current error (channel-to-channel, OUT0 to OUT15) ⁽²⁾ All OUT n = on, $V_{OUTn} = V_{OUTfix} = 0.8$ V, BC = 0Eh, $R_{REF} = 3.6$ k Ω , $T_A = 25^\circ\text{C}$		$\pm 3\%$	$\pm 6\%$	
$\Delta I_{OL(C1)}$	Constant-current error (device-to-device, OUT0 to OUT15) ⁽³⁾ All OUT n = on, $V_{OUTn} = V_{OUTfix} = 0.8$ V, BC = 7Fh, $R_{REF} = 1.6$ k Ω , $T_A = 25^\circ\text{C}$		$\pm 1\%$	$\pm 3\%$	
$\Delta I_{OL(C2)}$	Line regulation ⁽⁴⁾ All OUT n = on, $V_{OUTn} = V_{OUTfix} = 0.8$ V, BC = 7Fh, $R_{REF} = 1.6$ k Ω		± 0.1	± 1	%/V
$\Delta I_{OL(C3)}$	Load regulation ⁽⁵⁾ All OUT n = on, $V_{OUTn} = 0.8$ V to 3 V, $V_{OUTfix} = 0.8$ V, BC = 7Fh, $R_{REF} = 1.6$ k Ω		± 0.5	± 3	%/V
T_{TEF}	Thermal error flag threshold Junction temperature ⁽¹⁾	150	165	180	$^\circ\text{C}$
T_{HYS}	Thermal error flag hysteresis Junction temperature ⁽¹⁾	5	10	20	$^\circ\text{C}$
T_{PTW}	Pre-thermal warning threshold Junction temperature ⁽¹⁾	125	138	150	$^\circ\text{C}$

(2) The deviation of each output from the average of OUT0 to OUT15 constant-current. Deviation is calculated by the formula:

$$\Delta (\%) = 100 \times \left[\frac{\frac{I_{OLC(n)}}{\left(I_{OLC(0)} + I_{OLC(1)} + \dots + I_{OLC(14)} + I_{OLC(15)} \right)}}{16} - 1 \right]$$

(3) The deviation of the OUT0 to OUT15 constant-current average from the ideal constant-current value. Deviation is calculated by the formula:

$$\Delta (\%) = 100 \times \left[\frac{\left(I_{OLC(0)} + I_{OLC(1)} + \dots + I_{OLC(14)} + I_{OLC(15)} \right)}{16} - \text{Ideal Output Current} \right]$$

$$\text{Ideal current is calculated by the formula: } I_{OLC_IDEAL} = 54 \times \left(\frac{1.20}{R_{REF}} \right)$$

(4) Line regulation is calculated by the formula:

$$\Delta (\%) = 100 \times \left[\frac{\left(I_{OLC(n)} \text{ at } V_{CC} = 5.5 \text{ V} \right) - \left(I_{OLC(n)} \text{ at } V_{CC} = 3 \text{ V} \right)}{2.5 \times \left(I_{OLC(n)} \text{ at } V_{CC} = 3 \text{ V} \right)} \right]$$

(5) Load regulation is calculated by the equation:

$$\Delta (\%) = 100 \times \left[\frac{\left(I_{OLC(n)} \text{ at } V_{OUTn} = 3 \text{ V} \right) - \left(I_{OLC(n)} \text{ at } V_{OUTn} = 1 \text{ V} \right)}{2 \times \left(I_{OLC(n)} \text{ at } V_{OUTn} = 1 \text{ V} \right)} \right]$$

6.6 Switching Characteristics

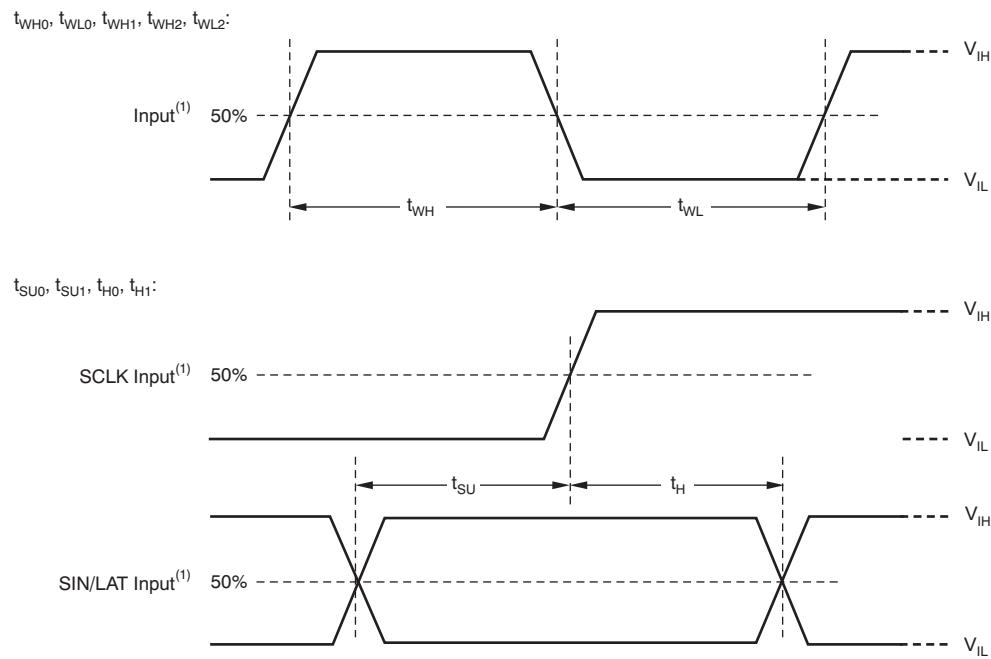
At $V_{CC} = 3$ V to 5.5 V, $T_A = -40^\circ\text{C}$ to 85°C , $C_L = 15$ pF, $R_L = 82$ Ω , $R_{REF} = 1.3$ k Ω , and $V_{LED} = 5$ V.

Typical values at $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{R0}	Rise time	At SOUT		10	15	ns
t_{R1}		At OUT n , BC = 7Fh		40	60	ns
t_{F0}	Fall time	At SOUT		10	15	ns
t_{F1}		At OUT n , BC = 7Fh		40	60	ns
t_{D0}	Propagation delay	SCLK \uparrow to SOUT $\uparrow\downarrow$		8	22	ns
t_{D1}		LAT \uparrow or BLANK $\uparrow\downarrow$ to OUT0 sink current on/off, BC = 7Fh		35	65	ns
t_{D2}		OUT n on/off to OUT $n + 1$ on/off, BC = 7Fh		2	6	ns
t_{D3}		LAT \uparrow to power-save mode by data writing for all output off			400	ns
t_{D4}		SCLK \uparrow to normal mode operation			100	μs
t_{D5}		BLANK $\uparrow\downarrow$ to SOUT $\uparrow\downarrow$ when BLANK MODE=0			100	ns
t_{ON_ERR}	Output on-time error ⁽¹⁾	Output on/off data = all '1', BLANK low pulse = 40 ns, BC = 7Fh	-30		20	ns
f_{osc}	Internal oscillator frequency		12	20	28	MHz

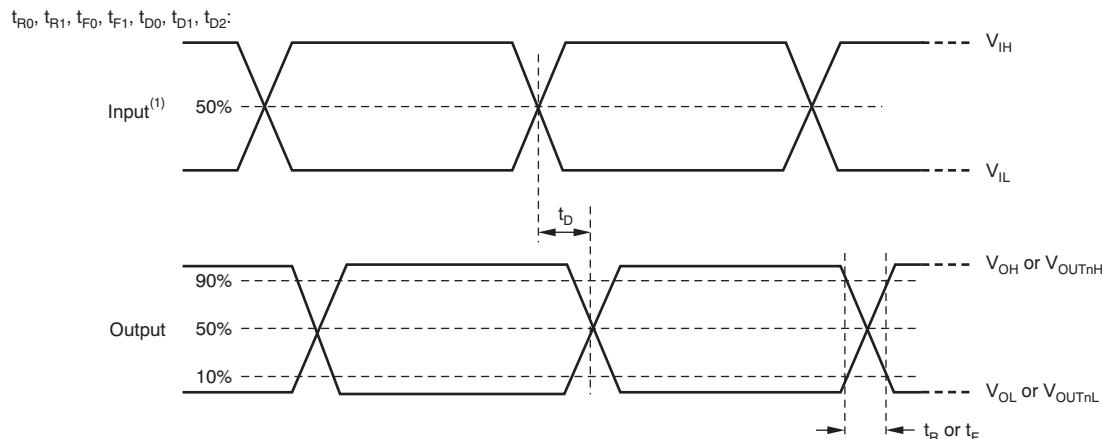
(1) Output on-time error (t_{ON_ERR}) is calculated by the formula: t_{ON_ERR} (ns) = t_{OUT_ON} – 40 ns. t_{OUT_ON} is the actual on-time of OUT n .

6.7 Timing Diagrams



(1) Input pulse rise and fall time is 1 ns to 3 ns.

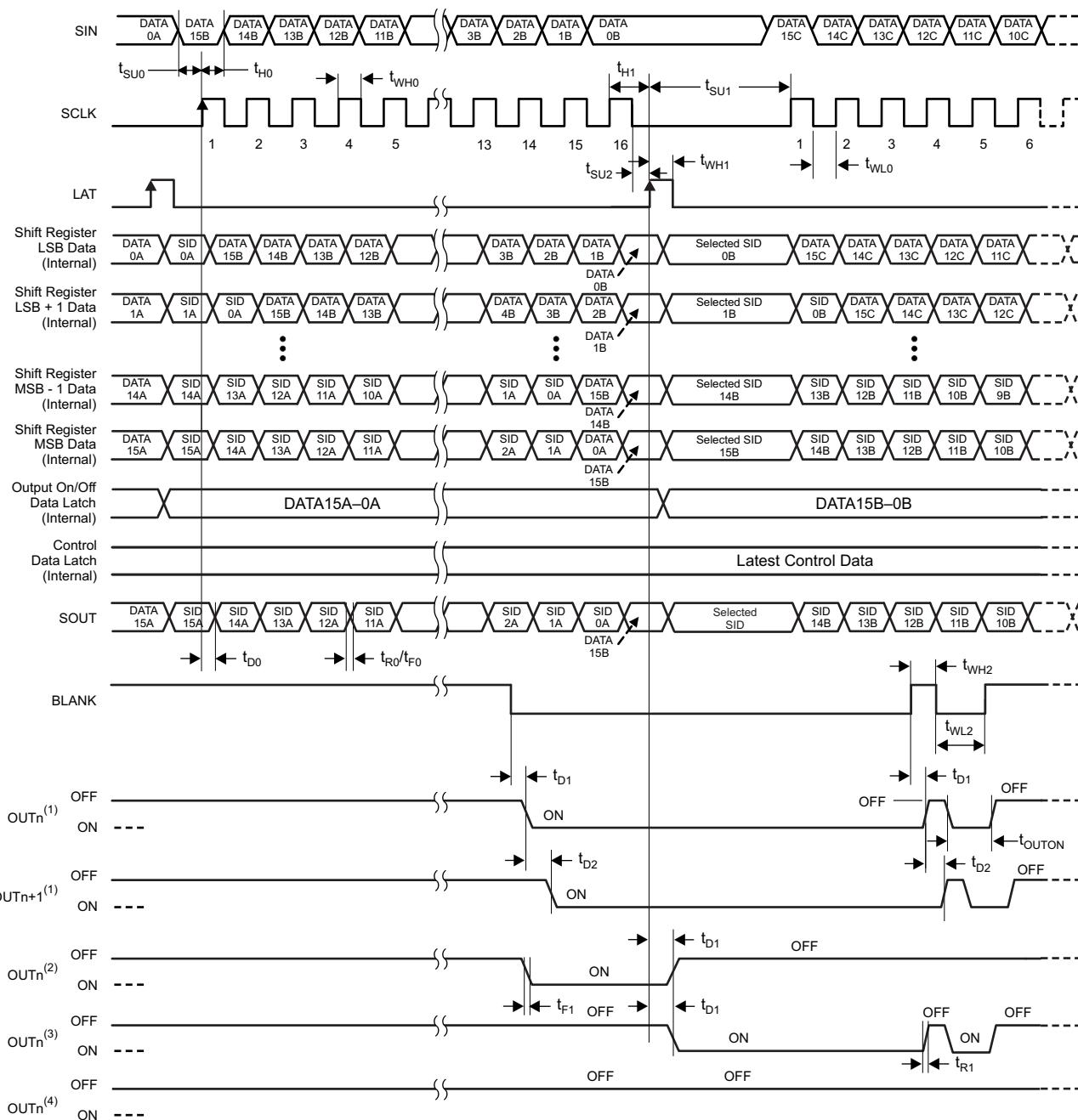
Figure 1. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 2. Output Timing

Timing Diagrams (continued)



(1) On/off latched data is '1'.

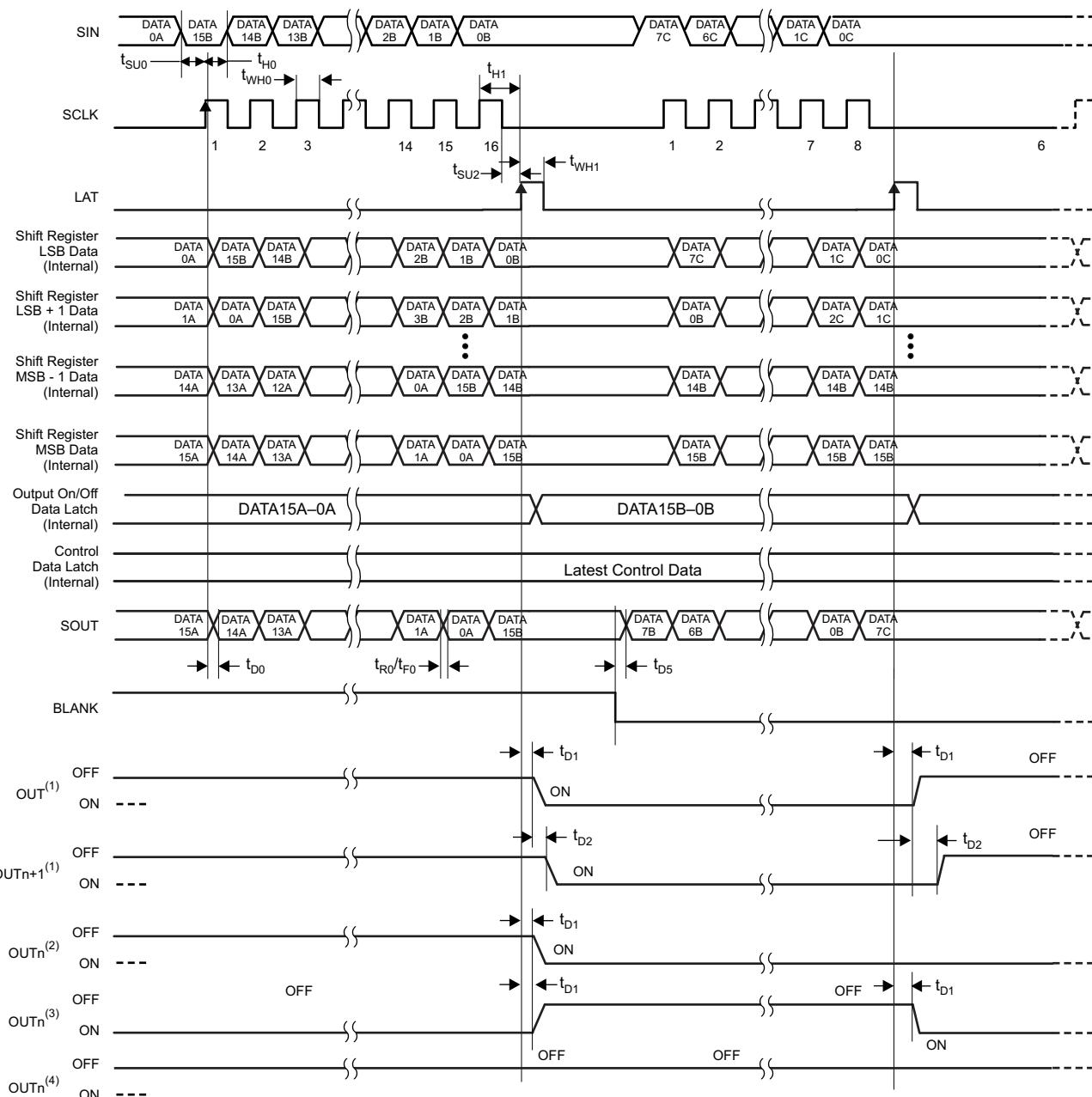
(2) On/off latched data change from '1' to '0' at second LAT signal.

(3) On/off latched data change from '0' to '1' at second LAT signal.

(4) On/off latched data is '0'.

Figure 3. Write for ON/Off Data and Output Timing (BLANK Mode = 1)

Timing Diagrams (continued)



- (1) If the on/off latched data is changed from "0" to "1" at 1'st LAT signal, changed from "1" to "0" at second LAT signal.
- (2) If the on/off latched data is changed from "0" to "1" at 1'st LAT signal, changed from "1" to "1" at second LAT signal.
- (3) If the on/off latched data is changed from "1" to "0" at 1'st LAT signal, changed from "0" to "1" at second LAT signal.
- (4) if the on/off latched data is "0".

Figure 4. Write for On/Off Data and Output Timing (BLANK Mode = 0)

Timing Diagrams (continued)

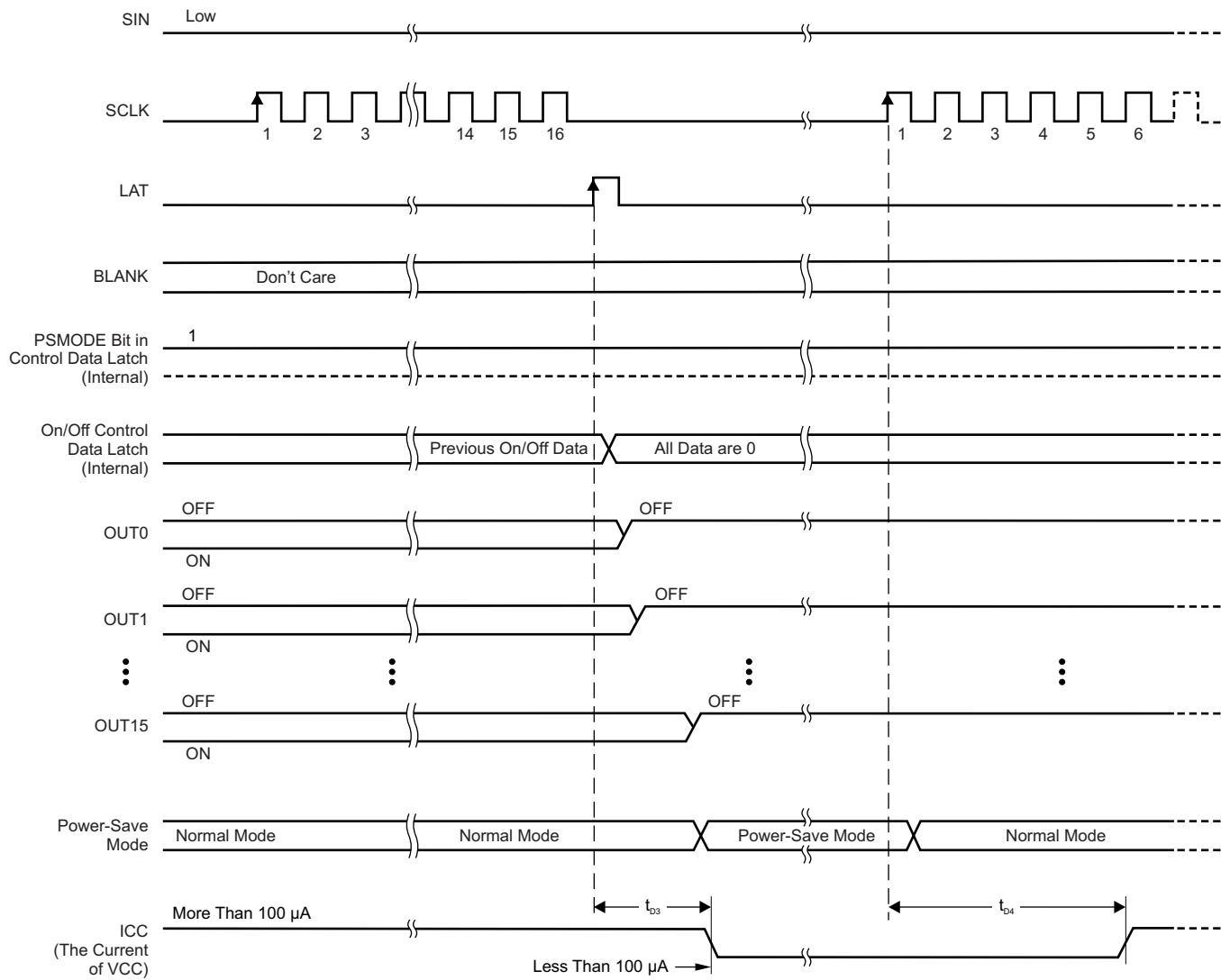


Figure 5. Power-Save Mode

Timing Diagrams (continued)

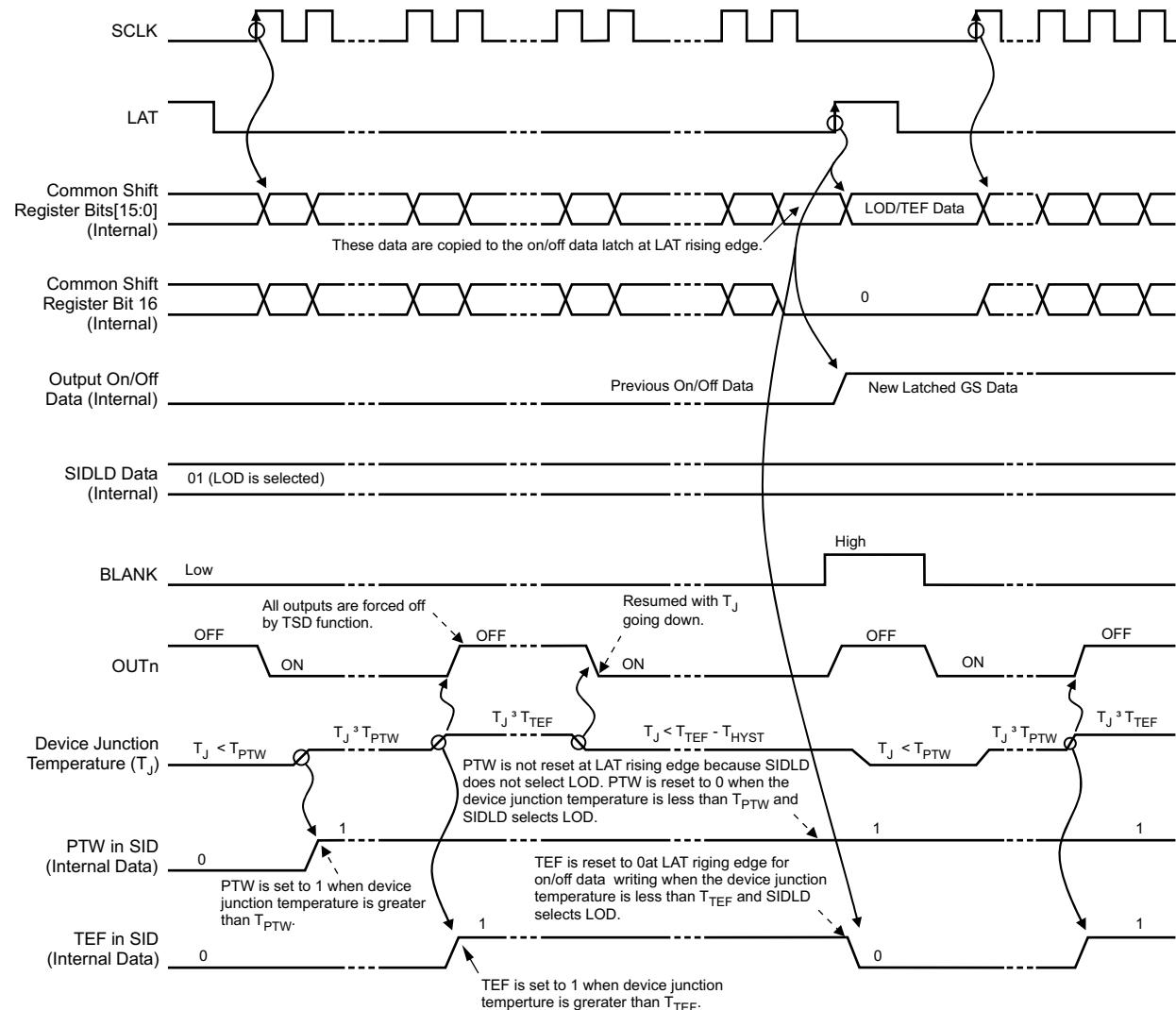


Figure 6. PTW/TEF/TSD Timing (LOD Selected)

Timing Diagrams (continued)

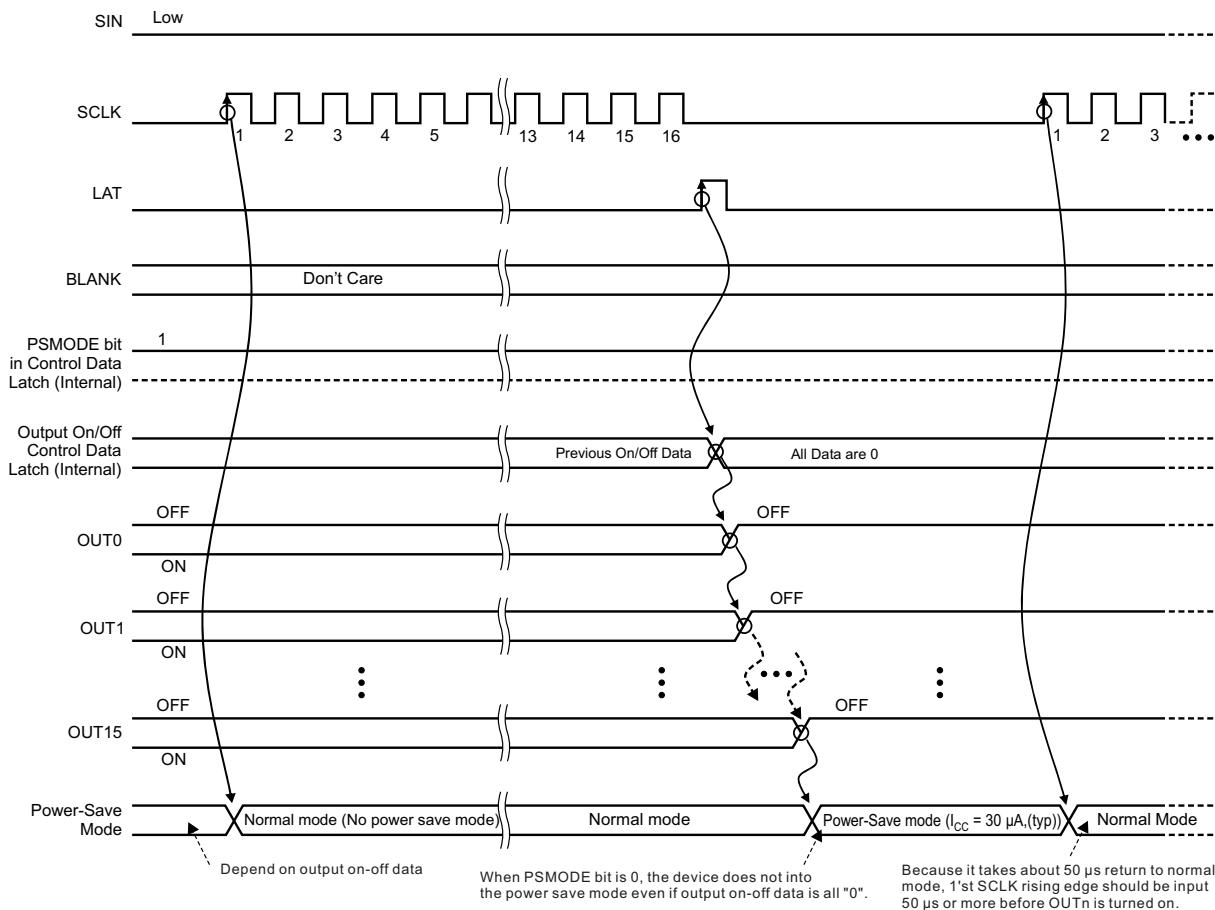


Figure 7. Power-Save Mode Timing

Timing Diagrams (continued)

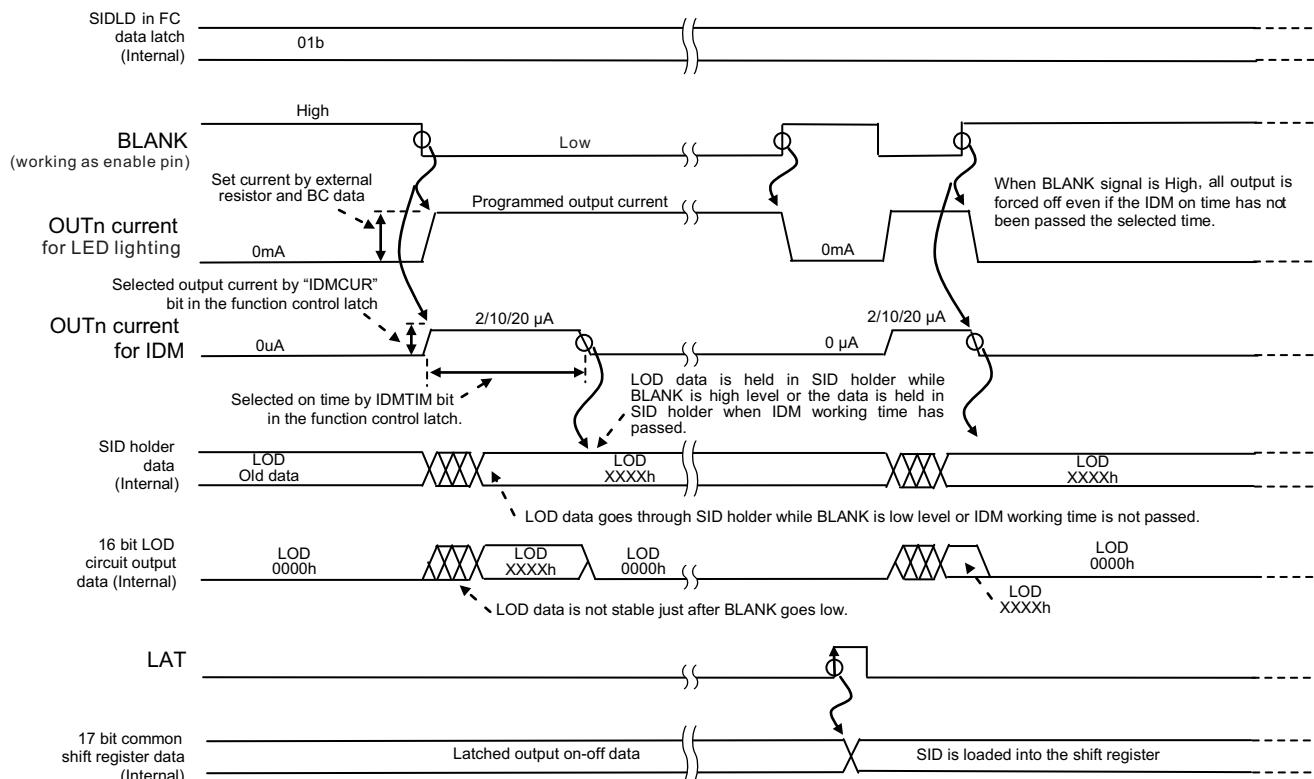


Figure 8. IDM Operation Timing with LOD Selected and IDM Enabled

Timing Diagrams (continued)

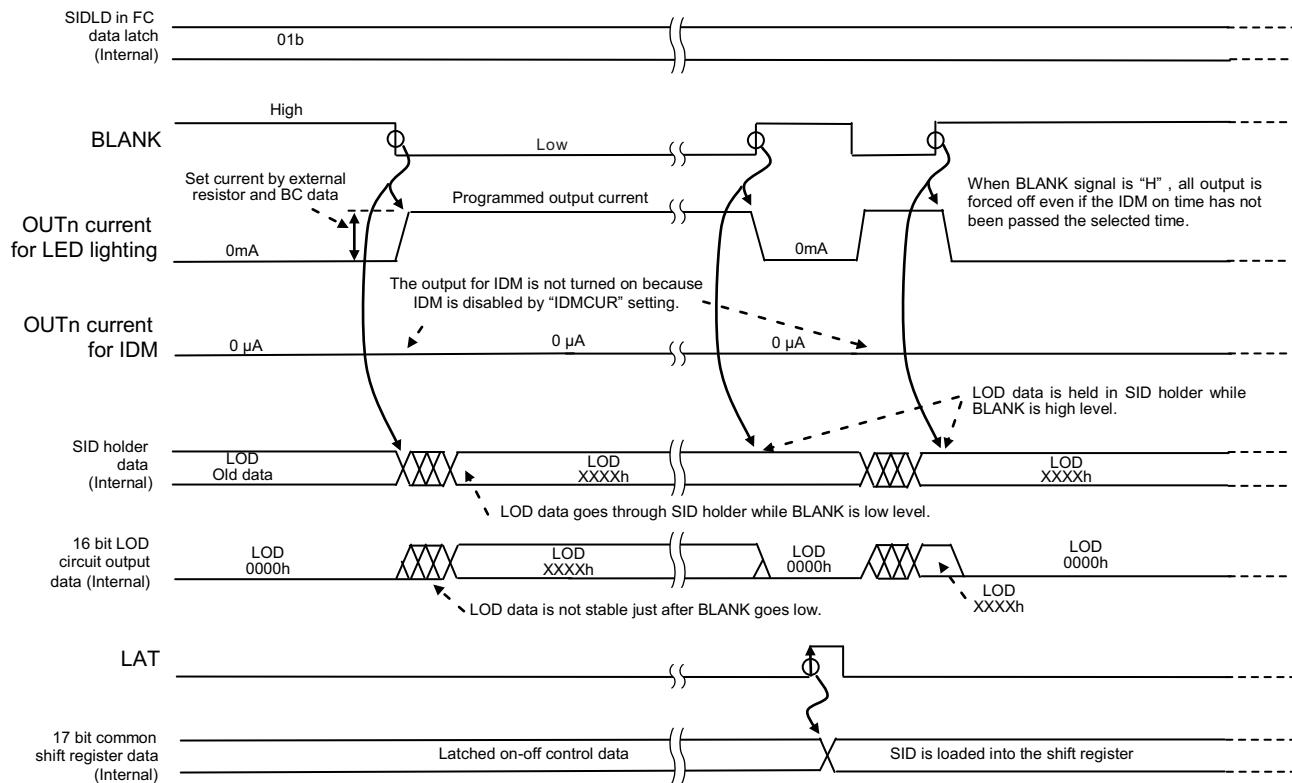


Figure 9. IDM Operation Timing with LOD Selected and IDM Disabled

Timing Diagrams (continued)

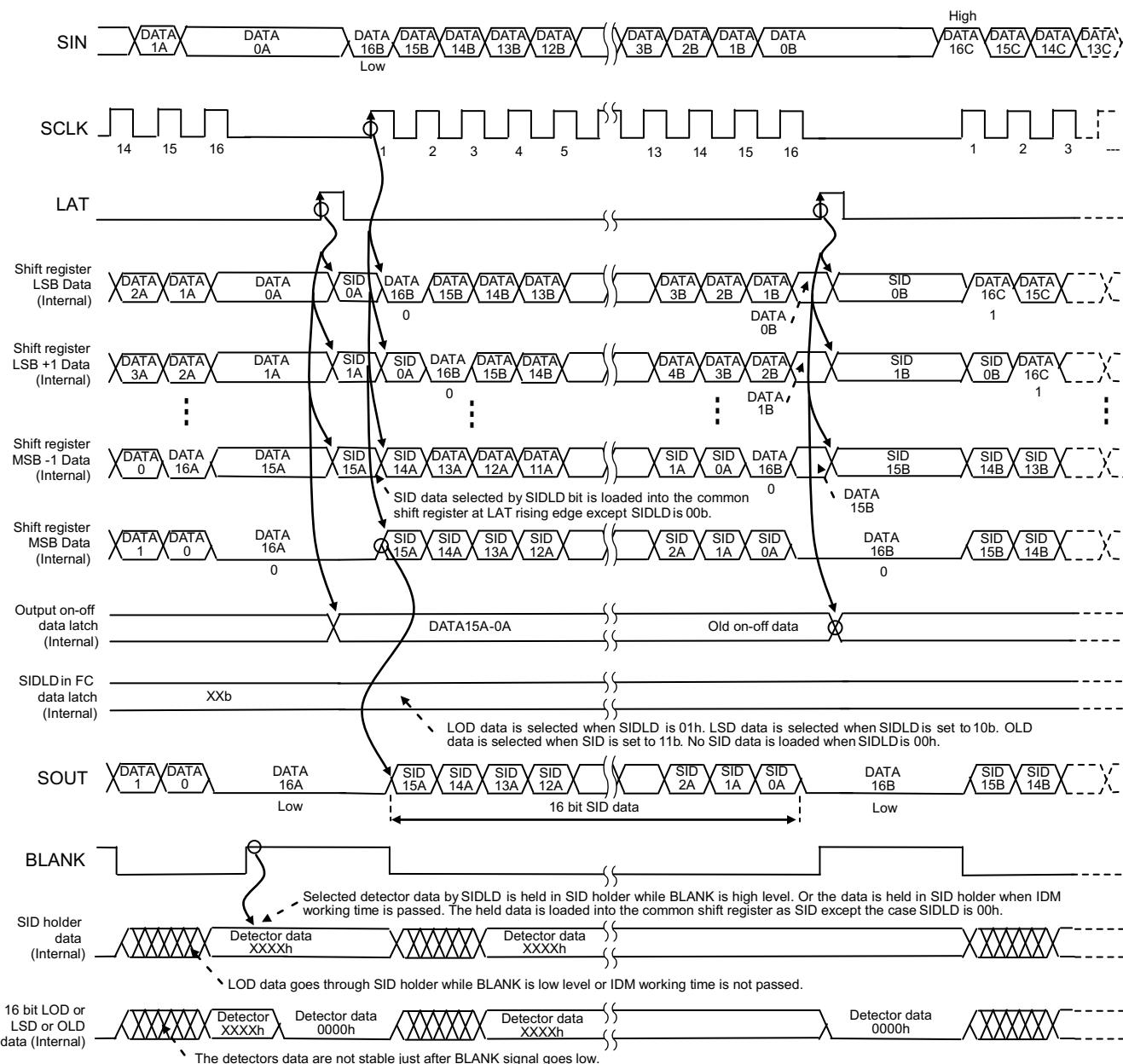
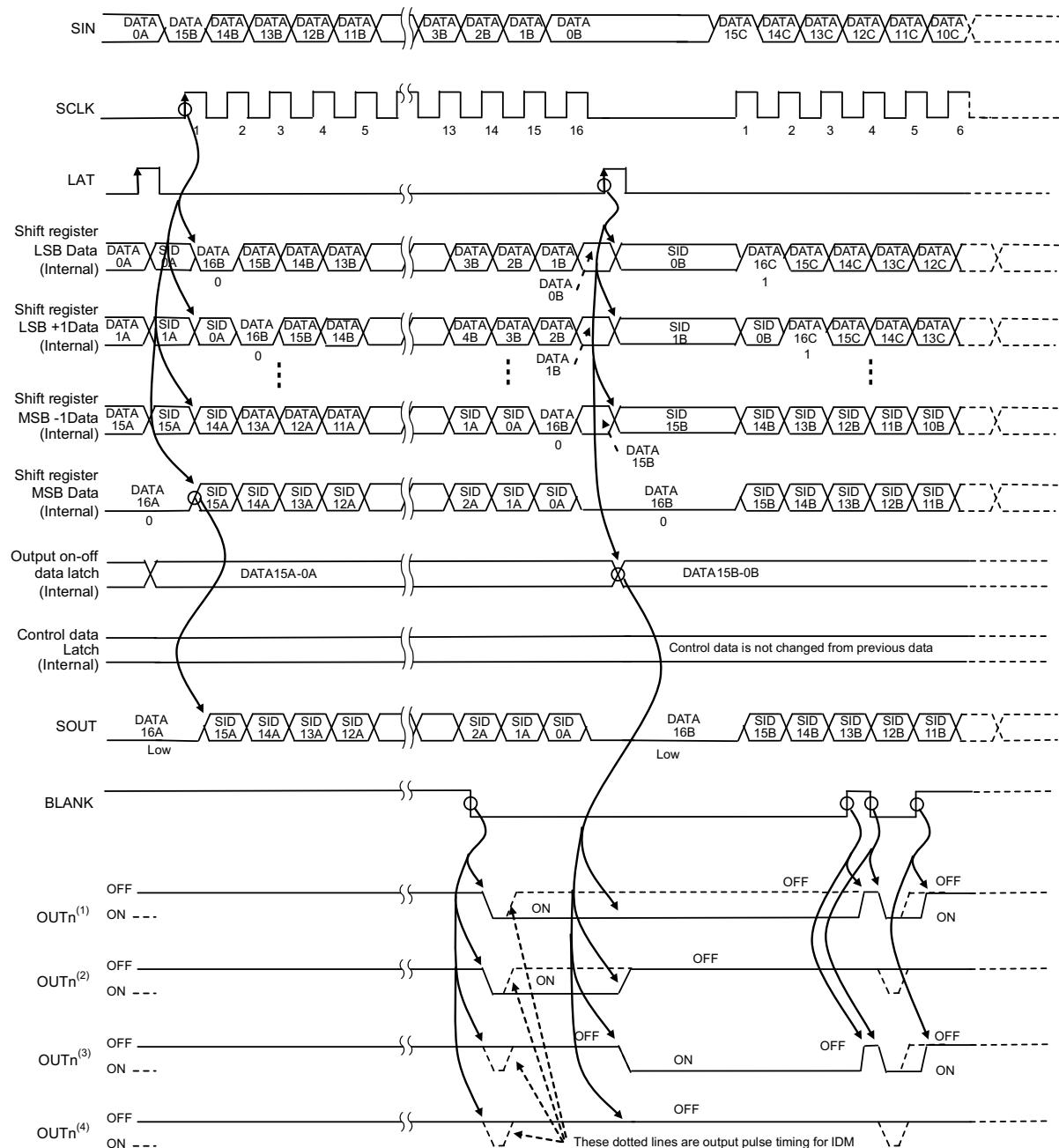


Figure 10. SID Read Timing

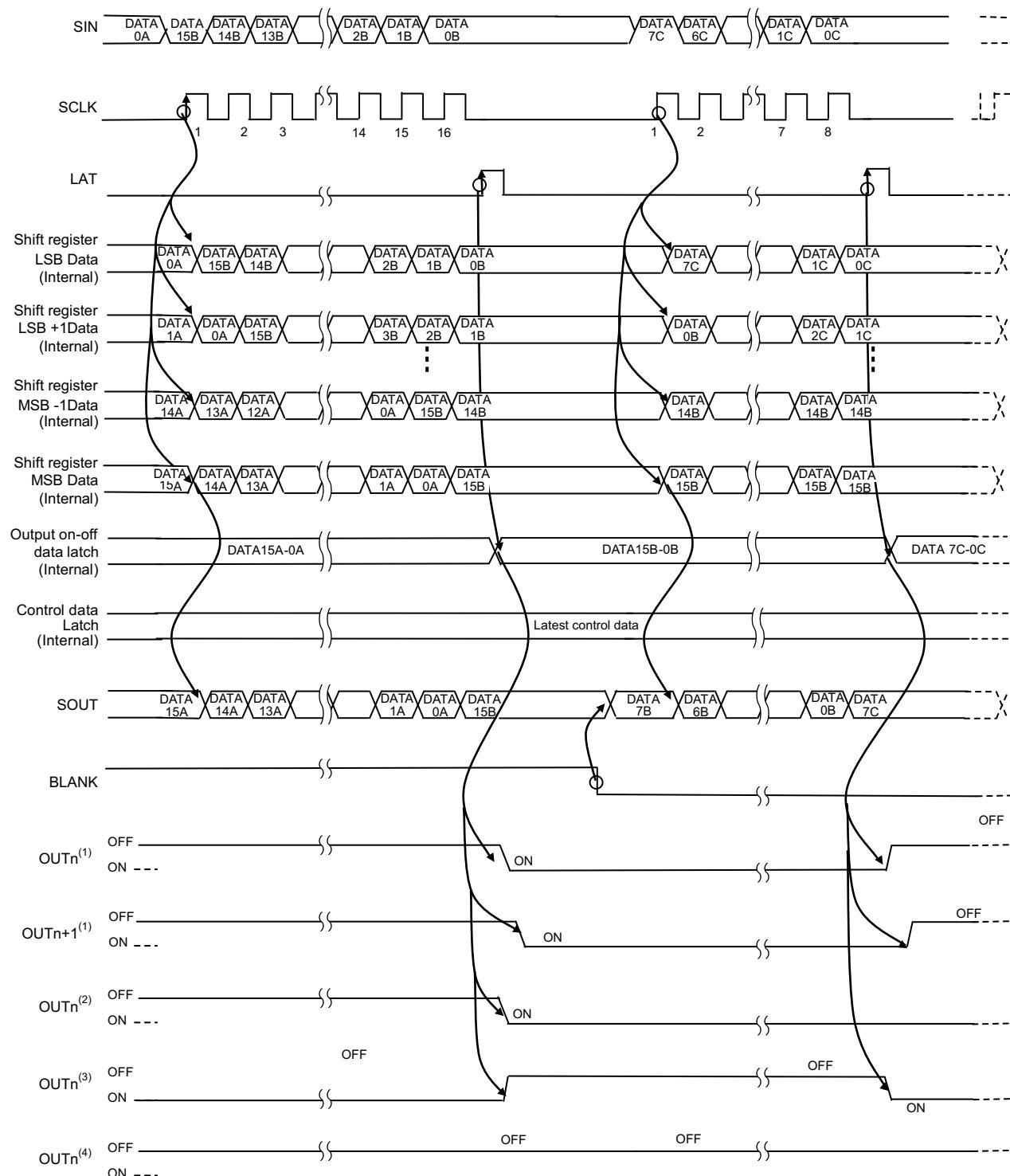
Timing Diagrams (continued)



- (1) On/off latch data is '1'.
- (2) On/off latch data change from '1' to '0' at second LAT signal.
- (3) On/off latch data is change from '0' to '1' at second LAT signal.
- (4) On/off latch data is '0'.

Figure 11. On-Off Control Data Write Timing (BLANK Mode = 1)

Timing Diagrams (continued)



- (1) If the on/off latched data is changed from “0” to “1” at 1’st LAT signal, changed from “1” to “0” at 2’nd LAT signal.
- (2) If the on/off latched data is changed from “0” to “1” at 1’st LAT signal, changed from “1” to “1” at 2’nd LAT signal.
- (3) If the on/off latched data is changed from “1” to “0” at 1’st LAT signal, changed from “0” to “1” at 2’nd LAT signal.
- (4) If the on/off latched data is “0”.

Figure 12. On-Off Control Data Write Timing (BLANK Mode = 0)

Timing Diagrams (continued)

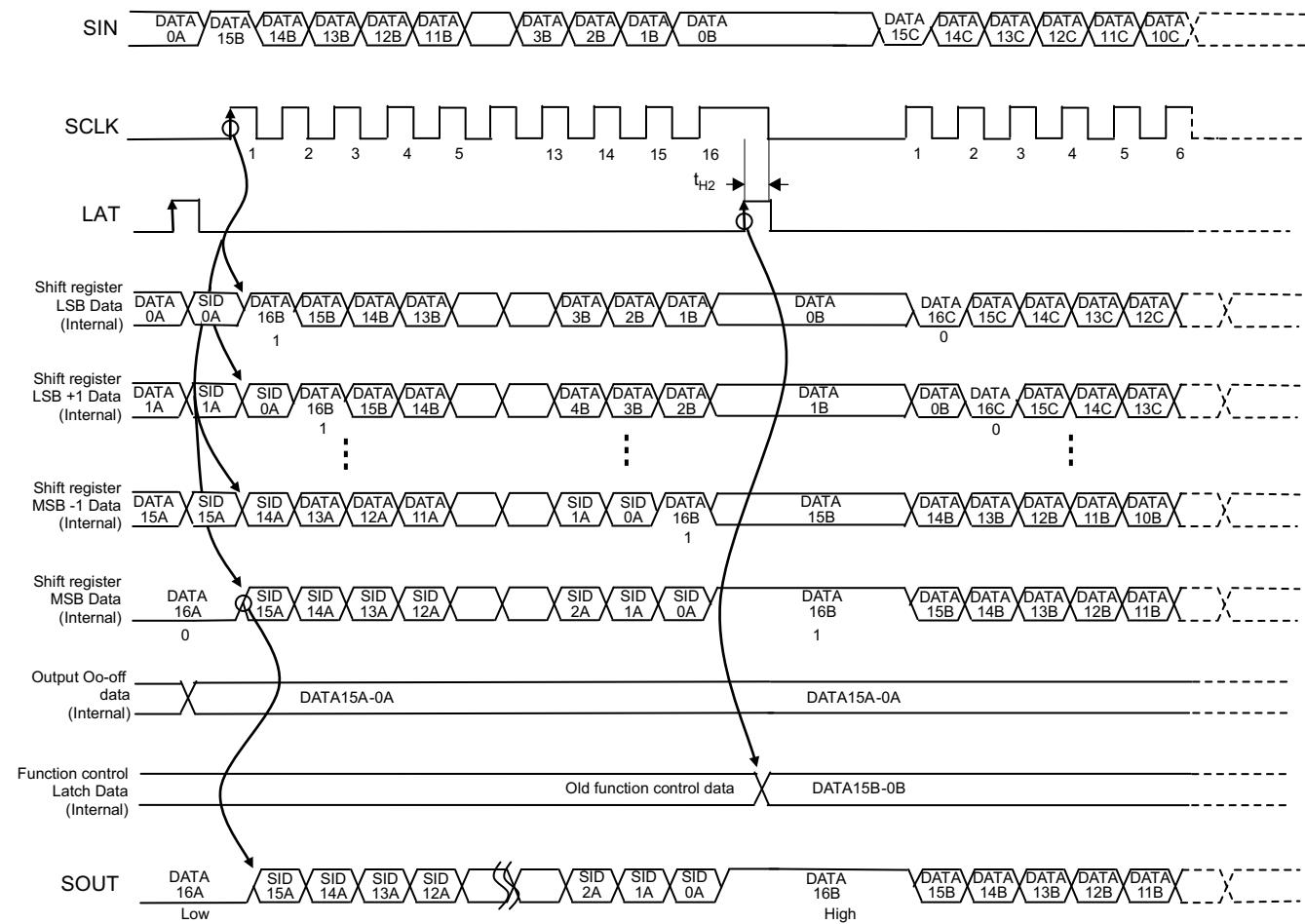


Figure 13. Function Control Data Write Timing

6.8 Typical Characteristics

At $T_A = 25^\circ\text{C}$, unless otherwise noted.

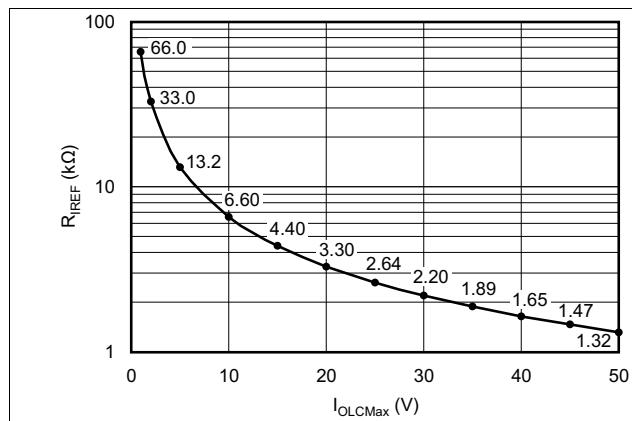


Figure 14. Reference Resistor vs Output Current

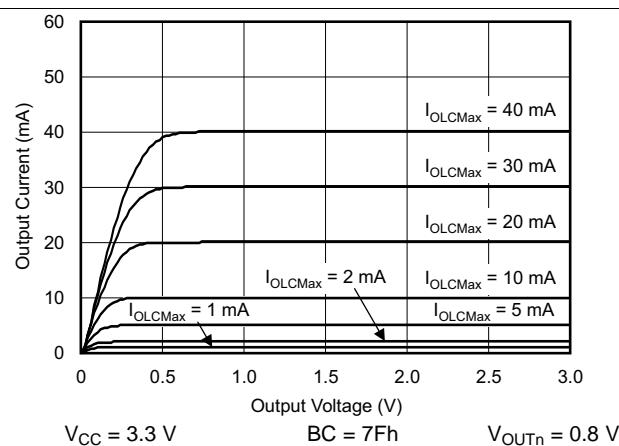


Figure 15. OUTn Current vs Output Voltage

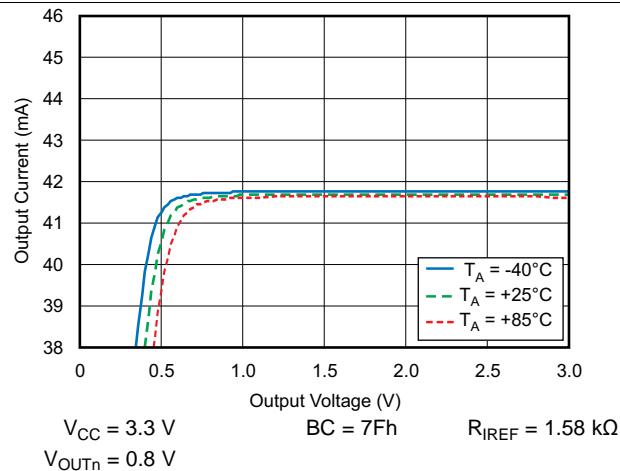


Figure 16. OUTn Current vs Output Voltage

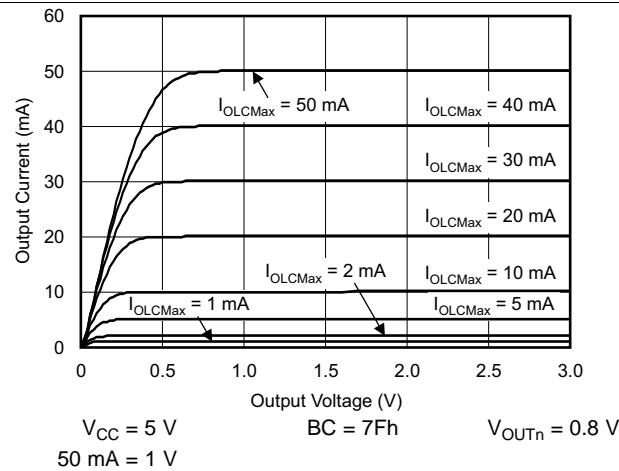


Figure 17. OUTn Current vs Output Voltage

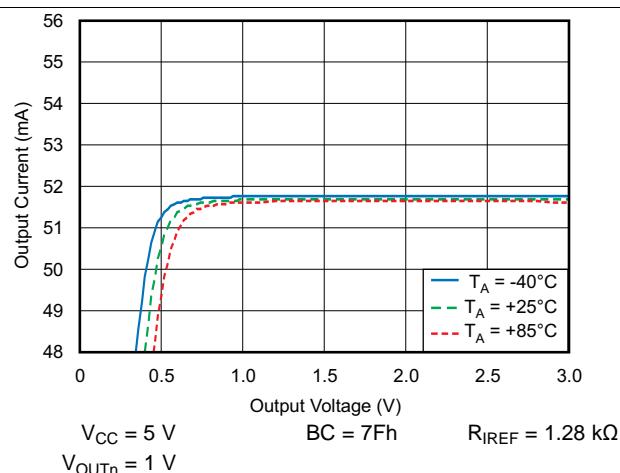


Figure 18. OUTn Current vs Output Voltage

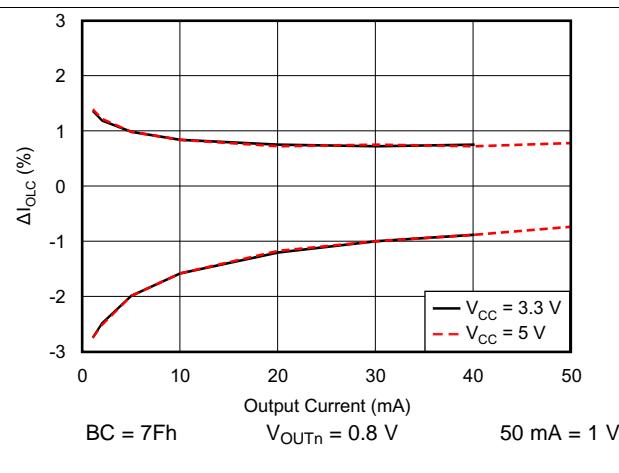


Figure 19. Constant-Current Error
vs Output Current set by R_REF or BC Data (Channel-to-
Channel)

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, unless otherwise noted.

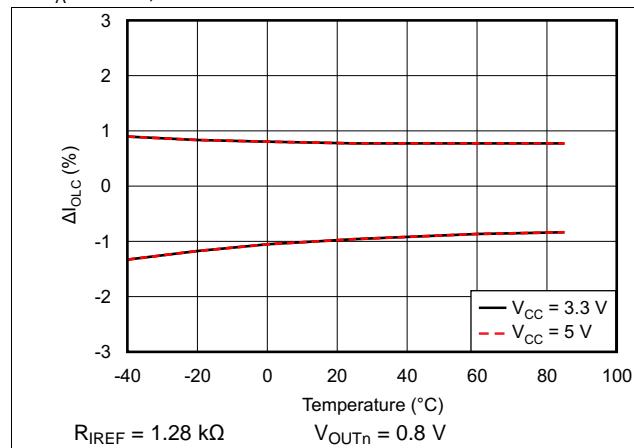


Figure 20. Constant-Current Error vs Ambient Temperature (Channel-to-Channel)

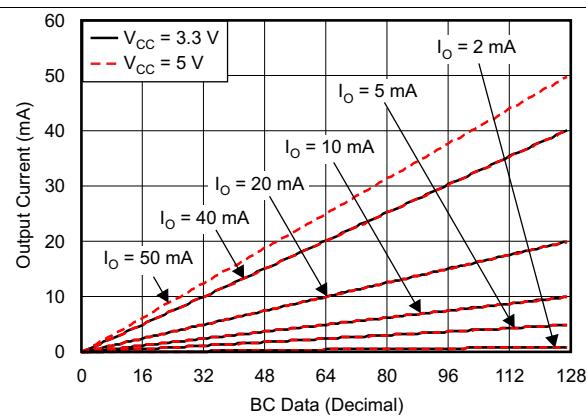


Figure 21. Global Brightness Control Linearity

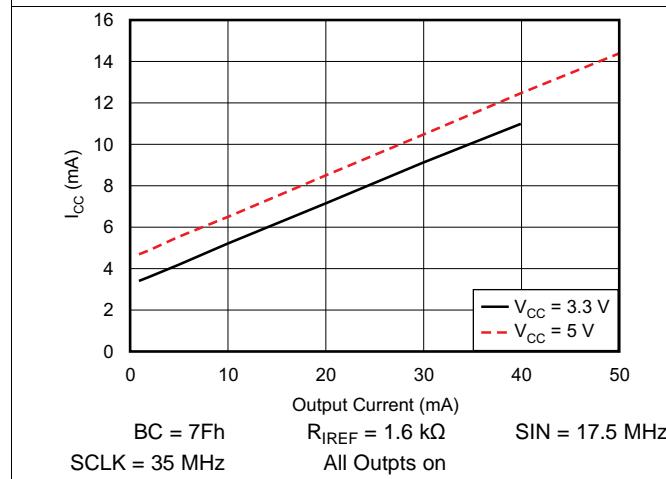


Figure 22. Supply Current vs Output Current Set by R_{REF}

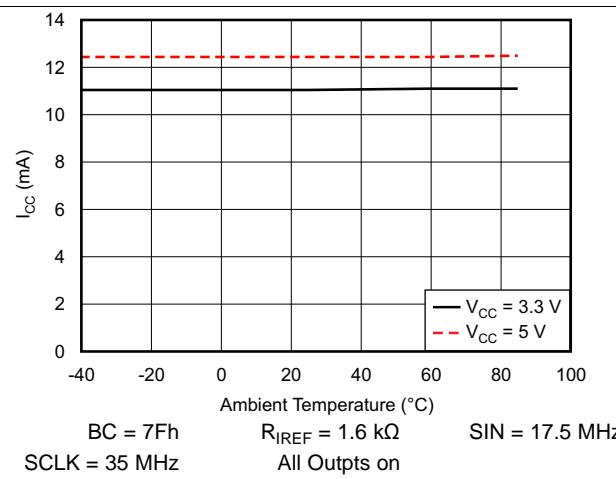


Figure 23. Supply Current vs Ambient Temperature

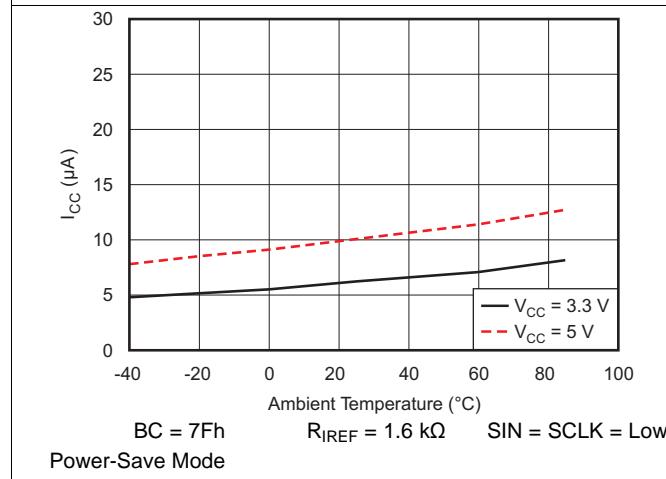


Figure 24. Supply Current in Power-Save Mode vs Ambient Temperature

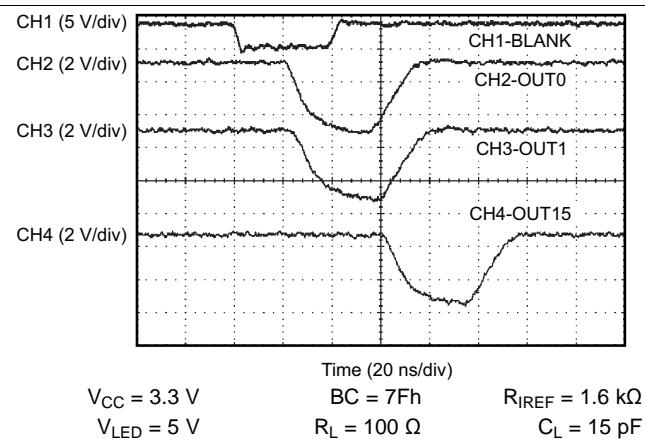
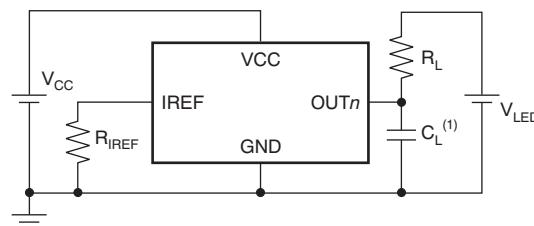


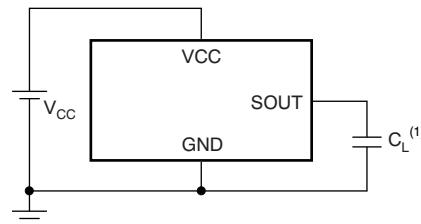
Figure 25. Constant-Current Output Voltage Waveform

7 Parameter Measurement Information



(1) C_L includes measurement probe and jig capacitance.

Figure 26. Rise Time and Fall Time Test Circuit for OUTn



(1) C_L includes measurement probe and jig capacitance.

Figure 27. Rise Time and Fall Time Test Circuit for SOUT

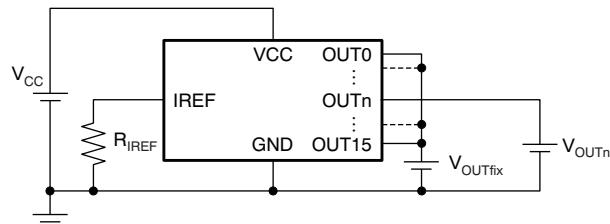


Figure 28. Constant-Current Test Circuit for OUTn

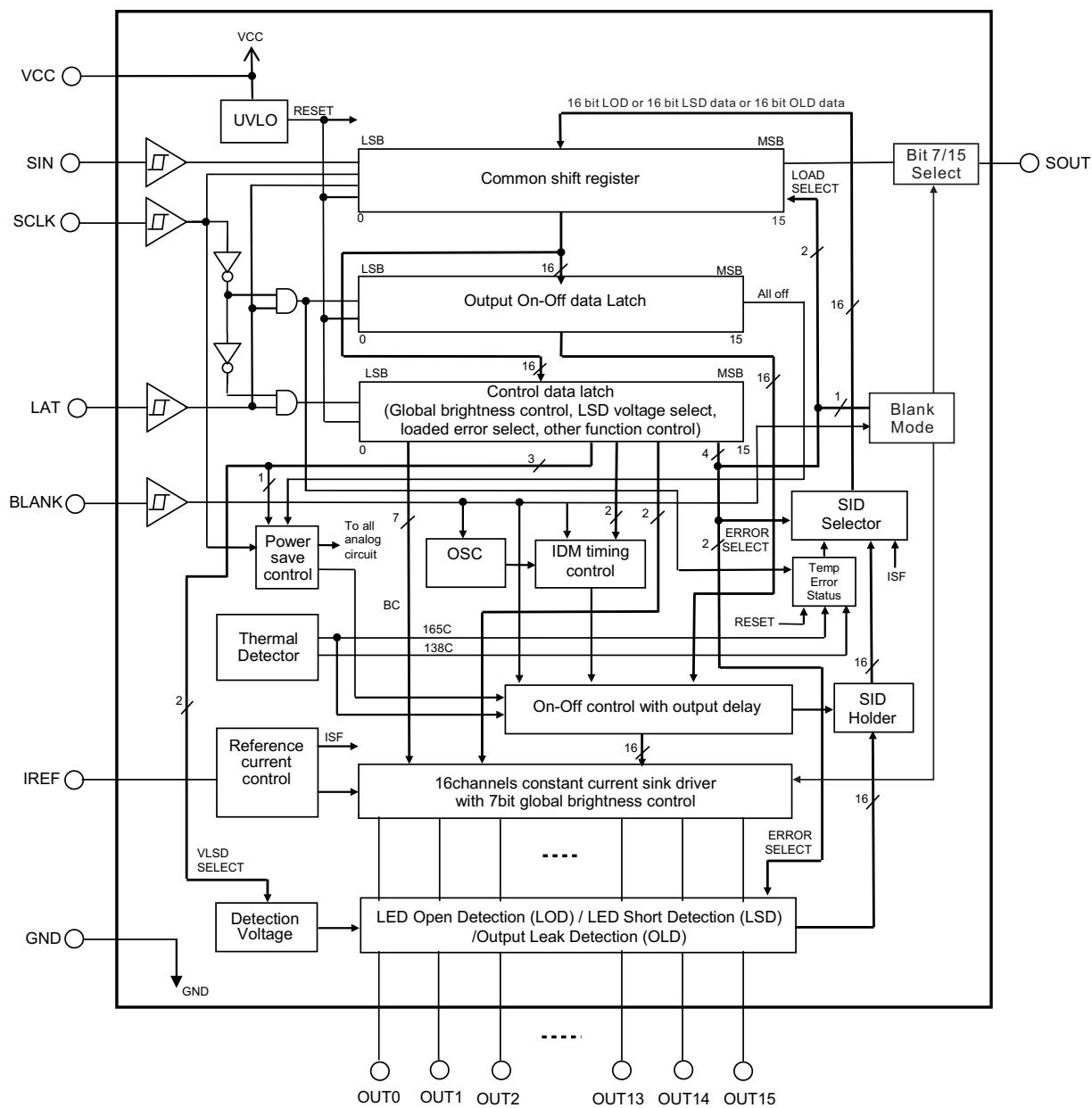
8 Detailed Description

8.1 Overview

The TLC59291 is a 8/16-channel constant current sink LED driver. Each channel can be turned on-off by writing data to an internal register. The constant current value of all 16 channels is set by a single external resistor and 128 steps for the global brightness control (BC).

The TLC59291 has six type error flags: LED open detection (LOD), LED short detection (LSD), output leak detection (OLD), reference terminal short detection (ISF), Pre thermal warning (PTW) and thermal error flag (TEF). In addition, the LOD and LSD functions have invisible detection mode (IDM) that can detect those errors even when the output is off. The error detection results can be read via a serial interface port.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Maximum Constant Sink Current

The maximum output current of each channel ($I_{O(LCmax)}$) is programmed by a single resistor (R_{IREF}) that is placed between the IREF and GND pins. The current value can be calculated by [Equation 1](#):

$$R_{IREF}(k\Omega) = \frac{V_{IREF}(V)}{I_{O(CL\max)}(mA)} \times 54.8$$

Where:

V_{IREF} = the internal reference voltage on IREF (typically 1.205 V when the global brightness control data are at maximum).

$I_{O(LCmax)}$ = 1 mA to 40 mA ($V_{CC} \leq 3.6$ V), or 1 mA to 50 mA ($V_{CC} > 3.6$ V) at OUT0 to OUT15 (BC = 7Fh) (1)

$I_{O(LCmax)}$ is the highest current for each output. Each output sinks $I_{O(LCmax)}$ current when it is turned on with the maximum global brightness control (BC) data. Each output sink current can be reduced by lowering the global brightness control value. R_{IREF} must be between 1.32 k Ω and 66 k Ω to hold $I_{O(LCmax)}$ between 50 mA (typical) and 1 mA (typical). Otherwise, the output may be unstable. Output currents lower than 1 mA can be achieved by setting $I_{O(LCmax)}$ to 1 mA or higher and then using the global brightness control to lower the output current.

[Figure 14](#) and [Table 1](#) show the characteristics of the constant-current sink versus the external resistor, R_{IREF} .

Table 1. Maximum Constant Current Output versus External Resistor Value

$I_{O(LCmax)}$ (mA)	R_{IREF} (k Ω , typ)
50 ($V_{CC} > 3.6$ V only)	1.32
45 ($V_{CC} > 3.6$ V only)	1.47
40	1.65
35	1.89
30	2.20
25	2.64
20	3.30
15	4.40
10	6.60
5	13.2
2	33
1	66

8.3.2 Global Brightness Control (BC) Function

The TLC59291 has the ability to adjust the output current of all constant current outputs simultaneously. This function is called *global brightness control* (BC). The global BC for all outputs (OUT0 to OUT15) can be set with a 7-bit word. The global BC adjusts all output currents in 128 steps from 0% to 100%, where 100% corresponds to the maximum output current set by R_{REF} . [Equation 2](#) calculates the actual output current. BC data can be set via the serial interface.

$$I_{O(LCn)}(\text{mA}) = \frac{I_{O(LCmax)}(\text{mA}) \times BC}{127d}$$

Where:

$I_{O(LCmax)}$ = the maximum constant-current value for each output determined by R_{REF} .

BC = the global brightness control value in the control data latch (0h to 127d) [\(2\)](#)

[Table 2](#) shows the BC data versus the constant-current ratio against $I_{O(LCmax)}$.

Table 2. BC Data versus Constant-Current Ratio Against $I_{O(LCmax)}$

BC DATA			RATIO OF OUTPUT CURRENT TO $I_{O(LCmax)}$ (%)	$I_{O(LC)}$ (mA, $I_{O(LCmax)} = 40\text{mA}$, typ)	$I_{O(LC)}$ (mA, $I_{O(LCmax)} = 1\text{mA}$, typ)
BINARY	DECIMAL	HEX			
000 0000	0	00	0	0	0
000 0001	1	01	0.8	0.31	0.01
000 0010	2	02	1.6	0.63	0.02
...
111 1101	125	7D	98.4	39.4	0.98
111 1110	126	7E	99.2	39.7	0.99
111 1111	127	7F	100.0	40.0	1.00

8.3.3 Thermal Shutdown (TSD) and Thermal Error Flag (TEF)

The thermal shutdown (TSD) function turns off all constant-current outputs when the junction temperature (T_J) exceeds the threshold ($T_{TEF} = 165^\circ\text{C}$, typical) and sets all LOD data bit to '1'. When the junction temperature drops below ($T_{TEF} - T_{HYST}$), the output control starts. The TEF is remains '1' until LAT is input even if low temperature. [Figure 6](#) shows a timing diagram and [Table 3](#) shows a truth table for TEF.

8.3.4 Pre-Thermal Warning (PTW)

The PTW function indicates that the IC junction temperature is high. The PTW is set and all LSD data bit are set to "1" while the IC junction temperature exceeds the temperature threshold ($T_{PTW} = 138^\circ\text{C}$, typical). Then OUTn are not forced off. When the PTW is set, the IC temperature should be reduced by lowering the power dissipated in the driver to avoid a forced shutdown by the thermal shutdown circuit. This reduction can be accomplished by lowering the values of the BC data. When the IC junction temperature decreases below the temperature of T_{PTW} , PTW is reset. [Figure 6](#) shows a timing diagram and [Table 3](#) shows a truth table for PTW.

8.3.5 Current Reference Terminal – IREF Terminal - Short Flag (ISF)

The ISF function indicates that IREF terminal is short to GND with low impedance. When IREF is set, all OLD data bit is set to “1”. Then all outputs (OUT n) are forced off and remain off until the short is removed. [Table 3](#) shows the truth table for ISF.

Table 3. TEF/PTW/ISF Truth Table

TEF	PTW	ISF	CORRESPONDING DATA BITS IN SID
Device temperature is lower than high-side detect temperature (temperature $\leq T_{TEF}$)	Device temperature is lower than pre-thermal warning temperature (temperature $\leq T_{PTW}$)	IREF terminal is not shorted	Depends on LOD/LSD/OLD
Device temperature is higher than high-side detect temperature and all outputs are forced off (temperature $> T_{TEF}$)	Device temperature is higher than pre-thermal warning temperature (temperature $> T_{PTW}$)	IREF terminal is shorted to GND with low impedance and all outputs (OUT0 to OUT15) are forced off	SID is all 1s for TEF when SIDLD bit = '01'. SID is all 1s for PTW when SIDLD = '10'. SID is all 1s for ISF when SIDLD = '11'.

8.3.6 Noise Reduction

Large surge currents may flow through the IC and the board on which the device is mounted if all 16 outputs turn on simultaneously when BLANK goes low or on-off data changes at LAT rising edge with BLANK low. These large current surges could induce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC59291 turns the outputs on in 2ns series delay for each output to provide a circuit soft-start feature.

8.4 Device Functional Modes

8.4.1 Blank Mode Selection (BLKMS)

The device has two configuration for BLANK pin, which is decided by BIT[9] in FC register. When BLANK mode = 1, the device is in ENABLE mode, BLANK pin is worked as OUTPUT enable pin: when BLANK=Low, all constant current outputs are controlled by the on/off control data in the data latch; when BLANK=High, all OUTx are forced off.

When BLANK mode = 0, the device is in SOUT mode, BLANK pin is worked as SOUT select pin; when BLANK= Low, SOUT is connected to the bit7 of the 16-bit shift register, worked as 8 channel device; when BLANK= High, SOUT is connected to the bit15 of the 16-bit shift register, worked as 16ch device. If device is already in ENABLE mode and we want to switch to SOUT mode, the new FC data with BIT[9]=0 must be input. Then it enter SOUT mode.

If device is already in SOUT mode and the user wants to switch to ENABLE mode. First make sure BLANK pin is high, SOUT is connected with bit15 of common shift register. Then input the new FC data with BIT[9] = 1. The device enters ENABLE mode

When the IC is powered on, SOUT mode is selected as default value. Refer to table 7 for detail.

8.4.2 Power-Save Mode

In this mode, the device dissipation current becomes 30 μ A (typical). When “PSMODE” bit is ‘1’, the power save mode is enabled. Then if LAT rising edge is input to write all ‘0’ data into the output on-off data latch or to write any data into the control data latch when the on-off data latch are all ‘0’, TLC5929 goes into the power save mode. When SCLK rising edge is input, the device returns to normal operation. The power-save mode timing is shown in [Figure 7](#).

8.4.3 LED Open Detection (LOD)

LOD detects the fault caused by LED open circuit or a short from OUT n to ground by comparing the OUT n voltage to the LOD detection threshold voltage level ($V_{LOD} = 0.3$ V typical). If the OUT n voltage is lower than V_{LOD} , that output LOD bit is set to '1' to indicate an open LED. Otherwise, the LOD bit is set to '0'. LOD data are only valid for outputs programmed to be on. LOD data for outputs programmed to be off are always '0' ([Table 11](#)).

The LOD data are stored into a 16-bit register called SID holder at BLANK rising edge when “SIDLD” bits is set to ‘01b’ ([Table6](#)) or when [Invisible Detection Mode \(IDM\)](#) is enabled, the LOD data are stored to SID holder at the end timing of IDM working time.

The stored LOD data can be read out through the common shift register as [Status Information Data \(SID\)](#) from SOUT pin. LOD/LSD data are not valid until 0.5 μ s after the falling edge of BLANK.

8.4.4 LED Short Detection (LSD)

LSD data detects the fault caused by a shorted LED by comparing the OUT n voltage to the LSD detection If the OUT n voltage is higher than the programmed voltage, that output LSD bit is set to '1' to indicate a shorted LED. Otherwise, the LSD bit is set to '0'. LSD data are only valid for outputs programmed to be on. LSD data for outputs programmed to be off are always '0' ([Table 4](#)).

The LSD data are stored into a 16-bit register called SID holder at BLANK rising edge when “SIDLD” bits is set to ‘10b’ ([Table6](#)) or when [Invisible Detection Mode \(IDM\)](#) is enabled, the LSD data are stored to SID holder at the end timing of IDM working time. The stored LSD data can be read out through the common shift register as [Status Information Data \(SID\)](#) from SOUT pin. LOD/LSD data are not stabled until 0.5 μ s after the falling edge of BLANK. Therefore, BLANK must be low for at least that time.

The LSD need to be executed after propagation delay, “ t_{d4} ” or more from the device operation resumed from the power save mode because LOD does not work during the power save mode.

Device Functional Modes (continued)

8.4.5 Invisible Detection Mode (IDM)

Invisible Detection Mode (IDM) is the mode which can detect LOD and LSD when output on-off data is set to off state. When “IDMCUR” bit in the control data latch are set any data except “00b”, OUTn start to sink the current set by the “IDMCUR” bit at BLANK falling edge and OUTn stop to sink the current at BLANK rising signal or the time set by “IDMTIM” has passed. When OUTn is stopped, the selected SID data by “SIDLD” bit are latched to into SID holder.

When IDM mode is enabled, OLD is always set to disable. When “IDMCUR” bit in the control data latch is set “00b”, OUTn doesn't start to sink the current set. [Figure 29](#) shows LOD/LSD/OLD/IDM circuit. [Figure 8](#) shows IDM operation timing and [Table 5](#) shows a truth table for LOD/LSD/OLD.

IDM can only be working when FC[9] = 1.

8.4.6 Output Leakage Detection (OLD)

Output leak detection (OLD) detects a fault caused by OUTn is short to GND with high resistance by comparing the OUTn voltage to the LSD detection threshold voltage when output on-off data is set to off state. Also OLD can detect the short between adjacent pins. Small current is sourced from OUTn turned off to LED to detect LED leaking when “SIDLD” bit are ‘11b’ and BLANK is low. OLD operation is disabled when SIDLD bit are set any data except “11b” and then the sourced current is stopped. Also OLD is disabled when [Invisible Detection Mode \(IDM\)](#) is enabled. If the OUTn voltage is lower than the programmed LSD threshold voltage, that output OLD bit is set to ‘1’ to indicate a leaking LED. Otherwise, the OLD bit is set to ‘0’. OLD result is valid for outputs programmed to off only. The OLD data is latched into SID holder when BLANK goes high. OLD data for outputs not programmed to off are always ‘0’. The OLD need to be executed after propagation delay, “td4” or more from the device operation resumed from the power save mode because OLD does not work during the power save mode.

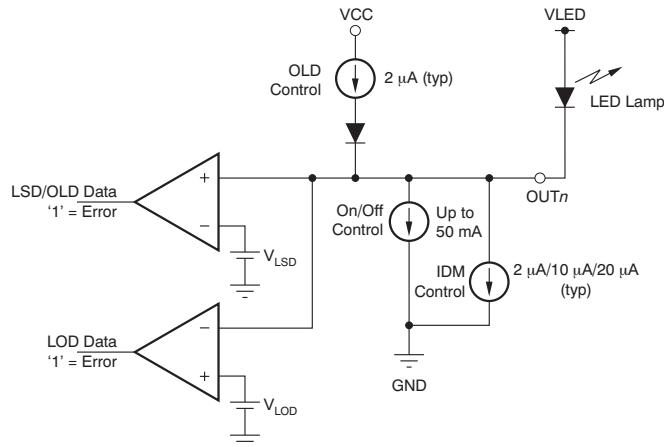


Figure 29. LOD/LSD/OLD/IDM Circuit

8.4.7 Status Information Data (SID)

The status information data (SID) contains the status of the [LED Open Detection \(LOD\)](#), [LED Short Detection \(LSD\)](#), [Output Leakage Detection \(OLD\)](#), [Pre-Thermal Warning \(PTW\)](#), [Thermal Shutdown \(TSD\)](#) and [Thermal Error Flag \(TEF\)](#) and [Current Reference Terminal – IREF Terminal - Short Flag \(ISF\)](#). The loaded SID data can be selected by “SIDLD” bits in the control data latch. When the MSB of the common shift register is set to ‘0’, the selected SID overwrites lower 16-bit data in the common shift register data at the rising edge of LAT after the data in the common shift register are copied to the output on-off data latch. If the common shift register MSB is ‘1’, the selected SID does not overwrite the 16-bit data in the common shift register.

Device Functional Modes (continued)

After being copied into the common shift register, new SID data are not available until new data are written into the common shift register. If new data are not written, the LAT signal is ignored. To recheck SID without changing the on-off control data, reprogram the common shift register with the same data currently programmed into the on-off data latch. When LAT goes high, the output on-off data is not changed, but new SID data are loaded into the common shift register. LOD, LSD, OLD, PTW, TEF, ISF are shifted out of SOUT with each rising edge of SCLK. The SID need to be read out after t_{d4} or more from the device operation resumed from the power save mode.

The SID reading must be delayed for a duration of t_{d4} or more after the device resumes operation from the power-save mode because SID does not indicate correct data during the power-save mode. The SID load configuration and SID read timing are shown in [Figure 10](#) and [Figure 30](#), respectively.

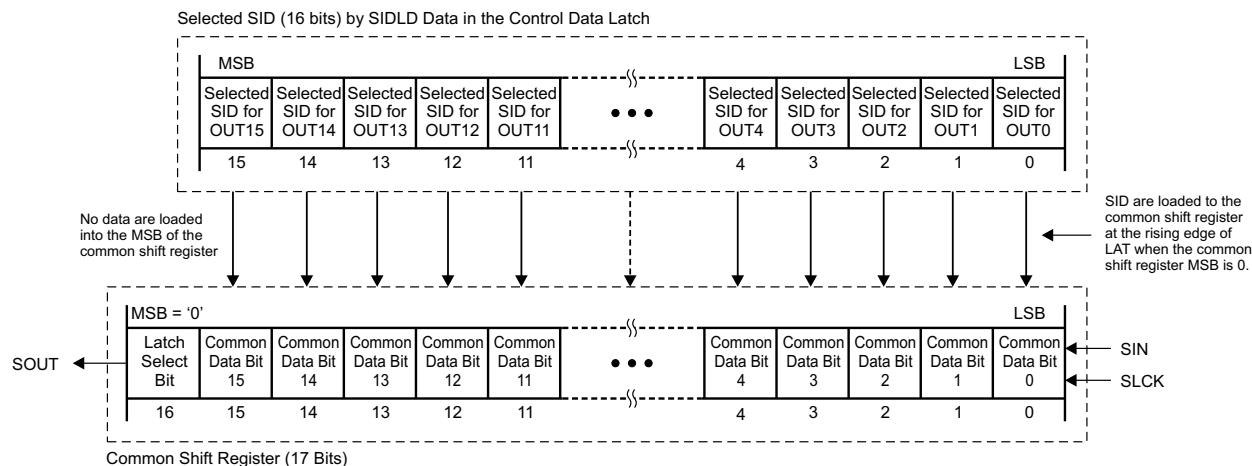


Figure 30. SID Load Configuration

Table 4. SID Load Assignment

SIDLD 1/0 BIT	SELECTED DETECTOR	CHECKED OUT n	BIT NUMBER LOADED INTO COMMON SHIFT REGISTER	DESCRIPTION
00b	No detector selected	—	No data loaded	
01b	LED open detection (LOD)	OUT0	0	The data in the common shift register are not changed. The data in the common shift register are updated with LOD or TEF data. All bits '1' = device junction temperature (T_J) is high ($T_J > T_{TEF}$) and all outputs are forced off by the thermal shutdown function. '1' = OUT n shows lower voltage than the LED open detection threshold (V_{LOD}). 0 = normal operation.
		OUT1	1	
		
		OUT14	14	
		OUT15	15	
10b	LED short detection (LSD)	OUT0	0	The data in the common shift register are updated with LSD or PTW data. All bits '1' = device junction temperature (T_J) is high ($T_J > T_{PTW}$). 1 = OUT n shows higher voltage than the LED short detection threshold (V_{LSD}) selected by LSDVLT. 0 = normal operation.
		OUT1	1	
		
		OUT14	14	
		OUT15	15	
11b	Output leakage detection (OLD)	OUT0	0	The data in the common shift register are updated with OLD or ISF data. All bits '1' = IREF pin is shorted to GND with low impedance. 1 = OUT n is leaking to GND with greater than 3 μ A. 0 = normal operation.
		OUT1	1	
		
		OUT14	14	
		OUT15	15	

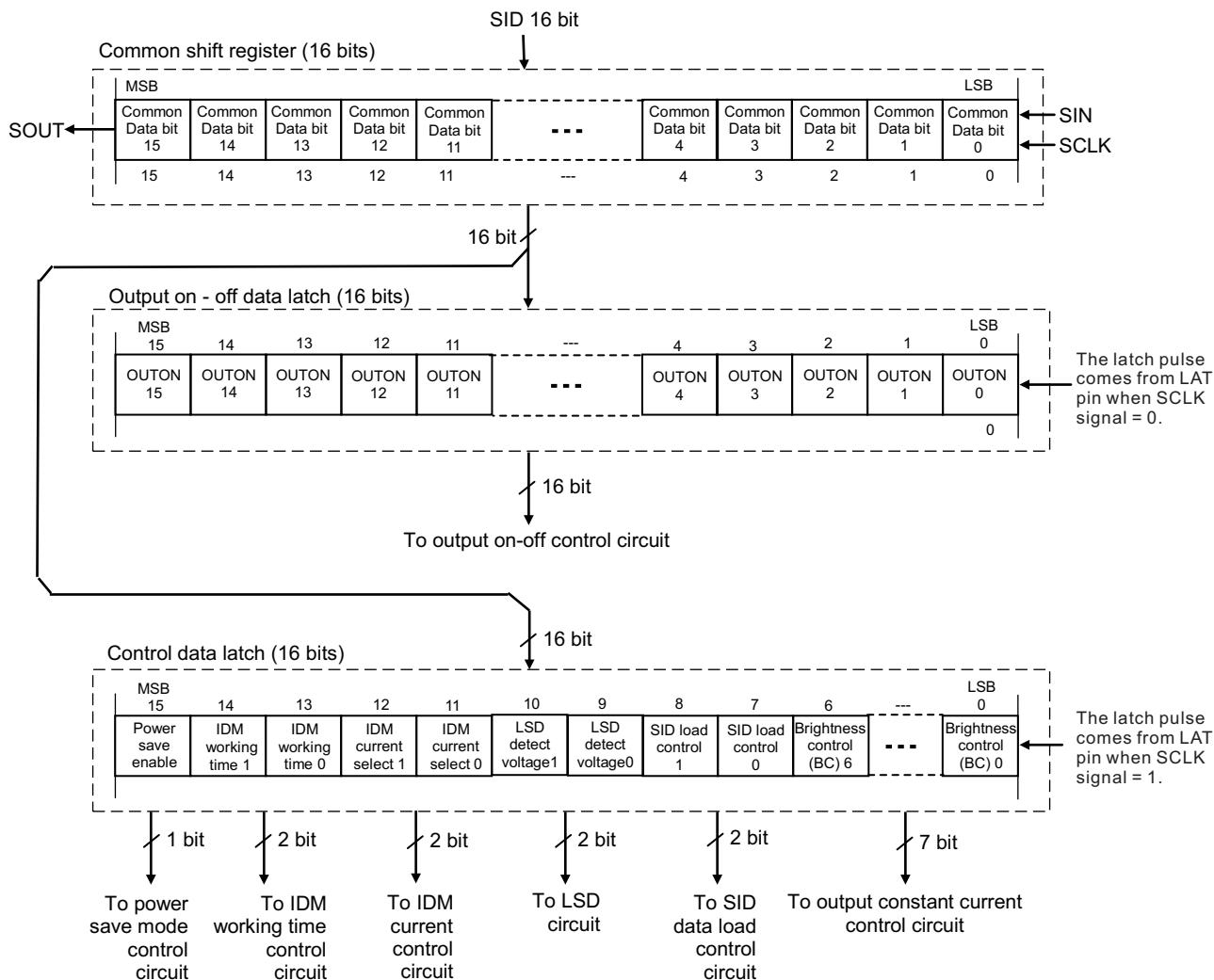
Table 5. LOD/LSD/OLD Truth Table

LOD	LSD	OLD	CORRESPONDING BIT IN SID
LED is not opened ($V_{OUTn} > V_{LOD}$)	LED is not shorted ($V_{OUTn} \leq V_{LSD}$)	$OUTn$ does not leak to GND ($V_{OUTn} > V_{LSD}$ when constant-current output off and $OUTn$ source current on)	0
LED is open or shorted to GND ($V_{OUTn} \leq V_{LOD}$)	LED is shorted between anode and cathode, or shorted to higher voltage side ($V_{OUTn} > V_{LSD}$)	Current leaks from $OUTn$ to internal GND, or $OUTn$ is shorted to external GND with high impedance ($V_{OUTn} \leq V_{LSD}$ when constant-current output off and $OUTn$ source current on)	1

8.5 Register Maps

8.5.1 Register and Data Latch Configuration

The TLC59291 has one common shift register and two control data latch. The common shift register is 16-bits in length and two control data latch is 16-bits length. When SCLK is '0' at LAT rising edge, the 16-bits common shift register are copied into the output on-off data latch. Also when SCLK is '1' at LAT rising edge the 16-bits data are copied into the control data latch. [Figure 31](#) shows the common shift register and two control data latches configuration.


Figure 31. Common Shift Register and Control Data Latches Configuration

Register Maps (continued)

8.5.1.1 Common Shift Register

The 16-bit common shift register is used to shift data from the SIN pin into the TLC59291. The data shifted into the register are used for the data writing for output on-off control, global brightness control, and some functions control. The register LSB is connected to SIN. On each SCLK rising edge, the data on SIN are shifted into the register LSB and all bits are shifted towards the MSB.

SOUT can be connected to either bit 15 or bit 7 of common shift register depending on BLANK signal and control data setting.

Also Status Information Data (SID) selected by the load select data in the control data latch are loaded to the common shift register when LAT rising edge is input with SCLK is "0" of the shift register.

When the device powered up, the data in the 16-bit common shift register is set to all "0".

8.5.1.2 Output On/Off Data Latch

The output on/off data latch is 16 bits long and sets the on or off status for each constant-current output.

When FC[9] = 1 and BLANK is high, all outputs are forced off. But then the data in the latch are not changed. In other case, the corresponding output is turned on if the data in the output on-off data latch are '1' and remains off if the data are '0'.

When the IC is initially powered on, the data in the data latch is set to all "0".

The output on/off data latch configuration is shown in [Figure 32](#) and the data bit assignment is shown in [Table 6](#).

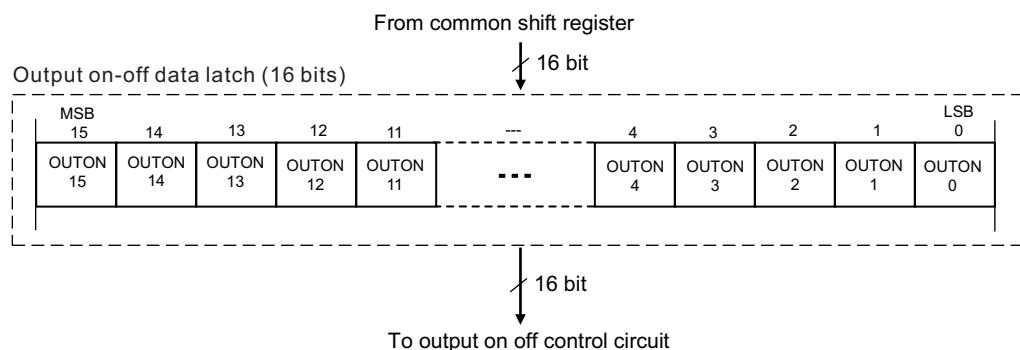


Figure 32. Output On/Off Data Latch Configuration

Table 6. On/Off Control Data Latch Bit Assignment

BIT NUMBER	BIT NAME	CONTROLLED CHANNEL
0	OUTON0	OUT0
1	OUTON1	OUT1
2	OUTON2	OUT2
...
13	OUTON13	OUT13
14	OUTON14	OUT14
15	OUTON15	OUT15

Figure 33. Output On/Off Data Latch

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Output On/Off Data Latch

Bit	Field	Type	Reset	Description
[15]	OUTON15	R/W	00	
[14]	OUTON14	R/W	00	
[13]	OUTON13	R/W	00	
[12]	OUTON12	R/W	00	
[11]	OUTON11	R/W	00	
[10]	OUTON10	R/W	00	
[9]	OUTON9	R/W	00	
[8]	OUTON8	R/W	00	
[7]	OUTON7	R/W	00	
[6]	OUTON6	R/W	00	
[5]	OUTON5	R/W	00	
[4]	OUTON4	R/W	00	
[3]	OUTON3	R/W	00	
[2]	OUTON2	R/W	00	
[1]	OUTON1	R/W	00	
[0]	OUTON0	R/W	00	

When IC is powered up, these all data are set to "0"
 0 = output OFF (default)
 1 = output ON

8.5.1.3 Control Data Latch

The control data latch is 16-bit in length and contains the *Global Brightness Control (BC) Function* data, *Status Information Data (SID)* load select data, *Blank Mode Selection (BLKMS)* data, the current value for *Invisible Detection Mode (IDM)*, IDM working time, and *Power-Save Mode* enable control data.

When the device is powered up, the data in this data latch are set to the default values shown in [Table 8](#).

The function control data latch configuration is shown in [Figure 34](#).

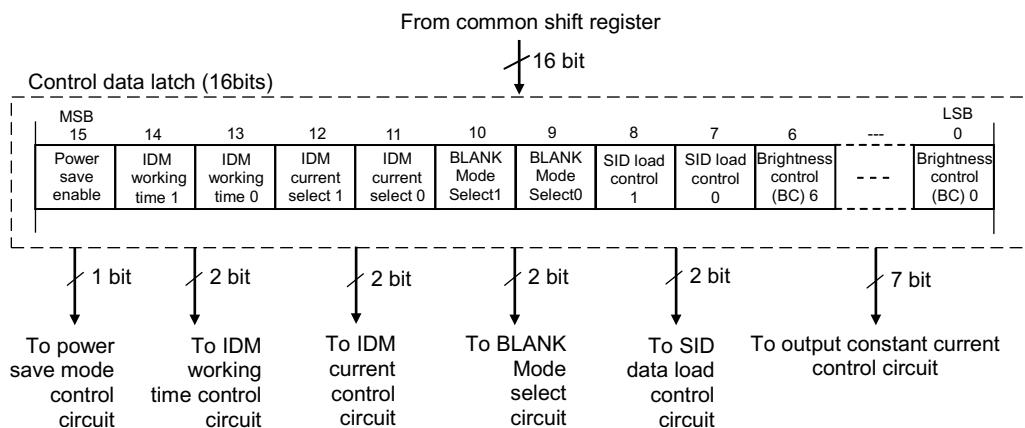

Figure 34. Function Control Data Latch Configuration

Figure 35. Control Data Latch

15	14	13	12	11	10	9	8
1	0	0	0	0	1	0	0
R/W							
7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. Control Data Latch

Bit	Field	Type	Reset	Description
[15]	PSMODE	R/W	1b	Power save mode enable (Default value = '1b') The data selects power save mode enable or disable. When the mode is enabled, the device goes into power save mode if all data in the on/off data latch are "0". Table 15 shows the power save mode truth table. Figure 7 shows the power save mode operation timing.
[14:13]	IDMTIM	R/W	00b	IDM working time select (Default value = '00b') The data selects the time of output current sink at OUTn for IDM to detect LED open detection (LOD) or LSD without visible lighting. Table 15 shows the work time truth table. Figure 9 shows the IDM operation timing.
[12:11]	IDMCUR	R/W	00b	IDM current select (Default value = '00b') The data selects the sink current at OUTn for IDM to detect LED open detection (LOD) or LSD without visible lighting. Table 14 shows the current value truth table. Figure 9 shows the IDM operation timing.
[10]	LSDVLT	R/W	1b	LSD detection voltage select. (Default value = '1b') These two bits select the detection threshold voltage for the LED short detection (LSD). Table 12 shows the detect voltage truth table.
[9]	BLKMS	R/W	0b	BLANK Mode Select (Default value = '0b') The data selects the working mode for BLANK pin. Table 11 shows the truth table.
[8:7]	SIDLD	R/W	00b	SID load control (Default value = '00b') The data selects the SID data loaded to the common register when LAT pulse is input for on-off data writing. Table 10 shows the selected data truth table.
[6:0]	BCALL	R/W	1111111b	Global brightness control (Default value = '1111111b') The 7-bit data controls the current of all output with 128 steps between 0–100% of the maximum current value set by a external resistor. Table 13 shows the current value truth table.

8.5.1.4 Output On/Off Data Write Timing and Output Control

When SCLK = "0" at LAT rising edge, the output on/off data can be updated with the 16-bit data in the shift register after the data are stored to the shift register using SIN and SCLK signals. When the on/off data latch is updated, SID is loaded into the shift register except SID load control is "00b". See [Figure 11](#).

When BLANK = SOUT mode, the timing is show in [Figure 12](#).

8.5.1.5 Function Control Data Writing

When SCLK = "1" at LAT rising edge, the control data latch can be updated with the 16-bit data in the shift register after the data are stored to the shift register using SIN and SCLK signals. When the control data latch is updated, SID is not loaded into the shift register.

If the device is in SOUT mode (FC[9] = 0) and BLANK = Low, SOUT is connected with BIT 7 of common shift register. Then FC data can't be input and not valid. See [Figure 13](#)

8.5.1.6 Function Control (FC) Data

The FC data latch is 16 bits long and is used to adjust output current values for LED brightness, select the SID, BLANK mode select, the output current for IDM, the output on time for IDM, and power-save mode enable/disable. When the IC is powered on, the control data latch is set to the default value (E67Fh). The control data latch truth tables are shown in [Table 9](#) through [Table 14](#).

Table 9. Global Brightness Control (BC) Truth Table

BCALL (BIT 6:0)		Brightness Control for all Output with Output Current
0000000		Output current of OUT n is set to $I_{O(LCmax)} \times 0\%$
0000001		$I_{O(LCmax)} \times 0.8\%$
...		...
1111110		$I_{O(LCmax)} \times 99.2\%$
1111111		$I_{O(LCmax)} \times 100\%$

Table 10. SID Load Control Truth Table

SIDLD		SID LOADED TO THE COMMON SHIFT REGISTER
BIT 8	BIT 7	
0	0	No data is loaded (default value)
0	1	LED open detection (LOD) or thermal error flag (TEF) data are loaded
1	0	LED short detection (LSD) or pre-thermal warning (PTW) data are loaded
1	1	Output leakage detection (OLD) or IREF pin short flag (ISF) data are loaded

Table 11. BLANK Mode Selection Table

BLKMS (BIT 9)		BLANK MODE SELECTION
0		SOUT mode, BLANK pin worked as SOUT 8/16 select signal (default)
1		Enable mode, BLANK pin worked as OUTPUT enable

Table 12. LSD Threshold Voltage Truth Table

LSDVLT (BIT 10)		LED SHORT DETECTION (LSD) THRESHOLD VOLTAGE
0		$V_{LSD0} (0.35 \times V_{CC} \text{ typ})$
1		$V_{LSD3} (0.65 \times V_{CC} \text{ typ, default value})$

Table 13. Current Select for IDM

IDMCUR		SINK CURRENT AT OUT n FOR INVISIBLE DETECTION MODE (IDM)
BIT 12	BIT 11	
0	0	IDM is disabled (default value)
0	1	2 μA (typ)
1	0	10 μA (typ)
1	1	20 μA (typ)

Table 14. IDM Work-Time Truth Table

IDMTIM		INVISIBLE DETECTION MODE (IDM) WORKING TIME
BIT 14	BIT 13	
0	0	All outputs are turned on for 17 OSC clocks (0.85 μs typ)
0	1	All outputs are turned on for 33 OSC clocks (1.65 μs typ)
1	0	All outputs are turned on for 65 OSC clocks (3.25 μs typ)
1	1	All outputs are turned on for 129 OSC clocks (6.45 μs typ, default value)

Table 15. Power-Save Mode Truth Table

PSMODE (BIT 15)	POWER-SAVE MODE FUNCTION
0	Power-save mode is disabled. The device does not go into power-save mode even if the bits in the output on/off data latch are all '0'.
1	Power save mode is enabled (default value). The device goes into power-save mode when the bits in the output on/off data latch are all '0'.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The device is a 8/16-channel, constant sink current, LED driver. This device is typically connected in series to drive many LED lamps with only a few controller ports. On/Off control data and FC control data can be written from the SIN input terminal. The device has six type error flags: LED open detection (LOD), LED short detection (LSD), output leak detection (OLD), reference terminal short detection (ISF), Pre thermal warning (PTW) and thermal error flag (TEF).

9.2 Typical Application

In this application, the device VCC and LED lamp anode voltages are supplied from different power supplies.

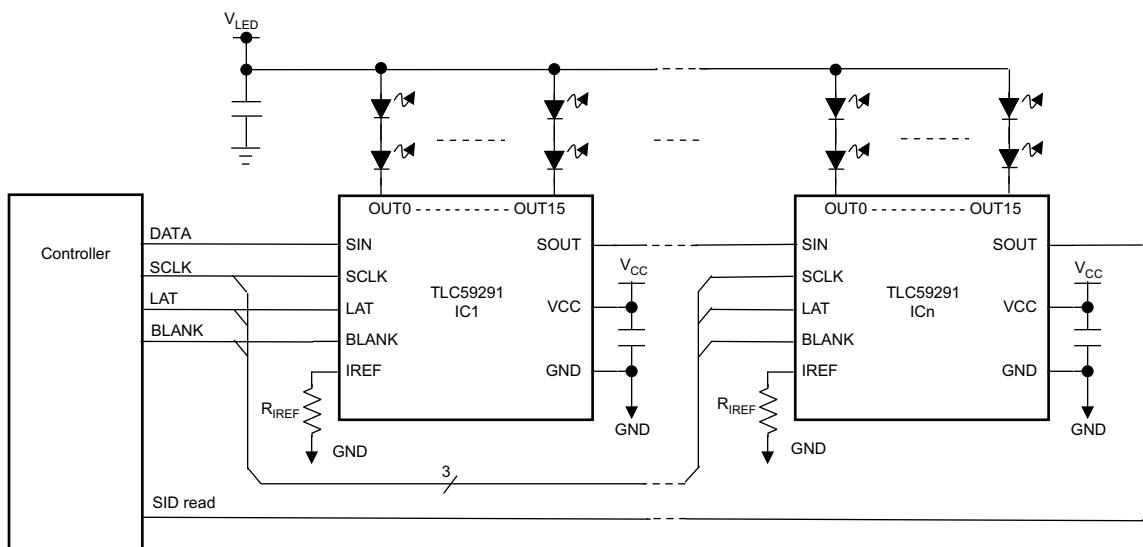


Figure 36. Multiple Daisy-chained TLC59291 Devices

9.2.1 Design Requirements

The parameters for the design example are shown in [Table 16](#).

Table 16. Design Parameters

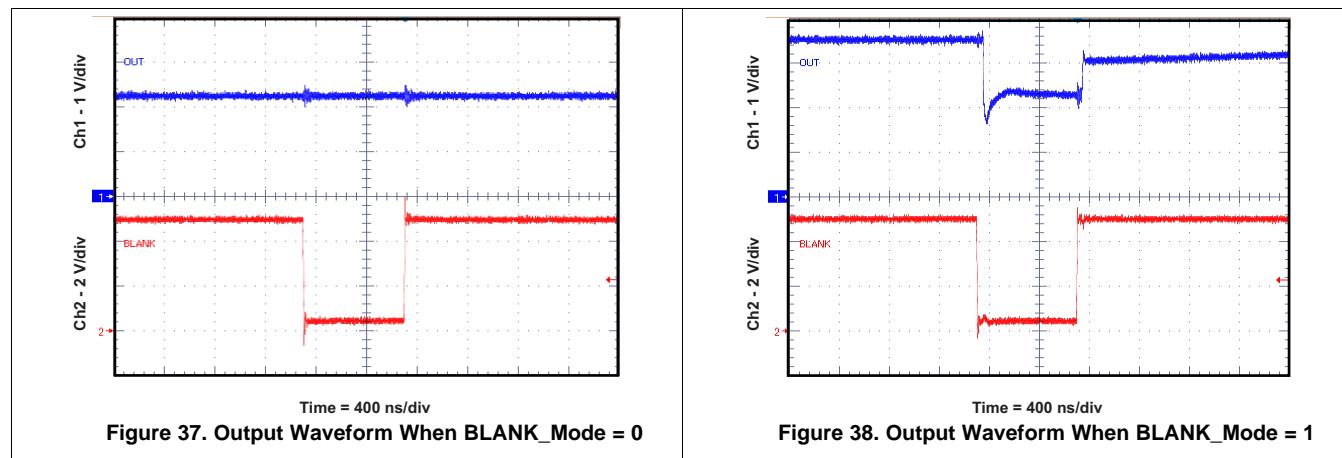
PARAMETER	VALUE
VCC input voltage range	3 V to 5.5 V
LED lamp (V_{LED}) input voltage range	Maximum LED forward voltage (V_F) + 0.3 V (knee voltage)
SIN, SCLK, LAT, and GSCLK voltage range	Low level = GND, High level = V_{CC}

9.2.2 Detailed Design Procedure

To begin the design process, a few parameters must be decided upon. The designer needs to know the following:

- Maximum output constant-current value for each color LED lamp.
- Maximum LED forward voltage (V_F).
- Which error flags are used.

9.2.3 Application Curves



10 Power Supply Recommendations

The VCC power supply voltage should be decoupled by placing a 0.1- μ F ceramic capacitor close to the VCC pin and GND plane. Depending on the panel size, several electrolytic capacitors must be placed on the board equally distributed to get a well regulated LED supply voltage (V_{LED}). The V_{LED} voltage ripple must be less than 5% of its nominal value. Furthermore, the V_{LED} must be set to the voltage calculated by [Equation 3](#).

$$V_{LED} > V_F + 0.4 \text{ V} \quad (10\text{-mA constant-current example}) \quad (3)$$

Where

- V_F = maximum forward voltage of all LEDs.

11 Layout

11.1 Layout Guidelines

- Place the decoupling capacitor near the VCC pin and GND plane
- Place the current programming resistor R_{REF} close to the IREF pin and the IREFGND pin.
- Route the GND pattern as widely as possible for large GND currents.
- The routing wire between the LED cathode side and the device OUTXn pin must be as short and straight as possible to reduce wire inductance.
- When several ICs are chained, symmetric placements are recommended.

11.2 Layout Example

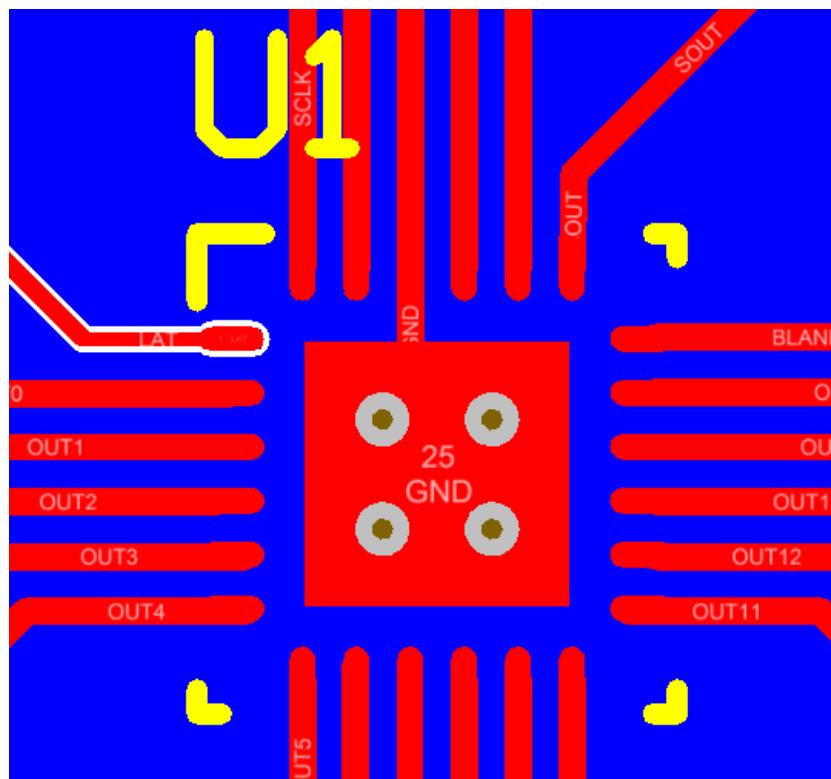


Figure 39. Layout

12 器件和文档支持

12.1 文档支持

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

E2E is a trademark of Texas Instruments.

12.4 静电放电警告

 这些装置包含有限的内置 ESD 保护。 存储或装卸时, 应将导线一起截短或将装置放置于导电泡棉中, 以防止 MOS 门极遭受静电损伤。

12.5 Glossary

[SLYZ022](#) — *TI Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本, 请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 **JESD46** 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改, 并有权根据 **JESD48** 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的**TI** 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 **TI** 半导体产品销售条件与条款的适用规范。仅在 **TI** 保证的范围内, 且 **TI** 认为有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定, 否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 **TI** 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险, 客户应提供充分的设计与操作安全措施。

TI 不对任何 **TI** 专利权、版权、屏蔽作品权或其它与使用了 **TI** 组件或服务的组合设备、机器或流程相关的 **TI** 知识产权中授予的直接或隐含权限作出任何保证或解释。**TI** 所发布的与第三方产品或服务有关的信息, 不能构成从 **TI** 获得使用这些产品或服务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可, 或是 **TI** 的专利权或其它知识产权方面的许可。

对于 **TI** 的产品手册或数据表中 **TI** 信息的重要部分, 仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。**TI** 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 **TI** 组件或服务时, 如果对该组件或服务参数的陈述与 **TI** 标明的参数相比存在差异或虚假成分, 则会失去相关 **TI** 组件或服务的所有明示或暗示授权, 且这是不正当的、欺诈性商业行为。**TI** 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意, 尽管任何应用相关信息或支持仍可能由 **TI** 提供, 但他们将独自负责满足与其产品及在其应用中使用 **TI** 产品相关的所有法律、法规和安全相关要求。客户声明并同意, 他们具备制定与实施安全措施所需的全部专业技术和知识, 可预见故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因在此类安全关键应用中使用任何 **TI** 组件而对 **TI** 及其代理造成任何损失。

在某些场合中, 为了推进安全相关应用有可能对 **TI** 组件进行特别的促销。**TI** 的目标是利用此类组件帮助客户设计和创立其特有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此, 此类组件仍然服从这些条款。

TI 组件未获得用于 **FDA Class III** (或类似的生命攸关医疗设备) 的授权许可, 除非各方授权官员已经达成了专门管控此类使用的特别协议。

只有那些 **TI** 特别注明属于军用等级或“增强型塑料”的 **TI** 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同意, 对并非指定面向军事或航空航天用途的 **TI** 组件进行军事或航空航天方面的应用, 其风险由客户单独承担, 并且由客户独自负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 **ISO/TS16949** 要求的产品, 这些产品主要用于汽车。在任何情况下, 因使用非指定产品而无法达到 **ISO/TS16949** 要求, **TI** 不承担任何责任。

产品	应用
数字音频	www.ti.com.cn/audio
放大器和线性器件	www.ti.com.cn/amplifiers
数据转换器	www.ti.com.cn/dataconverters
DLP® 产品	www.dlp.com
DSP - 数字信号处理器	www.ti.com.cn/dsp
时钟和计时器	www.ti.com.cn/clockandtimers
接口	www.ti.com.cn/interface
逻辑	www.ti.com.cn/logic
电源管理	www.ti.com.cn/power
微控制器 (MCU)	www.ti.com.cn/microcontrollers
RFID 系统	www.ti.com.cn/rfidsys
OMAP应用处理器	www.ti.com/omap
无线连通性	www.ti.com.cn/wirelessconnectivity
	德州仪器在线技术支持社区 www.deyisupport.com

邮寄地址: 上海市浦东新区世纪大道1568号, 中建大厦32楼邮政编码: 200122

Copyright © 2016, 德州仪器半导体技术(上海)有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC59291RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 59291	Samples
TLC59291RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 59291	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



www.ti.com

PACKAGE OPTION ADDENDUM

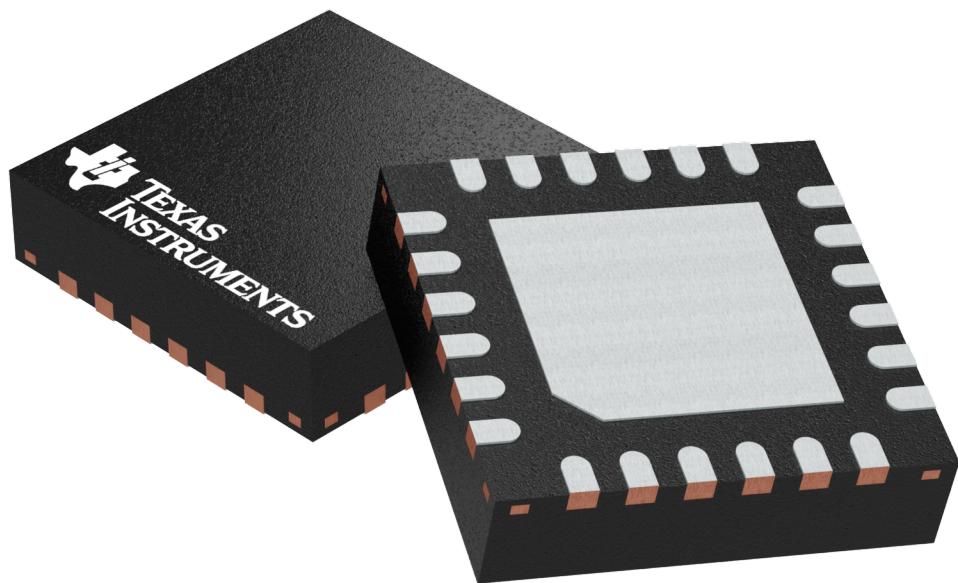
10-Dec-2020

GENERIC PACKAGE VIEW

RGE 24

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

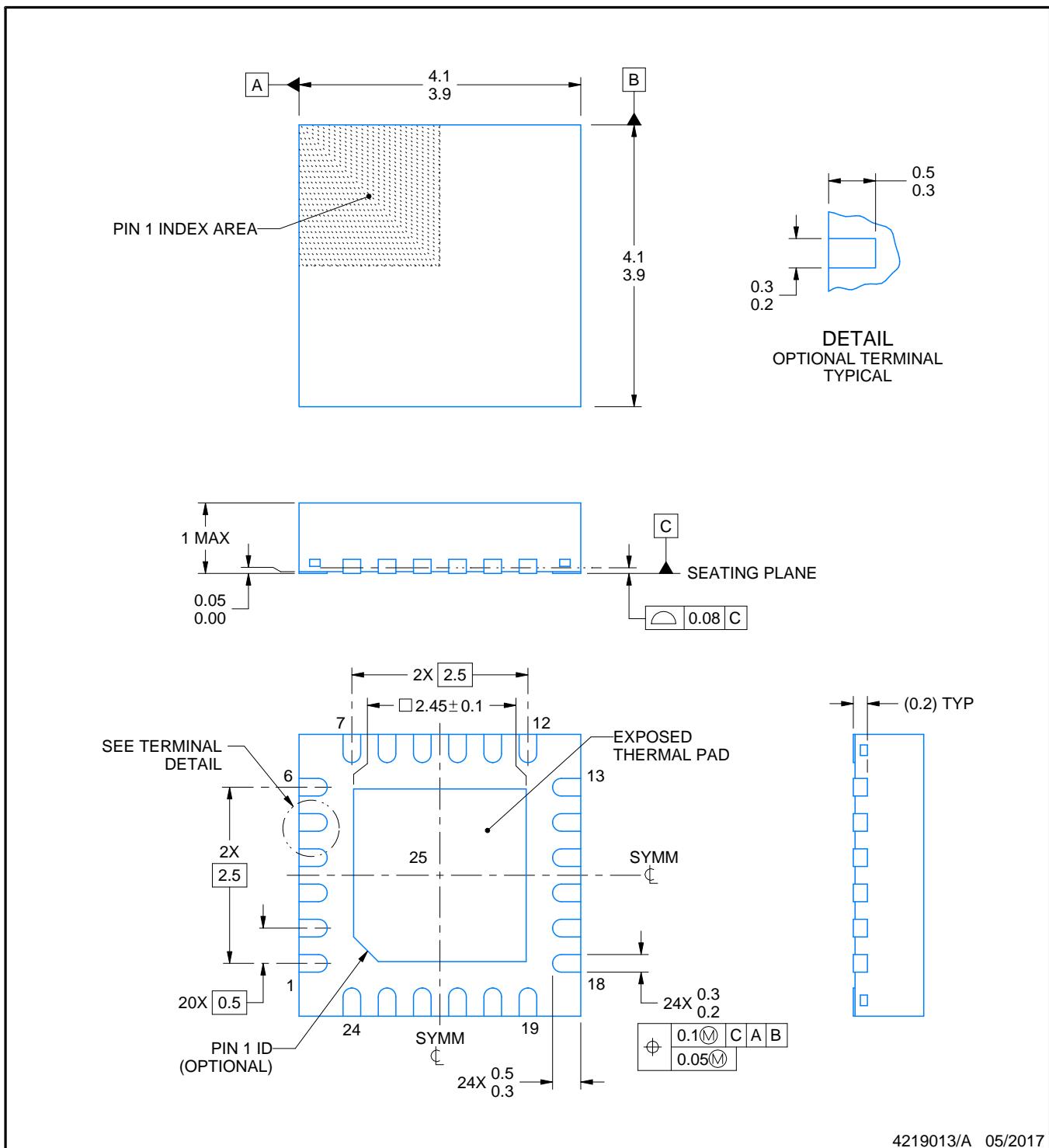
RGE0024B



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

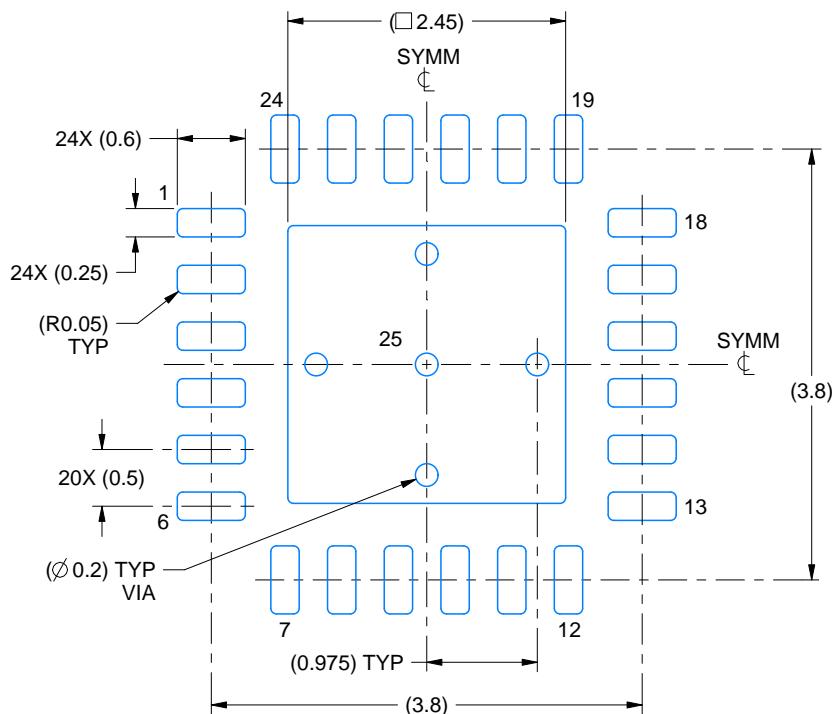
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

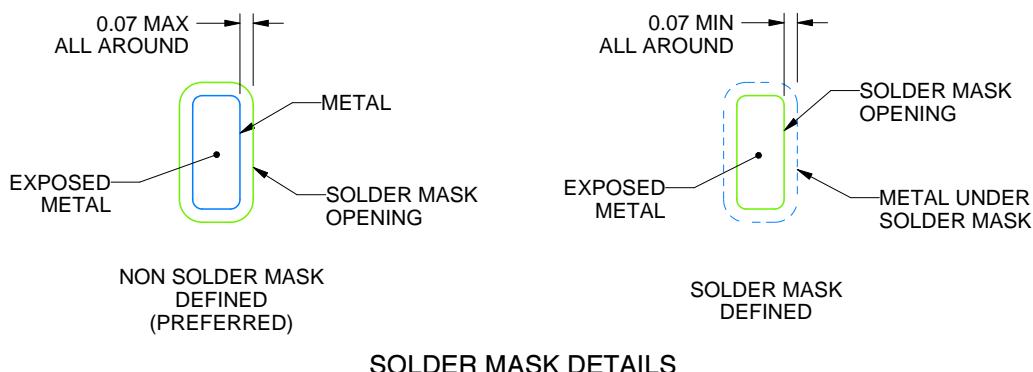
RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



4219013/A 05/2017

NOTES: (continued)

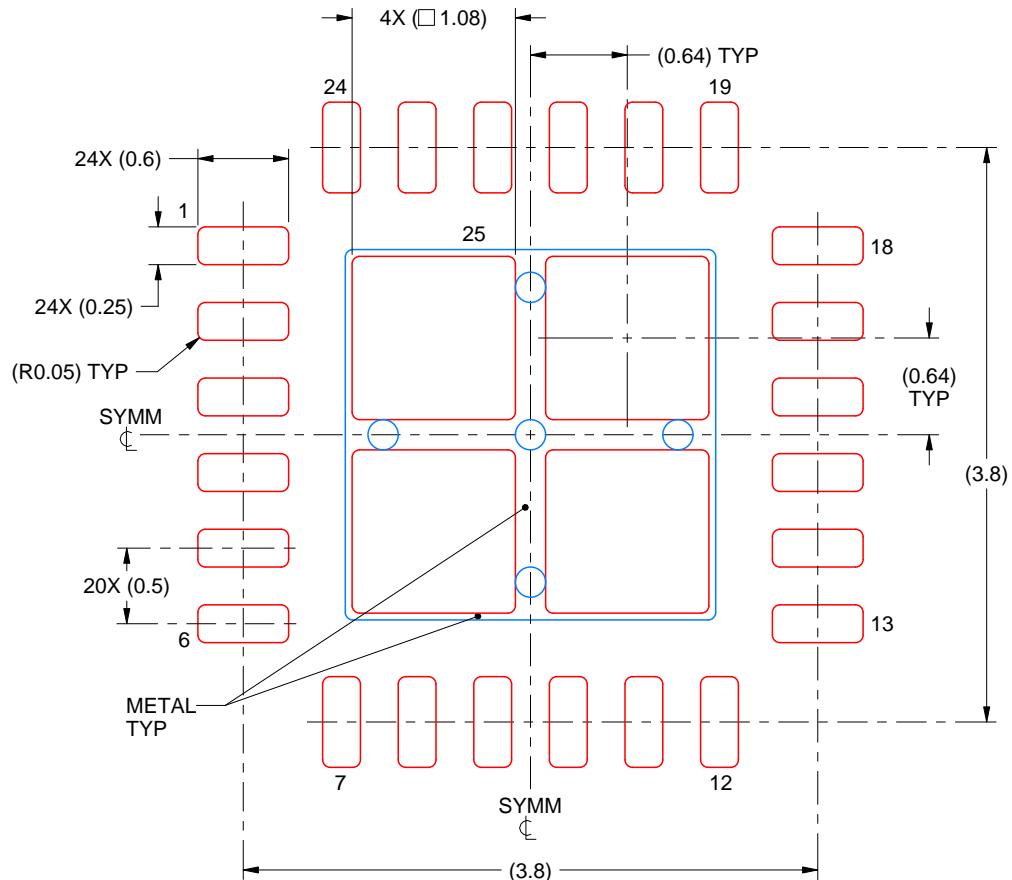
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及ti.com.cn 上或随附TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2020 德州仪器半导体技术（上海）有限公司