

TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

SLOS191D – FEBRUARY 1997 – REVISED NOVEMBER 2010

- Supply Current . . . 300 μ A Max
- High Unity-Gain Bandwidth . . . 2 MHz Typ
- High Slew Rate . . . 0.45 V/ μ s Min
- Supply-Current Change Over Military Temp Range . . . 10 μ A Typ at $V_{CC} \pm \pm 15$ V
- Specified for Both 5-V Single-Supply and ± 15 -V Operation
- Phase-Reversal Protection
- High Open-Loop Gain . . . 6.5 V/ μ V (136 dB) Typ
- Low Offset Voltage . . . 100 μ V Max
- Offset Voltage Drift With Time 0.005 μ V/mo Typ
- Low Input Bias Current . . . 50 nA Max
- Low Noise Voltage . . . 19 nV/ $\sqrt{\text{Hz}}$ Typ

description

The TLE202x, TLE202xA, and TLE202xB devices are precision, high-speed, low-power operational amplifiers using a new Texas Instruments Excalibur process. These devices combine the best features of the OP21 with highly improved slew rate and unity-gain bandwidth.

The complementary bipolar Excalibur process utilizes isolated vertical pnp transistors that yield dramatic improvement in unity-gain bandwidth and slew rate over similar devices.

The addition of a bias circuit in conjunction with this process results in extremely stable parameters with both time and temperature. This means that a precision device remains a precision device even with changes in temperature and over years of use.

This combination of excellent dc performance with a common-mode input voltage range that includes the negative rail makes these devices the ideal choice for low-level signal conditioning applications in either single-supply or split-supply configurations. In addition, these devices offer phase-reversal protection circuitry that eliminates an unexpected change in output states when one of the inputs goes below the negative supply rail.

A variety of available options includes small-outline and chip-carrier versions for high-density systems applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.



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TLE2021 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES						CHIP FORM [§] (Y)
		SMALL OUTLINE [†] (D)	SSOP [‡] (DB)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP [‡] (PW)	
0°C to 70°C	200 µV 500 µV	TLE2021ACD TLE2021CD	TLE2021CDBLE	—	—	TLE2021ACP TLE2021CP	— TLE2021CPWLE	— TLE2021Y
–40°C to 85°C	200 µV 500 µV	TLE2021AID TLE2021ID	—	—	—	TLE2021AIP TLE2021IP	—	—
–55°C to 125°C	100 µV 500 µV	— TLE2021MD	—	TLE2021BMFK TLE2021MFK	TLE2021BMJG TLE2021MJG	— TLE2021MP	—	—

[†] The D packages are available taped and reeled. To order a taped and reeled part, add the suffix R (e.g., TLE2021CDR).

[‡] The DB and PW packages are only available left-end taped and reeled.

[§] Chip forms are tested at 25°C only.

TLE2022 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES						CHIP FORM [§] (Y)
		SMALL OUTLINE [†] (D)	SSOP [‡] (DB)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP [‡] (PW)	
0°C to 70°C	150 µV 300 µV 500 µV	TLE2022BCD TLE2022ACD TLE2022CD	— — TLE2022CDBLE	—	—	— TLE2022ACP TLE2022CP	— — TLE2022CPWLE	— — TLE2022Y
–40°C to 85°C	150 µV 300 µV 500 µV	TLE2022BID TLE2022AID TLE2022ID	—	—	—	— TLE2022AIP TLE2022IP	—	—
–55°C to 125°C	150 µV 300 µV 500 µV	— TLE2022AMD TLE2022MD	—	— TLE2022AMFK TLE2022MFK	TLE2022BMJG TLE2022AMJG TLE2022MJG	— TLE2022AMP TLE2022MP	—	—

[†] The D packages are available taped and reeled. To order a taped and reeled part, add the suffix R (e.g., TLE2022CDR).

[‡] The DB and PW packages are only available left-end taped and reeled.

[§] Chip forms are tested at 25°C only.

TLE2024 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES				CHIP FORM [§] (Y)
		SMALL OUTLINE (DW)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	
0°C to 70°C	500 µV 750 µV 1000 µV	TLE2024BCDW TLE2024ACDW TLE2024CDW	—	—	TLE2024BCN TLE2024ACN TLE2024CN	— — TLE2024Y
–40°C to 85°C	500 µV 750 µV 1000 µV	TLE2024BIDW TLE2024AIDW TLE2024IDW	—	—	TLE2024BIN TLE2024AIN TLE2024IN	—
–55°C to 125°C	500 µV 750 µV 1000 µV	TLE2024BMDW TLE2024AMDW TLE2024MDW	TLE2024BMFK TLE2024AMFK TLE2024MFK	TLE2024BMJ TLE2024AMJ TLE2024MJ	TLE2024BMN TLE2024AMN TLE2024MN	—

[§] Chip forms are tested at 25°C only.

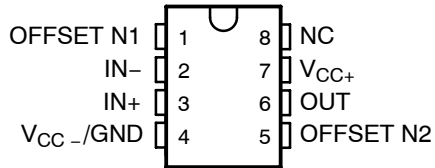


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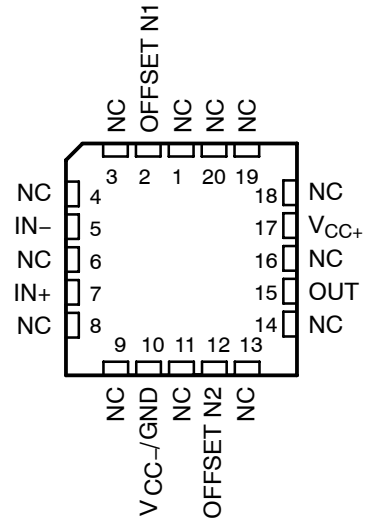
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TLE2021
D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)

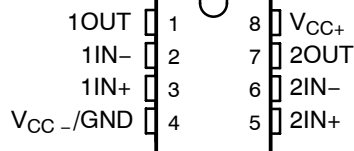


NC – No internal connection

TLE2021
FK PACKAGE
(TOP VIEW)

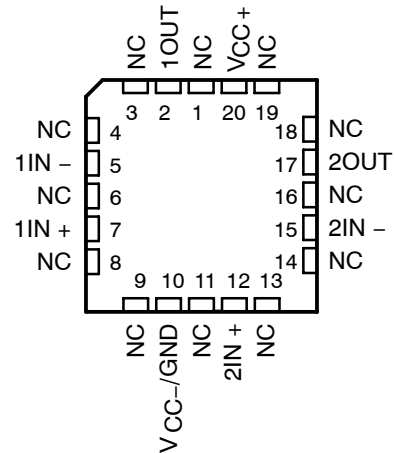


D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)

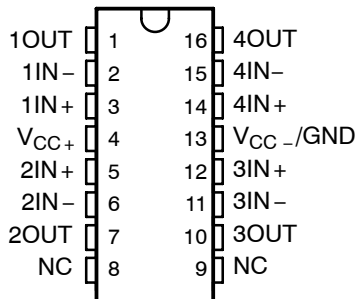


NC – No internal connection

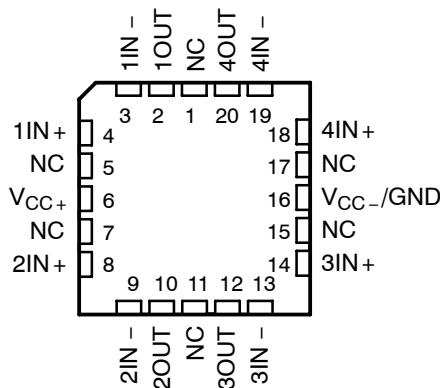
FK PACKAGE
(TOP VIEW)



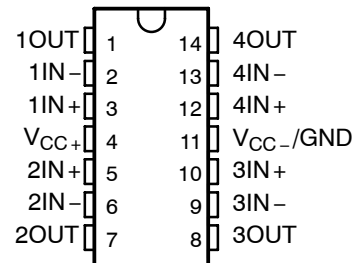
DW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



J OR N PACKAGE
(TOP VIEW)



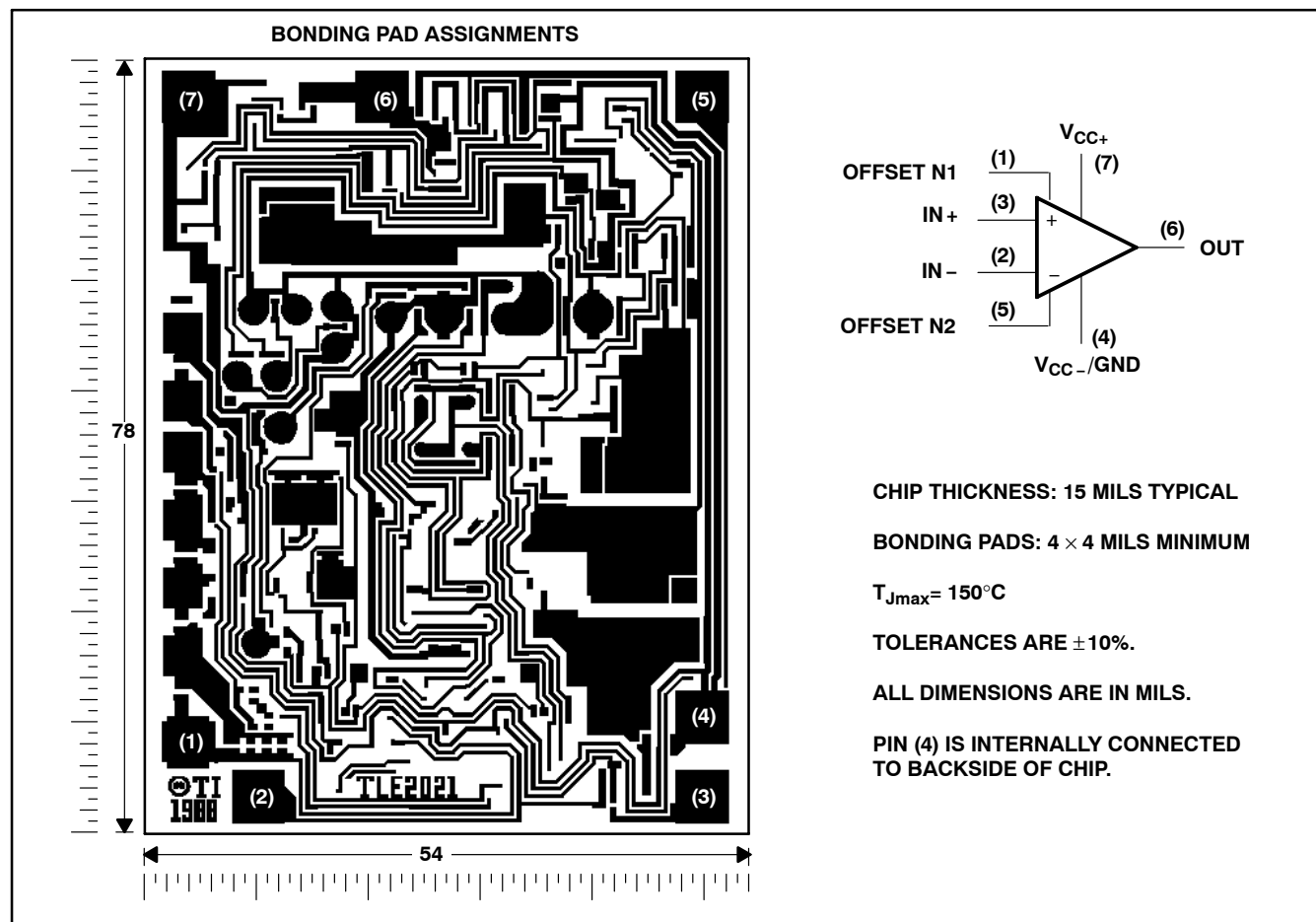
NC – No internal connection

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TLE2021Y chip information

This chip, when properly assembled, display characteristics similar to the TLE2021. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

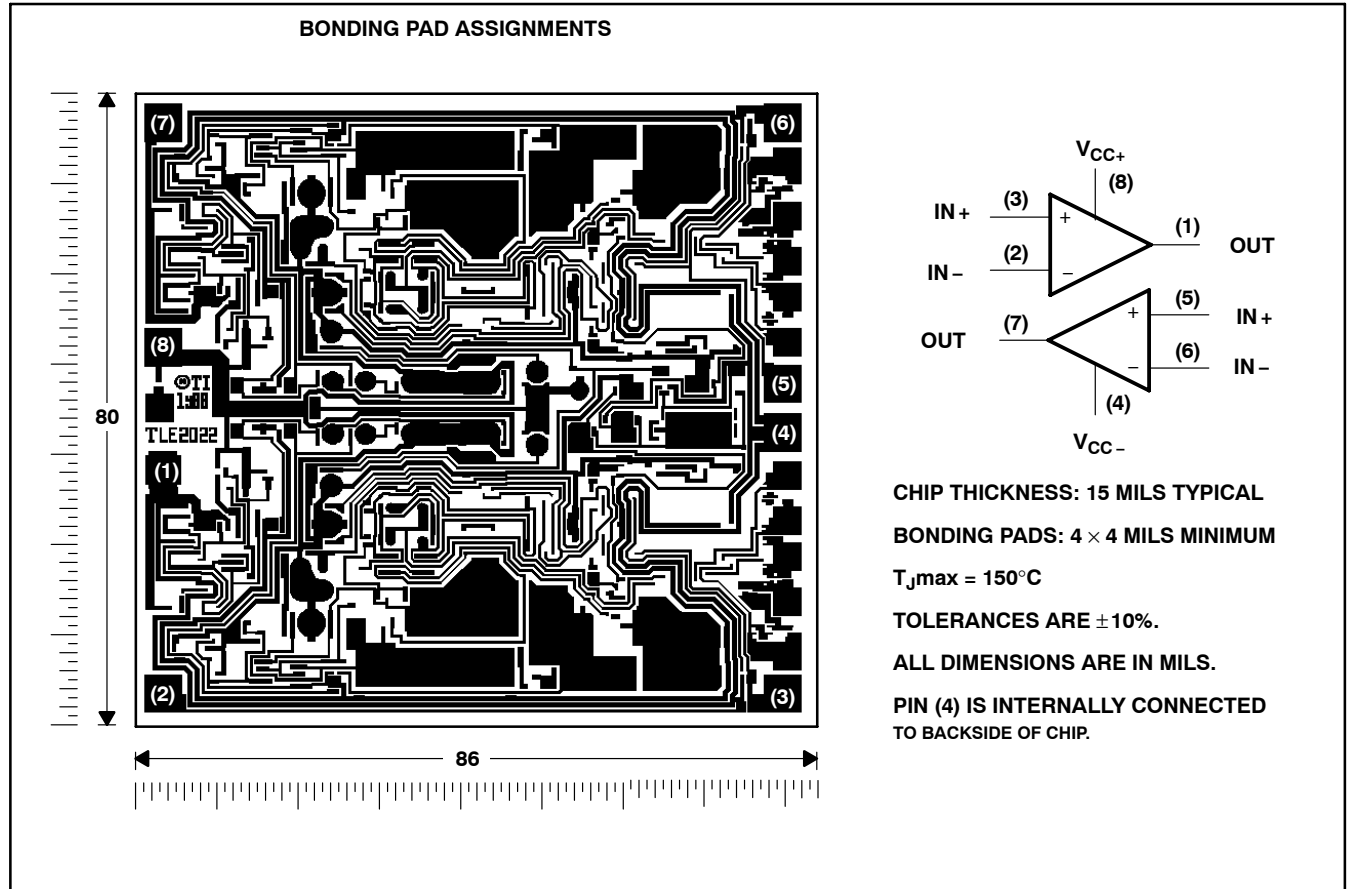


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TLE2022Y chip information

This chip, when properly assembled, displays characteristics similar to TLE2022. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.



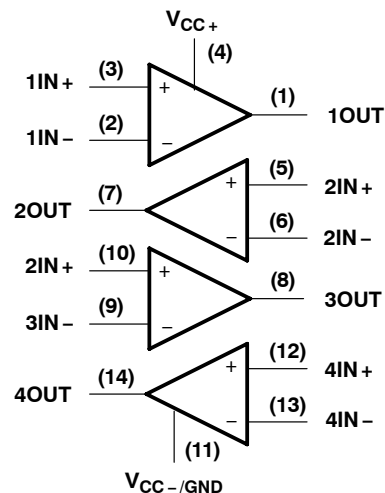
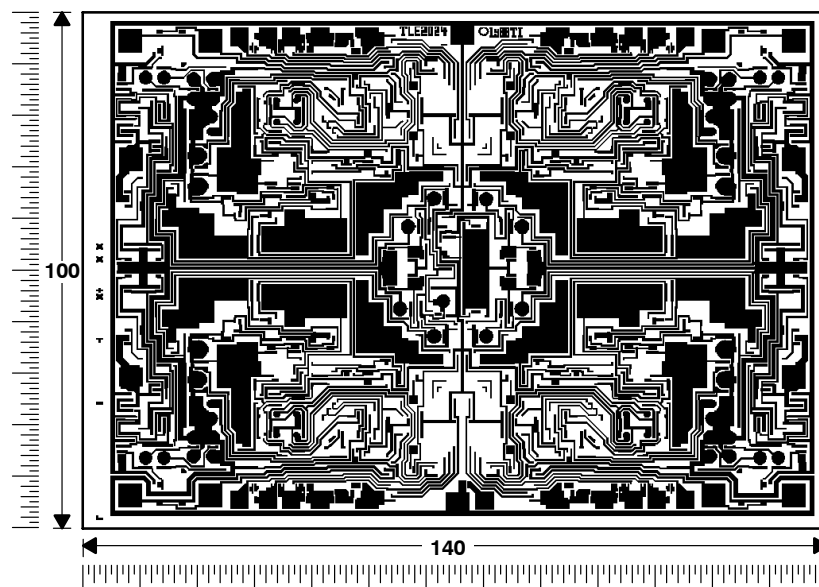
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TLE2024Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2024. Thermal compression or ultrasonic bonding may be used on the doped aluminum-bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4×4 MILS MINIMUM

$T_{Jmax} = 150^{\circ}\text{C}$

TOLERANCES ARE $\pm 10\%$.

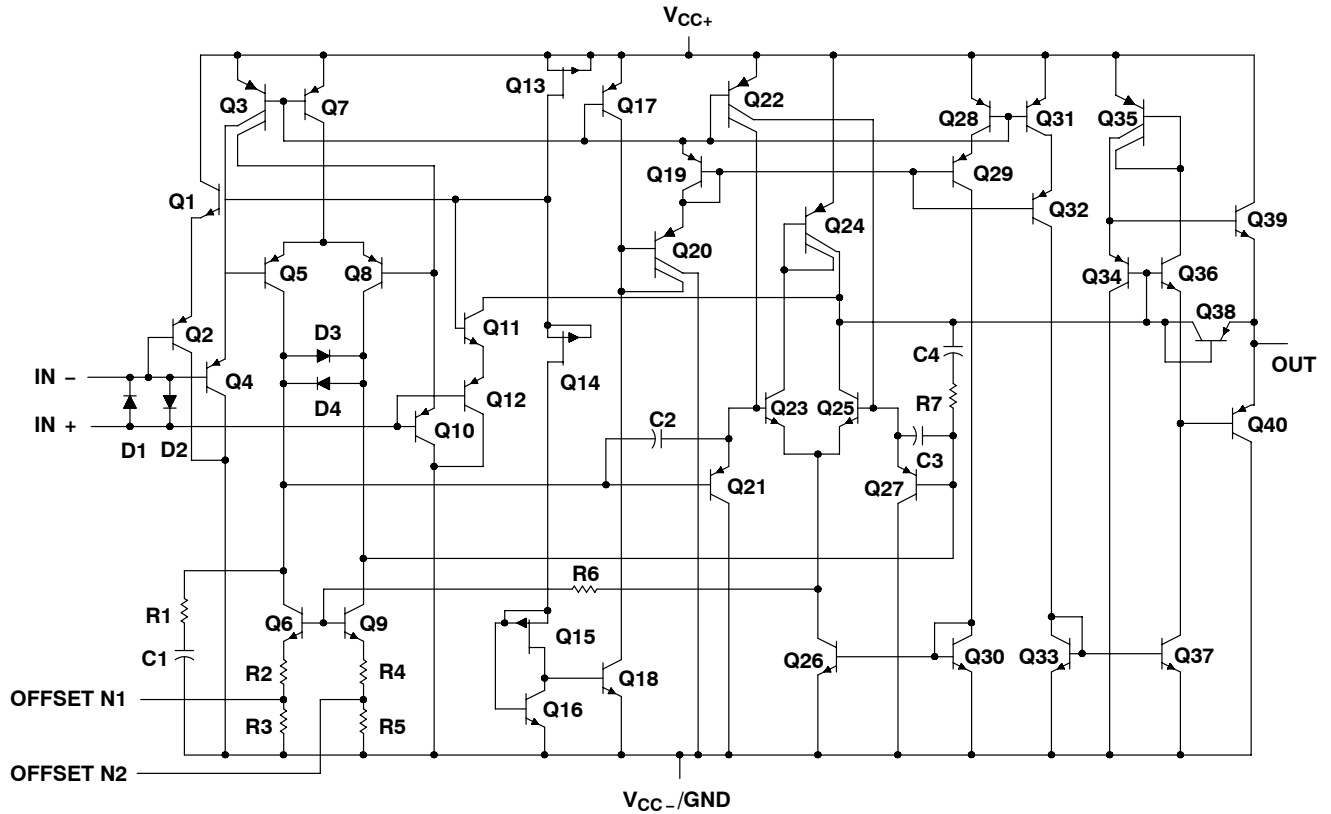
ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED
TO BACKSIDE OF CHIP.

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equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT			
COMPONENT	TLE2021	TLE2022	TLE2024
Transistors	40	80	160
Resistors	7	14	28
Diodes	4	8	16
Capacitors	4	8	16

TLE202x, TLE202xA, TLE202xB, TLE202xY

EXCALIBUR HIGH-SPEED LOW-POWER PRECISION

OPERATIONAL AMPLIFIERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC+} (see Note 1)	20 V
Supply voltage, V_{CC-} (see Note 1)	–20 V
Differential input voltage, V_{ID} (see Note 2)	± 0.6 V
Input voltage range, V_I (any input, see Note 1)	$\pm V_{CC}$
Input current, I_I (each input)	± 1 mA
Output current, I_O (each output): TLE2021	± 20 mA
TLE2022	± 30 mA
TLE2024	± 40 mA
Total current into V_{CC+}	80 mA
Total current out of V_{CC-}	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	–40°C to 85°C
M suffix	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 60 seconds, T_C : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DP, P, or PW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
2. Differential voltages are at $IN+$ with respect to $IN-$. Excessive current flows if a differential input voltage in excess of approximately ± 600 mV is applied between the inputs unless some limiting resistance is used.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D–8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DB–8	525 mW	4.2 mW/°C	336 mW	—	—
DW–16	1025 mW	8.2 mW/°C	656 mW	533 mW	205 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J–14	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG–8	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N–14	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P–8	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW–8	525 mW	4.2 mW/°C	336 mW	—	—

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}		± 2	± 20	± 2	± 20	± 2	± 20	V
Common-mode input voltage, V_{IC}	$V_{CC} = \pm 5$ V	0	3.5	0	3.2	0	3.2	V
	$V_{CC\pm} = \pm 15$ V	–15	13.5	–15	13.2	–15	13.2	
Operating free-air temperature, T_A		0	70	–40	85	–55	125	°C



TLE2021 electrical characteristics at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2021C			TLE2021AC			TLE2021BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0, R _S = 50 Ω	25°C	120		600	100		300	80		200	μV
			Full range			850			600			300	
α _{VIO}	Temperature coefficient of input offset voltage		Full range	2			2			2			μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C	0.005			0.005			0.005			μV/mo
I _{IO}	Input offset current		25°C	0.2		6	0.2		6	0.2		6	nA
			Full range			10			10			10	
I _{IB}	Input bias current		25°C	25		70	25		70	25		70	nA
			Full range			90			90			90	
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω	25°C	0 to 3.5	– 0.3 to 4		0 to 3.5	– 0.3 to 4		0 to 3.5	– 0.3 to 4		V
			Full range	0 to 3.5			0 to 3.5			0 to 3.5			
V _{OH}	High-level output voltage	R _L = 10 kΩ	25°C	4	4.3		4	4.3		4	4.3		V
			Full range	3.9			3.9			3.9			
V _{OL}	Low-level output voltage		25°C	0.7		0.8	0.7		0.8	0.7		0.8	V
			Full range			0.85			0.85			0.85	
A _{VD}	Large-signal differential voltage amplification	V _O = 1.4 V to 4 V, R _L = 10 kΩ	25°C	0.3	1.5		0.3	1.5		0.3	1.5		V/μV
			Full range	0.3			0.3			0.3			
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	85	110		85	110		85	110		dB
			Full range	80			80			80			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC} /ΔV _{IO})	V _{CC} = 5 V to 30 V	25°C	105	120		105	120		105	120		dB
			Full range	100			100			100			
I _{CC}	Supply current	V _O = 2.5 V, No load	25°C	200	300		200	300		200	300		μA
			Full range			300			300			300	
ΔI _{CC}	Supply-current change over operating temperature range			Full range	5			5			5		μA

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2021 electrical characteristics at specified free-air temperature, $V_{CC} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2021C			TLE2021AC			TLE2021BC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		120	500		80	200		40	100	μV
		Full range			750			500			200	
α_{VIO} Temperature coefficient of input offset voltage		Full range		2			2			2		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.2	6		0.2	6		0.2	6	nA
		Full range			10			10			10	
I_{IB} Input bias current		25°C		25	70		25	70		25	70	nA
		Full range			90			90			90	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	–15 to 13.5	–15.3 to 14		–15 to 13.5	–15.3 to 14		–15 to 13.5	–15.3 to 14		V
		Full range	–15 to 13.5			–15 to 13.5			–15 to 13.5			
V_{OM+} Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	14	14.3		14	14.3		14	14.3		V
		Full range	13.9			13.9			13.9			
V_{OM-} Maximum negative peak output voltage swing		25°C	–13.7	–14.1		–13.7	–14.1		–13.7	–14.1		V
		Full range	–13.7			–13.7			–13.7			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}, R_L = 10\ \text{k}\Omega$	25°C	1	6.5		1	6.5		1	6.5		$\text{V}/\mu\text{V}$
		Full range	1			1			1			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{ min}, R_S = 50\ \Omega$	25°C	100	115		100	115		100	115		dB
		Full range	96			96			96			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\text{ V to } \pm 15\text{ V}$	25°C	105	120		105	120		105	120		dB
		Full range	100			100			100			
I_{CC} Supply current	$V_O = 0, \text{ No load}$	25°C		240	350		240	350		240	350	μA
		Full range			350			350			350	
ΔI_{CC} Supply-current change over operating temperature range		Full range		6			6			6		μA

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2022 electrical characteristics at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2022C			TLE2022AC			TLE2022BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0, R _S = 50 Ω	25°C	600			400			250			μV
			Full range	800			550			400			
αV _{IO}	Temperature coefficient of input offset voltage		Full range	2			2			2			μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C	0.005			0.005			0.005			μV/mo
I _{IO}	Input offset current		25°C	0.5 6			0.4 6			0.3 6			nA
			Full range	10			10			10			
I _{IB}	Input bias current		25°C	35 70			33 70			30 70			nA
			Full range	90			90			90			
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω	25°C	0 to 3.5	–0.3 to 4	0 to 3.5	–0.3 to 4	0 to 3.5	–0.3 to 4	0 to 3.5	–0.3 to 4	V	
			Full range	0 to 3.5		0 to 3.5		0 to 3.5					
V _{OH}	High-level output voltage	R _L = 10 kΩ	25°C	4	4.3	4	4.3	4	4.3	4	4.3	V	
			Full range	3.9		3.9		3.9					
V _{OL}	Low-level output voltage		25°C	0.7	0.8	0.7	0.8	0.7	0.8	0.7	0.8	V	
			Full range	0.85		0.85		0.85					
A _{VD}	Large-signal differential voltage amplification	V _O = 1.4 V to 4 V, R _L = 10 kΩ	25°C	0.3	1.5	0.4	1.5	0.5	1.5			V/μV	
			Full range	0.3		0.4		0.5					
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min, R _S = 50 Ω	25°C	85	100	87	102	90	105			dB	
			Full range	80		82		85					
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC} ±/ΔV _{IO})	V _{CC} = 5 V to 30 V	25°C	100	115	103	118	105	120			dB	
			Full range	95		98		100					
I _{CC}	Supply current	V _O = 2.5 V, No load	25°C	450	600	450	600	450	600			μA	
			Full range	600		600		600					
ΔI _{CC}	Supply current change over operating temperature range		Full range	7		7		7			μA		

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2022 electrical characteristics at specified free-air temperature, $V_{CC} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2022C			TLE2022AC			TLE2022BC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50 \Omega$	25°C		150	500		120	300		70	150	μV
		Full range			700			450			300	
α_{VIO} Temperature coefficient of input offset voltage		Full range		2			2			2		$\mu V/^\circ C$
Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		$\mu V/mo$
I_{IO} Input offset current		25°C		0.5	6		0.4	6		0.3	6	nA
		Full range			10			10			10	
I_{IB} Input bias current		25°C		35	70		33	70		30	70	nA
		Full range			90			90			90	
V_{ICR} Common-mode input voltage range	$R_S = 50 \Omega$	25°C	–15 to 13.5	–15.3 to 14		–15 to 13.5	–15.3 to 14		–15 to 13.5	–15.3 to 14		V
		Full range	–15 to 13.5			–15 to 13.5			–15 to 13.5			
V_{OM+} Maximum positive peak output voltage swing	$R_L = 10 k\Omega$	25°C		14	14.3		14	14.3		14	14.3	V
		Full range		13.9			13.9			13.9		
V_{OM-} Maximum negative peak output voltage swing		25°C		–13.7	–14.1		–13.7	–14.1		–13.7	–14.1	V
		Full range		–13.7			–13.7			–13.7		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10 k\Omega$	25°C		0.8	4		1	7		1.5	10	V/ μV
		Full range		0.8			1			1.5		
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50 \Omega$	25°C		95	106		97	109		100	112	dB
		Full range		91			93			96		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ± 15 V	25°C		100	115		103	118		105	120	dB
		Full range		95			98			100		
I_{CC} Supply current	$V_O = 0,$ No load	25°C		550	700		550	700		550	700	μA
		Full range			700			700			700	
ΔI_{CC} Supply current change over operating temperature range		Full range		9			9			9		μA

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2024 electrical characteristics at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2024C			TLE2024AC			TLE2024BC			UNIT	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
V _{IO}	Input offset voltage	V _{IC} = 0, R _S = 50 Ω	25°C	1100			850			600			μV	
			Full range	1300			1050			800				
α _{VIO}	Temperature coefficient of input offset voltage		Full range	2			2			2			μV/°C	
	Input offset voltage long-term drift (see Note 4)		25°C	0.005			0.005			0.005			μV/mo	
I _{IO}	Input offset current		25°C	0.6 6			0.5 6			0.4 6			nA	
			Full range	10			10			10				
I _{IB}	Input bias current		25°C	45 70			40 70			35 70			nA	
			Full range	90			90			90				
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω	25°C	0 to 3.5	–0.3 to 4		0 to 3.5	–0.3 to 4		0 to 3.5	–0.3 to 4		V	
			Full range	0 to 3.5			0 to 3.5			0 to 3.5				
V _{OH}	High-level output voltage	R _L = 10 kΩ	25°C	3.9	4.2		3.9	4.2		4	4.3		V	
			Full range	3.7			3.7			3.8				
V _{OL}	Low-level output voltage		25°C		0.7	0.8			0.7	0.8		0.7	0.8	V
			Full range		0.95				0.95			0.95		
A _{VD}	Large-signal differential voltage amplification	V _O = 1.4 V to 4 V, R _L = 10 kΩ	25°C	0.2	1.5		0.3	1.5		0.4	1.5		V/μV	
			Full range	0.1			0.1			0.1				
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	80	90		82	92		85	95		dB	
			Full range	80			82			85				
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC} /ΔV _{IO})	V _{CC} = 5 V to 30 V	25°C	98	112		100	115		103	117		dB	
			Full range	93			95			98				
I _{CC}	Supply current	V _O = 2.5 V, No load	25°C	800	1200		800	1200		800	1200		μA	
			Full range		1200			1200			1200			
ΔI _{CC}	Supply current change over operating temperature range		Full range		15			15			15		μA	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2024 electrical characteristics at specified free-air temperature, $V_{CC} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2024C			TLE2024AC			TLE2024BC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50 \Omega$	25°C			1000			750			500	μV
		Full range			1200			950			700	
α_{VIO} Temperature coefficient of input offset voltage		Full range		2			2			2		$\mu V/^\circ C$
Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		$\mu V/mo$
I_{IO} Input offset current		25°C		0.6	6		0.5	6		0.4	6	nA
		Full range			10			10			10	
I_{IB} Input bias current		25°C		50	70		45	70		40	70	nA
		Full range			90			90			90	
V_{ICR} Common-mode input voltage range	$R_S = 50 \Omega$	25°C	– 15 to 13.5	– 15.3 to 14		– 15 to 13.5	– 15.3 to 14		– 15 to 13.5	– 15.3 to 14		V
		Full range	– 15 to 13.5			– 15 to 13.5			– 15 to 13.5			
V_{OM+} Maximum positive peak output voltage swing	$R_L = 10 k\Omega$	25°C	13.8	14.1		13.9	14.2		14	14.3		V
		Full range	13.7			13.8			13.9			
V_{OM-} Maximum negative peak output voltage swing		25°C	– 13.7	– 14.1		– 13.7	– 14.1		– 13.7	– 14.1		V
		Full range	– 13.6			– 13.6			– 13.6			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10 k\Omega$	25°C	0.4	2		0.8	4		1	7		V/ μV
		Full range	0.4			0.8			1			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50 \Omega$	25°C	92	102		94	105		97	108		dB
		Full range	88			90			93			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ± 15 V	25°C	98	112		100	115		103	117		dB
		Full range	93			95			98			
I_{CC} Supply current	$V_O = 0, \text{ No load}$	25°C		1050	1400		1050	1400		1050	1400	μA
		Full range			1400			1400			1400	
ΔI_{CC} Supply current change over operating temperature range		Full range		20			20			20		μA

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2021 electrical characteristics at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2021I			TLE2021AI			TLE2021BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0, R _S = 50 Ω	25°C	120	600	100	300	80	200	μV			
			Full range	950			600				300		
α _{VIO}	Temperature coefficient of input offset voltage		Full range	2			2			2	μV/°C		
	Input offset voltage long-term drift (see Note 4)		25°C	0.005			0.005			0.005	μV/mo		
I _{IO}	Input offset current		25°C	0.2	6	0.2	6	0.2	6	nA			
			Full range	10			10				10		
I _{IB}	Input bias current		25°C	25	70	25	70	25	70	nA			
			Full range	90			90				90		
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω	25°C	0 to 3.5	–0.3 to 4	0 to 3.5	–0.3 to 4	0 to 3.5	–0.3 to 4	V			
			Full range	0 to 3.2		0 to 3.2		0 to 3.2					
V _{OH}	High-level output voltage	R _L = 10 kΩ	25°C	4	4.3	4	4.3	4	4.3	V			
			Full range	3.9		3.9		3.9					
V _{OL}	Low-level output voltage		25°C	0.7	0.8	0.7	0.8	0.7	0.8	V			
			Full range	0.9		0.9		0.9					
A _{VD}	Large-signal differential voltage amplification	V _O = 1.4 V to 4 V, R _L = 10 kΩ	25°C	0.3	1.5	0.3	1.5	0.3	1.5	V/μV			
		Full range	0.25		0.25		0.25						
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min, R _S = 50 Ω	25°C	85	110	85	110	85	110	dB			
		Full range	80		80		80						
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC} /ΔV _{IO})	V _{CC} = 5 V to 30 V	25°C	105	120	105	120	105	120	dB			
		Full range	100		100		100						
I _{CC}	Supply current	V _O = 2.5 V, No load	25°C	200	300	200	300	200	300	μA			
			Full range	300		300		300					
ΔI _{CC}	Supply-current change over operating temperature range		Full range	6		6		6		μA			

† Full range is –40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2021 electrical characteristics at specified free-air temperature, $V_{CC} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2021I			TLE2021AI			TLE2021BI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		120	500		80	200		40	100	μV
		Full range			850			500			200	
α_{VIO} Temperature coefficient of input offset voltage		Full range		2			2			2		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.2	6		0.2	6		0.2	6	nA
		Full range			10			10			10	
I_{IB} Input bias current		25°C		25	70		25	70		25	70	nA
		Full range			90			90			90	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	– 15 to 13.5	– 15.3 to 14		– 15 to 13.5	– 15.3 to 14		– 15 to 13.5	– 15.3 to 14		V
		Full range	– 15 to 13.2			– 15 to 13.2			– 15 to 13.2			
V_{OM+} Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C		14	14.3		14	14.3		14	14.3	V
		Full range			13.9			13.9			13.9	
V_{OM-} Maximum negative peak output voltage swing		25°C		– 13.7	– 14.1		– 13.7	– 14.1		– 13.7	– 14.1	V
		Full range			– 13.6			– 13.6			– 13.6	
A_{VD} Large-signal differential voltage amplification	$V_O = 10\text{ V}, R_L = 10\ \text{k}\Omega$	25°C		1	6.5		1	6.5		1	6.5	$\text{V}/\mu\text{V}$
		Full range			0.75			0.75			0.75	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR\text{ min}}, R_S = 50\ \Omega$	25°C		100	115		100	115		100	115	dB
		Full range			96			96			96	
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\text{ V}$ to $\pm 15\text{ V}$	25°C		105	120		105	120		105	120	dB
		Full range			100			100			100	
I_{CC} Supply current	$V_O = 0\text{ V}, \text{ No load}$	25°C		240	350		240	350		240	350	μA
		Full range			350			350			350	
ΔI_{CC} Supply-current change over operating temperature range		Full range		7			7			7		μA

† Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2022 electrical characteristics at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2022I			TLE2022AI			TLE2022BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0, R _S = 50 Ω	25°C	600			400			250			μV
			Full range	800			550			400			
α _{VIO}	Temperature coefficient of input offset voltage		Full range	2			2			2			μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C	0.005			0.005			0.005			μV/mo
I _{IO}	Input offset current		25°C	0.5			0.4			0.3			nA
			Full range	10			10			10			
I _{IB}	Input bias current		25°C	35			33			30			nA
			Full range	90			90			90			
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω	25°C	0 to 3.5	–0.3 to 4	0 to 3.5	–0.3 to 4	0 to 3.5	–0.3 to 4	V			
			Full range	0 to 3.2		0 to 3.2		0 to 3.2					
V _{OH}	High-level output voltage	R _L = 10 kΩ	25°C	4	4.3	4	4.3	4	4.3	V			
			Full range	3.9		3.9		3.9					
V _{OL}	Low-level output voltage		25°C	0.7			0.7			V			
			Full range	0.9			0.9						
A _{VD}	Large-signal differential voltage amplification	V _O = 1.4 V to 4 V, R _L = 10 kΩ	25°C	0.3	1.5	0.4	1.5	0.5	1.5	V/μV			
			Full range	0.2		0.2		0.2					
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	85	100	87	102	90	105	dB			
			Full range	80		82		85					
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	V _{CC} = 5 V to 30 V	25°C	100	115	103	118	105	120	dB			
			Full range	95		98		100					
I _{CC}	Supply current	V _O = 2.5 V, No load	25°C	450			450			μA			
			Full range	600			600						
ΔI _{CC}	Supply current change over operating temperature range		Full range	15			15			μA			

† Full range is -40°C to 85°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2022 electrical characteristics at specified free-air temperature, $V_{CC} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2022I			TLE2022AI			TLE2022BI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, \quad R_S = 50\ \Omega$	25°C		150	500		120	300		70	150	μV
		Full range			700			450			300	
α_{VIO} Temperature coefficient of input offset voltage		Full range		2			2			2		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.5	6		0.4	6		0.3	6	nA
		Full range			10			10			10	
I_{IB} Input bias current		25°C		35	70		33	70		30	70	nA
		Full range			90			90			90	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	– 15 to 13.5	– 15.3 to 14		– 15 to 13.5	– 15.3 to 14		– 15 to 13.5	– 15.3 to 14		V
		Full range	– 15 to 13.2			– 15 to 13.2			– 15 to 13.2			
V_{OM+} Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C		14	14.3		14	14.3		14	14.3	V
		Full range			13.9			13.9			13.9	
V_{OM-} Maximum negative peak output voltage swing		25°C		– 13.7	– 14.1		– 13.7	– 14.1		– 13.7	– 14.1	V
		Full range			– 13.6			– 13.6			– 13.6	
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}, \quad R_L = 10\ \text{k}\Omega$	25°C		0.8	4		1	7		1.5	10	$\text{V}/\mu\text{V}$
		Full range			0.8			1			1.5	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, \quad R_S = 50\ \Omega$	25°C		95	106		97	109		100	112	dB
		Full range			91			93			96	
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 2.5\text{ V to } \pm 15\text{ V}$	25°C		100	115		103	118		105	120	dB
		Full range			95			98			100	
I_{CC} Supply current	$V_O = 0, \quad \text{No load}$	25°C		550	700		550	700		550	700	μA
		Full range			700			700			700	
ΔI_{CC} Supply current change over operating temperature range		Full range		30			30			30		μA

† Full range is -40°C to 85°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2024 electrical characteristics at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2024I			TLE2024AI			TLE2024BI			UNIT	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
V _{IO}	Input offset voltage	V _{IC} = 0, R _S = 50 Ω	25°C	1100			850			600			μV	
			Full range	1300			1050			800				
α _{VIO}	Temperature coefficient of input offset voltage		Full range	2			2			2			μV/°C	
	Input offset voltage long-term drift (see Note 4)		25°C	0.005			0.005			0.005			μV/mo	
I _{IO}	Input offset current		25°C	0.6			6	0.5		6	0.4		6	nA
			Full range	10			10			10				
I _{IB}	Input bias current		25°C	45			70	40		70	35		70	nA
			Full range	90			90			90				
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω	25°C	0 to 3.5	–0.3 to 4		0 to 3.5	–0.3 to 4		0 to 3.5	–0.3 to 4		V	
			Full range	0 to 3.2			0 to 3.2			0 to 3.2				
V _{OM+}	Maximum positive peak output voltage swing	R _L = 10 kΩ	25°C	3.9	4.2		3.9	4.2		4	4.3		V	
			Full range	3.7			3.7			3.8				
V _{OM–}	Maximum negative peak output voltage swing		25°C	0.7			0.8	0.7		0.8	0.7		0.8	V
			Full range	0.95			0.95			0.95				
A _{VD}	Large-signal differential voltage amplification	V _O = 1.4 V to 4 V, R _L = 10 kΩ	25°C	0.2	1.5		0.3	1.5		0.4	1.5		V/μV	
			Full range	0.1			0.1			0.1				
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min, R _S = 50 Ω	25°C	80	90		82	92		85	95		dB	
			Full range	80			82			85				
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	V _{CC±} = ±2.5 V to ±15 V	25°C	98	112		100	115		103	117		dB	
			Full range	93			95			98				
I _{CC}	Supply current	V _O = 0, No load	25°C	800	1200		800	1200		800	1200		μA	
			Full range	1200			1200			1200				
ΔI _{CC}	Supply current change over operating temperature range		Full range	30			30			30			μA	

† Full range is -40°C to 85°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2024 electrical characteristics at specified free-air temperature, $V_{CC} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2024I			TLE2024AI			TLE2024BI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, \quad R_S = 50\ \Omega$	25°C			1000			750			500	μV
		Full range			1200			950			700	
α_{VIO} Temperature coefficient of input offset voltage		Full range		2			2			2		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.6	6		0.5	6		0.4	6	nA
		Full range			10			10			10	
I_{IB} Input bias current		25°C		50	70		45	70		40	70	nA
		Full range			90			90			90	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	–15 to 13.5	–15.3 to 14		–15 to 13.5	–15.3 to 14		–15 to 13.5	–15.3 to 14		V
		Full range	–15 to 13.2			–15 to 13.2			–15 to 13.2			
V_{OM+} Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	13.8	14.1		13.9	14.2		14	14.3		V
		Full range	13.7			13.7			13.8			
V_{OM-} Maximum negative peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	–13.7	–14.1		–13.7	–14.1		–13.7	–14.1		V
		Full range	–13.6			–13.6			–13.6			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}, \quad R_L = 10\ \text{k}\Omega$	25°C	0.4	2		0.8	4		1	7		$\text{V}/\mu\text{V}$
		Full range	0.4			0.8			1			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, \quad R_S = 50\ \Omega$	25°C	92	102		94	105		97	108		dB
		Full range	88			90			93			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\text{ V to } \pm 15\text{ V}$	25°C	98	112		100	115		103	117		dB
		Full range	93			95			98			
I_{CC} Supply current	$V_O = 0, \quad \text{No load}$	25°C		1050	1400		1050	1400		1050	1400	μA
		Full range			1400			1400			1400	
ΔI_{CC} Supply current change over operating temperature range		Full range		50			50			50		μA

† Full range is –40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2021 electrical characteristics at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2021M			TLE2021BM			UNIT	
				MIN	TYP	MAX	MIN	TYP	MAX		
V _{IO}	Input offset voltage	V _{IC} = 0, R _S = 50 Ω	25°C		120	600		80	200	μV	
			Full range		1100			300			
α _{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		μV/°C	
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005		μV/mo	
I _{IO}	Input offset current		25°C		0.2			0.2			nA
			Full range		10			10			
I _{IB}	Input bias current		25°C		25			25			nA
			Full range		90			90			
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω	25°C	0	–0.3		0	–0.3		V	
			Full range		0	to 3.2		0	to 3.2		
V _{OH}	High-level output voltage	R _L = 10 kΩ	25°C	4	4.3		4	4.3		V	
			Full range		3.8			3.8			
V _{OL}	Low-level output voltage		25°C		0.7			0.7			V
			Full range		0.95			0.95			
A _{VD}	Large-signal differential voltage amplification	V _O = 1.4 V to 4 V, R _L = 10 kΩ	25°C	0.3	1.5		0.3	1.5		V/μV	
			Full range		0.1			0.1			
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	85	110		85	110		dB	
			Full range		80			80			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	V _{CC} = 5 V to 30 V	25°C	105	120		105	120		dB	
			Full range		100			100			
I _{CC}	Supply current	V _O = 2.5 V, No load	25°C		170	230		170	230	μA	
			Full range		230			230			
ΔI _{CC}	Supply current change over operating temperature range		Full range		9			9		μA	

† Full range is -55°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2021 electrical characteristics at specified free-air temperature, $V_{CC} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2021M			TLE2021BM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, \quad R_S = 50 \, \Omega$	25°C	120	500		40	100		μV
		Full range		1000			200		
α_{VIO} Temperature coefficient of input offset voltage		Full range	2			2			$\mu V/^\circ C$
Input offset voltage long-term drift (see Note 4)		25°C	0.006			0.006			$\mu V/mo$
I_{IO} Input offset current		25°C	0.2	6		0.2	6		nA
		Full range		10			10		
I_{IB} Input bias current	$R_S = 50 \, \Omega$	25°C	25	70		25	70		nA
		Full range		90			90		
V_{ICR} Common-mode input voltage range	$R_S = 50 \, \Omega$	25°C	–15 to 13.5	–15.3 to 14		–15 to 13.5	–15.3 to 14		V
		Full range	–15 to 13.2			–15 to 13.2			
V_{OM+} Maximum positive peak output voltage swing	$R_L = 10 \, k\Omega$	25°C	14	14.3		14	14.3		V
		Full range	13.8			13.8			
V_{OM-} Maximum negative peak output voltage swing		25°C	–13.7	–14.1		–13.7	–14.1		V
		Full range	–13.6			–13.6			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10 \, k\Omega$	25°C	1	6.5		1	6.5		V/ μV
		Full range	0.5			0.5			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, \quad R_S = 50 \, \Omega$	25°C	100	115		100	115		dB
		Full range	96			96			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ± 15 V	25°C	105	120		105	120		dB
		Full range	100			100			
I_{CC} Supply current	$V_O = 0, \quad \text{No load}$	25°C	200	300		200	300		μA
		Full range		300			300		
ΔI_{CC} Supply current change over operating temperature range		Full range	10			10			μA

† Full range is $-55^\circ C$ to $125^\circ C$.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2022 electrical characteristics at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2022M			TLE2022AM			TLE2022BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0, R _S = 50 Ω	25°C	600			400			250			μV
			Full range	800			550			400			
α _{VIO}	Temperature coefficient of input offset voltage		Full range	2			2			2			μV/°C
Input offset voltage long-term drift (see Note 4)			25°C	0.005			0.005			0.005			μV/mo
I _{IO}	Input offset current		25°C	0.5 6			0.4 6			0.3 6			nA
			Full range	10			10			10			
I _{IB}	Input bias current		25°C	35 70			33 70			30 70			nA
			Full range	90			90			90			
V _{ICR}	Common-mode input voltage range		R _S = 50 Ω	25°C	0 –0.3 to to 3.5 4	0 –0.3 to to 3.5 4			0 –0.3 to to 3.5 4			V	
				Full range	0 to 3.2	0 to 3.2			0 to 3.2				
V _{OH}	High-level output voltage	R _L = 10 kΩ	25°C	4 4.3	4 4.3			4 4.3			V		
			Full range	3.8	3.8			3.8					
V _{OL}	Low-level output voltage		25°C	0.7 0.8	0.7 0.8			0.7 0.8			V		
			Full range	0.95	0.95			0.95					
A _{VD}	Large-signal differential voltage amplification	V _O = 1.4 V to 4 V, R _L = 10 kΩ	25°C	0.3 1.5	0.4 1.5			0.5 1.5			V/μV		
			Full range	0.1	0.1			0.1					
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min, R _S = 50 Ω	25°C	85 100	87 102			90 105			dB		
			Full range	80	82			85					
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	V _{CC} = 5 V to 30 V	25°C	100 115	103 118			105 120			dB		
			Full range	95	98			100					
I _{CC}	Supply current	V _O = 2.5 V, No load	25°C	450 600	450 600			450 600			μA		
			Full range	600	600			600					
ΔI _{CC}	Supply current change over operating temperature range		Full range	37	37			37			μA		

† Full range is -55°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2022 electrical characteristics at specified free-air temperature, $V_{CC} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2022M			TLE2022AM			TLE2022BM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50 \Omega$	25°C		150	500		120	300		70	150	μV
		Full range			700			450			300	
$^{\circ}V_{IO}$ Temperature coefficient of input offset voltage		Full range		2			2			2		$\mu V/^{\circ}C$
Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		$\mu V/mo$
I_{IO} Input offset current		25°C		0.5	6		0.4	6		0.3	6	nA
		Full range			10			10			10	
I_{IB} Input bias current		25°C		35	70		33	70		30	70	nA
		Full range			90			90			90	
V_{ICR} Common-mode input voltage range	$R_S = 50 \Omega$	25°C	– 15 to 13.5	– 15.3 to 14		– 15 to 13.5	– 15.3 to 14		– 15 to 13.5	– 15.3 to 14		V
		Full range	– 15 to 13.2			– 15 to 13.2			– 15 to 13.2			
V_{OM+} Maximum positive peak output voltage swing	$R_L = 10 k\Omega$	25°C		14	14.3		14	14.3		14	14.3	V
		Full range		13.9			13.9			13.9		
V_{OM-} Maximum negative peak output voltage swing		25°C		– 13.7	– 14.1		– 13.7	– 14.1		– 13.7	– 14.1	V
		Full range		– 13.6			– 13.6			– 13.6		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10 k\Omega$	25°C		0.8	4		1	7		1.5	10	$V/\mu V$
		Full range		0.8			1			1.5		
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50 \Omega$	25°C		95	106		97	109		100	112	dB
		Full range		91			93			96		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5$ V to ± 15 V	25°C		100	115		103	118		105	120	dB
		Full range		95			98			100		
I_{CC} Supply current	$V_O = 0, \text{ No load}$	25°C		550	700		550	700		550	700	μA
		Full range			700			700			700	
ΔI_{CC} Supply current change over operating temperature range		Full range		60			60			60		μA

† Full range is –55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^{\circ}C$ extrapolated to $T_A = 25^{\circ}C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2024 electrical characteristics at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A [†]	TLE2024M			TLE2024AM			TLE2024BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0, R _S = 50 Ω	25°C	1100			850			600			μV
			Full range	1300			1050			800			
α _{VIO}	Temperature coefficient of input offset voltage		Full range	2			2			2			μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C	0.005			0.005			0.005			μV/mo
I _{IO}	Input offset current		25°C	0.6 6			0.5 6			0.4 6			nA
			Full range	10			10			10			
I _{IB}	Input bias current		25°C	45 70			40 70			35 70			nA
			Full range	90			90			90			
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω	25°C	0 –0.3 to to 3.5 4			0 –0.3 to to 3.5 4			0 –0.3 to to 3.5 4			V
			Full range	0 to 3.2			0 to 3.2			0 to 3.2			
V _{OM+}	Maximum positive peak output voltage swing	R _L = 10 kΩ	25°C	3.9 4.2			3.9 4.2			4 4.3			V
			Full range	3.7			3.7			3.8			
V _{OM–}	Maximum negative peak output voltage swing		25°C	0.7 0.8			0.7 0.8			0.7 0.8			V
			Full range	0.95			0.95			0.95			
A _{VD}	Large-signal differential voltage amplification	V _O = 1.4 V to 4 V, R _L = 10 kΩ	25°C	0.2 1.5			0.3 1.5			0.4 1.5			V/μV
			Full range	0.1			0.1			0.1			
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	80 90			82 92			85 95			dB
			Full range	80			82			85			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	V _{CC±} = ±2.5 V to ±15 V	25°C	98 112			100 115			103 117			dB
			Full range	93			95			98			
I _{CC}	Supply current	V _O = 0, No load	25°C	800 1200			800 1200			800 1200			μA
			Full range	1200			1200			1200			
ΔI _{CC}	Supply current change over operating temperature range		Full range	50			50			50			μA

† Full range is -55°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2024 electrical characteristics at specified free-air temperature, $V_{CC} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2024M			TLE2024AM			TLE2024BM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C			1000			750			500	μV
		Full range			1200			950			700	
α_{VIO} Temperature coefficient of input offset voltage		Full range		2			2			2		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.6	6		0.5	6		0.4	6	nA
		Full range			10			10			10	
I_{IB} Input bias current		25°C		50	70		45	70		40	70	nA
		Full range			90			90			90	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	–15 to 13.5	–15.3 to 14		–15 to 13.5	–15.3 to 14		–15 to 13.5	–15.3 to 14		V
		Full range	–15 to 13.2			–15 to 13.2			–15 to 13.2			
V_{OM+} Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	13.8	14.1		13.9	14.2		14	14.3		V
		Full range	13.7			13.7			13.8			
V_{OM-} Maximum negative peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	–13.7	–14.1		–13.7	–14.1		–13.7	–14.1		V
		Full range	–13.6			–13.6			–13.6			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}, R_L = 10\ \text{k}\Omega$	25°C	0.4	2		0.8	4		1	7		V/ μV
		Full range	0.4			0.8			1			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50\ \Omega$	25°C	92	102		94	105		97	108		dB
		Full range	88			90			93			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\text{ V to } \pm 15\text{ V}$	25°C	98	112		100	115		103	117		dB
		Full range	93			95			98			
I_{CC} Supply current	$V_O = 0, \text{ No load}$	25°C		1050	1400		1050	1400		1050	1400	μA
		Full range			1400			1400			1400	
ΔI_{CC} Supply current change over operating temperature range		Full range		85			85			85		μA

[†] Full range is –55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2021 operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	T _A	C SUFFIX			I SUFFIX			M SUFFIX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 1 V to 3 V, See Figure 1	25°C	0.5			0.5			0.5			V/μs
V _n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C	21			21			21			nV/Hz
		f = 1 kHz	25°C	17			17			17			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C	0.16			0.16			0.16			μV
		f = 0.1 to 10 Hz	25°C	0.47			0.47			0.47			
I _n	Equivalent input noise current		25°C	0.09			0.09			0.9			pA/Hz
B ₁	Unity-gain bandwidth	See Figure 3	25°C	1.2			1.2			1.2			MHz
φ _m	Phase margin at unity gain	See Figure 3	25°C	42°			42°			42°			

TLE2021 operating characteristics at specified free-air temperature, $V_{CC} = \pm 15\text{ V}$

PARAMETER		TEST CONDITIONS	T _A [†]	C SUFFIX			I SUFFIX			M SUFFIX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 1V to 3 V, See Figure 1	25°C	0.45	0.65		0.45	0.65		0.45	0.65		V/μs
			Full range	0.45			0.42			0.45			
V _n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19	50		19	50		19		nV/Hz
		f = 1 kHz	25°C		15	30		15	30		15		
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I _n	Equivalent input noise current		25°C		0.09			0.09			0.09		pA/Hz
B ₁	Unity-gain bandwidth	See Figure 3	25°C		2			2			2		MHz
φ _m	Phase margin at unity gain	See Figure 3	25°C		46°			46°			46°		

[†] Full range is 0°C to 70°C for the C-suffix devices, –40°C to 85°C for the I-suffix devices, and –55°C to 125°C for the M-suffix devices.

TLE2022 operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	C SUFFIX			I SUFFIX			M SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1\text{ V to }3\text{ V}$, See Figure 1		0.5			0.5			0.5		$\text{V}/\mu\text{s}$
V_n	Equivalent input noise voltage (see Figure 2)	$f = 10\text{ Hz}$		21	50		21	50		21		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		17	30		17	30		17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ to }1\text{ Hz}$		0.16			0.16			0.16		μV
		$f = 0.1\text{ to }10\text{ Hz}$		0.47			0.47			0.47		
I_n	Equivalent input noise current			0.1			0.1			0.1		$\text{pA}/\sqrt{\text{Hz}}$
B_1	Unity-gain bandwidth	See Figure 3		1.7			1.7			1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3		47°			47°			47°		

TLE2022 operating characteristics at specified free-air temperature, $V_{CC} = \pm 15\text{ V}$

PARAMETER		TEST CONDITIONS	T_A	C SUFFIX†			I SUFFIX†			M SUFFIX†			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 10\text{ V}$, See Figure 1	25°C	0.45	0.65		0.45	0.65		0.45	0.65		$\text{V}/\mu\text{s}$
			Full range	0.45			0.42			0.4			
V_n	Equivalent input noise voltage (see Figure 2)	$f = 10\text{ Hz}$	25°C		19	50		19	50		19		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$	25°C		15	30		15	30		15		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ to }1\text{ Hz}$	25°C		0.16			0.16			0.16		μV
		$f = 0.1\text{ to }10\text{ Hz}$	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		$\text{pA}/\sqrt{\text{Hz}}$
B_1	Unity-gain bandwidth	See Figure 3	25°C		2.8			2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		52°			52°			52°		

† Full range is 0°C to 70°C for the C-suffix devices, -40°C to 85°C for the I suffix devices and -55°C to 125°C for the I-suffix devices.

TLE2024 operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	C SUFFIX			I SUFFIX			M SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 1 V to 3 V, See Figure 1	0.5			0.5			0.5			V/μs
V _n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	21			21			21			nV/√Hz
		f = 1 kHz	17			17			17			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	0.16			0.16			0.16			μV
		f = 0.1 to 10 Hz	0.47			0.47			0.47			
I _n	Equivalent input noise current		0.1			0.1			0.1			pA/√Hz
B ₁	Unity-gain bandwidth	See Figure 3	1.7			1.7			1.7			MHz
φ _m	Phase margin at unity gain	See Figure 3	47°			47°			47°			

TLE2024 operating characteristics at specified free-air temperature, $V_{CC} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A	C SUFFIX†			I SUFFIX†			M SUFFIX†			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±10 V, See Figure 1	25°C	0.45	0.7		0.45	0.7		0.45	0.7		V/μs
			Full range	0.45			0.42			0.4			
V _n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C	19		50	19		50	19			nV/√Hz
		f = 1 kHz	25°C	15		30	15		30	15			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C	0.16			0.16			0.16			μV
		f = 0.1 to 10 Hz	25°C	0.47			0.47			0.47			
I _n	Equivalent input noise current		25°C	0.1			0.1			0.1			pA/√Hz
B ₁	Unity-gain bandwidth	See Figure 3	25°C	2.8			2.8			2.8			MHz
φ _m	Phase margin at unity gain	See Figure 3	25°C	52°			52°			52°			

† Full range is 0°C to 70°C for the C-suffix devices, -40°C to 85°C for the I suffix devices and -55°C to 125°C for the I-suffix devices.

TLE202x, TLE202xA, TLE202xB, TLE202xY

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TLE2021Y electrical characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLE2021Y			UNIT
		MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$		150		μV
Input offset voltage long-term drift (see Note 4)			0.005		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current			0.5		nA
I_{IB} Input bias current			35		nA
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$		-0.3 to 4		V
V_{OH} Maximum high-level output voltage	$R_L = 10\ \text{k}\Omega$		4.3		V
V_{OL} Maximum low-level output voltage			0.7		V
A_{VD} Large-signal differential voltage amplification	$V_O = 1.4\text{ to }4\text{ V}$, $R_L = 10\ \text{k}\Omega$		1.5		$\text{V}/\mu\text{V}$
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{ min}$, $R_S = 50\ \Omega$		100		dB
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = 5\text{ V to }30\text{ V}$		115		dB
I_{CC} Supply current	$V_O = 2.5\text{ V}$, No load		400		μA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2021Y operating characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TLE2021Y			UNIT
		MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1\text{ V to }3\text{ V}$		0.5		$\text{V}/\mu\text{s}$
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$		21		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$		17		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ to }1\text{ Hz}$		0.16		μV
	$f = 0.1\text{ to }10\text{ Hz}$		0.47		
I_n Equivalent input noise current			0.1		$\text{pA}/\sqrt{\text{Hz}}$
B_1 Unity-gain bandwidth			1.7		MHz
ϕ_m Phase margin at unity gain			47°		

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TLE2022Y electrical characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLE2022Y			UNIT
		MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$		150	600	μV
Input offset voltage long-term drift (see Note 4)			0.005		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current			0.5		nA
I_{IB} Input bias current			35		nA
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$		– 0.3 to 4		V
V_{OH} Maximum high-level output voltage	$R_L = 10\ \text{k}\Omega$		4.3		V
V_{OL} Maximum low-level output voltage			0.7		V
A_{VD} Large-signal differential voltage amplification	$V_O = 1.4\text{ to }4\text{ V}$, $R_L = 10\ \text{k}\Omega$		1.5		$\text{V}/\mu\text{V}$
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{ min}$, $R_S = 50\ \Omega$		100		dB
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = 5\text{ V to }30\text{ V}$		115		dB
I_{CC} Supply current	$V_O = 2.5\text{ V}$, No load		450		μA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2022Y operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TLE2022Y			UNIT
		MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1\text{ V to }3\text{ V}$, See Figure 1		0.5		$\text{V}/\mu\text{s}$
V_n Equivalent input noise voltage (see Figure 2)	$f = 10\text{ Hz}$		21		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$		17		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ to }1\text{ Hz}$		0.16		μV
	$f = 0.1\text{ to }10\text{ Hz}$		0.47		
I_n Equivalent input noise current			0.1		$\text{pA}/\sqrt{\text{Hz}}$
B_1 Unity-gain bandwidth	See Figure 3		1.7		MHz
ϕ_m Phase margin at unity gain	See Figure 3		47°		

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TLE2024Y electrical characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

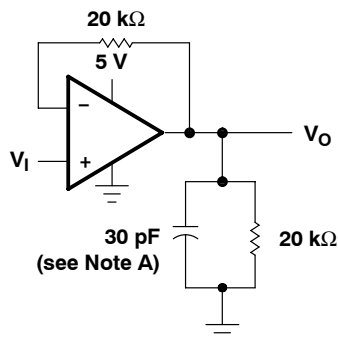
PARAMETER	TEST CONDITIONS	TLE2024Y			UNIT
		MIN	TYP	MAX	
Input offset voltage long-term drift (see Note 4)			0.005		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current	$V_{IC} = 0$, $R_S = 50\ \Omega$		0.6		nA
I_{IB} Input bias current			45		nA
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$		-0.3 to 4		V
V_{OH} High-level output voltage	$R_L = 10\ \text{k}\Omega$		4.2		V
V_{OL} Low-level output voltage			0.7		V
A_{VD} Large-signal differential voltage amplification	$V_O = 1.4\text{ V to }4\text{ V}$, $R_L = 10\ \text{k}\Omega$		1.5		$\text{V}/\mu\text{V}$
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$, $R_S = 50\ \Omega$		90		dB
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC} = 5\text{ V to }30\text{ V}$		112		dB
I_{CC} Supply current	$V_O = 2.5\text{ V}$, No load		800		μA

NOTE 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

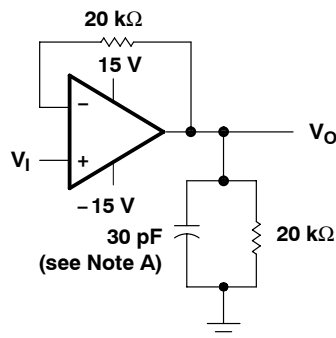
TLE2024Y operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TLE2024Y			UNIT
		MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1\text{ V to }3\text{ V}$, See Figure 1		0.5		$\text{V}/\mu\text{s}$
V_n Equivalent input noise voltage (see Figure 2)	$f = 10\text{ Hz}$		21		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$		17		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ to }1\text{ Hz}$		0.16		μV
	$f = 0.1\text{ to }10\text{ Hz}$		0.47		
I_n Equivalent input noise current			0.1		$\text{pA}/\sqrt{\text{Hz}}$
B_1 Unity-gain bandwidth	See Figure 3		1.7		MHz
ϕ_m Phase margin at unity gain	See Figure 3		47°		

PARAMETER MEASUREMENT INFORMATION



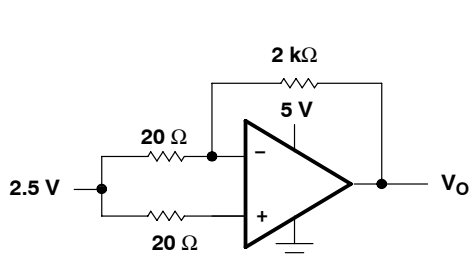
(a) SINGLE SUPPLY



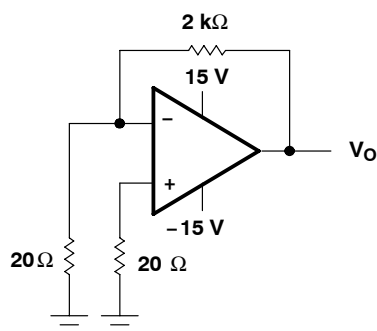
(b) SPLIT SUPPLY

NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

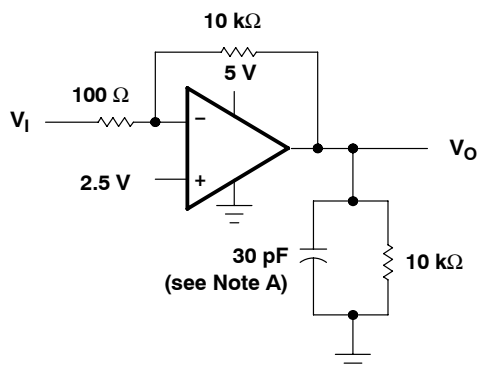


(a) SINGLE SUPPLY

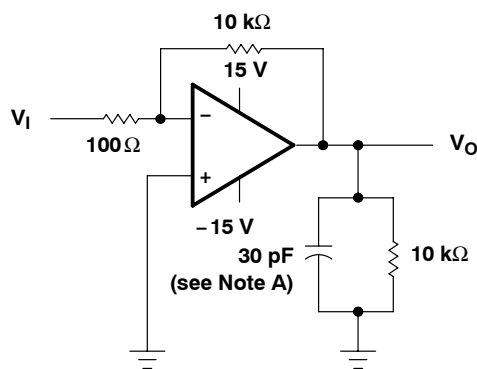


(b) SPLIT SUPPLY

Figure 2. Noise-Voltage Test Circuit



(a) SINGLE SUPPLY



(b) SPLIT SUPPLY

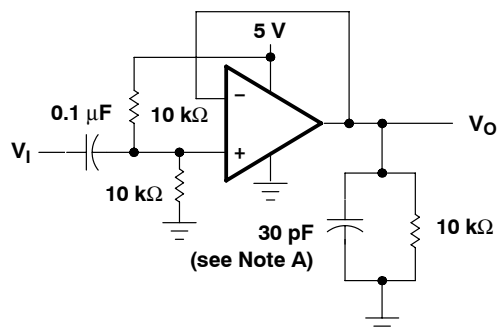
NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit

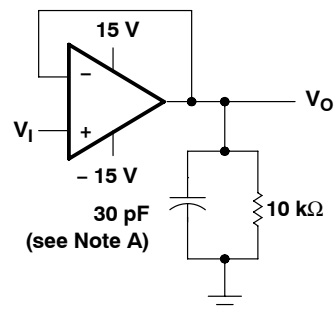
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PARAMETER MEASUREMENT INFORMATION



(a) SINGLE SUPPLY



(b) SPLIT SUPPLY

NOTE A: C_L includes fixture capacitance.

Figure 4. Small-Signal Pulse-Response Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	5, 6, 7
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	8, 9, 10 11, 12, 13
I_I	Input current	vs Differential input voltage	14
V_{OM}	Maximum peak output voltage	vs Output current vs Free-air temperature	15, 16, 17 18
V_{OH}	High-level output voltage	vs High-level output current vs Free-air temperature	19, 20 21
V_{OL}	Low-level output voltage	vs Low-level output current vs Free-air temperature	22 23
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	24, 25
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	26 27, 28, 29
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	30 – 33 34 – 37
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	38, 39, 40 41, 42, 43
CMRR	Common-mode rejection ratio	vs Frequency	44, 45, 46
SR	Slew rate	vs Free-air temperature	47, 48, 49
	Voltage-follower small-signal pulse response		50, 51
	Voltage-follower large-signal pulse response		52 – 57
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	0.1 to 1 Hz 0.1 to 10 Hz	58 59
V_n	Equivalent input noise voltage	vs Frequency	60
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	61, 62 63, 64
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	65, 66 67, 68 69, 70
	Phase shift	vs Frequency	26



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TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLE2021
INPUT OFFSET VOLTAGE**

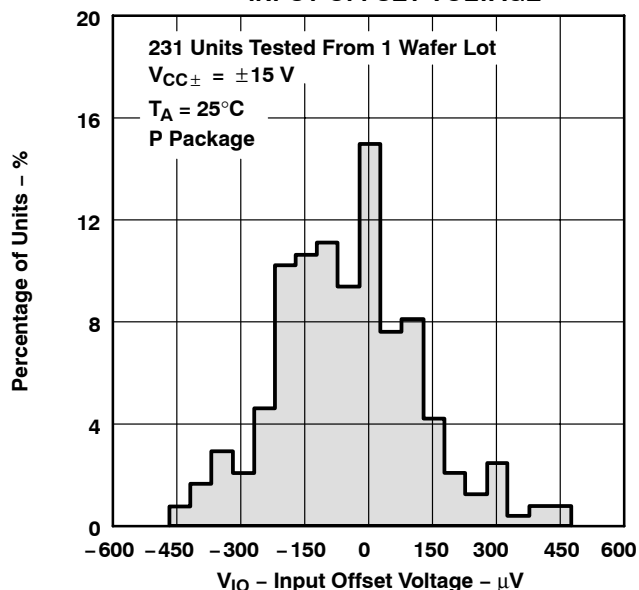


Figure 5

**DISTRIBUTION OF TLE2022
INPUT OFFSET VOLTAGE**

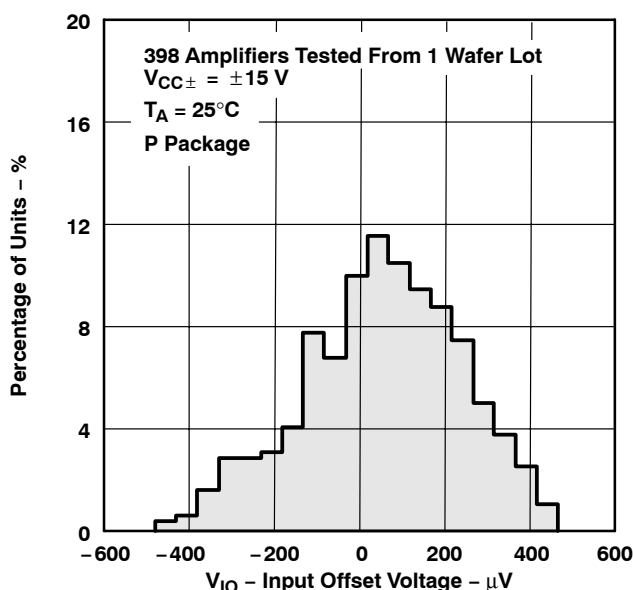


Figure 6

**DISTRIBUTION OF TLE2024
INPUT OFFSET VOLTAGE**

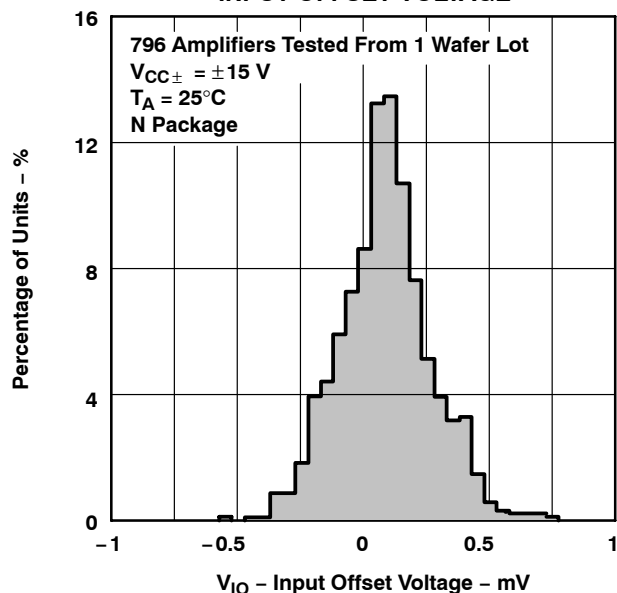


Figure 7

**TLE2021
INPUT BIAS CURRENT
vs**

COMMON-MODE INPUT VOLTAGE

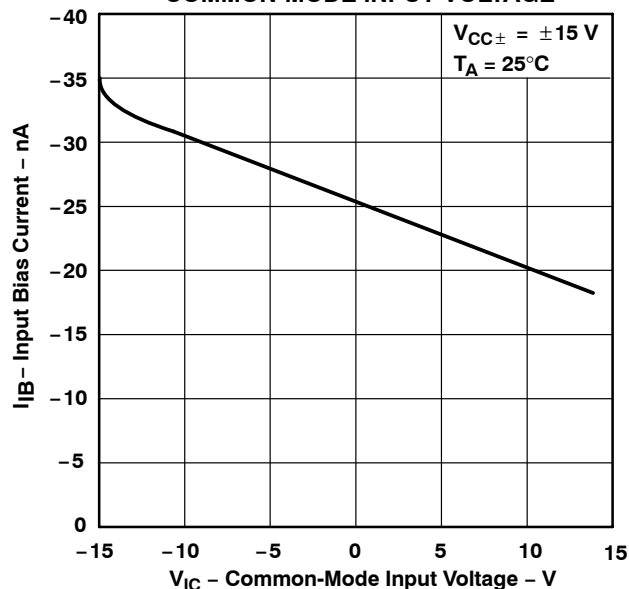
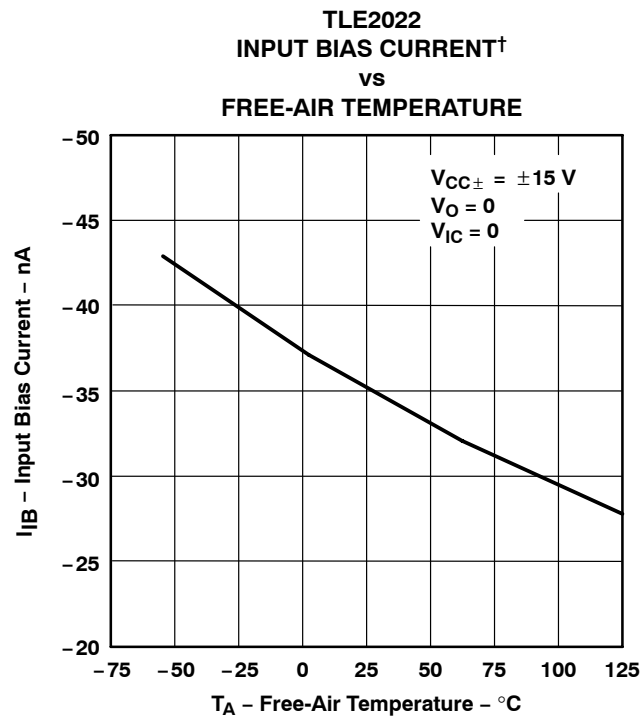
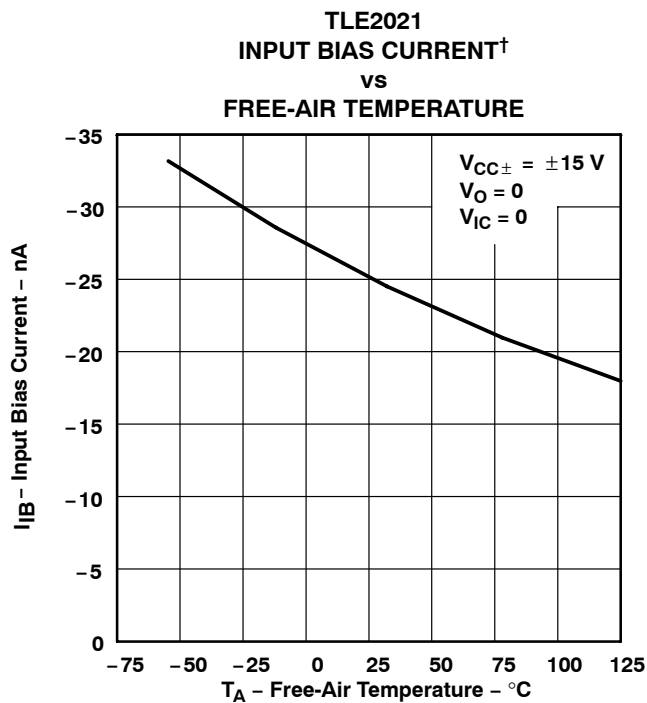
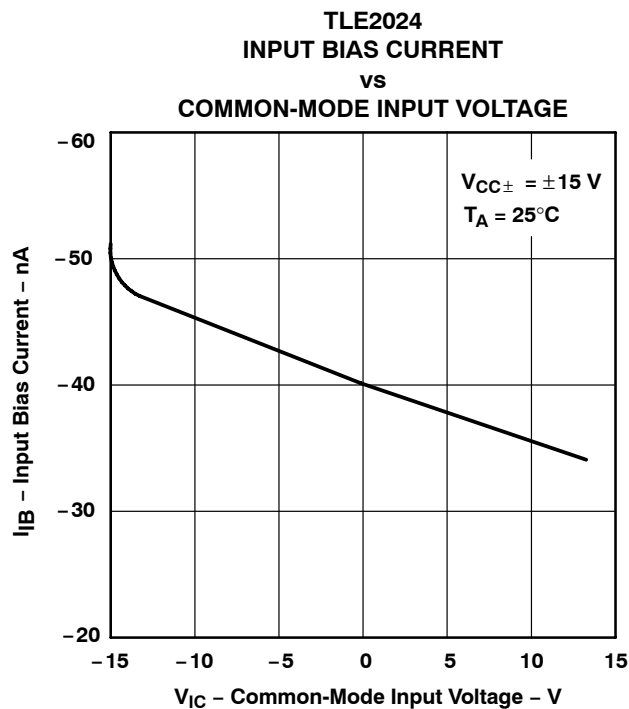
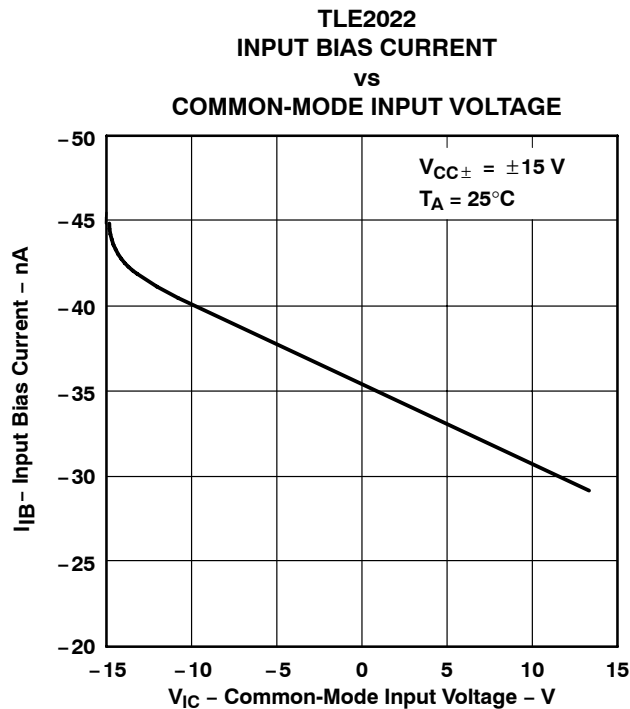


Figure 8

TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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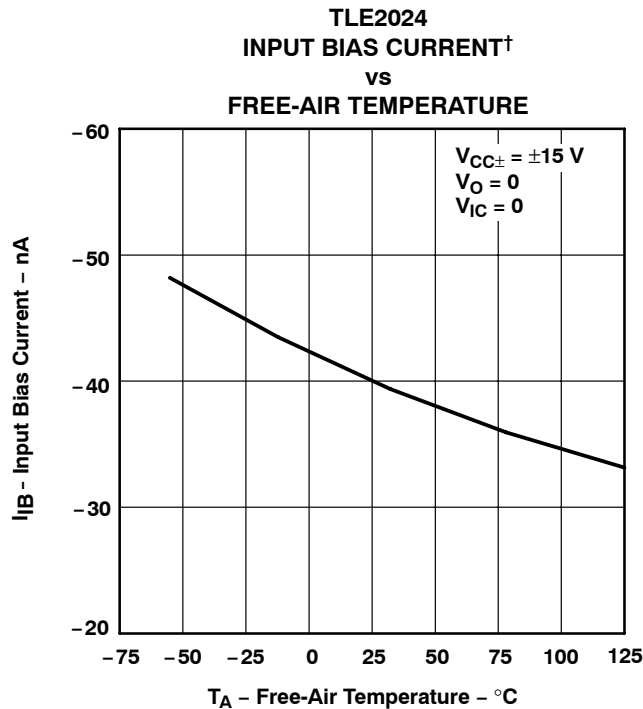


Figure 13

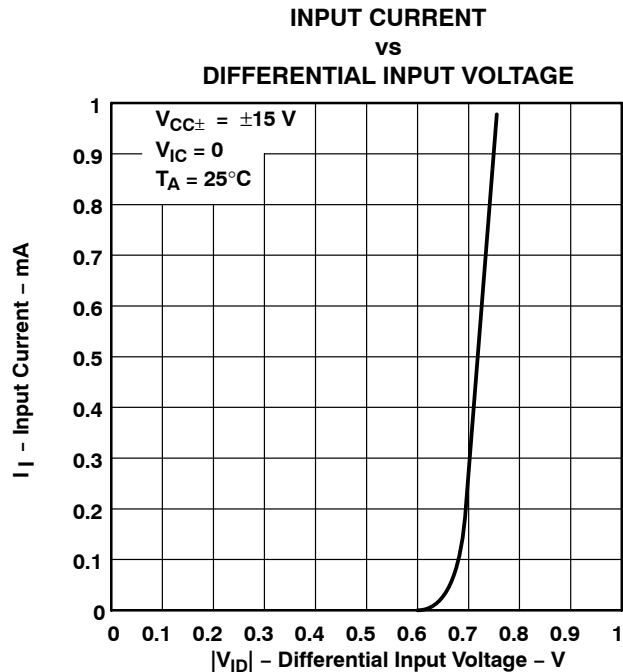


Figure 14

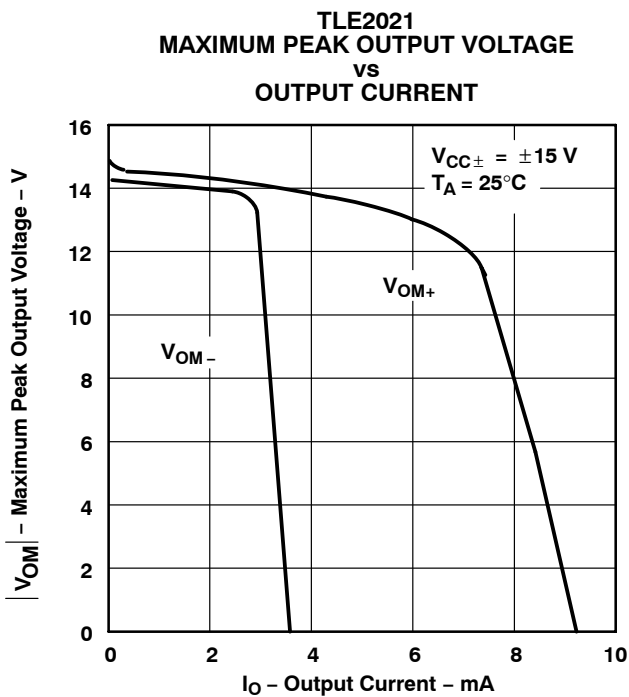


Figure 15

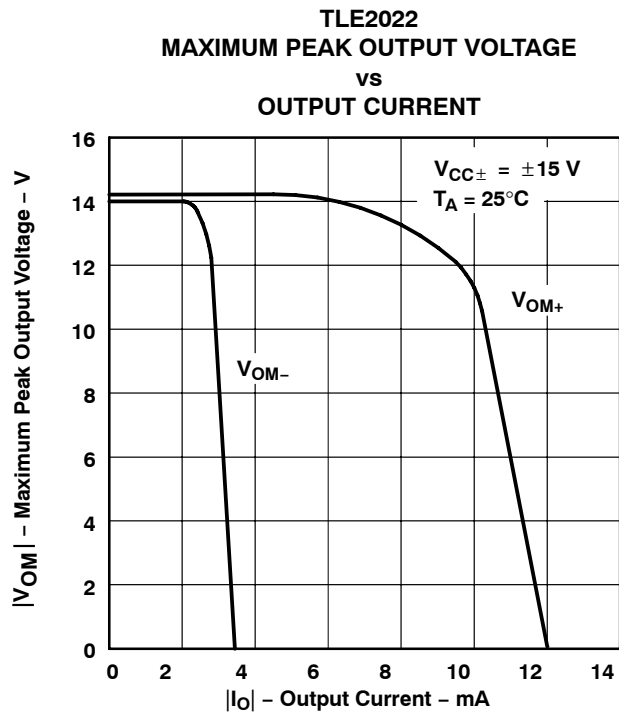


Figure 16

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

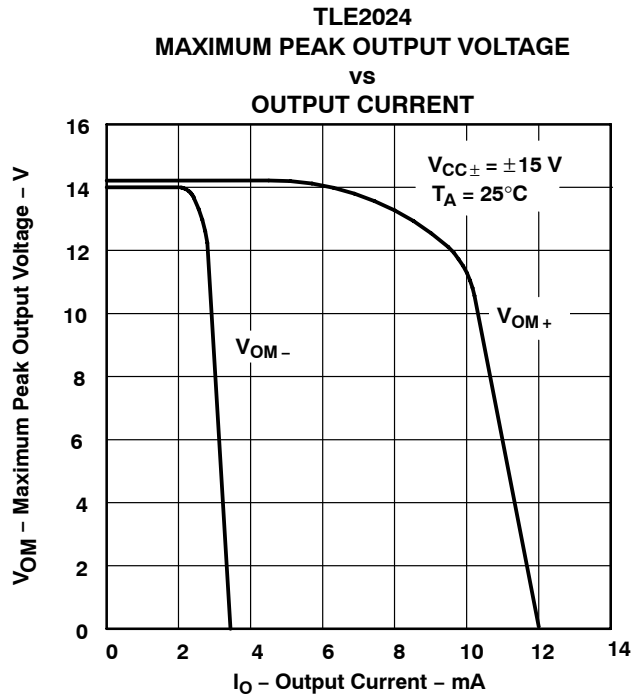


Figure 17

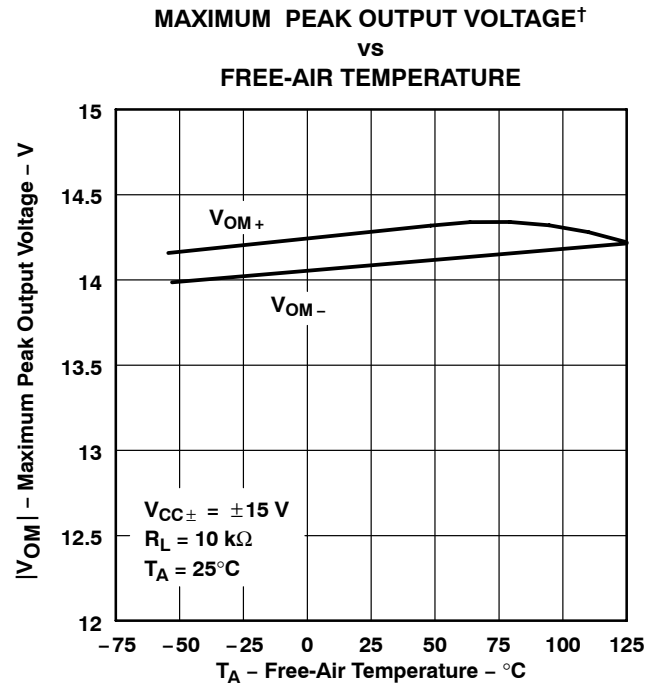


Figure 18

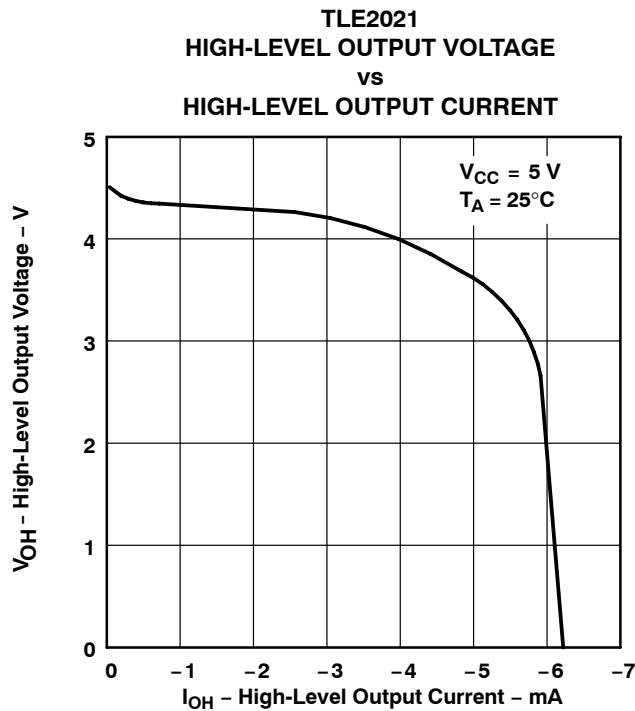


Figure 19

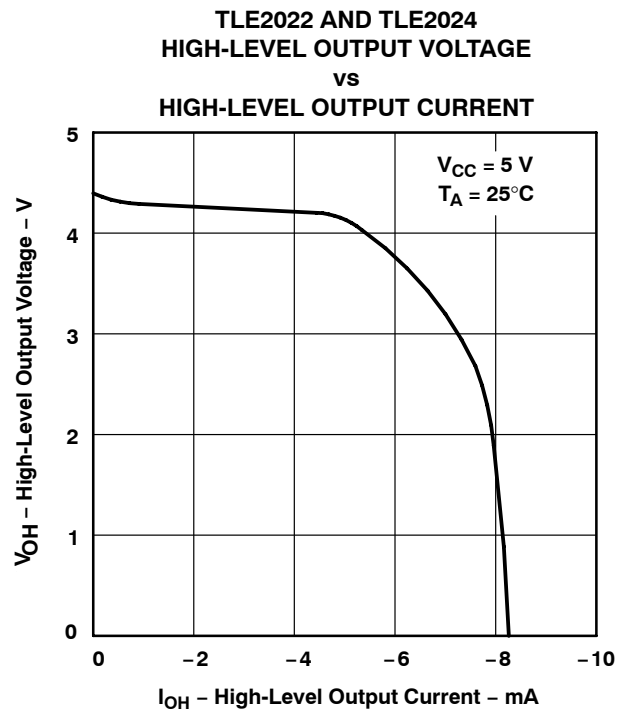


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

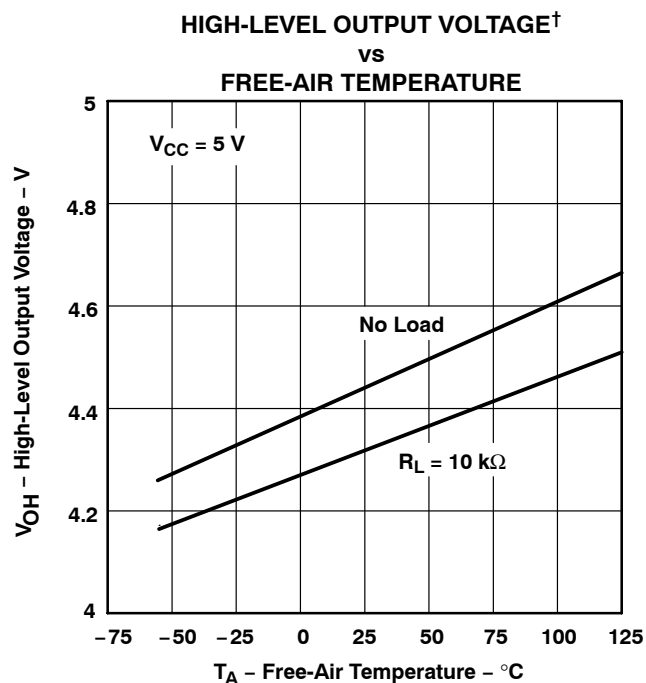


Figure 21

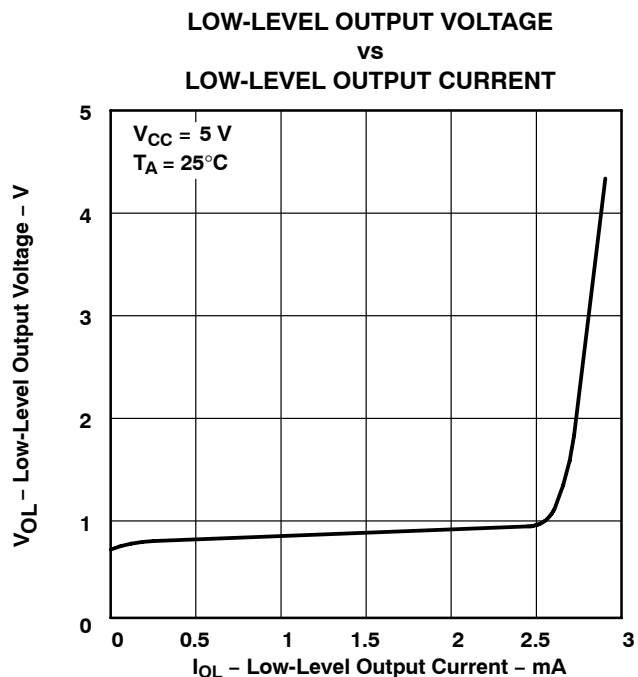


Figure 22

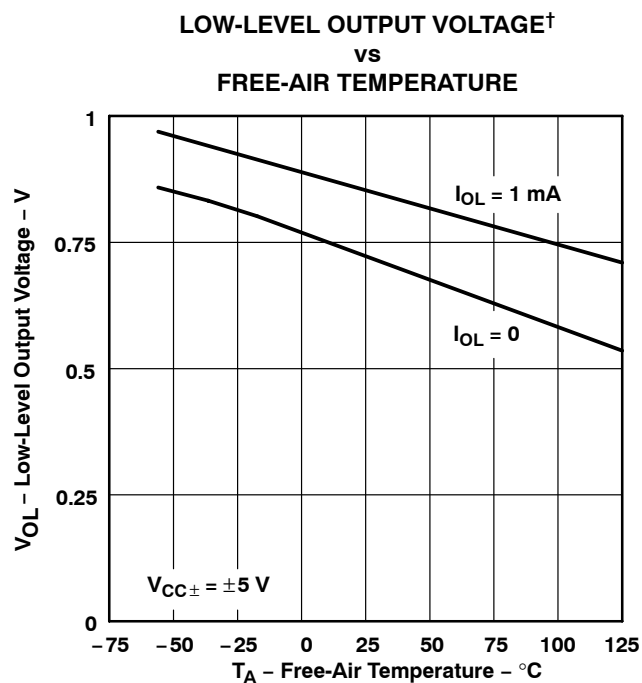


Figure 23

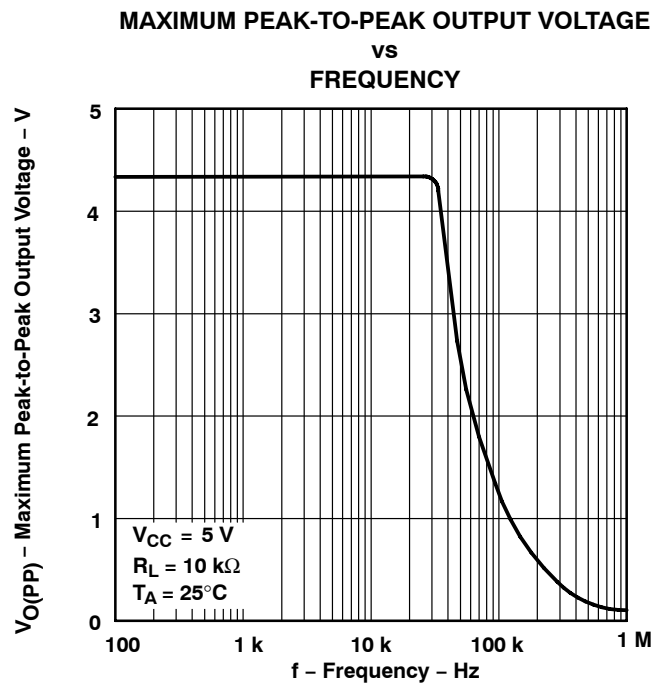


Figure 24

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

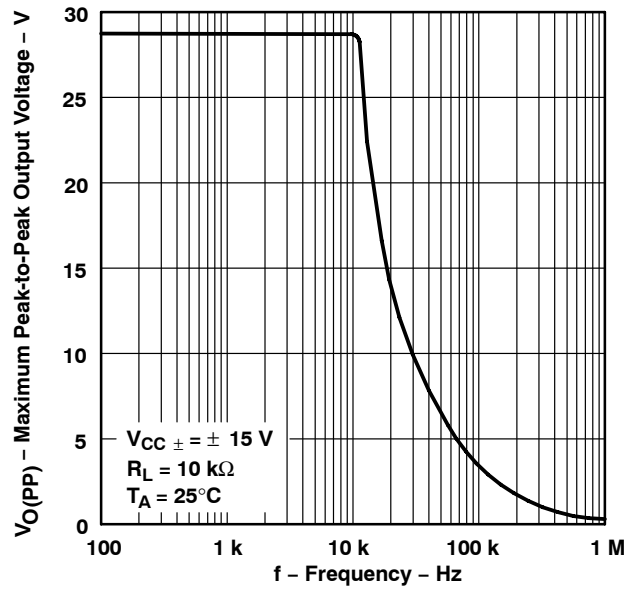


Figure 25

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

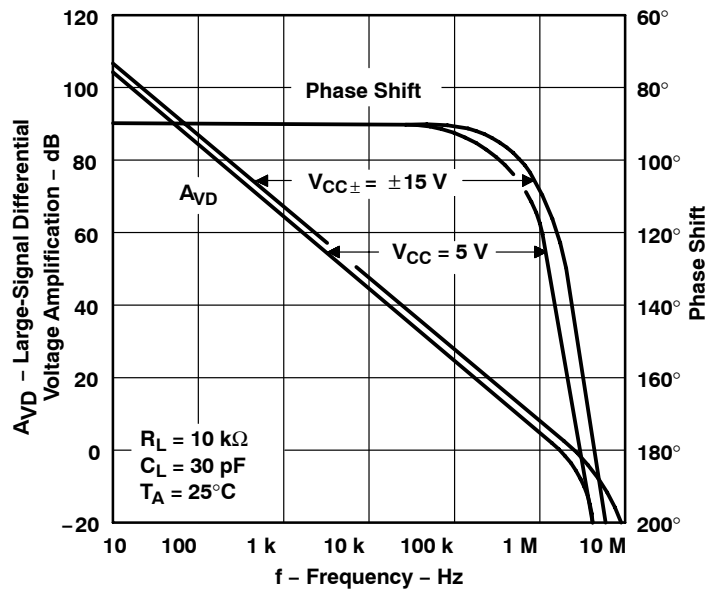


Figure 26

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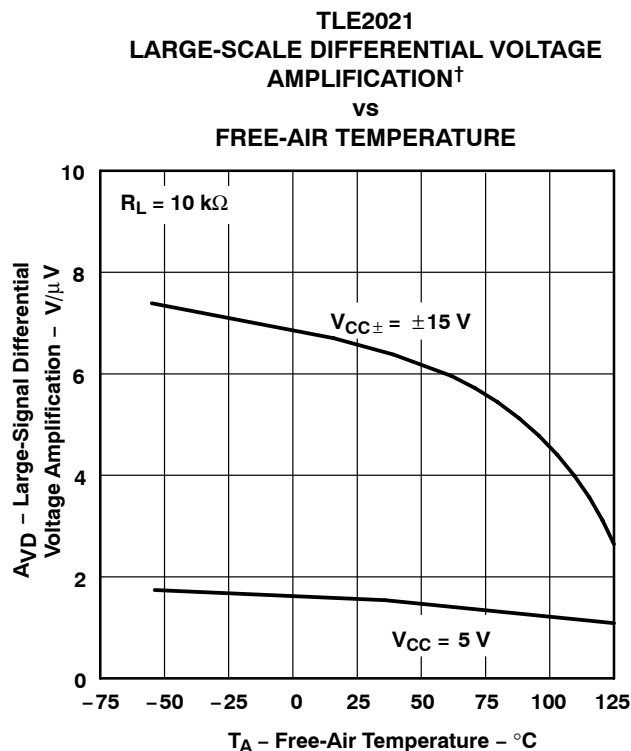


Figure 27

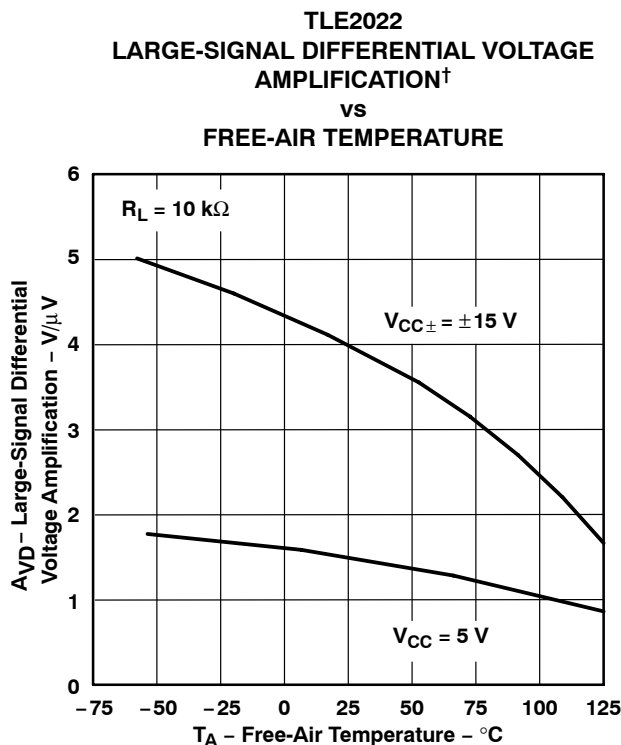


Figure 28

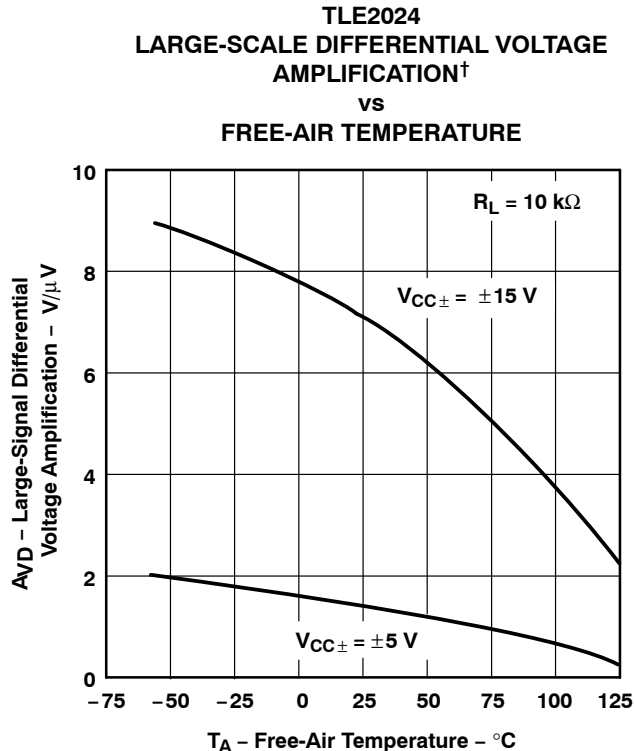


Figure 29

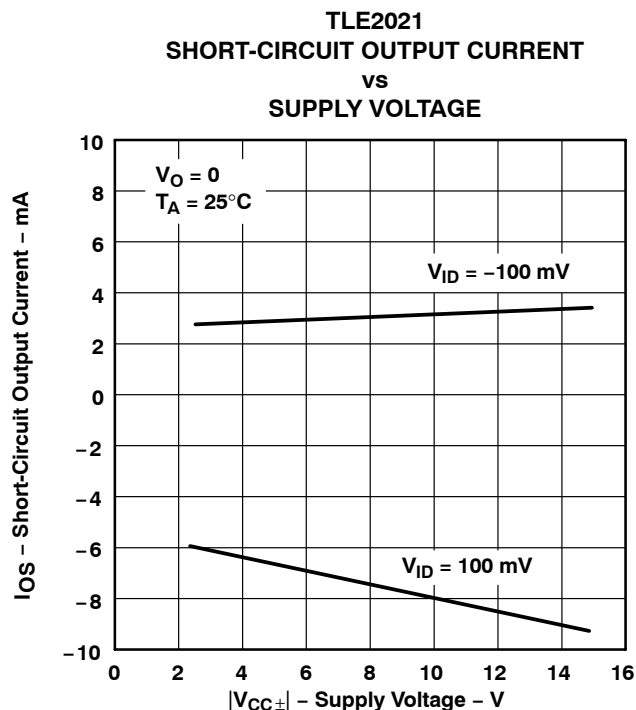


Figure 30

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

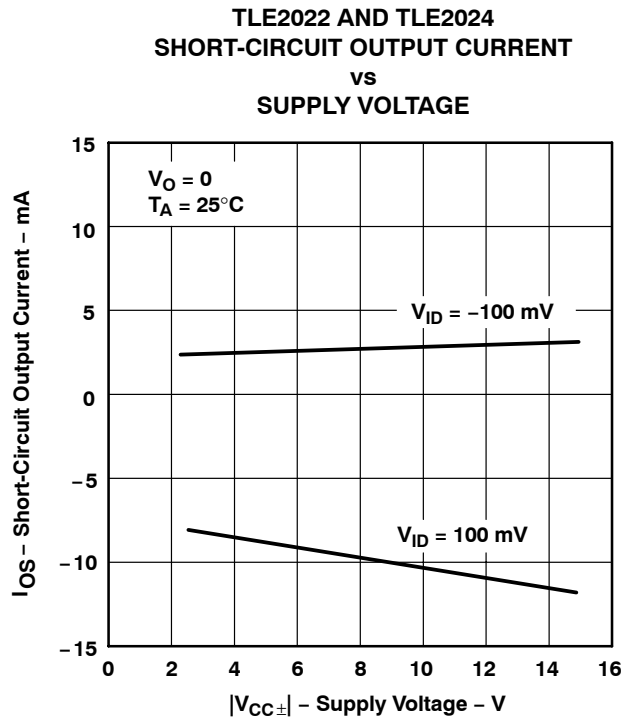


Figure 31

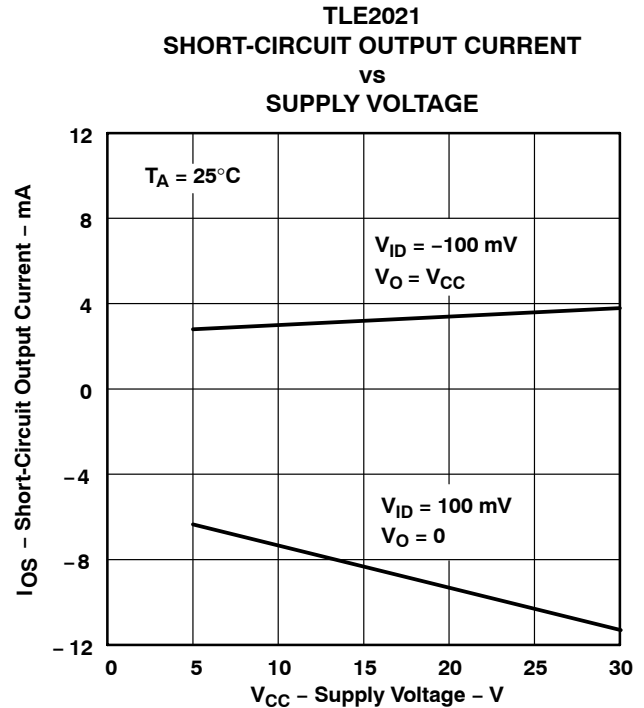


Figure 32

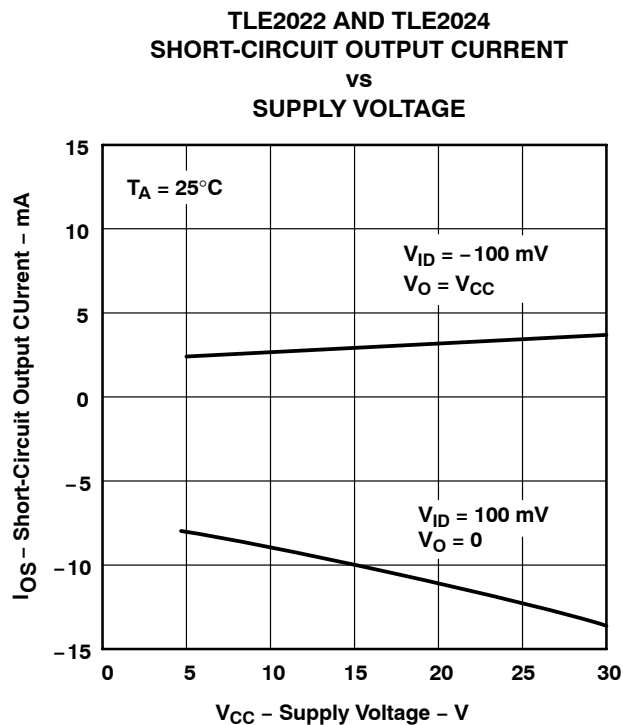


Figure 33

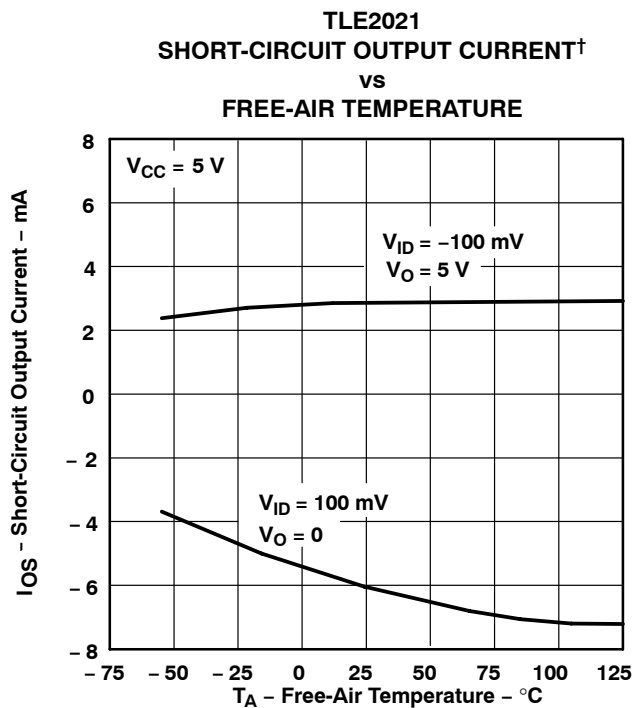


Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

**TLE2022 AND TLE2024
SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE**

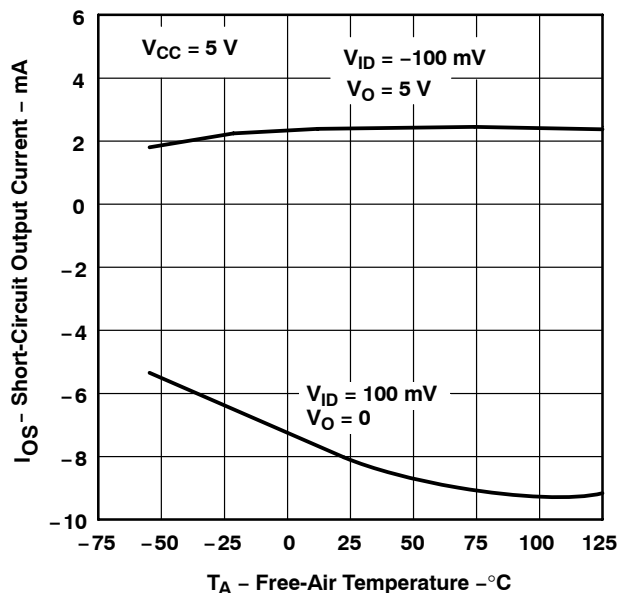


Figure 35

**TLE2021
SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE**

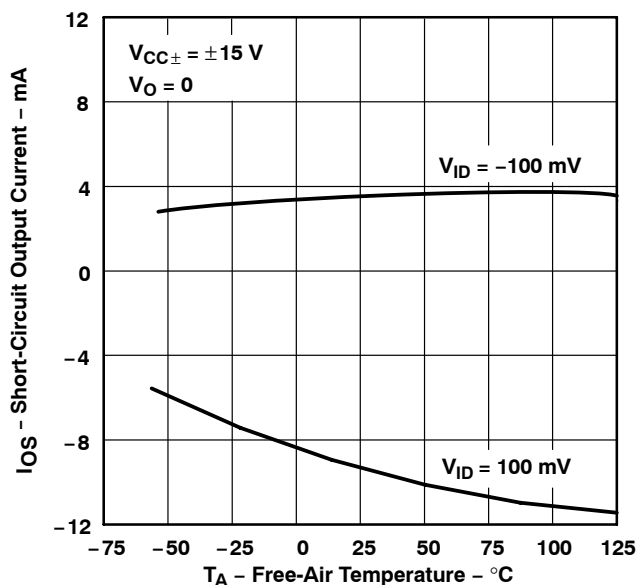


Figure 36

**TLE2022 AND TLE2024
SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE**

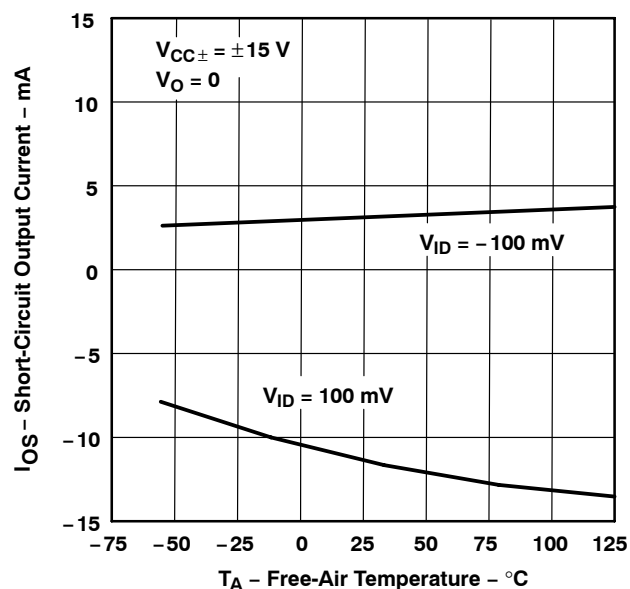


Figure 37

**TLE2021
SUPPLY CURRENT
vs
SUPPLY VOLTAGE**

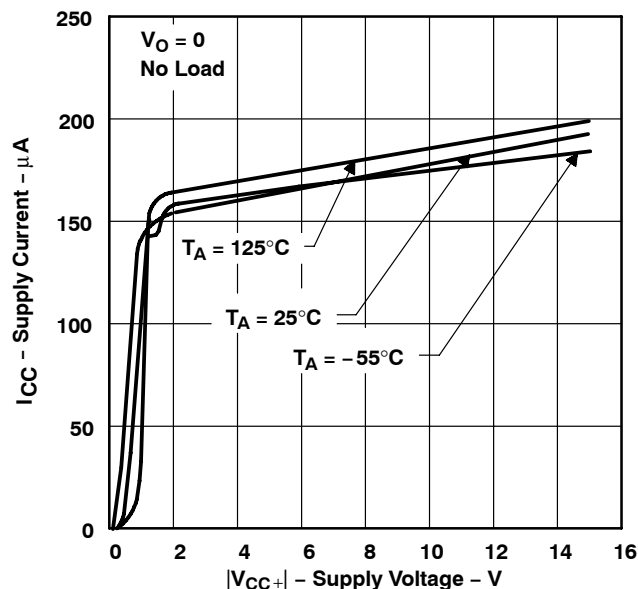


Figure 38

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

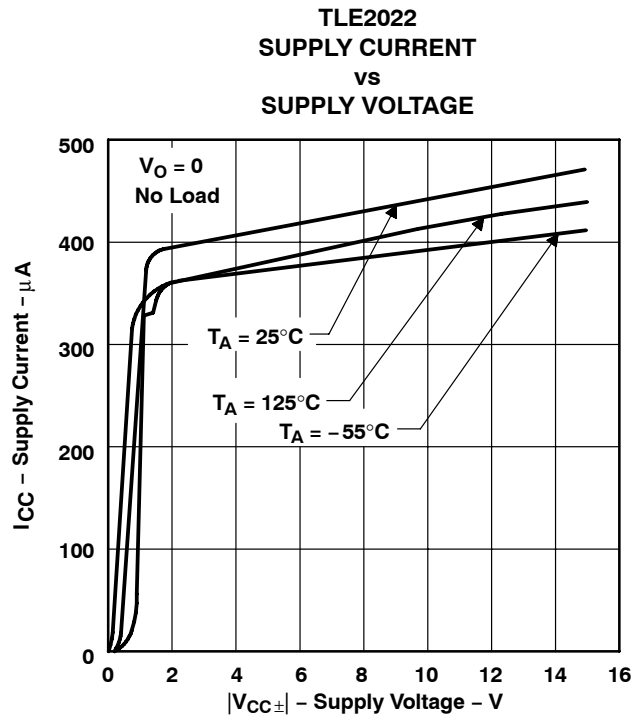


Figure 39

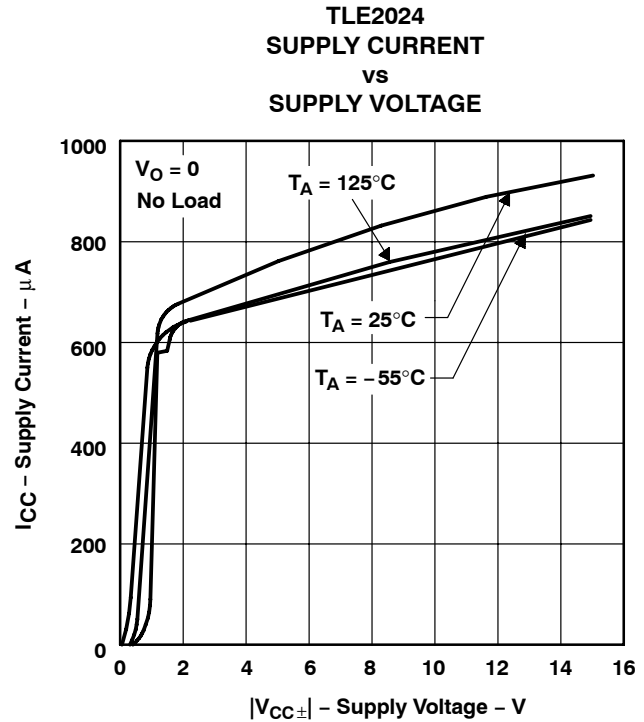


Figure 40

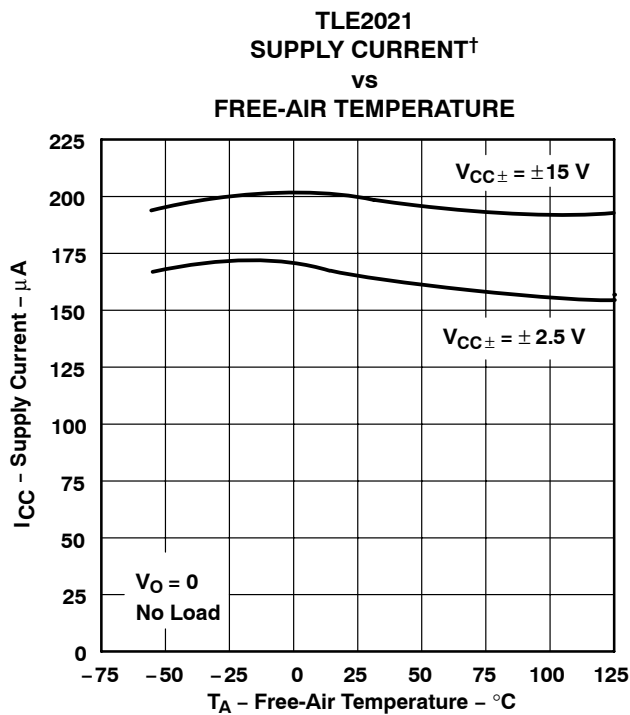


Figure 41

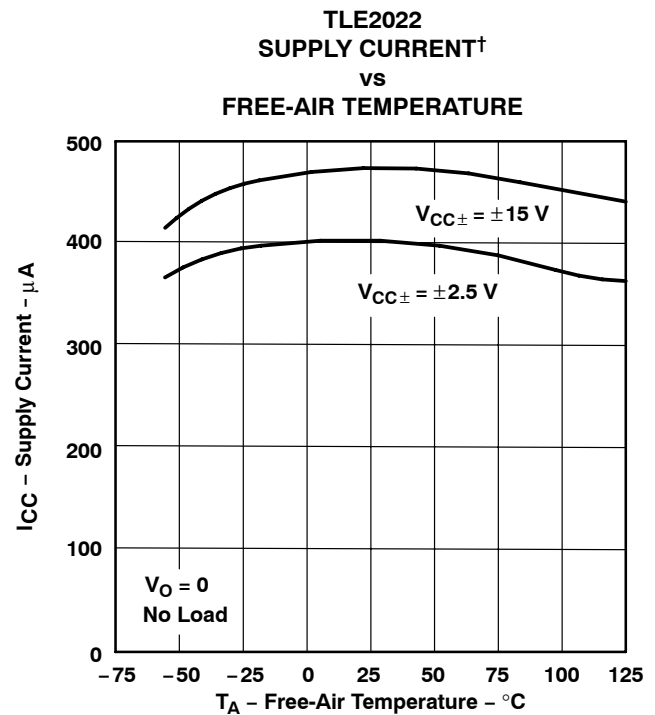


Figure 42

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

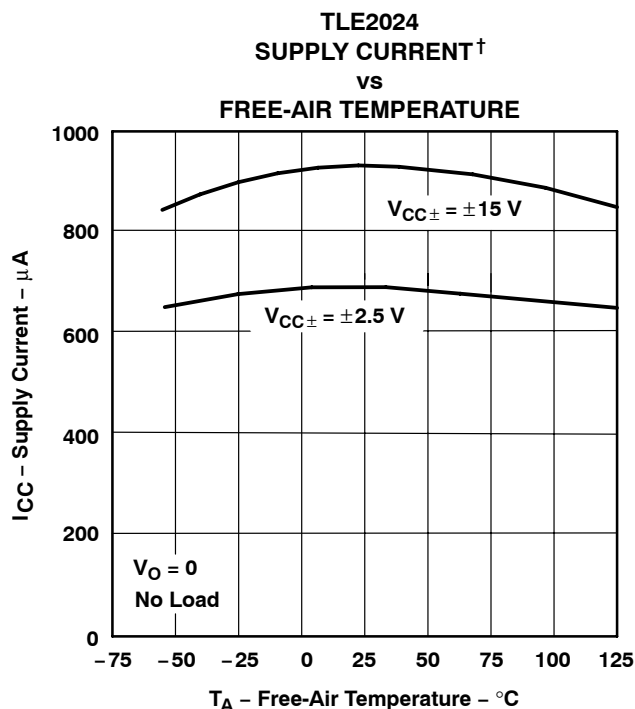


Figure 43

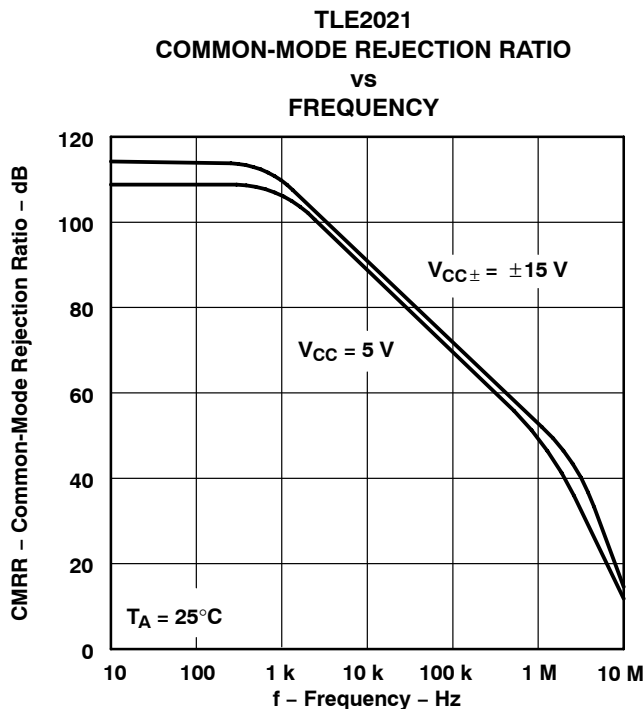


Figure 44

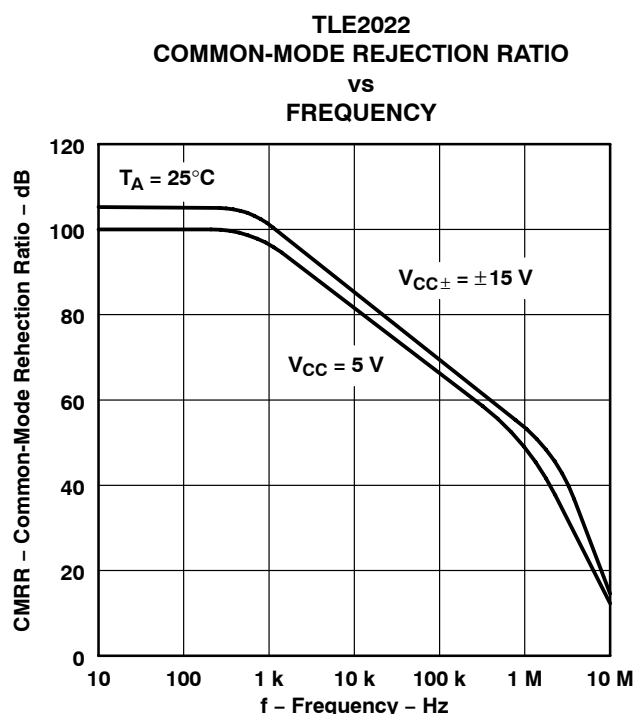


Figure 45

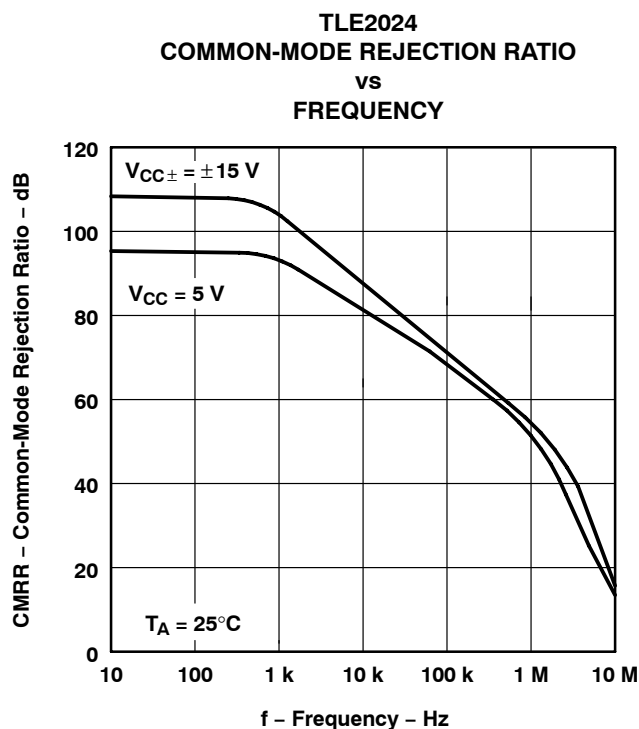


Figure 46

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

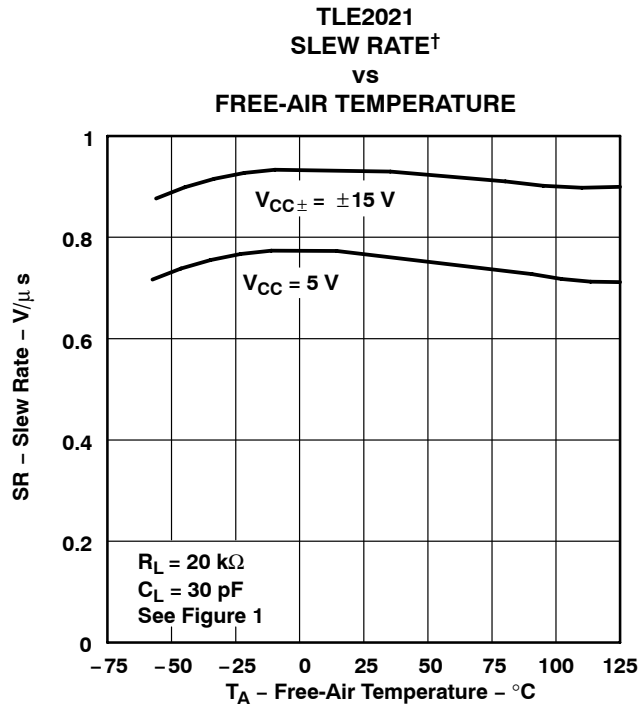


Figure 47

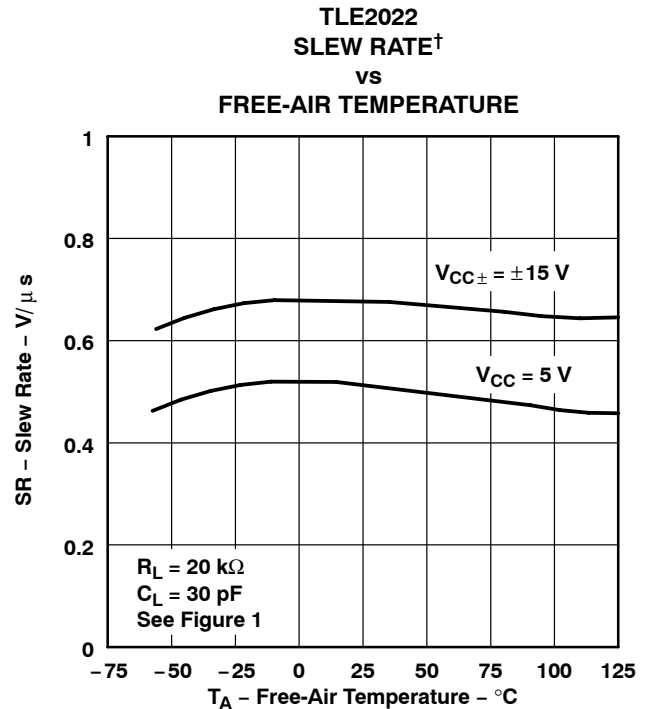


Figure 48

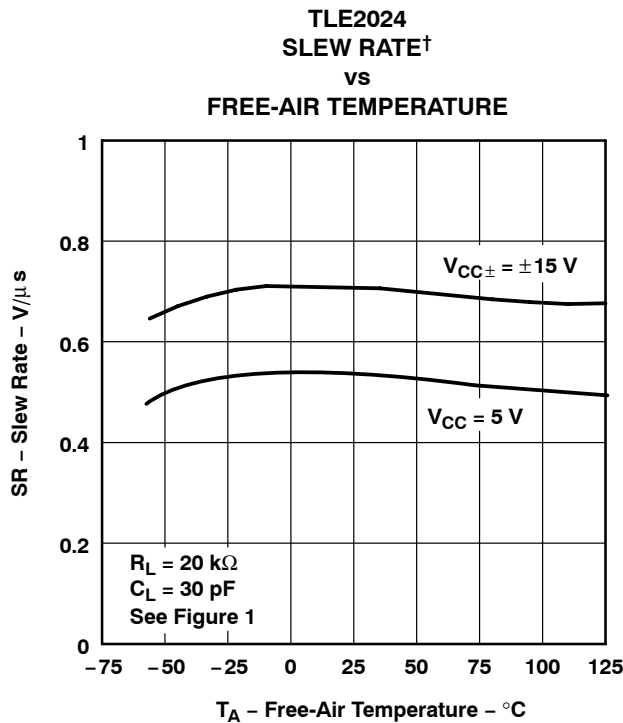


Figure 49

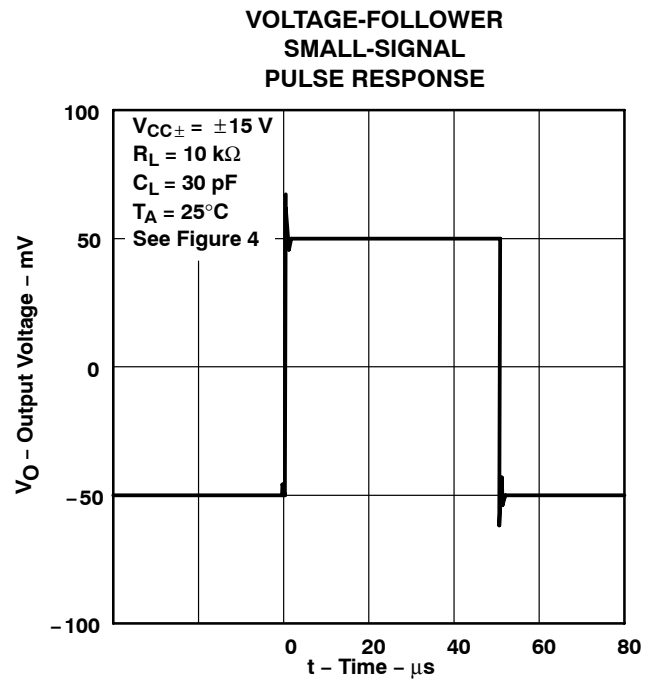


Figure 50

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

**VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE**

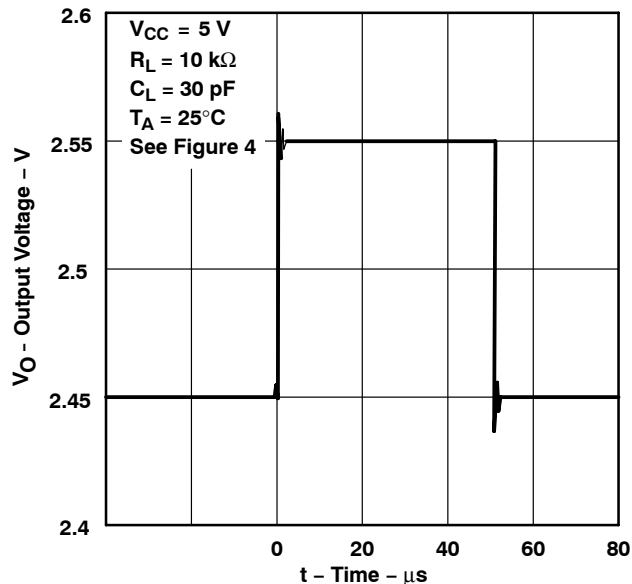


Figure 51

**TLE2021
VOLTAGE-FOLLOWER LARGE-SIGNAL
PULSE RESPONSE**

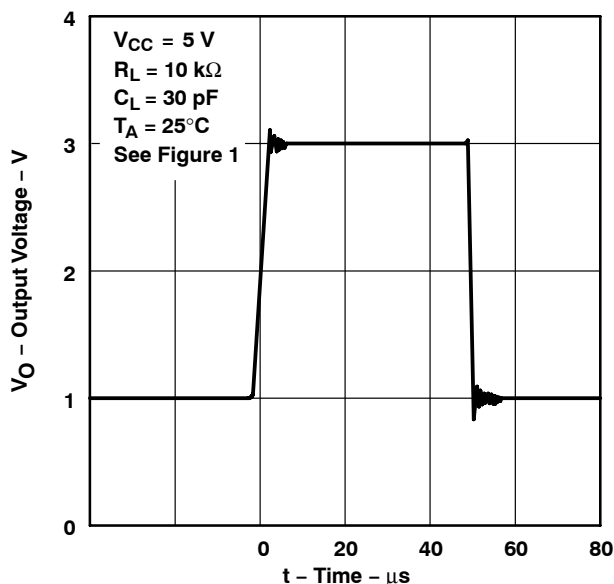


Figure 52

**TLE2022
VOLTAGE-FOLLOWER LARGE-SIGNAL
PULSE RESPONSE**

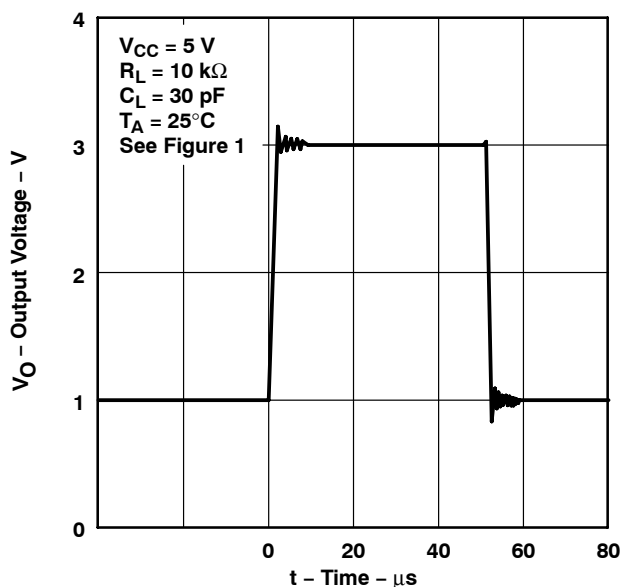


Figure 53

**TLE2024
VOLTAGE-FOLLOWER LARGE-SCALE
PULSE RESPONSE**

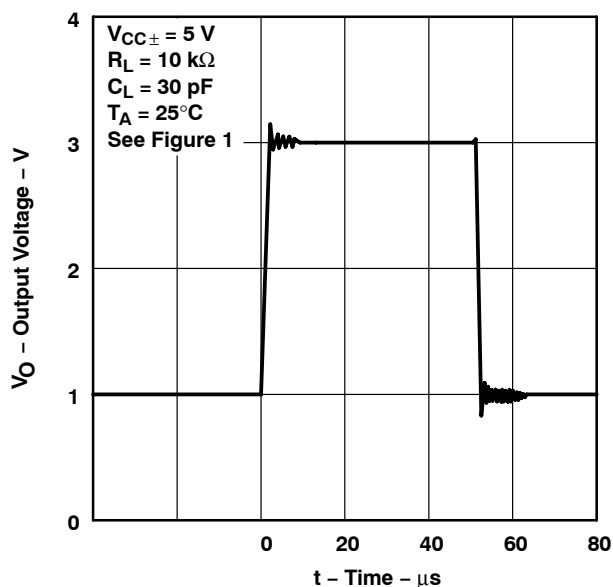


Figure 54

TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

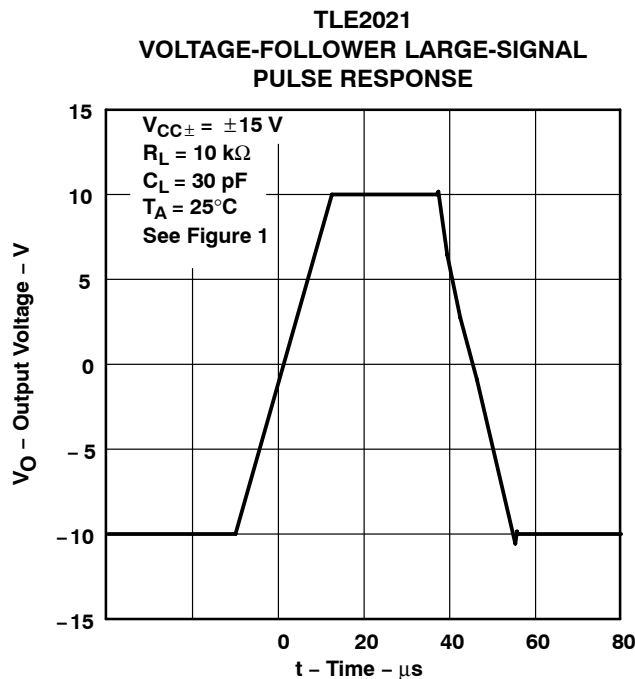


Figure 55

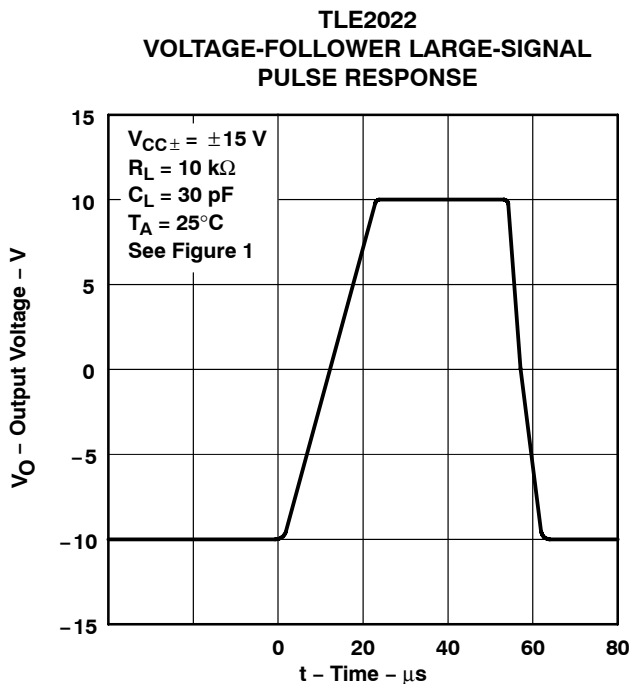


Figure 56

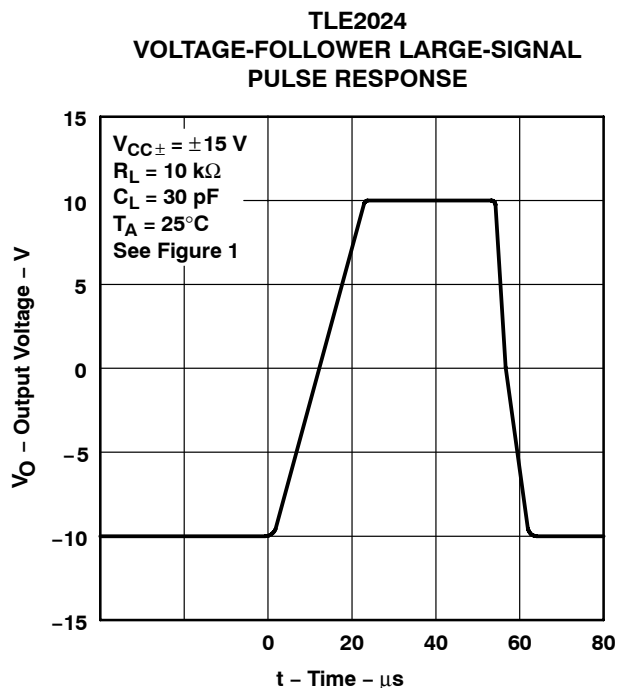


Figure 57

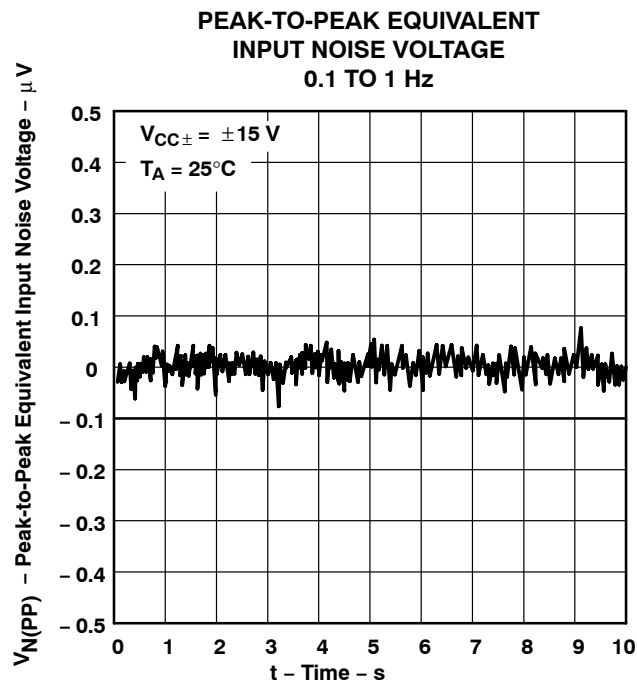


Figure 58

TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

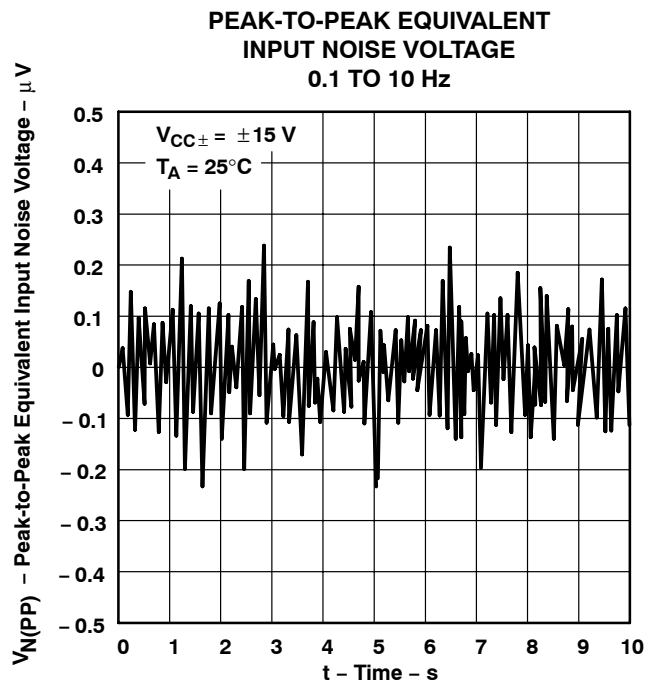


Figure 59

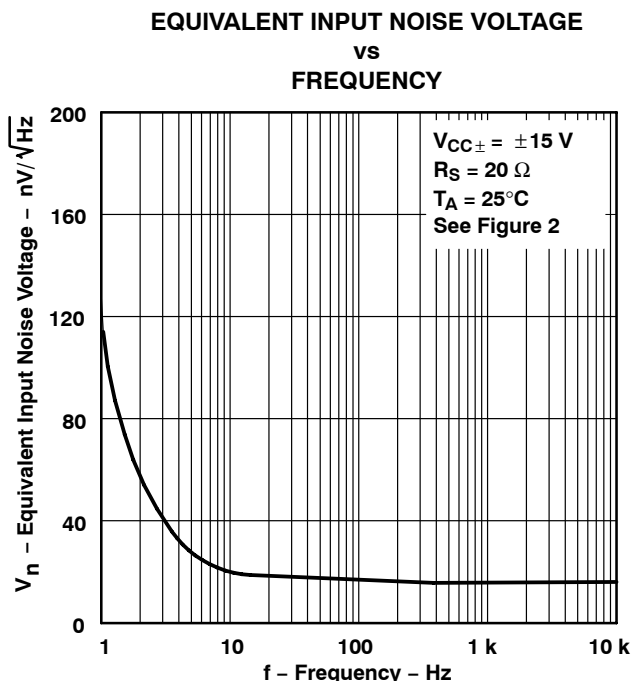


Figure 60

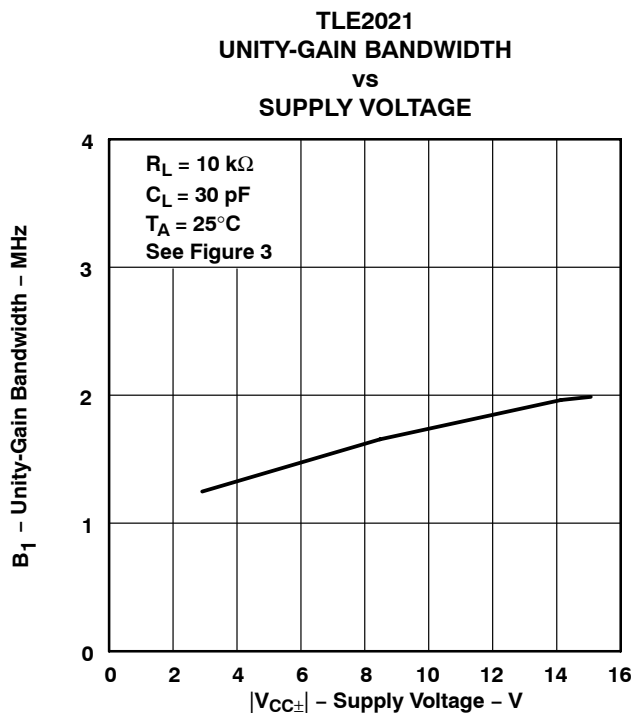


Figure 61

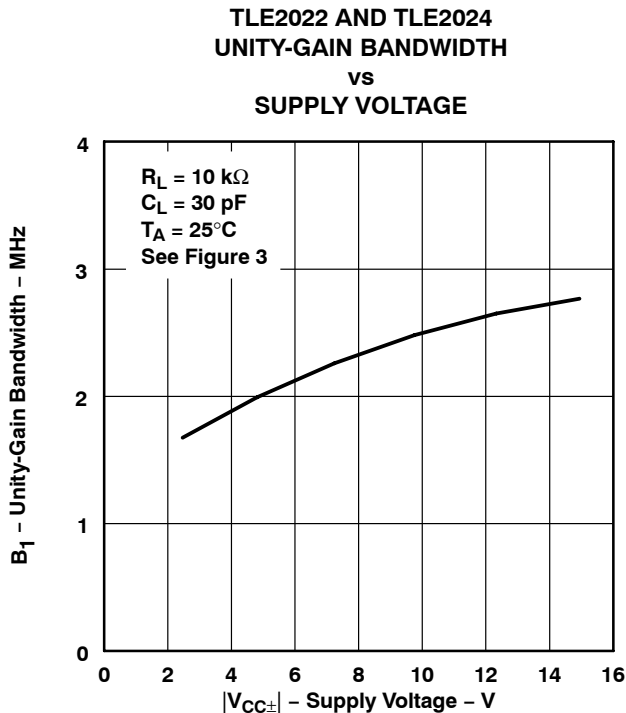


Figure 62

TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

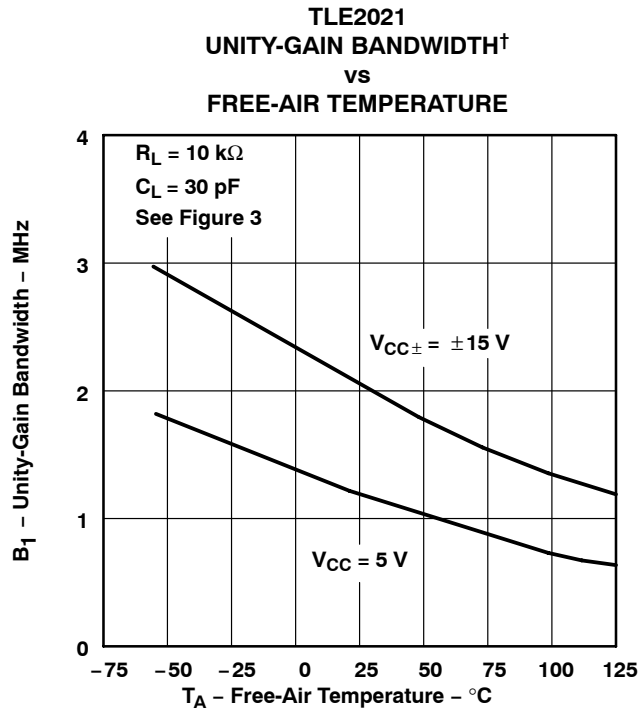


Figure 63

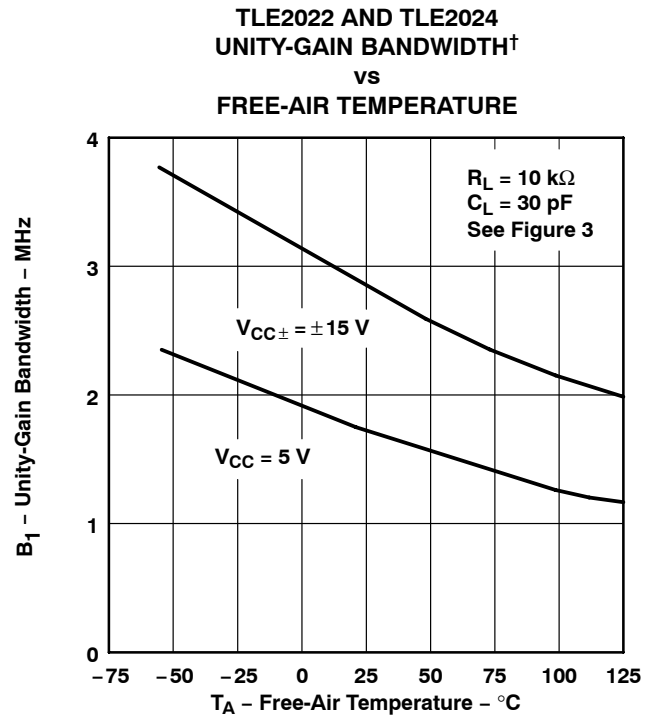


Figure 64

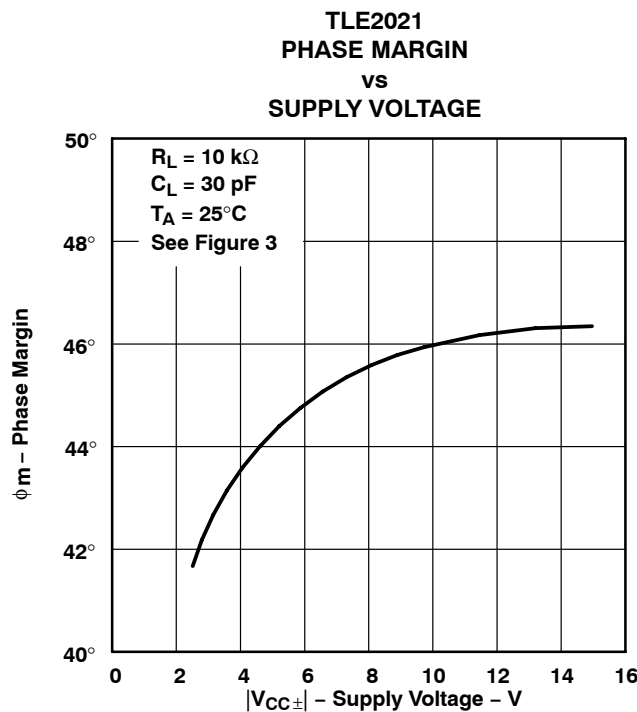


Figure 65

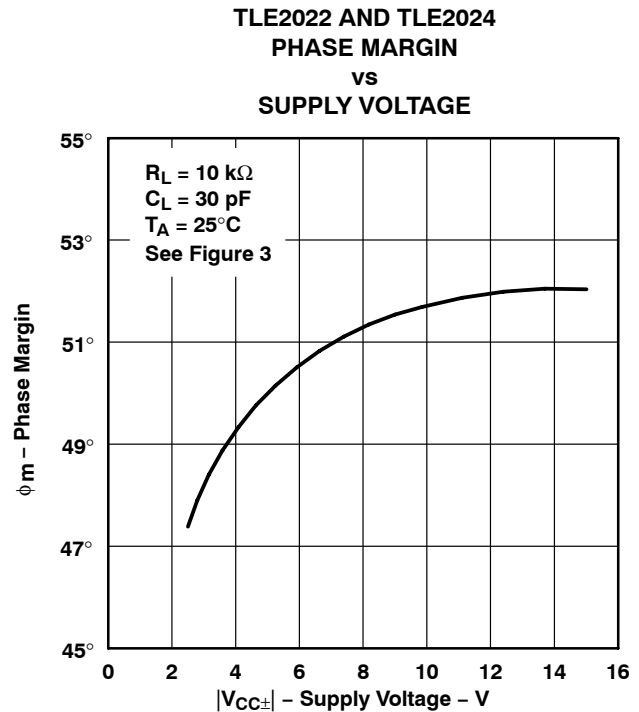


Figure 66

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

**TLE2021
PHASE MARGIN
vs
LOAD CAPACITANCE**

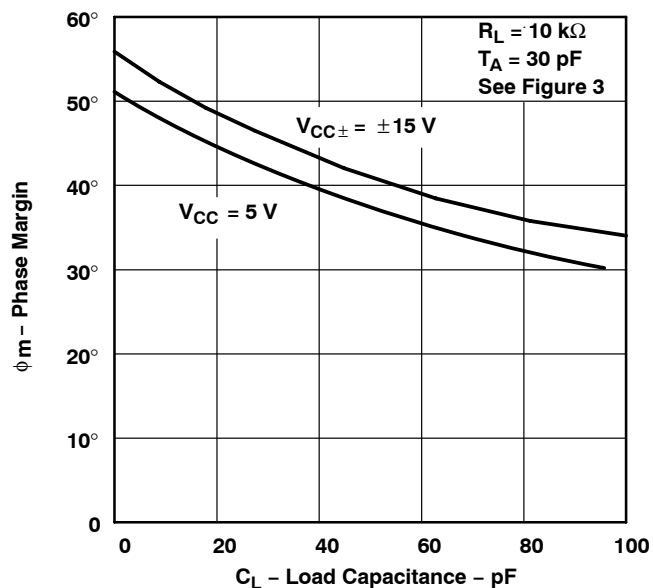


Figure 67

**TLE2022 AND TLE2024
PHASE MARGIN
vs
LOAD CAPACITANCE**

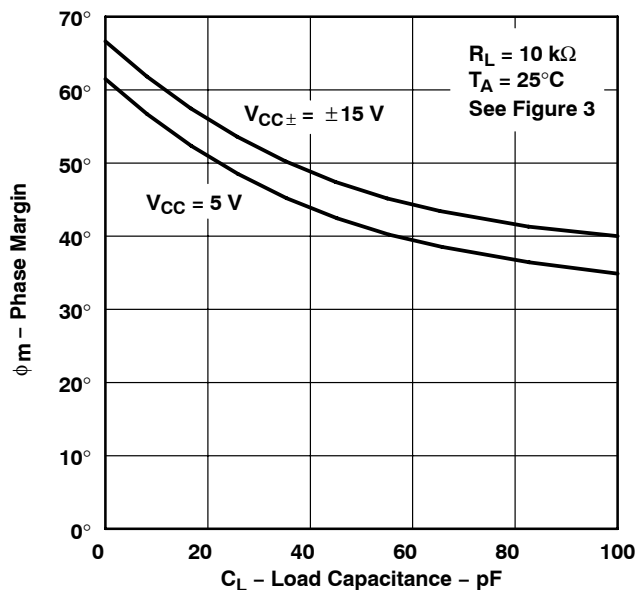


Figure 68

**TLE2021
PHASE MARGIN†
vs
FREE-AIR TEMPERATURE**

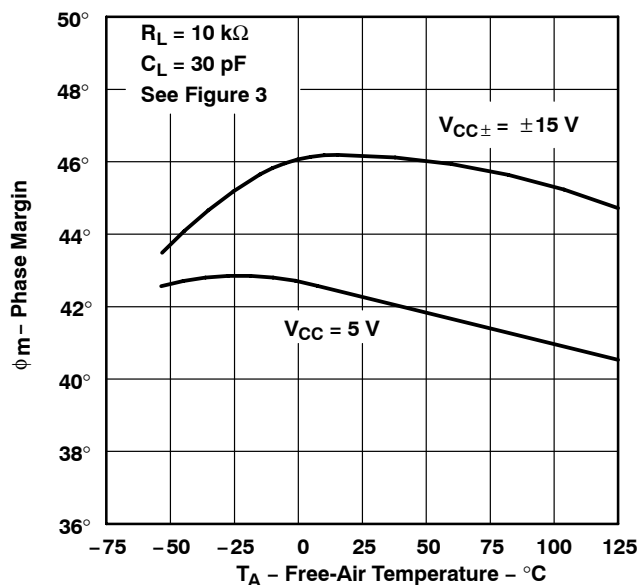


Figure 69

**TLE2022 AND TLE2024
PHASE MARGIN†
vs
FREE-AIR TEMPERATURE**

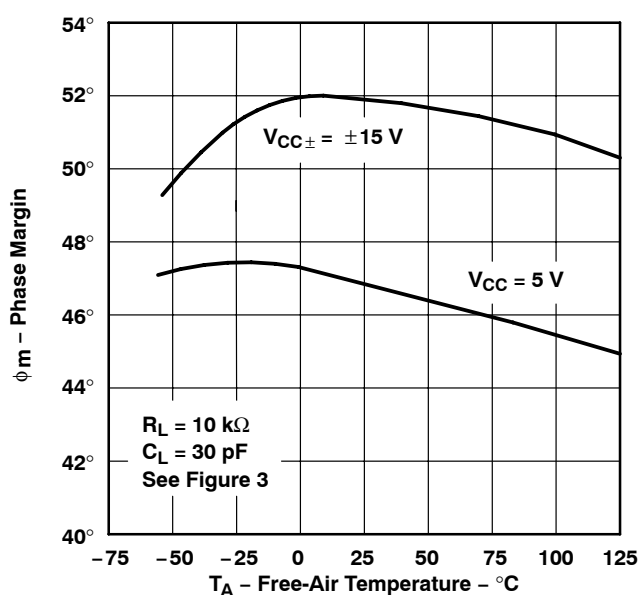


Figure 70

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

voltage-follower applications

The TLE202x circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. It is recommended that a feedback resistor be used to limit the current to a maximum of 1 mA to prevent degradation of the device. This feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10 k Ω , this pole degrades the amplifier phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 71).

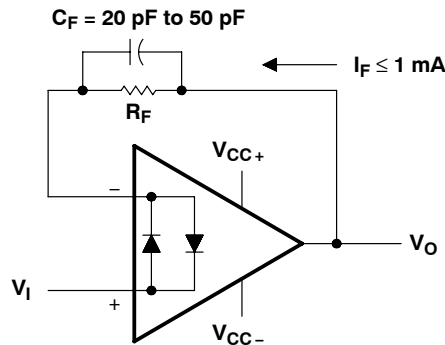


Figure 71. Voltage Follower

Input offset voltage nulling

The TLE202x series offers external null pins that further reduce the input offset voltage. The circuit in Figure 72 can be connected as shown if this feature is desired. When external nulling is not needed, the null pins may be left disconnected.

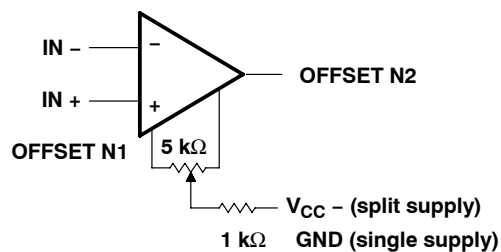


Figure 72. Input Offset Voltage Null Circuit

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APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 73, Figure 74, and Figure 75 were generated using the TLE202x typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

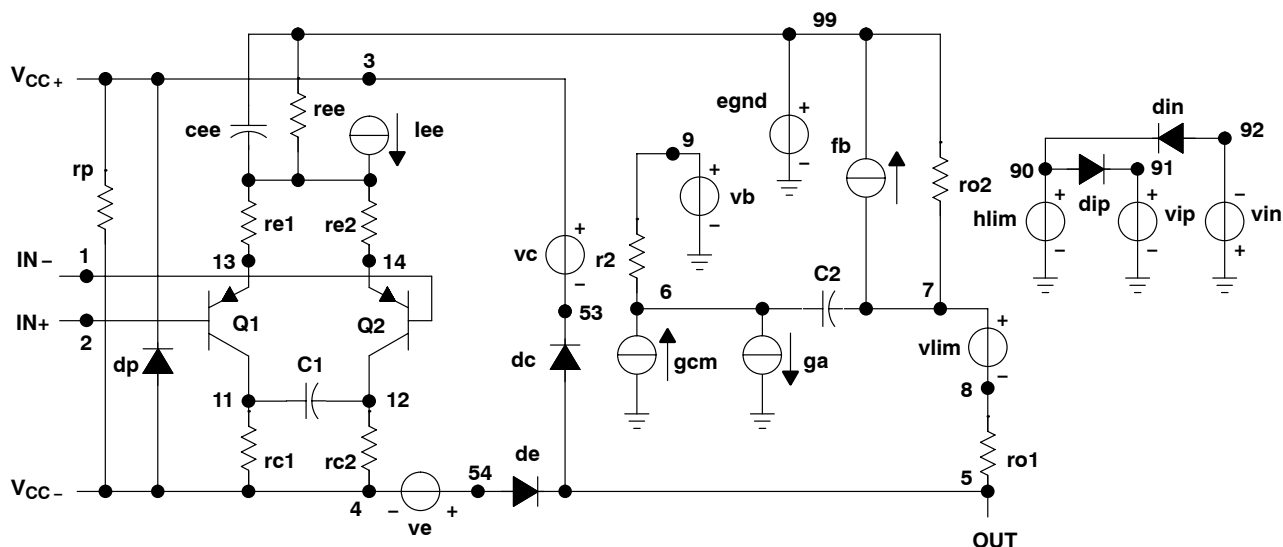


Figure 73. Boyle Subcircuit

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```
.SUBCKT TLE2021 1 2 3 4 5
*
c1 11 12 6.244E-12
c2 6 7 13.4E-12
c3 87 0 10.64E-9
cpsr 85 86 15.9E-9
dcm+ 81 82 dx
dcm- 83 81 dx
dc 5 53 dx
de 54 5 dx
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
ecmr 84 99 (2 99) 1
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
epsr 85 0 poly(1) (3,4) -60E-6 2.0E-6
ense 89 2 poly(1) (88,0) 120E-6 1
fb 7 99 poly(6) vb vc ve vlp vln vpsr 0 547.3E6
+ -50E7 50E7 50E7 -50E7 547E6
ga 6 0 11 12 188.5E-6
gcm 0 6 10 99 335.2E-12
gpsr 85 86 (85,86) 100E-6
grc1 4 11 (4,11) 1.885E-4
grc2 4 12 (4,12) 1.885E-4
gre1 13 10 (13,10) 6.82E-4
gre2 14 10 (14,10) 6.82E-4
hlim 90 0 vlim 1k

hcmr 80 1 poly(2) vcm+ vcm- 0 1E2 1E2
irp 3 4 185E-6
iee 3 10 dc 15.67E-6
iio 2 0 2E-9
ii 88 0 1E-21
q1 11 89 13 qx
q2 12 80 14 qx
R2 6 9 100.0E3
rcm 84 81 1K
ree 10 99 14.76E6
rn1 87 0 2.55E8
rn2 87 88 11.67E3
ro1 8 5 62
ro2 7 99 63
vcm+ 82 99 13.3
vcm- 83 99 -14.6
vb 9 0 dc 0
vc 3 53 dc 1.300
ve 54 4 dc 1.500
vlim 7 8 dc 0
vlp 91 0 dc 3.600
vln 0 92 dc 3.600
vpsr 0 86 dc 0
.model dx d(is=800.0E-18)
.model qx pnp(is=800.0E-18 bf=270)
.ends
```

Figure 74. Boyle Macromodel for the TLE2021

```
.SUBCKT TLE2022 1 2 3 4 5
*
c1 11 12 6.814E-12
c2 6 7 20.00E-12
dc 5 53 dx
de 54 5 dx
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb 7 99 poly(5) vb vc ve vlp vln 0
+ 45.47E6 -50E6 50E6 50E6 -50E6
ga 6 0 11 12 377.9E-6
gcm 0 6 10 99 7.84E-10
iee 3 10 DC 18.07E-6
hlim 90 0 vlim 1k
q1 11 2 13 qx
q2 12 1 14 qx
r2 6 9 100.0E3

rc1 4 11 2.842E3
rc2 4 12 2.842E3
ge1 13 10 (10,13) 31.299E-3
ge2 14 10 (10,14) 31.299E-3
ree 10 99 11.07E6
ro1 8 5 250
ro2 7 99 250
rp 3 4 137.2E3
vb 9 0 dc 0
vc 3 53 dc 1.300
ve 54 4 dc 1.500
vlim 7 8 dc 0
vlp 91 0 dc 3
vln 0 92 dc 3
.model dx d(is=800.0E-18)
.model qx pnp(is=800.0E-18 bf=257.1)
.ends
```

Figure 75. Boyle Macromodel for the TLE2022



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9088101MPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9088101MPA TLE2021M	Samples
5962-9088102M2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9088102M2A TLE2022MFKB	Samples
5962-9088102MPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9088102MPA TLE2022M	Samples
5962-9088103M2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9088103M2A TLE2024MFKB	Samples
5962-9088103MCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9088103MC A TLE2024MJB	Samples
5962-9088104Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9088104Q2A TLE2021 AMFKB	Samples
5962-9088104QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9088104QPA TLE2021AM	Samples
5962-9088105Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9088105Q2A TLE2022A MFKB	Samples
5962-9088105QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9088105QPA TLE2022AM	Samples
5962-9088106Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9088106Q2A TLE2024A MFKB	Samples
5962-9088106QCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9088106QC A TLE2024AMJB	Samples
5962-9088107Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9088107Q2A TLE2021	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										BMFKB	
5962-9088107QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9088107QPA TLE2021BM	Samples
5962-9088108Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9088108Q2A TLE2022B MFKB	Samples
5962-9088108QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9088108QPA TLE2022BM	Samples
5962-9088109Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9088109Q2A TLE2024 BMFKB	Samples
5962-9088109QCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9088109QC A TLE2024BMJB	Samples
TLE2021ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2021AC	Samples
TLE2021ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2021AC	Samples
TLE2021ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		TLE2021AC	Samples
TLE2021AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2021AI	Samples
TLE2021AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2021AI	Samples
TLE2021AIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		TLE2021AI	Samples
TLE2021AMFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9088104Q2A TLE2021 AMFKB	Samples
TLE2021AMJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9088104QPA TLE2021AM	Samples
TLE2021BMFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type		5962- 9088107Q2A TLE2021 BMFKB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2021BMJG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TLE2021 BMJG	Samples
TLE2021BMJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type		9088107QPA TLE2021BM	Samples
TLE2021CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2021C	Samples
TLE2021CDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2021C	Samples
TLE2021CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2021C	Samples
TLE2021CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLE2021CP	Samples
TLE2021CPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLE2021CP	Samples
TLE2021ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2021I	Samples
TLE2021IDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2021I	Samples
TLE2021IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2021I	Samples
TLE2021IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2021I	Samples
TLE2021IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLE2021IP	Samples
TLE2021MD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2021M	Samples
TLE2021MDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2021M	Samples
TLE2021MJG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TLE2021MJG	Samples
TLE2021MJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9088101MPA TLE2021M	Samples
TLE2022ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2022AC	Samples
TLE2022ACDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2022AC	Samples
TLE2022ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2022AC	Samples
TLE2022ACDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2022AC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2022ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		TLE2022AC	Samples
TLE2022ACPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		TLE2022AC	Samples
TLE2022AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2022AI	Samples
TLE2022AIDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2022AI	Samples
TLE2022AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2022AI	Samples
TLE2022AIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		TLE2022AI	Samples
TLE2022AMD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2022AM	Samples
TLE2022AMDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2022AM	Samples
TLE2022AMDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2022AM	Samples
TLE2022AMDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2022AM	Samples
TLE2022AMFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9088105Q2A TLE2022A MFKB	Samples
TLE2022AMJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9088105QPA TLE2022AM	Samples
TLE2022BMFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9088108Q2A TLE2022B MFKB	Samples
TLE2022BMJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9088108QPA TLE2022BM	Samples
TLE2022CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2022C	Samples
TLE2022CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2022C	Samples
TLE2022CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		TLE2022CP	Samples
TLE2022CPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		TLE2022CP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2022ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2022I	Samples
TLE2022IDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2022I	Samples
TLE2022IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2022I	Samples
TLE2022IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		TLE2022IP	Samples
TLE2022IPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		TLE2022IP	Samples
TLE2022MD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2022M	Samples
TLE2022MDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2022M	Samples
TLE2022MDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		2022M	Samples
TLE2022MFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9088102M2A TLE2022MFKB	Samples
TLE2022MJG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TLE2022MJG	Samples
TLE2022MJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9088102MPA TLE2022M	Samples
TLE2024ACDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLE2024AC	Samples
TLE2024ACDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLE2024AC	Samples
TLE2024ACN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type		TLE2024ACN	Samples
TLE2024AIDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLE2024AI	Samples
TLE2024AIN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type		TLE2024AIN	Samples
TLE2024AMFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9088106Q2A TLE2024A MFKB	Samples
TLE2024AMJB	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9088106QC A TLE2024AMJB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2024BMDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2024BM	Samples
TLE2024BMDWG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLE2024BM	Samples
TLE2024BMDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2024BM	Samples
TLE2024BMFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9088109Q2A TLE2024 BMFKB	Samples
TLE2024BMJ	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TLE2024BMJ	Samples
TLE2024BMJB	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9088109QC A TLE2024BMJB	Samples
TLE2024CDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLE2024C	Samples
TLE2024CDWG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLE2024C	Samples
TLE2024CDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLE2024C	Samples
TLE2024CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type		TLE2024CN	Samples
TLE2024CNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type		TLE2024CN	Samples
TLE2024IDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLE2024I	Samples
TLE2024IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type		TLE2024IN	Samples
TLE2024MDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2024M	Samples
TLE2024MDWG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2024M	Samples
TLE2024MFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9088103M2A TLE2024MFKB	Samples
TLE2024MJB	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9088103MC A TLE2024MJB	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLE2021, TLE2021A, TLE2021AM, TLE2021M, TLE2022, TLE2022A, TLE2022AM, TLE2022M, TLE2024, TLE2024A, TLE2024AM, TLE2024B, TLE2024BM, TLE2024M :

• Catalog : [TLE2021A](#), [TLE2021](#), [TLE2022A](#), [TLE2022](#), [TLE2024A](#), [TLE2024B](#), [TLE2024](#)

• Automotive : [TLE2021-Q1](#), [TLE2021A-Q1](#), [TLE2021A-Q1](#), [TLE2021-Q1](#), [TLE2022-Q1](#), [TLE2022A-Q1](#), [TLE2022A-Q1](#), [TLE2022-Q1](#), [TLE2024-Q1](#), [TLE2024A-Q1](#), [TLE2024A-Q1](#), [TLE2024-Q1](#)

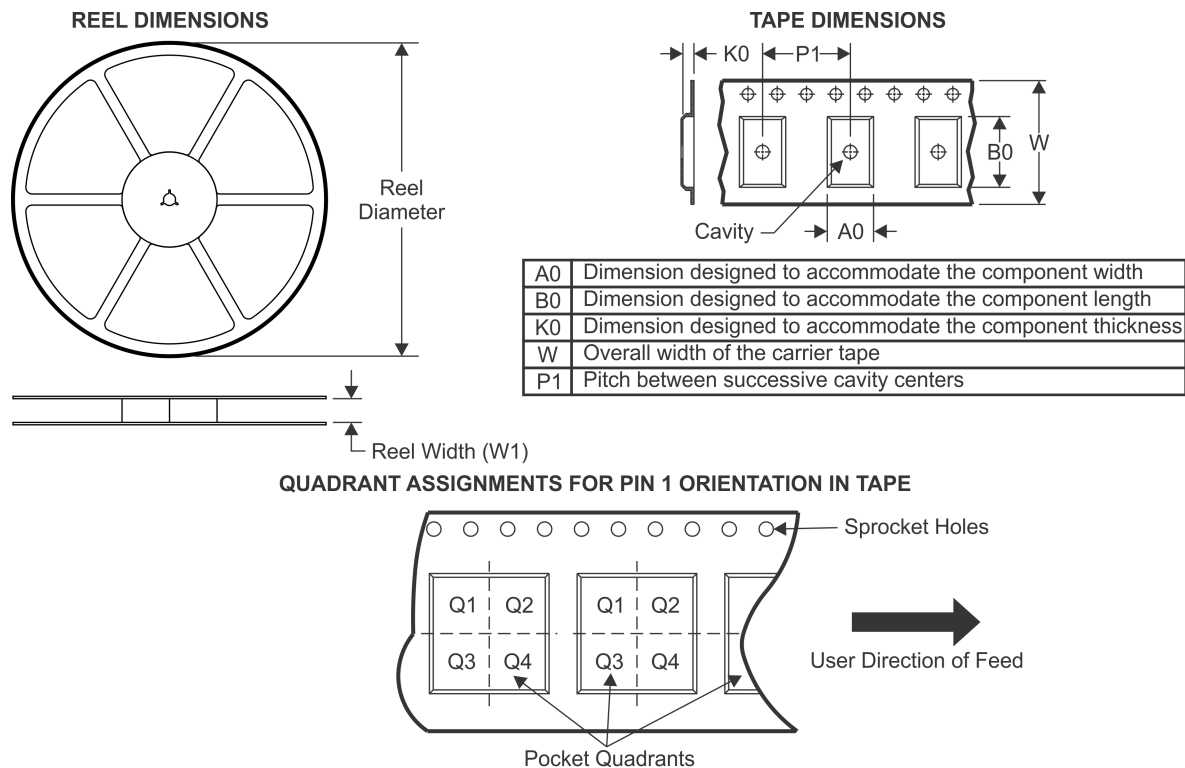
• Enhanced Product : [TLE2021-EP](#), [TLE2021A-EP](#), [TLE2021A-EP](#), [TLE2021-EP](#), [TLE2022-EP](#), [TLE2022A-EP](#), [TLE2022A-EP](#), [TLE2022-EP](#), [TLE2024-EP](#), [TLE2024A-EP](#), [TLE2024A-EP](#), [TLE2024-EP](#)

- Military : [TLE2021M](#), [TLE2021AM](#), [TLE2022M](#), [TLE2022AM](#), [TLE2024M](#), [TLE2024AM](#), [TLE2024BM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

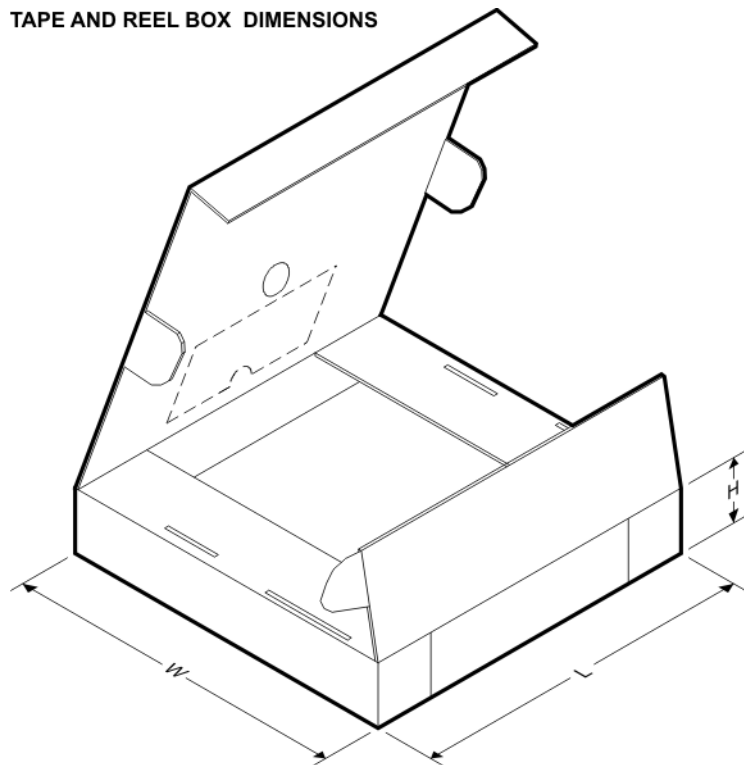
TAPE AND REEL INFORMATION



*All dimensions are nominal

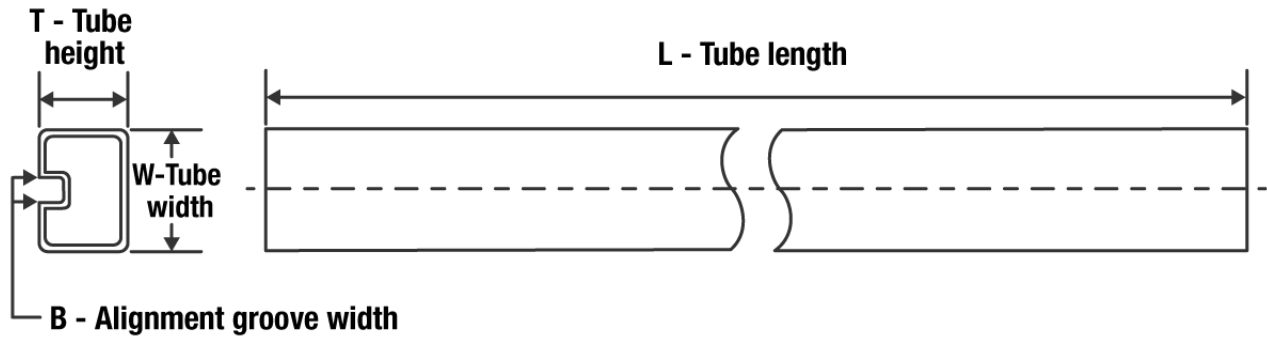
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2021ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2021AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2021CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2021IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022AMDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022AMDRG4	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2024ACDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TLE2024CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2021ACDR	SOIC	D	8	2500	340.5	336.1	25.0
TLE2021AIDR	SOIC	D	8	2500	340.5	336.1	25.0
TLE2021CDR	SOIC	D	8	2500	340.5	336.1	25.0
TLE2021IDR	SOIC	D	8	2500	340.5	336.1	25.0
TLE2022ACDR	SOIC	D	8	2500	340.5	336.1	25.0
TLE2022AIDR	SOIC	D	8	2500	340.5	336.1	25.0
TLE2022AMDR	SOIC	D	8	2500	350.0	350.0	43.0
TLE2022AMDRG4	SOIC	D	8	2500	340.5	336.1	25.0
TLE2022CDR	SOIC	D	8	2500	340.5	336.1	25.0
TLE2022IDR	SOIC	D	8	2500	340.5	336.1	25.0
TLE2022MDR	SOIC	D	8	2500	350.0	350.0	43.0
TLE2024ACDWR	SOIC	DW	16	2000	350.0	350.0	43.0
TLE2024CDWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9088102M2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9088103M2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9088104Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9088105Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9088106Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9088107Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9088108Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9088109Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
TLE2021ACD	D	SOIC	8	75	505.46	6.76	3810	4
TLE2021ACD	D	SOIC	8	75	507	8	3940	4.32
TLE2021ACP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2021AID	D	SOIC	8	75	507	8	3940	4.32
TLE2021AID	D	SOIC	8	75	505.46	6.76	3810	4
TLE2021AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2021AMFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TLE2021BMFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TLE2021CD	D	SOIC	8	75	505.46	6.76	3810	4
TLE2021CD	D	SOIC	8	75	507	8	3940	4.32
TLE2021CDG4	D	SOIC	8	75	507	8	3940	4.32
TLE2021CDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLE2021CP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2021CPE4	P	PDIP	8	50	506	13.97	11230	4.32
TLE2021ID	D	SOIC	8	75	507	8	3940	4.32
TLE2021ID	D	SOIC	8	75	505.46	6.76	3810	4
TLE2021IDG4	D	SOIC	8	75	507	8	3940	4.32
TLE2021IDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLE2021IP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2021MD	D	SOIC	8	75	505.46	6.76	3810	4

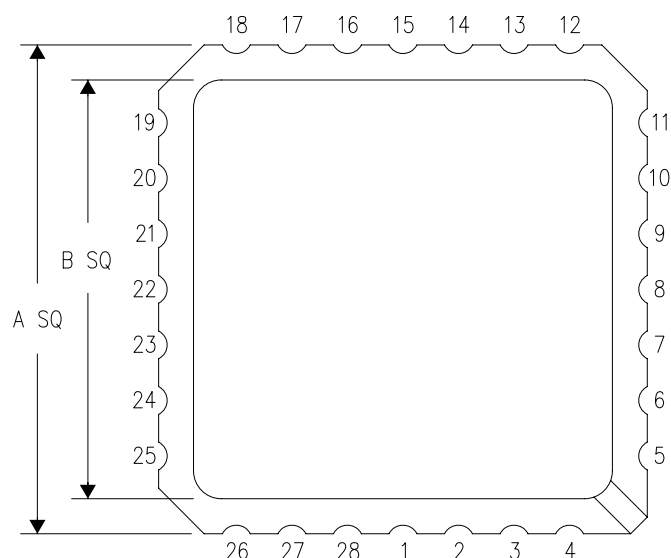
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLE2021MDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLE2022ACD	D	SOIC	8	75	505.46	6.76	3810	4
TLE2022ACD	D	SOIC	8	75	507	8	3940	4.32
TLE2022ACDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLE2022ACDG4	D	SOIC	8	75	507	8	3940	4.32
TLE2022ACP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022ACPE4	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022AID	D	SOIC	8	75	507	8	3940	4.32
TLE2022AID	D	SOIC	8	75	505.46	6.76	3810	4
TLE2022AIDG4	D	SOIC	8	75	507	8	3940	4.32
TLE2022AIDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLE2022AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022AMD	D	SOIC	8	75	505.46	6.76	3810	4
TLE2022AMDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLE2022AMFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TLE2022BMFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TLE2022CD	D	SOIC	8	75	505.46	6.76	3810	4
TLE2022CD	D	SOIC	8	75	507	8	3940	4.32
TLE2022CP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022CPE4	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022ID	D	SOIC	8	75	505.46	6.76	3810	4
TLE2022ID	D	SOIC	8	75	507	8	3940	4.32
TLE2022IDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLE2022IDG4	D	SOIC	8	75	507	8	3940	4.32
TLE2022IP	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022IPE4	P	PDIP	8	50	506	13.97	11230	4.32
TLE2022MD	D	SOIC	8	75	505.46	6.76	3810	4
TLE2022MFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TLE2024ACDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
TLE2024ACN	N	PDIP	14	25	506	13.97	11230	4.32
TLE2024AIDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
TLE2024AIN	N	PDIP	14	25	506	13.97	11230	4.32
TLE2024AMFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TLE2024BMDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
TLE2024BMDWG4	DW	SOIC	16	40	506.98	12.7	4826	6.6
TLE2024BMFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TLE2024CDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
TLE2024CDWG4	DW	SOIC	16	40	506.98	12.7	4826	6.6
TLE2024CN	N	PDIP	14	25	506	13.97	11230	4.32
TLE2024CNE4	N	PDIP	14	25	506	13.97	11230	4.32
TLE2024IDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
TLE2024IN	N	PDIP	14	25	506	13.97	11230	4.32
TLE2024MDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
TLE2024MDWG4	DW	SOIC	16	40	506.98	12.7	4826	6.6

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLE2024MFKB	FK	LCCC	20	1	506.98	12.06	2030	NA

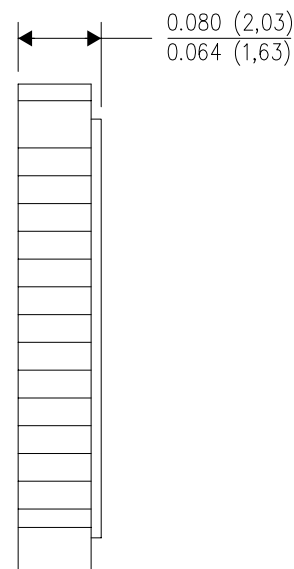
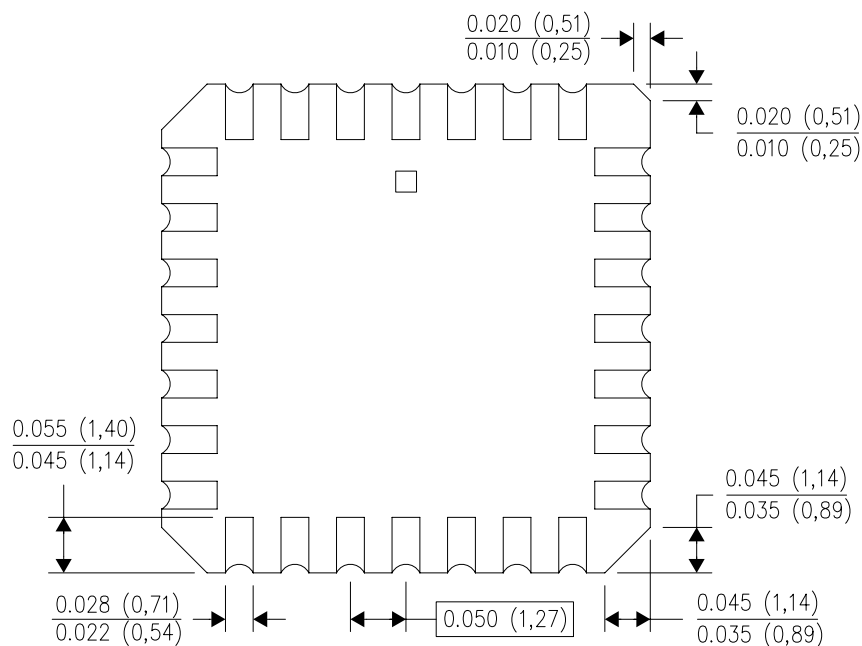
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

GENERIC PACKAGE VIEW

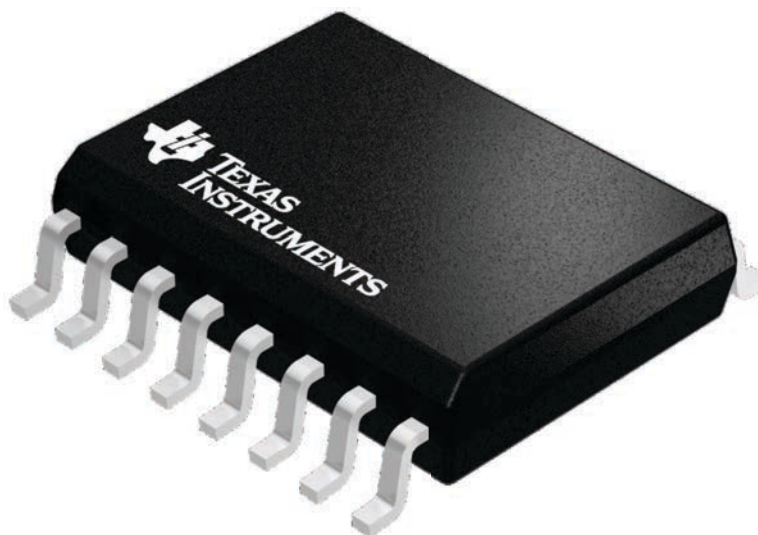
DW 16

SOIC - 2.65 mm max height

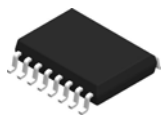
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

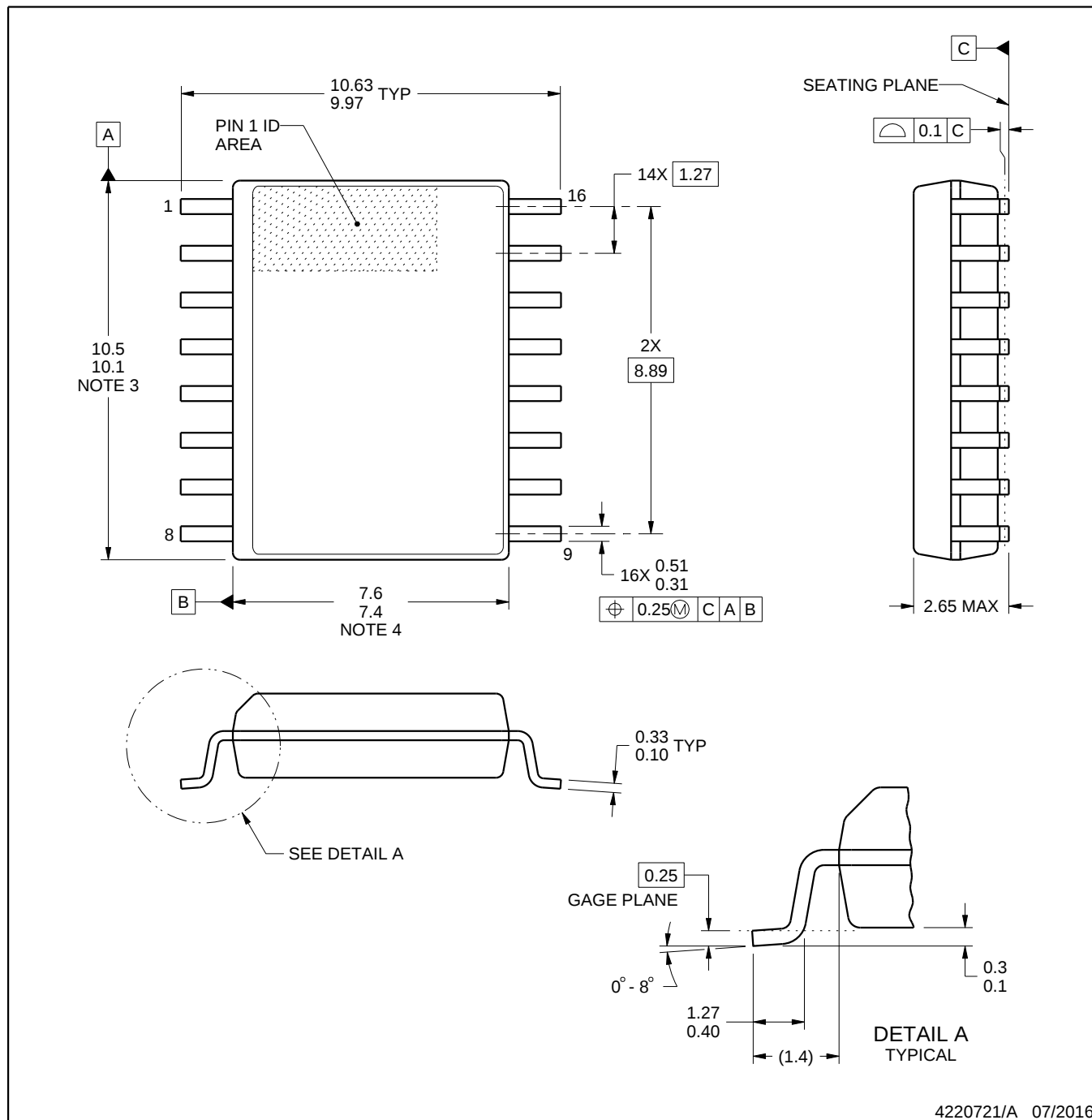


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

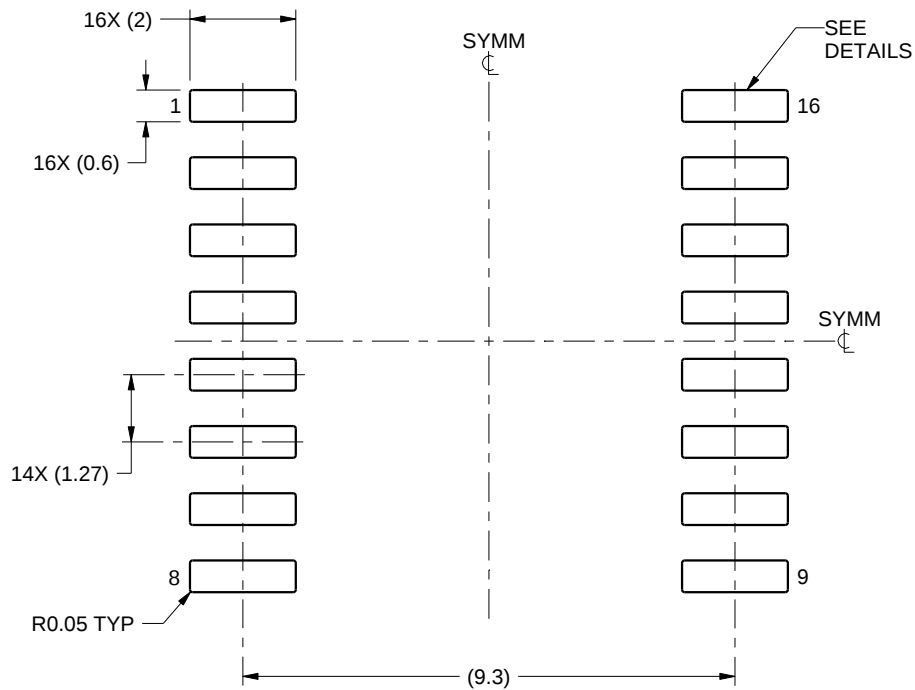
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

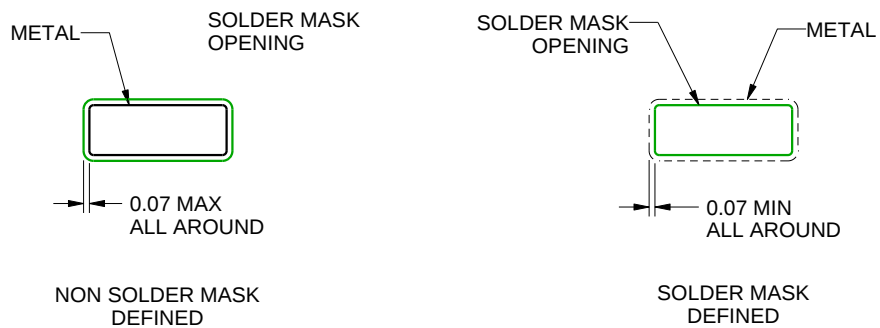
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

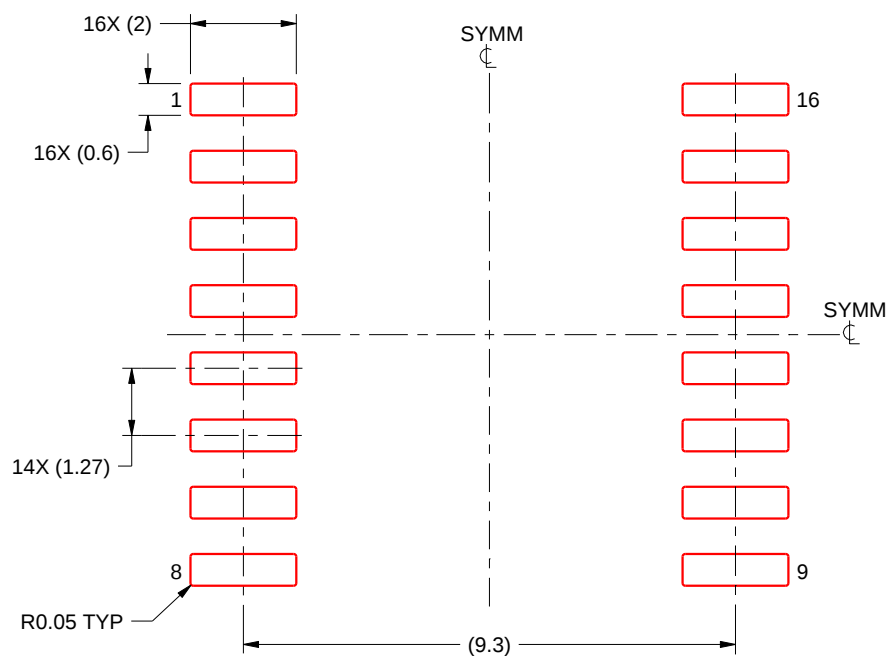
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

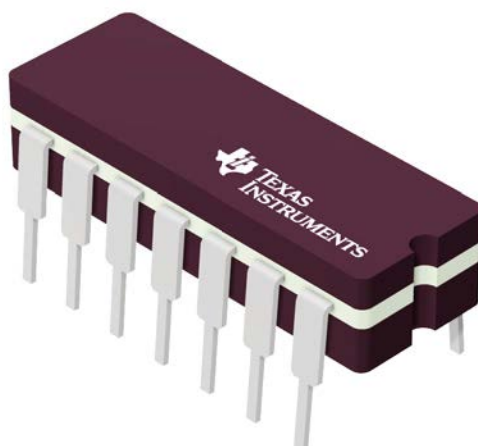
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J 14

GENERIC PACKAGE VIEW

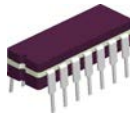
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

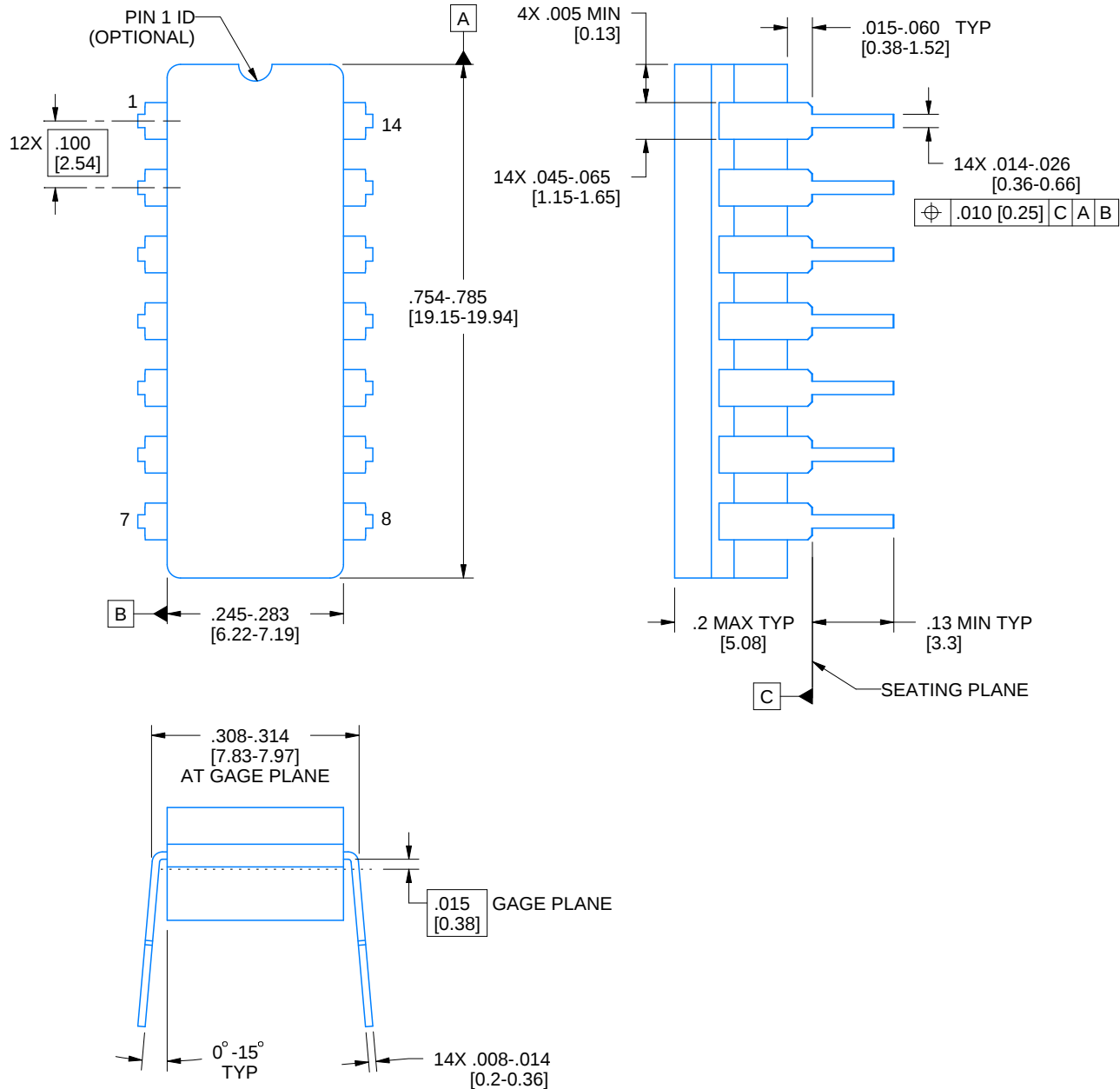


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

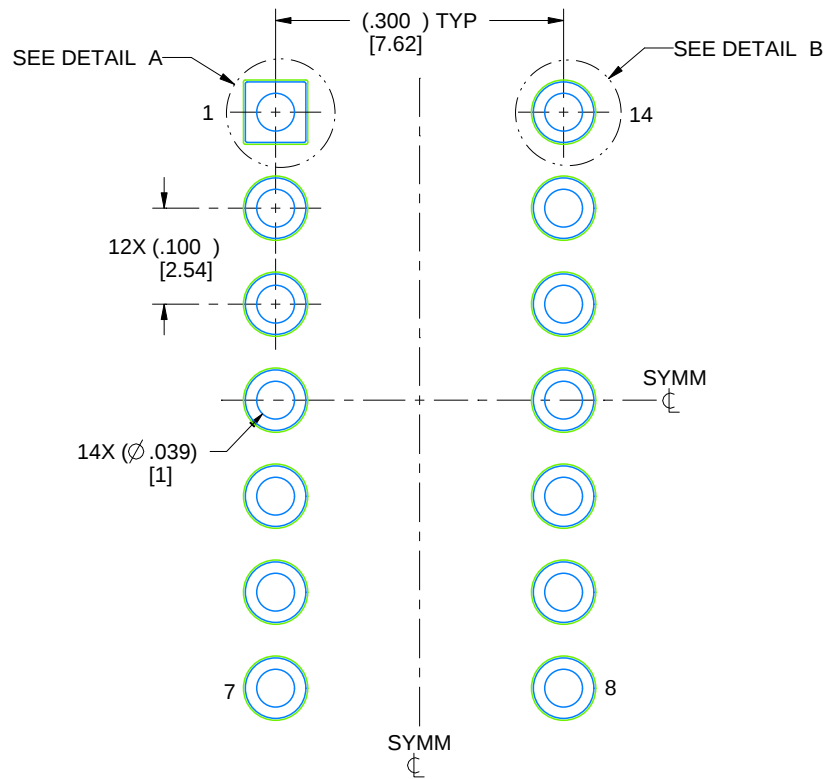
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

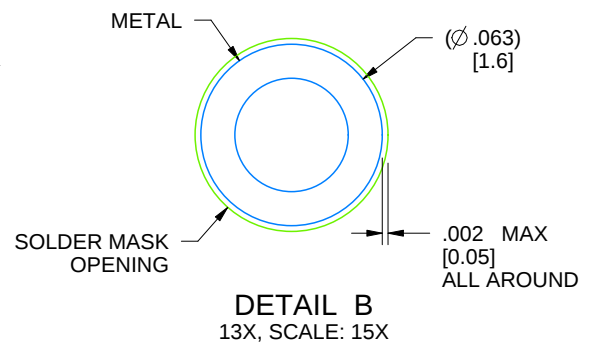
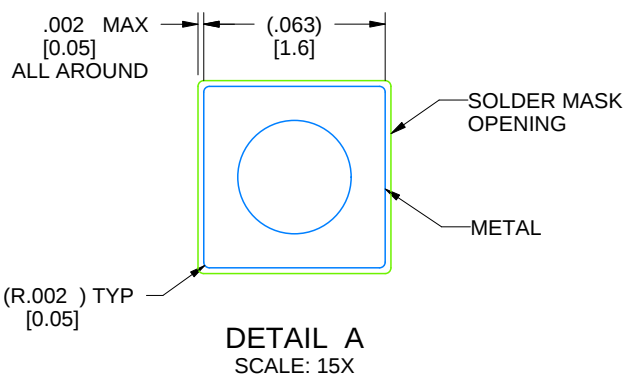
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



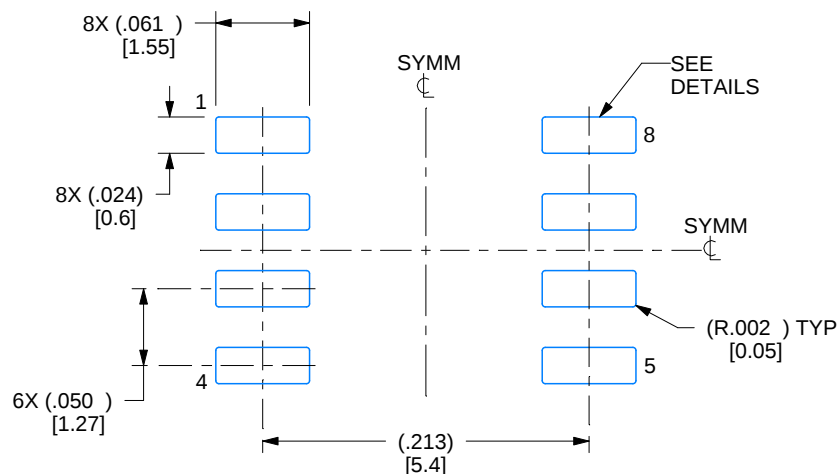
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

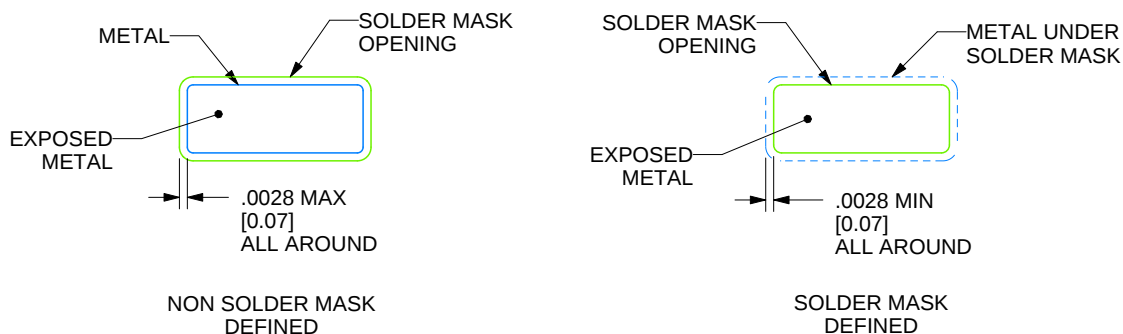
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

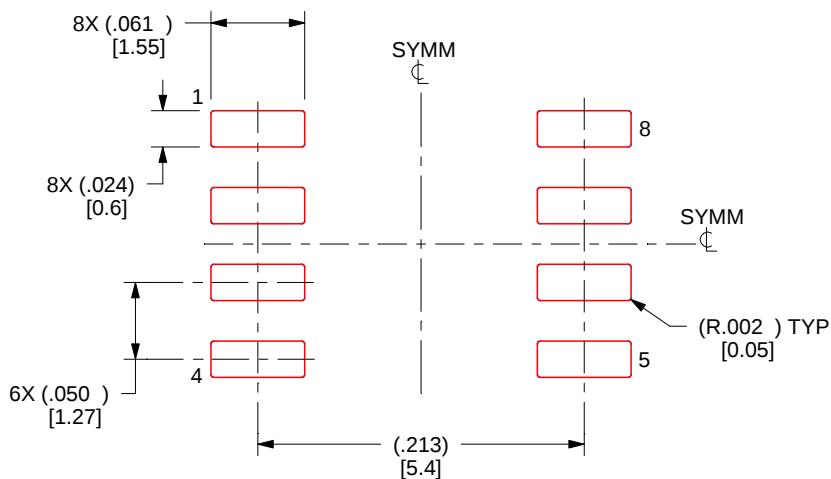
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

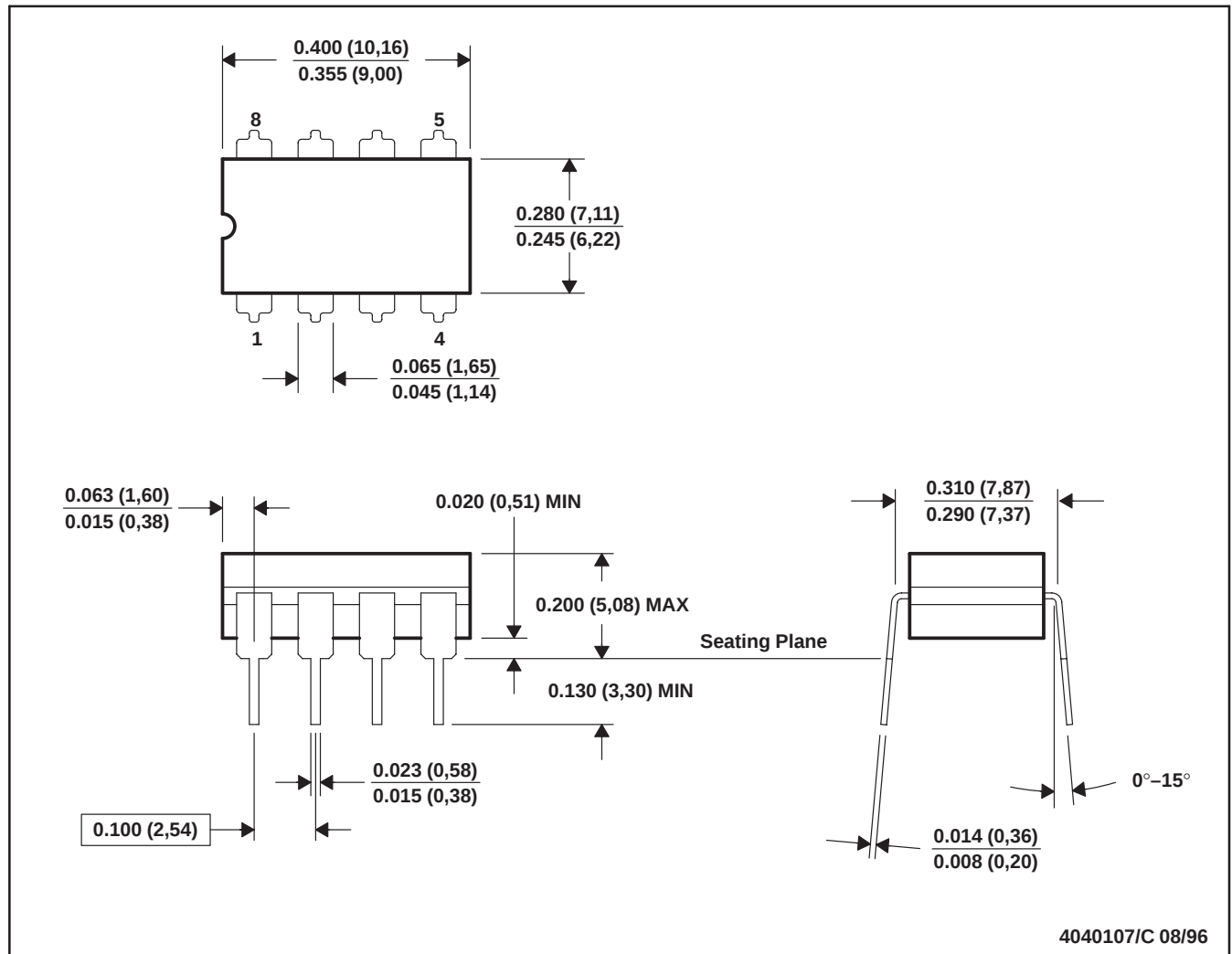
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification.
 - E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

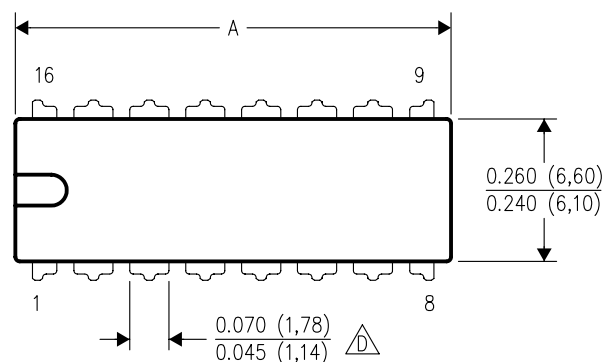


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

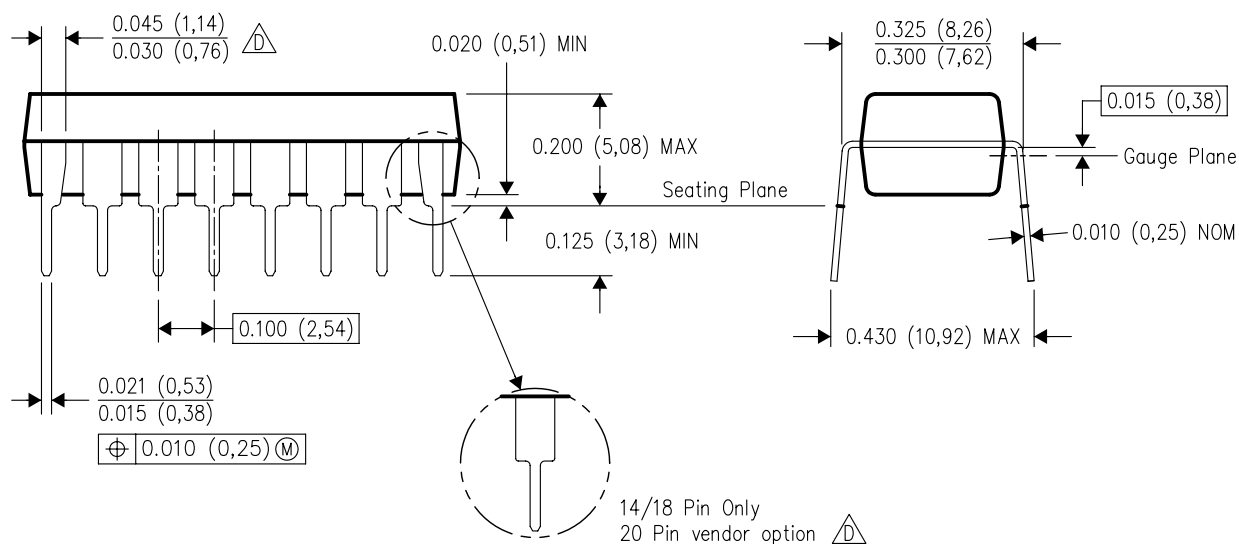
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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