

CSD18511KCS 40V N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

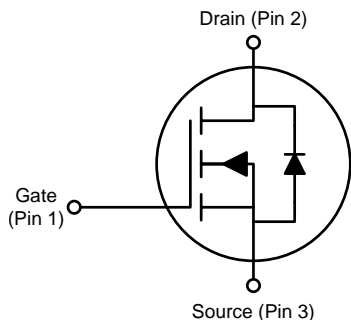
- 低 Q_g 和 Q_{gd}
- 低 $R_{DS(ON)}$
- 低热阻
- 雪崩额定值
- 无铅引脚镀层
- 符合 RoHS 环保标准
- 无卤素
- 晶体管 (TO)-220 塑料封装

2 应用范围

- 次级侧同步整流器
- 电机控制

3 说明

此 40V、2.1m Ω 、TO-220 NexFET™ 功率 MOSFET 被设计成大大降低功率转换 损耗的理想选择。



产品概要

$T_A = 25^\circ\text{C}$		典型值		单位
V_{DS}	漏源电压	40		V
Q_g	栅极电荷总量 (10V)	63.9		nC
Q_{gd}	栅极电荷 (栅极到漏极)	9.7		nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 4.5\text{V}$	3.2	m Ω
		$V_{GS} = 10\text{V}$	2.1	
$V_{GS(th)}$	阈值电压	1.8		V

器件信息(1)

器件	包装介质	数量	封装	运输
CSD18511KCS	管	50	TO-220 塑料封装	管

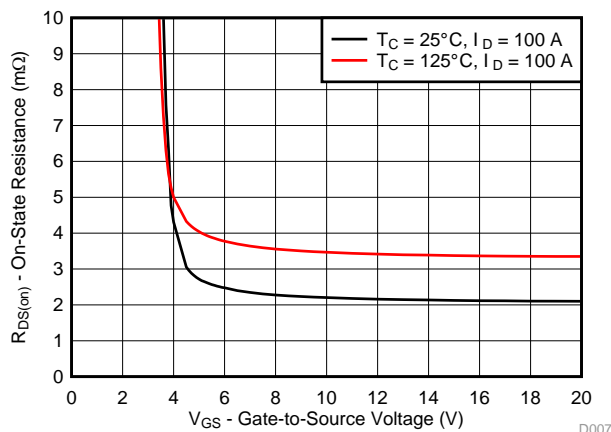
(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	40	V
V_{GS}	栅源电压	± 20	V
I_D	持续漏极电流 (受封装限制)	110	A
	持续漏极电流 (受芯片限制), $T_C = 25^\circ\text{C}$ 时测得	194	
	持续漏极电流 (受芯片限制), $T_C = 100^\circ\text{C}$ 时测得	137	
I_{DM}	脉冲漏极电流(1)	400	A
P_D	功率耗散	188	W
T_J, T_{stg}	工作结温, 储存温度	-55 至 175	$^\circ\text{C}$
E_{AS}	雪崩能量, 单一脉冲 $I_D = 56\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	156	mJ

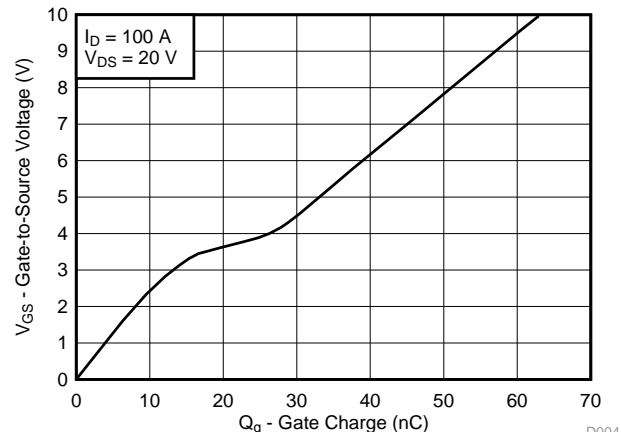
(1) 最大 $R_{\theta JC} = 0.8^\circ\text{C}/\text{W}$, 脉冲持续时间 $\leq 100\mu\text{s}$, 占空比 $\leq 1\%$ 。

$R_{DS(on)}$ 与 V_{GS} 对比



D007

栅极电荷



D004



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4 修订历史记录

日期	修订版本	注意
2017 年 7 月	*	初始发行版。

5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
V_{DSS}	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	40			V
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 32\text{ V}$			1	μA
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.5	1.8	2.4	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 4.5\text{ V}, I_D = 100\text{ A}$		3.2	4.2	m Ω
		$V_{GS} = 10\text{ V}, I_D = 100\text{ A}$		2.1	2.6	
g_{fs}	Transconductance	$V_{DS} = 4\text{ V}, I_D = 100\text{ A}$		249		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}, f = 1\text{ MHz}$		4570	5940	pF
C_{oss}	Output capacitance			454	591	pF
C_{rss}	Reverse transfer capacitance			235	306	pF
R_G	Series gate resistance		0.9	1.8		Ω
Q_g	Gate charge total (4.5 V)	$V_{DS} = 20\text{ V}, I_D = 100\text{ A}$		31		nC
Q_g	Gate charge total (10 V)			64		nC
Q_{gd}	Gate charge gate-to-drain			9.7		nC
Q_{gs}	Gate charge gate-to-source			17.9		nC
$Q_{g(th)}$	Gate charge at V_{th}			7.4		nC
Q_{oss}	Output charge		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$		20.7	
$t_{d(on)}$	Turnon delay time	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 100\text{ A}, R_G = 0\ \Omega$		8		ns
t_r	Rise time			6		ns
$t_{d(off)}$	Turnoff delay time			17		ns
t_f	Fall time			3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	$I_{SD} = 100\text{ A}, V_{GS} = 0\text{ V}$		0.9	1.0	V
Q_{rr}	Reverse recovery charge	$V_{DS} = 20\text{ V}, I_F = 100\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		62		nC
t_{rr}	Reverse recovery time			31		ns

5.2 Thermal Information

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	$^\circ\text{C}/\text{W}$

5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

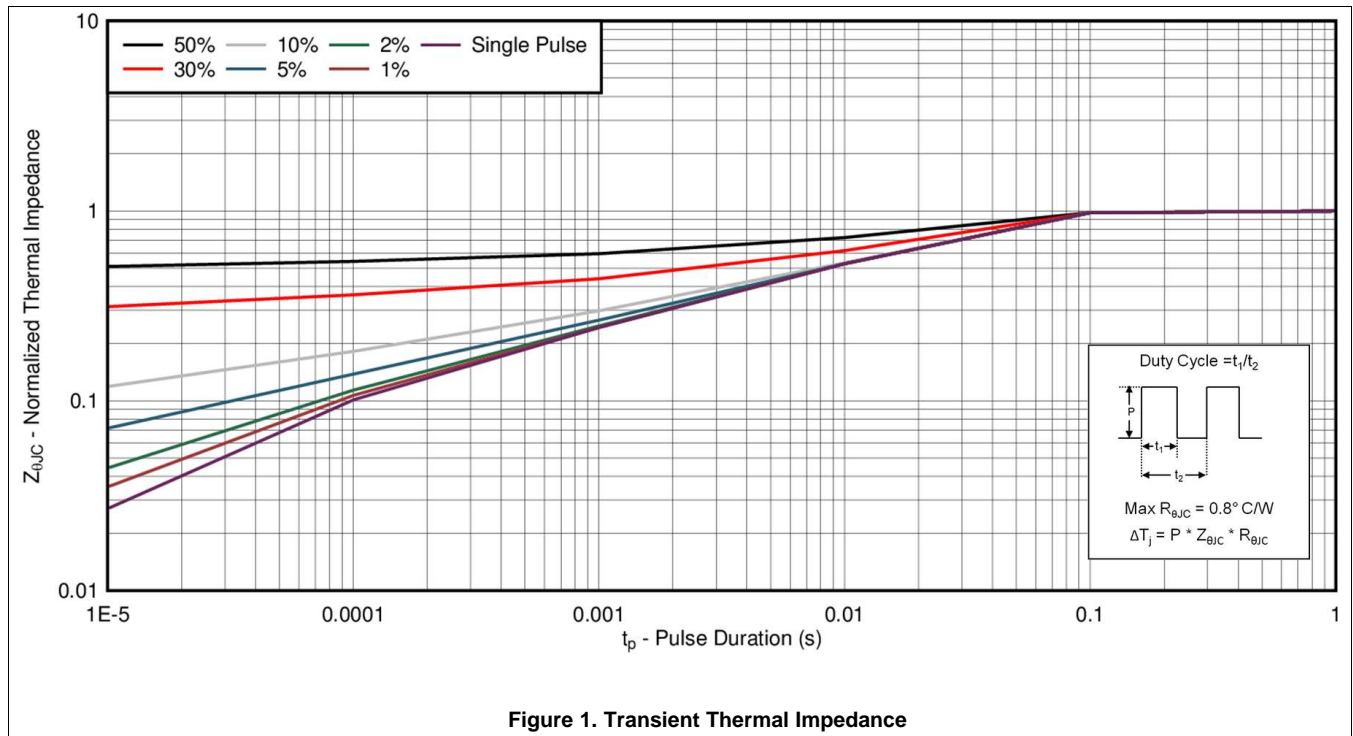


Figure 1. Transient Thermal Impedance

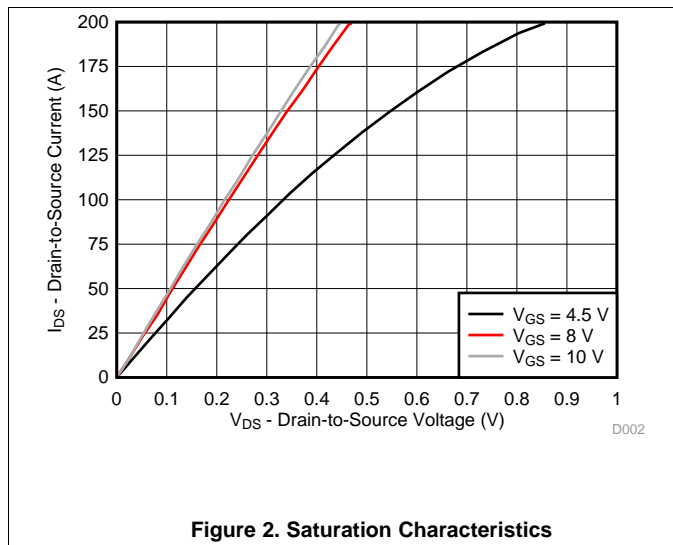


Figure 2. Saturation Characteristics

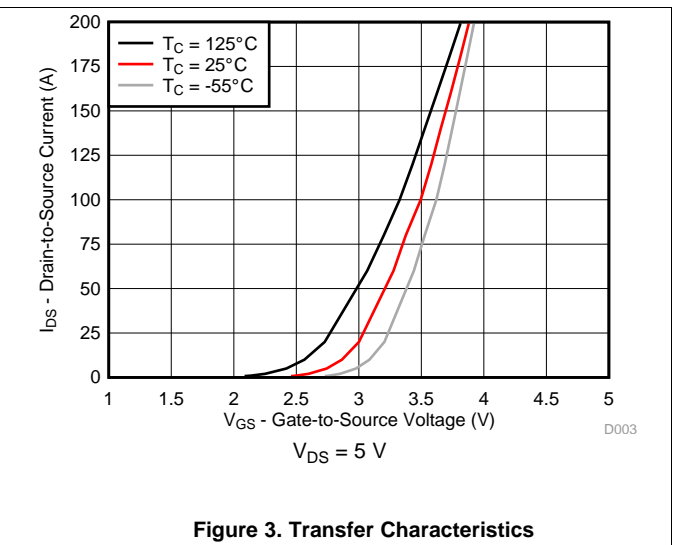


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

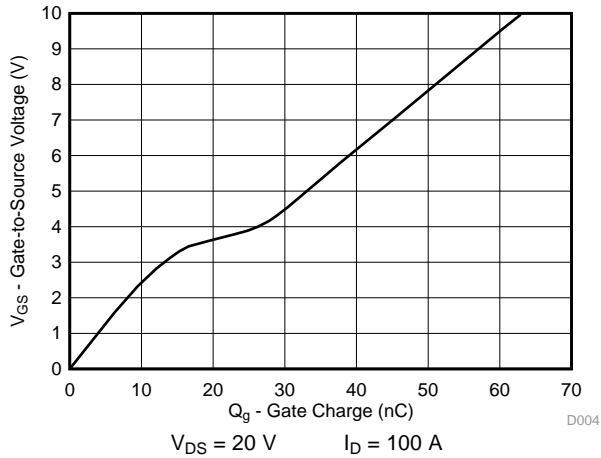


Figure 4. Gate Charge

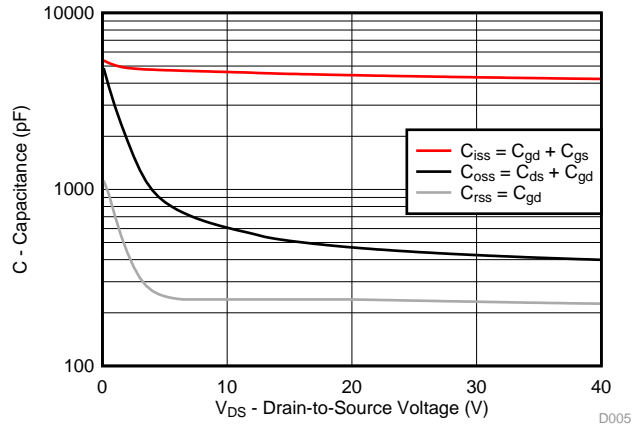


Figure 5. Capacitance

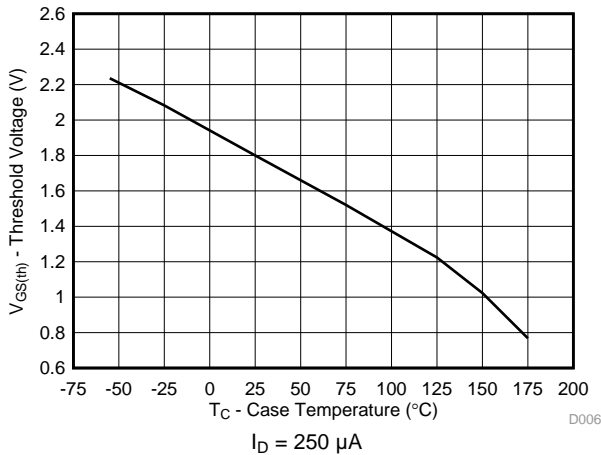


Figure 6. Threshold Voltage vs Temperature

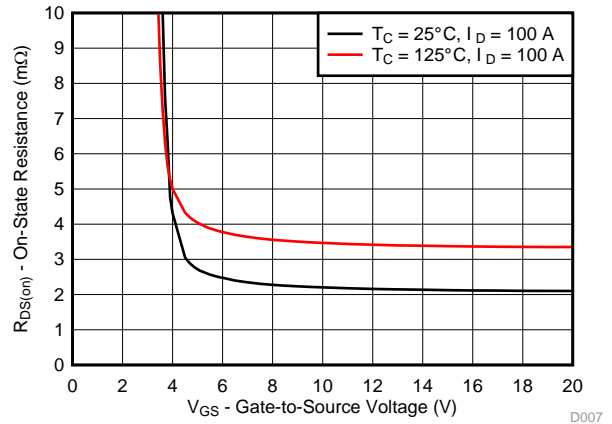


Figure 7. On-State Resistance vs Gate-to-Source Voltage

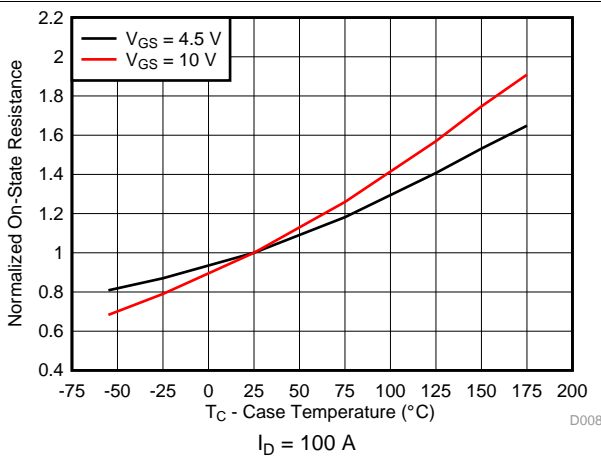


Figure 8. Normalized On-State Resistance vs Temperature

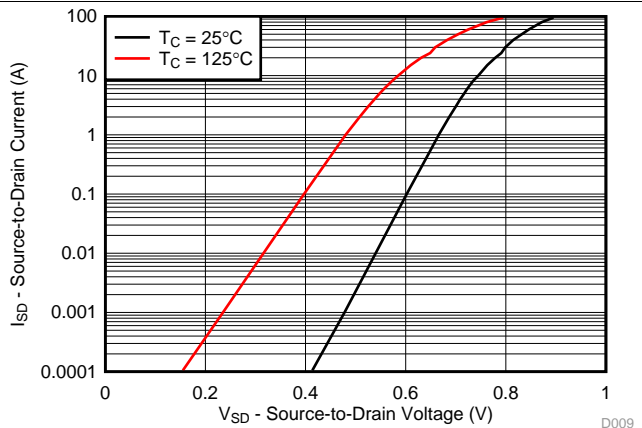
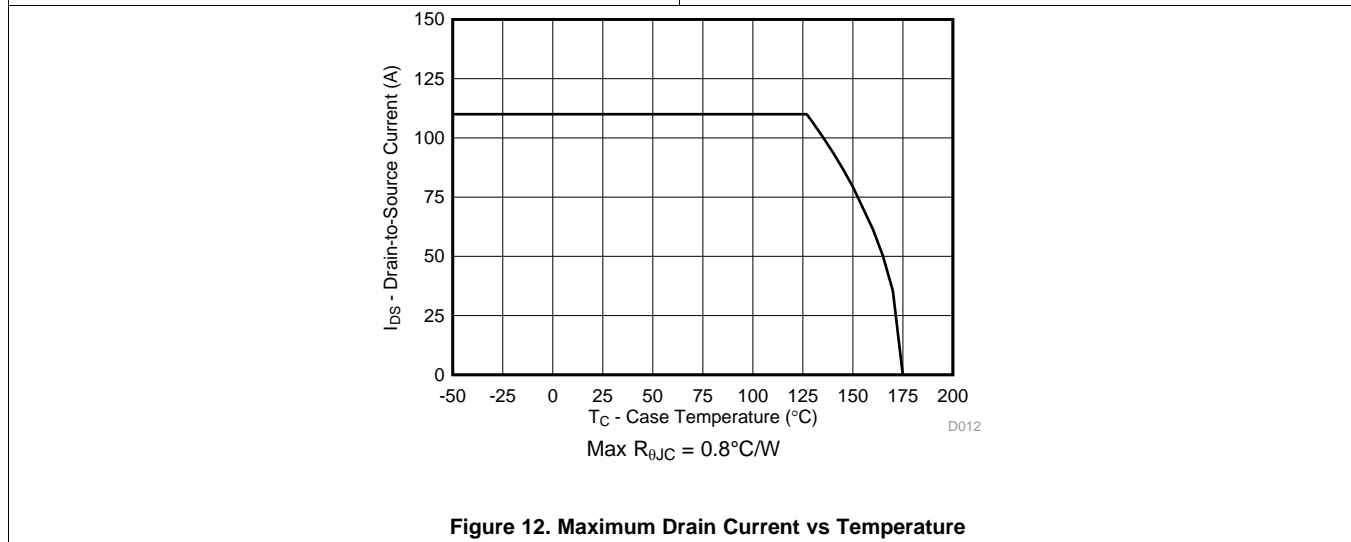
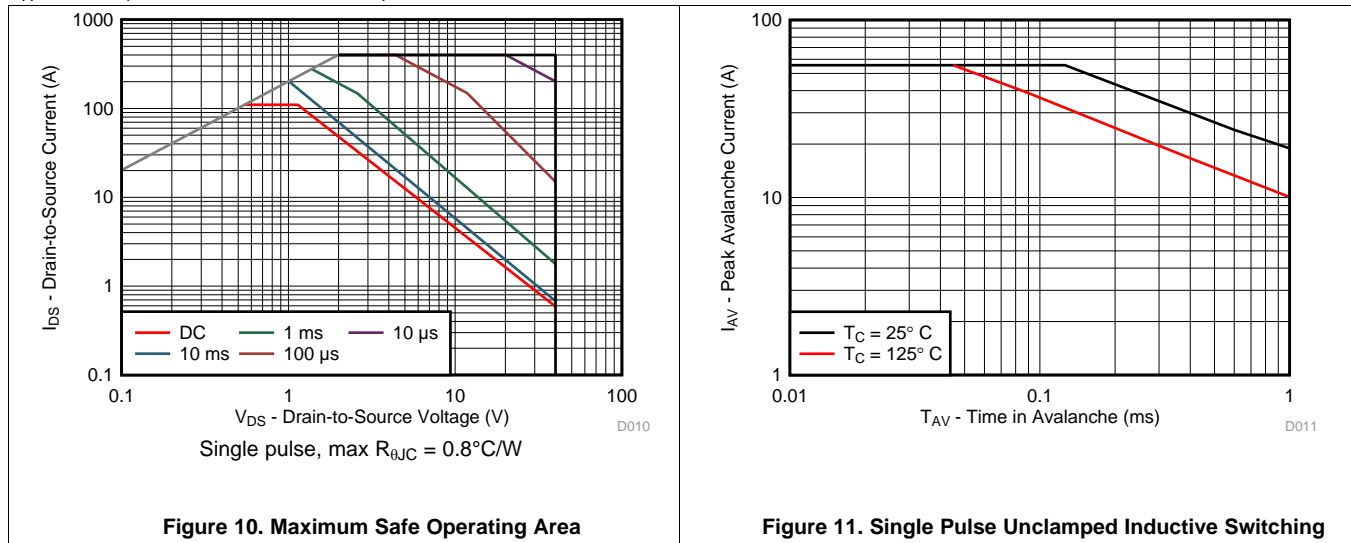


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)



6 器件和文档支持

6.1 接收文档更新通知

要接收文档更新通知，请导航至德州仪器 TI.com.cn 上的器件产品文件夹。请单击右上角的 *通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

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下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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6.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

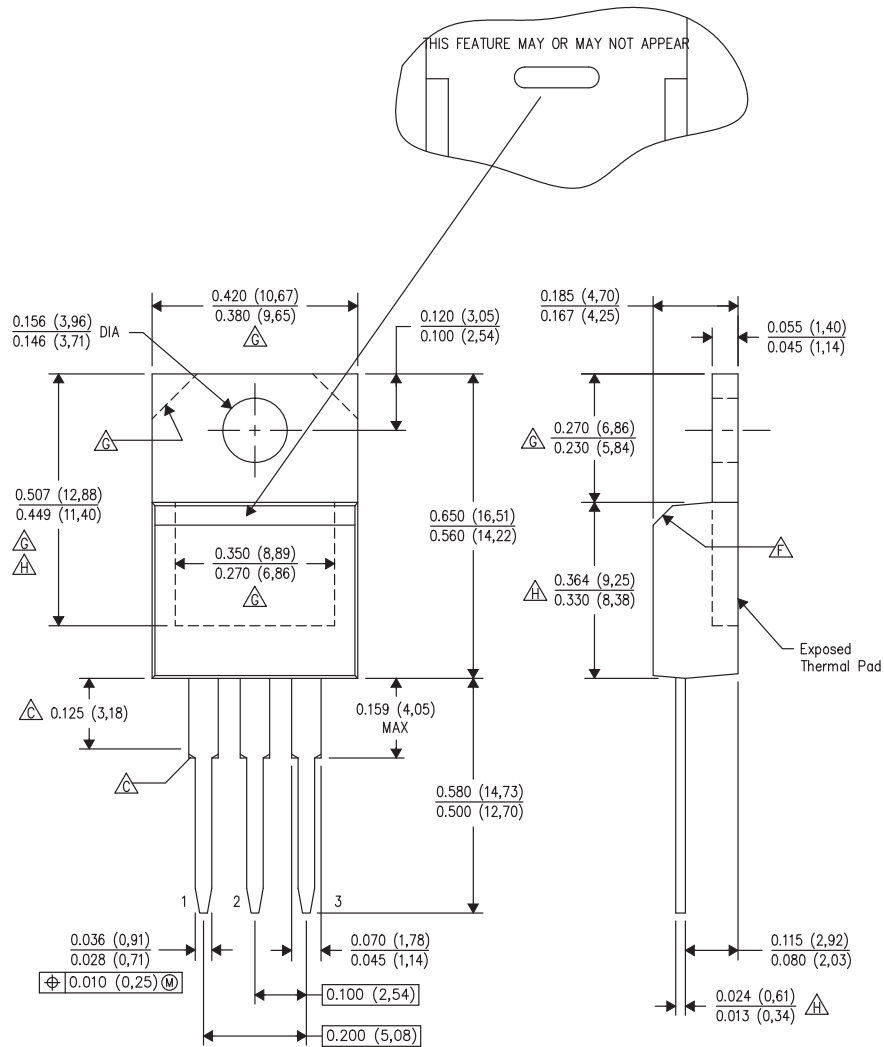
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

7.1 KCS 封装尺寸







- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Lead dimensions are not controlled within this area. Chamfer may or may not appear.
 - D. All lead dimensions apply before solder dip.
 - E. The center lead is in electrical contact with the mounting tab.
 -  The chamfer is optional.
 -  Thermal pad contour optional within these dimensions.
 -  Falls within JEDEC TO-220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

表 1. 引脚配置

位置	名称
引脚 1	栅极
引脚 2 / 标签	漏极
引脚 3	源极

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18511KCS	ACTIVE	TO-220	KCS	3	50	RoHS-Exempt & Green	SN	N / A for Pkg Type	-55 to 175	CSD18511KCS	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


*All dimensions are nominal

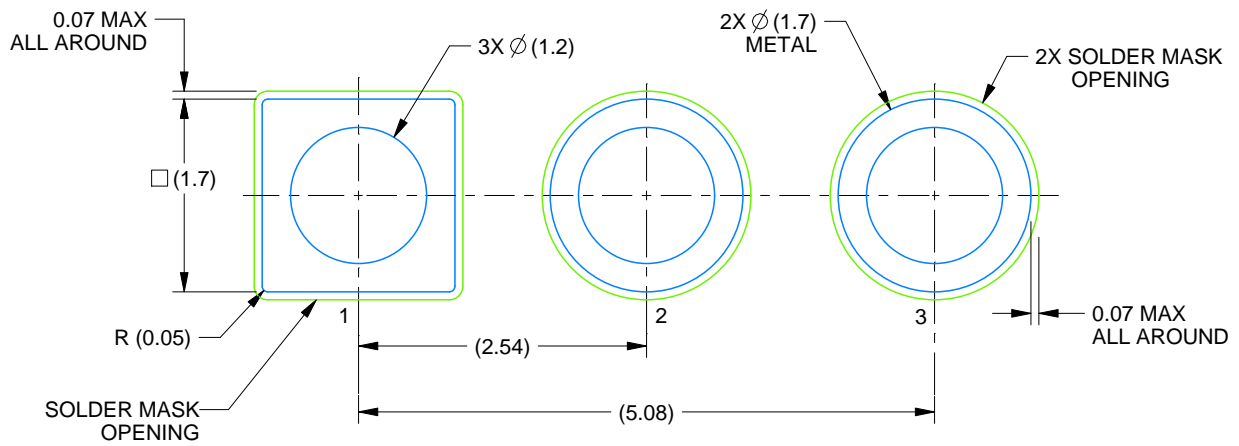
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CSD18511KCS	KCS	TO-220	3	50	532	34.1	700	9.6

EXAMPLE BOARD LAYOUT

KCS0003B

TO-220 - 19.65 mm max height

TO-220



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

4222214/B 08/2018

重要声明和免责声明

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