# CDx4HC11 Triple 3-Input AND Gates

## 1 Features

- Buffered inputs
- Wide operating voltage range: 2 V to 6 V
- Wide operating temperature range: –55°C to +125°C
- Supports fanout up to 10 LSTTL loads
- Significant power reduction compared to LSTTL logic ICs

## 2 Applications

- Combining power good signals
- Enable digital signals

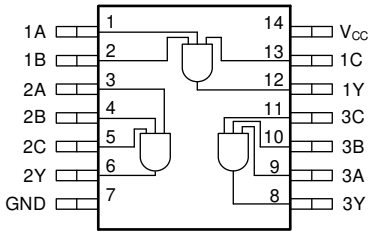
## 3 Description

This device contains three independent 3-input AND gates. Each gate performs the Boolean function Y = A ● B ● C in positive logic.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| CD74HC11M | SOIC (14) | 8.70 mm × 3.90 mm |
| CD74HC11E | PDIP (14) | 19.30 mm × 6.40 mm |
| CD54HC11F | CDIP (14) | 21.30 mm × 7.60 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Functional pinout**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (September 2003) to Revision F (April 2021) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Updated to new data sheet standards | 1 |
| • Moved the HCT devices to a standalone data sheet (SCHS405) | 1 |
| • $R_{\theta JA}$ increased for the D package (86 to 133.6 °C/W) and decreased for the N package (80 to 65.2 °C/W) | 5 |


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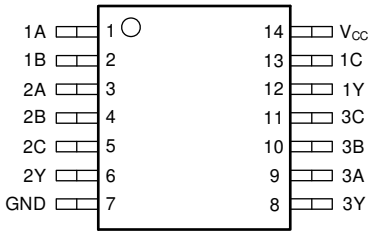



**Figure 5-1. D, N, or J Package**
**14-Pin SOIC, PDIP, or CDIP**
**Top View**

## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1A | 1 | Input | Channel 1, Input A |
| 1B | 2 | Input | Channel 1, Input B |
| 2A | 3 | Input | Channel 2, Input A |
| 2B | 4 | Input | Channel 2, Input B |
| 2C | 5 | Input | Channel 2, Input C |
| 2Y | 6 | Output | Channel 2, Output Y |
| GND | 7 | — | Ground |
| 3Y | 8 | Output | Channel 3, Output Y |
| 3A | 9 | Input | Channel 3, Input A |
| 3B | 10 | Input | Channel 3, Input B |
| 3C | 11 | Input | Channel 3, Input C |
| 1Y | 12 | Output | Channel 1, Output Y |
| 1C | 13 | Input | Channel 1, Input C |
| $V_{CC}$ | 14 | — | Positive Supply |

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $I_{IK}$ | Input clamp current(2) | $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V | | ±20 | mA |
| $I_{OK}$ | Output clamp current(2) | $V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O > –0.5$ V or $V_O < V_{CC} + 0.5$ V | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_J$ | Junction temperature(3) | Plastic package | | 150 | °C |
| | | Hermetic package or die | | 175 | |
| | Lead temperature (soldering 10s) | SOIC - lead tips only | | 300 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Guaranteed by design.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | | |
| | | $V_{CC}$ = 6 V | 4.2 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | | 0.5 | V |
| | | $V_{CC}$ = 4.5 V | | | 1.35 | |
| | | $V_{CC}$ = 6 V | | | 1.8 | |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | V |
| $t_t$ | Input transition time | $V_{CC}$ = 2 V | | | 1000 | ns |
| | | $V_{CC}$ = 4.5 V | | | 500 | |
| | | $V_{CC}$ = 6 V | | | 400 | |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | °C |


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## 5.4 Thermal Information

| THERMAL METRIC(1) | | CD74HC11 | | UNIT |
|---|---|---|---|---|
| | | N (PDIP) | D (SOIC) | |
| | | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 65.2 | 133.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 52.9 | 89.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 44.9 | 89.5 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 32.5 | 45.5 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 44.7 | 89.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | Operating free-air temperature ($T_A$) | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 25°C | | | –40°C to 85°C | | | –55°C to 125°C | | | |
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | High-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –20 µA | 2 V | 1.9 | | | 1.9 | | | 1.9 | | | V |
| | | | | 4.5 V | 4.4 | | | 4.4 | | | 4.4 | | | |
| | | | | 6 V | 5.9 | | | 5.9 | | | 5.9 | | | |
| | | | $I_{OH}$ = –4 mA | 4.5 V | 3.98 | | | 3.84 | | | 3.7 | | | |
| | | | $I_{OH}$ = –5.2 mA | 6 V | 5.48 | | | 5.34 | | | 5.2 | | | |
| $V_{OL}$ | Low-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | 2 V | | | 0.1 | | | 0.1 | | | 0.1 | V |
| | | | | 4.5 V | | | 0.1 | | | 0.1 | | | 0.1 | |
| | | | | 6 V | | | 0.1 | | | 0.1 | | | 0.1 | |
| | | | $I_{OL}$ = 4 mA | 4.5 V | | | 0.26 | | | 0.33 | | | 0.4 | |
| | | | $I_{OL}$ = 5.2 mA | 6 V | | | 0.26 | | | 0.33 | | | 0.4 | |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or GND | | 6 V | | | ±0.1 | | | ±1 | | | ±1 | µA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND | $I_O$ = 0 | 6 V | | | 2 | | | 20 | | | 40 | µA |
| $C_i$ | Input capacitance | | | 5 V | | | 10 | | | 10 | | | 10 | pF |

## 5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted).

| PARAMETER | | FROM | TO | TEST CONDITIONS | $V_{CC}$ | Operating free-air temperature ($T_A$) | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 25°C | | | –40°C to 85°C | | | –55°C to 125°C | | | |
| | | | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{pd}$ | Propagation delay | A, B, or C | Y | $C_L$ = 50 pF | 2 V | | | 100 | | | 125 | | | 150 | ns |
| | | | | | 4.5 V | | | 20 | | | 25 | | | 30 | |
| | | | | | 6 V | | | 17 | | | 21 | | | 26 | |
| | | A, B, or C | Y | $C_L$ = 15 pF | 5 V | | 8 | | | | | | | | |

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over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted).

| PARAMETER | | FROM | TO | TEST CONDITIONS | $V_{CC}$ | Operating free-air temperature ($T_A$) | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 25°C | | | –40°C to 85°C | | | –55°C to 125°C | | | |
| | | | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_t$ | Transition-time | | Y | $C_L$ = 50 pF | 2 V | | | 75 | | | 95 | | | 110 | ns |
| | | | | | 4.5 V | | | 15 | | | 19 | | | 22 | |
| | | | | | 6 V | | | 13 | | | 16 | | | 19 | |

## 5.7 Operating Characteristics

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per gate | No load | 2 V to 6 V | | 26 | | pF |

## 5.8 Typical Characteristics

$T_A$ = 25°C

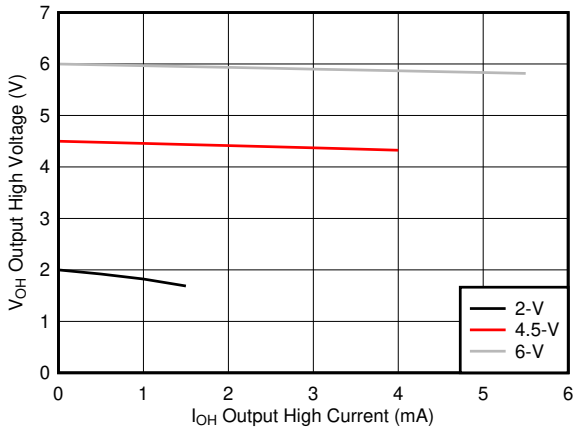



**Figure 5-1. Typical output voltage in the high state ($V_{OH}$)**

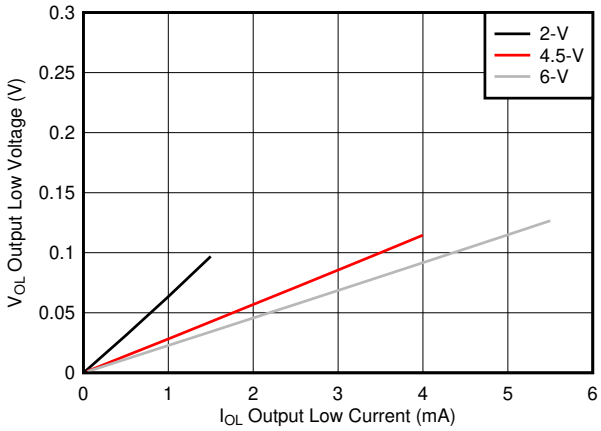
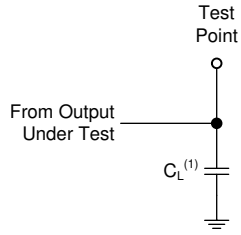



**Figure 5-2. Typical output voltage in the low state ($V_{OL}$)**


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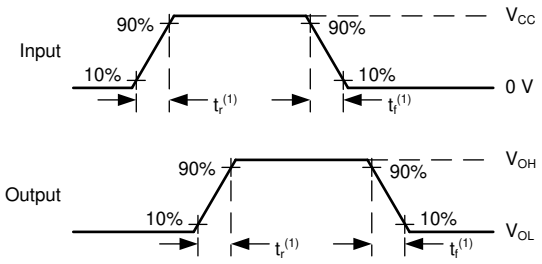
## 6 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_t$ < 6 ns.
- The outputs are measured one at a time, with one input transition per measurement.



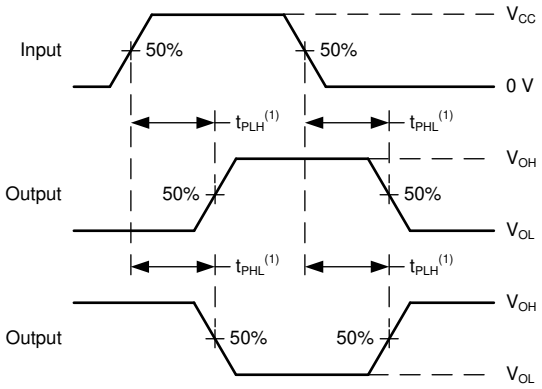

A. $C_L$ = 50 pF and includes probe and jig capacitance.

**Figure 6-1. Load Circuit**




A. $t_t$ is the greater of $t_r$ and $t_f$.

**Figure 6-2. Voltage Waveforms Transition Times**




A. The maximum between $t_{PLH}$ and $t_{PHL}$ is used for $t_{pd}$.

**Figure 6-3. Voltage Waveforms Propagation Delays**

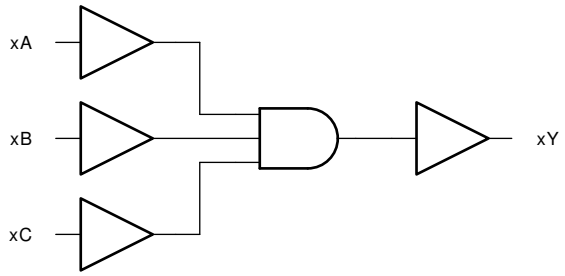
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# 7 Detailed Description

## 7.1 Overview

This device contains three independent 3-input AND gates. Each gate performs the Boolean function Y = A ● B ● C in positive logic.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

The CD74HC11 can drive a load with a total capacitance less than or equal to the maximum load listed in the *Switching Characteristics* connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the *Absolute Maximum Ratings*.

### 7.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.


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### 7.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 7-1.

**CAUTION**

Voltages beyond the values specified in the Absolute Maximum Ratings table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

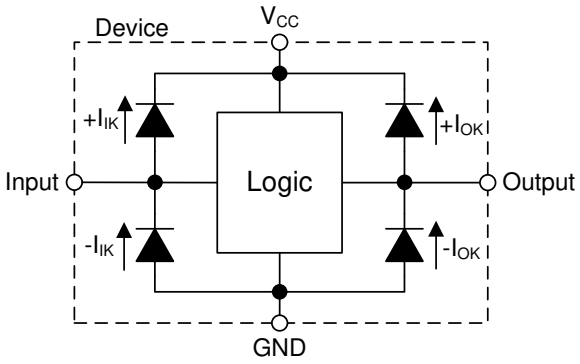



**Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output**

## 7.4 Device Functional Modes

**Table 7-1. Function Table**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| H | H | H | H |
| L | X | X | L |
| X | L | X | L |
| X | X | L | L |

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

In this application, this device is used to directly control the RESET pin of a motor controller. The controller requires three input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 3-input AND gate function combines the three individual reset signals into a single active-low reset signal.

## 8.2 Typical Application

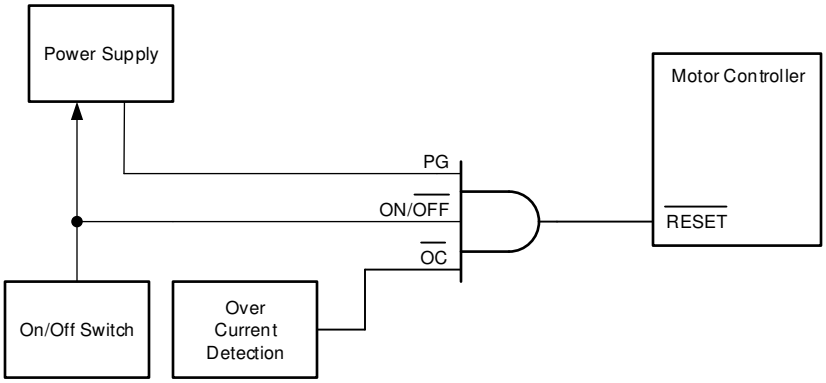



**Figure 8-1. Typical application schematic**

### 8.2.1 Design Requirements

#### *8.2.1.1 Power Considerations*

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the CD74HC11 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or $V_{CC}$ listed in the *Absolute Maximum Ratings*.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and $C_{pd}$ Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

**CAUTION**

The maximum junction temperature, $T_J$(max) listed in the *Absolute Maximum Ratings*, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.


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#### 8.2.1.2 Input Considerations

Unused inputs must be terminated to either $V_{CC}$ or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the CD74HC11, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The CD74HC11 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the *Recommended Operating Conditions*.

Refer to *Section 7.3* for additional information regarding the inputs for this device.

#### 8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to *Section 7.3* for additional information regarding the outputs for this device.

### 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in *Section 9*.
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the CD74HC11 to the receiving device.
3. Ensure the resistive load at the output is larger than ($V_{CC}$ / $I_O$(max)) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation

### 8.2.3 Application Curves

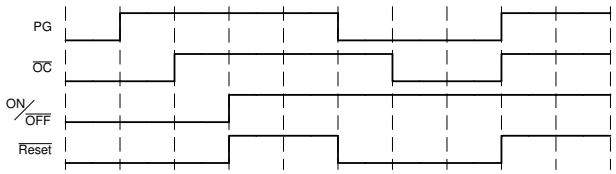



**Figure 8-2. Typical application timing diagram**

## Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in *Figure 9-1*.

# 9 Layout

## 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

## 9.2 Layout Example

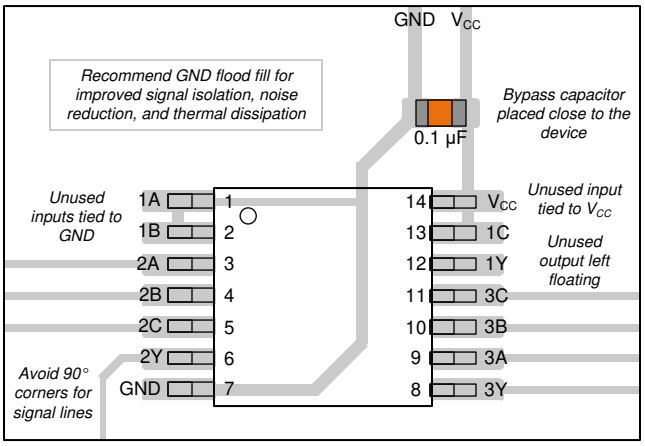



**Figure 9-1. Example layout for the CD74HC11**


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# 10 Device and Documentation Support

## 10.1 Documentation Support

### 10.1.1 Related Documentation

For related documentation see the following:

- HCMOS Design Considerations
- CMOS Power Consumption and CPD Calculation
- Designing with Logic

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 10.4 Trademarks

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## 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.6 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

## 10.7 Community Resources

## 10.8 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD54HC11F | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54HC11F | Samples |
| CD54HC11F3A | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8404801CA CD54HC11F3A | Samples |
| CD74HC11E | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC11E | Samples |
| CD74HC11EE4 | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC11E | Samples |
| CD74HC11M | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC11M | Samples |
| CD74HC11M96 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -55 to 125 | HC11M | Samples |
| CD74HC11MT | ACTIVE | SOIC | D | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC11M | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC11, CD74HC11 :**

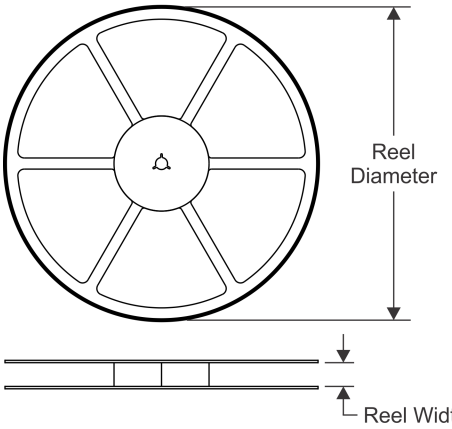
- Catalog : CD74HC11
- Military : CD54HC11

NOTE: Qualified Version Definitions:

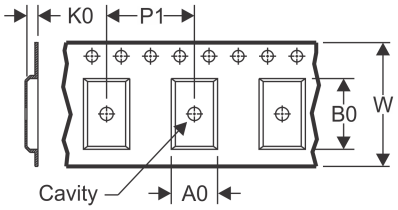
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

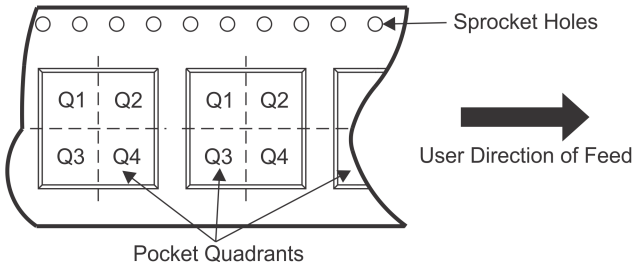



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

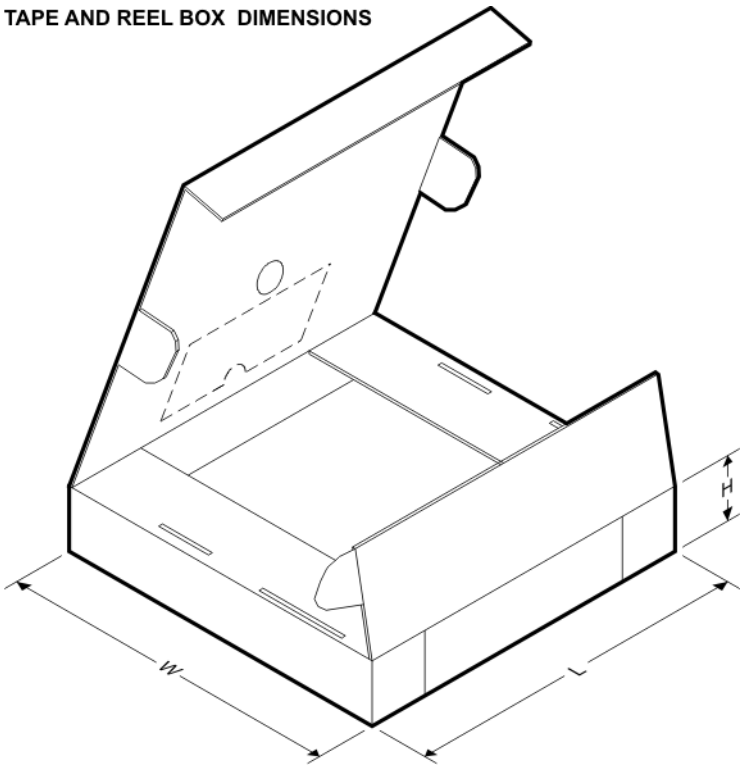
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC11M96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.6 | 9.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC11M96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC11MT | SOIC | D | 14 | 250 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

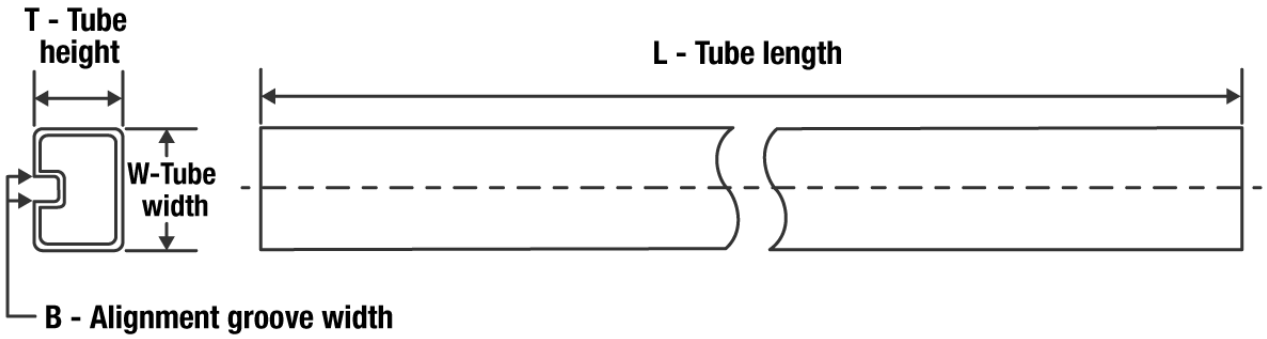
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC11M96 | SOIC | D | 14 | 2500 | 366.0 | 364.0 | 50.0 |
| CD74HC11M96 | SOIC | D | 14 | 2500 | 853.0 | 449.0 | 35.0 |
| CD74HC11MT | SOIC | D | 14 | 250 | 210.0 | 185.0 | 35.0 |

## TUBE



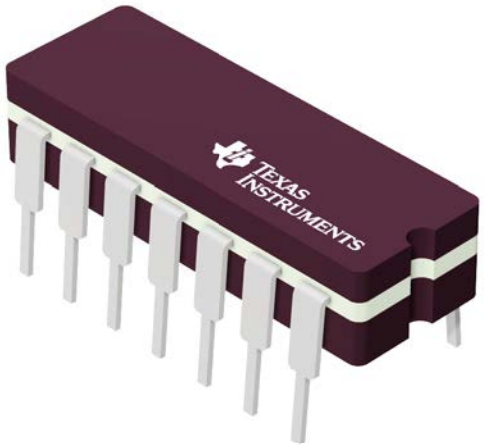

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74HC11E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC11E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC11EE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC11EE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC11M | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |

# GENERIC PACKAGE VIEW

## J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

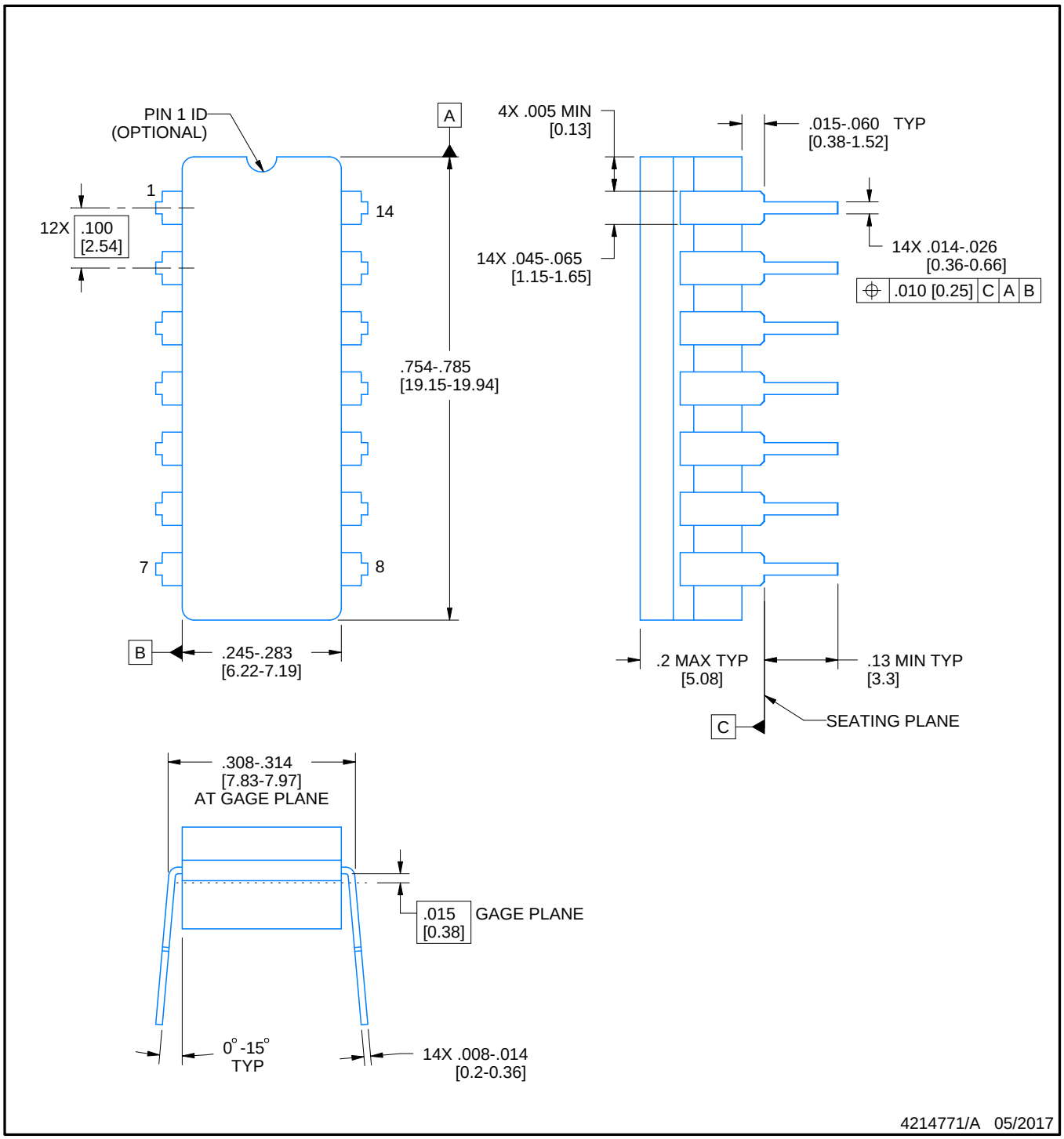


# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

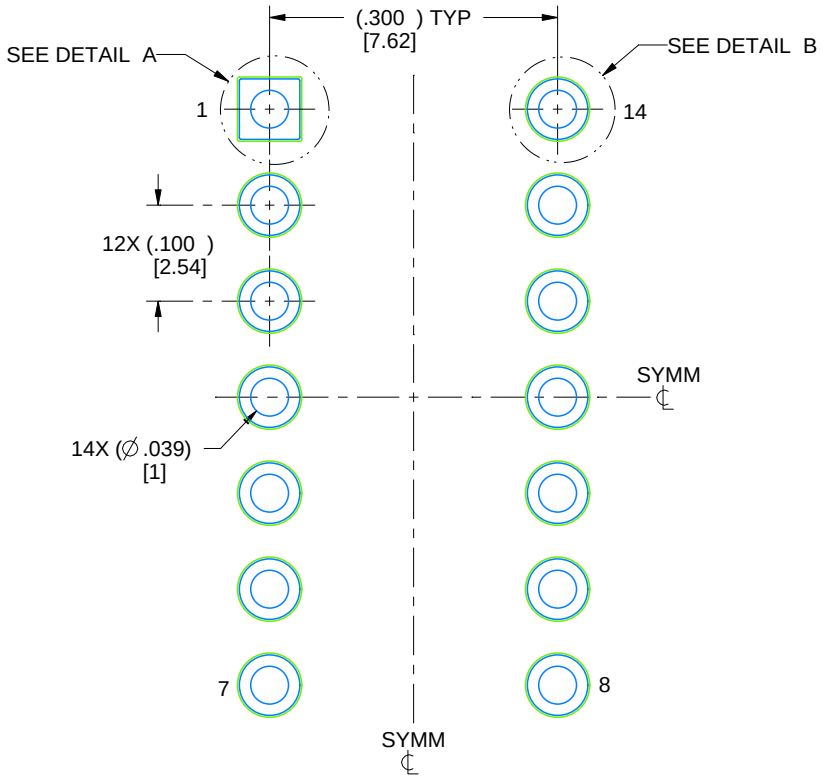
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

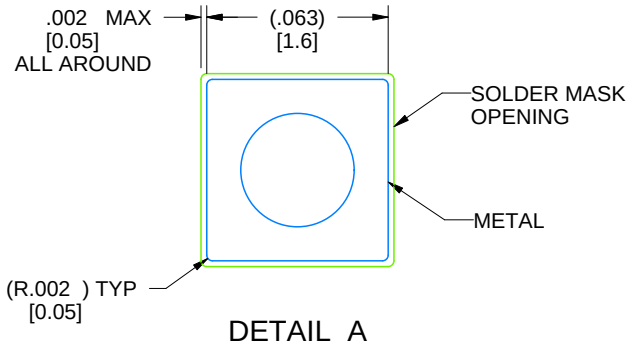
## J0014A

## CDIP - 5.08 mm max height

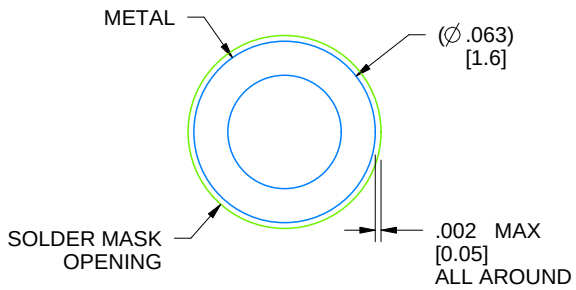
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



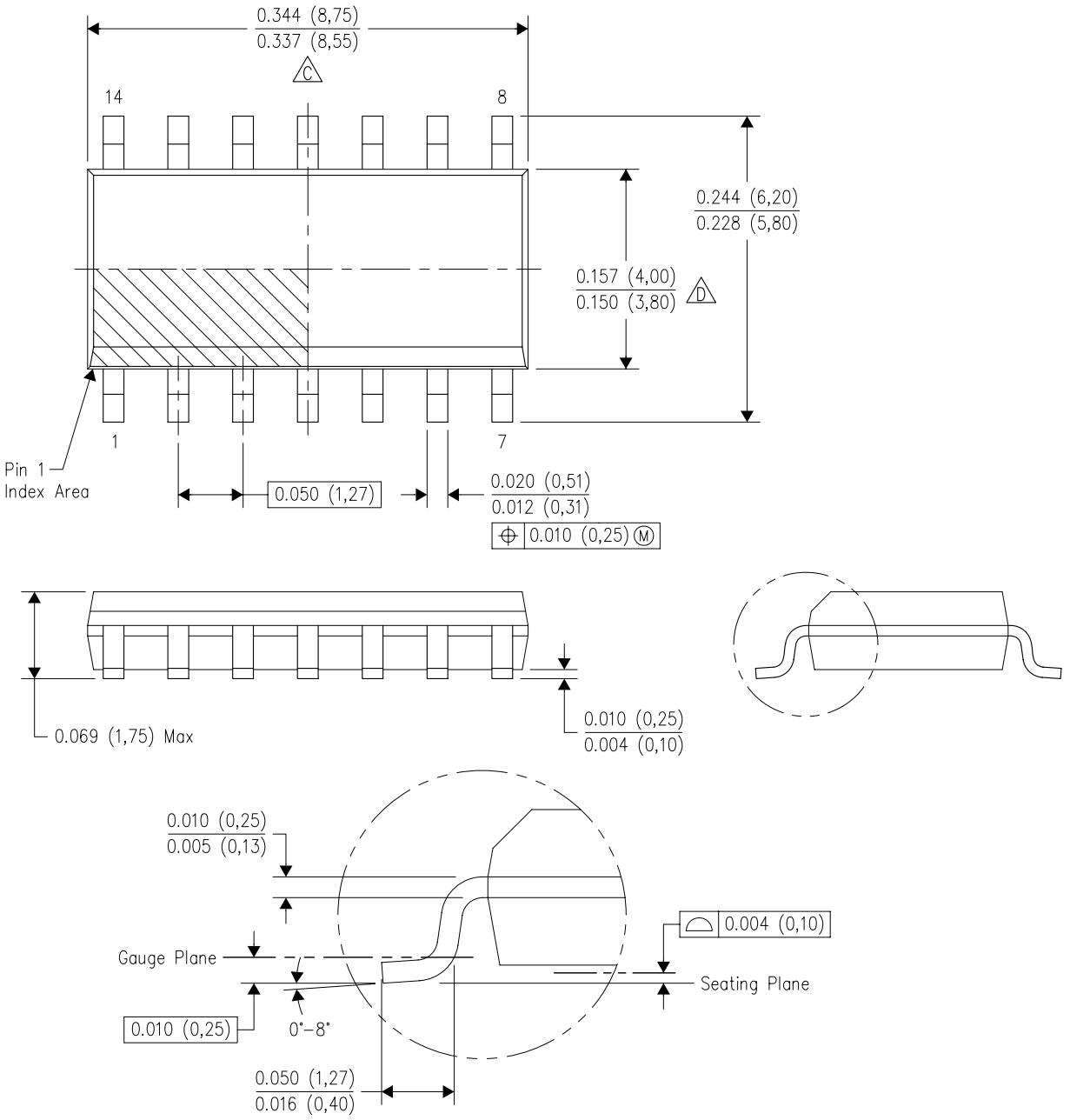

DETAIL A
SCALE: 15X




DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

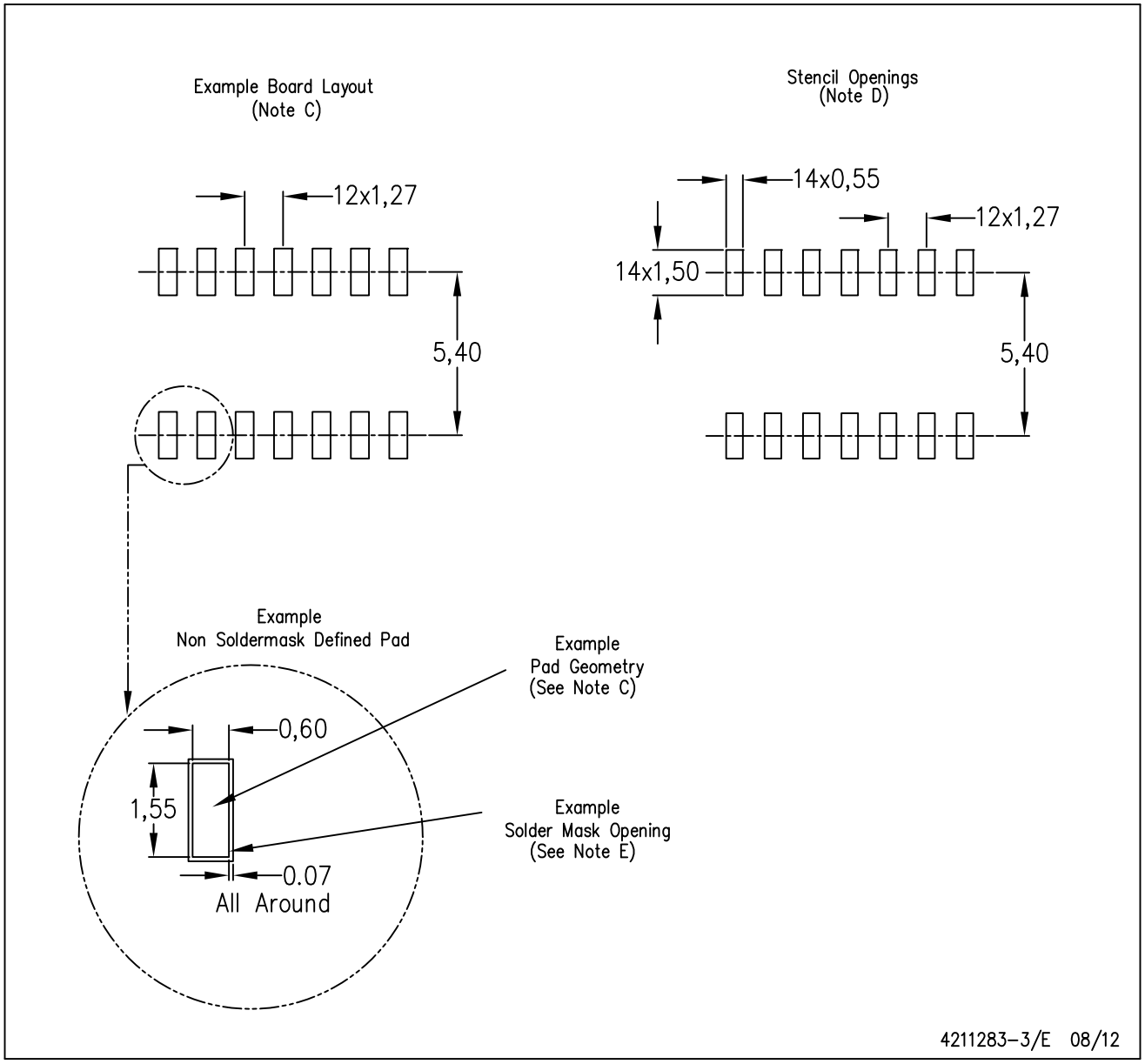
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

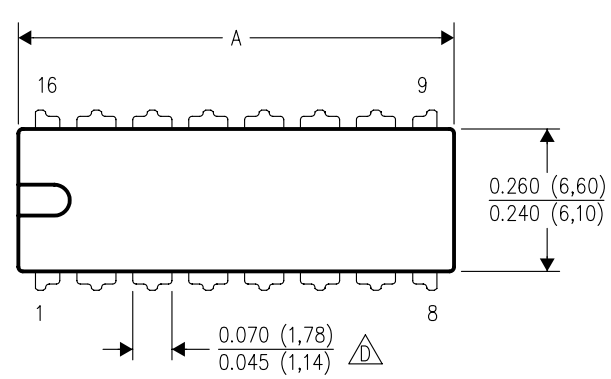



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

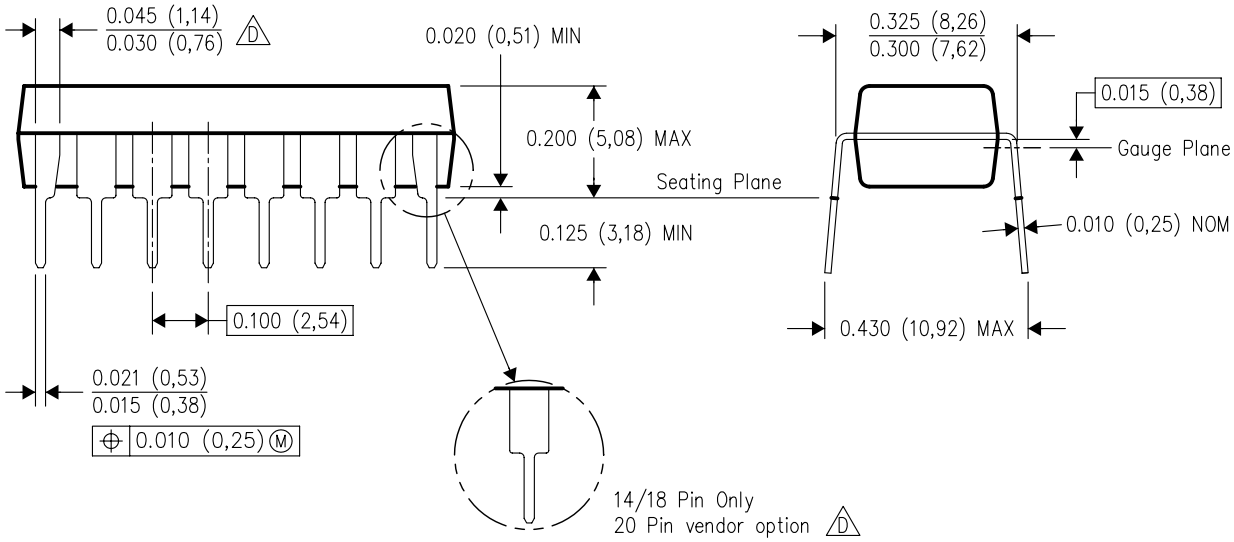
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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